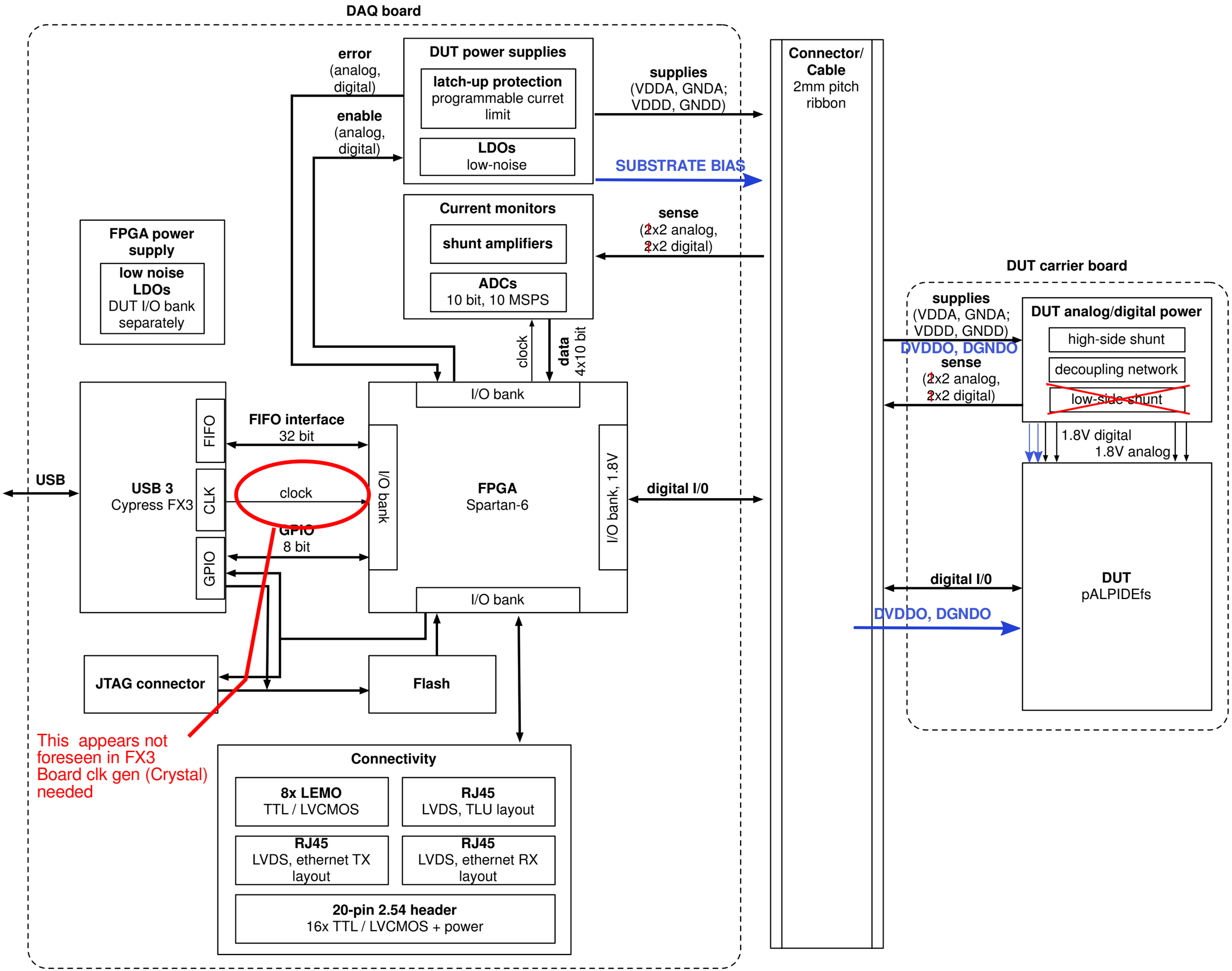
DAQ board
DUT power supplies
latch-up protection
programmable curret limit
LDOs
low-noise
error
(analog, digital)
enable
(analog, digital)
supplies
(VDDA, GNDA; VDDD, GNDD)
SUBSTRATE BIAS
Current monitors
shunt amplifiers
ADCs
10 bit, 10 MSPS
sense
(2x2 analog, 2x2 digital)
FPGA power supply
low noise LDOs
DUT I/O bank separately
clock
data
4x10 bit
I/O bank
FIFO
FIFO interface
32 bit
USB
USB 3
Cypress FX3
CLK
clock
GPIO
GPIO
8 bit
I/O bank
FPGA
Spartan-6
I/O bank, 1.8V
digital I/0
I/O bank
JTAG connector
Flash
This appears not foreseen in FX3
Board clk gen (Crystal) needed
Connectivity
8x LEMO
TTL / LVCMOS
RJ45
LVDS, TLU layout
RJ45
LVDS, ethernet TX layout
RJ45
LVDS, ethernet RX layout
20-pin 2.54 header
16x TTL / LVCMOS + power
Connector/ Cable
2mm pitch ribbon
DUT carrier board
supplies
(VDDA, GNDA; VDDD, GNDD)
DVDDO, DGNDO
sense
(2x2 analog, 2x2 digital)
DUT analog/digital power
high-side shunt
decoupling network
low-side shunt
1.8V digital
1.8V analog
digital I/0
DVDDO, DGNDO
DUT
pALPIDEfs