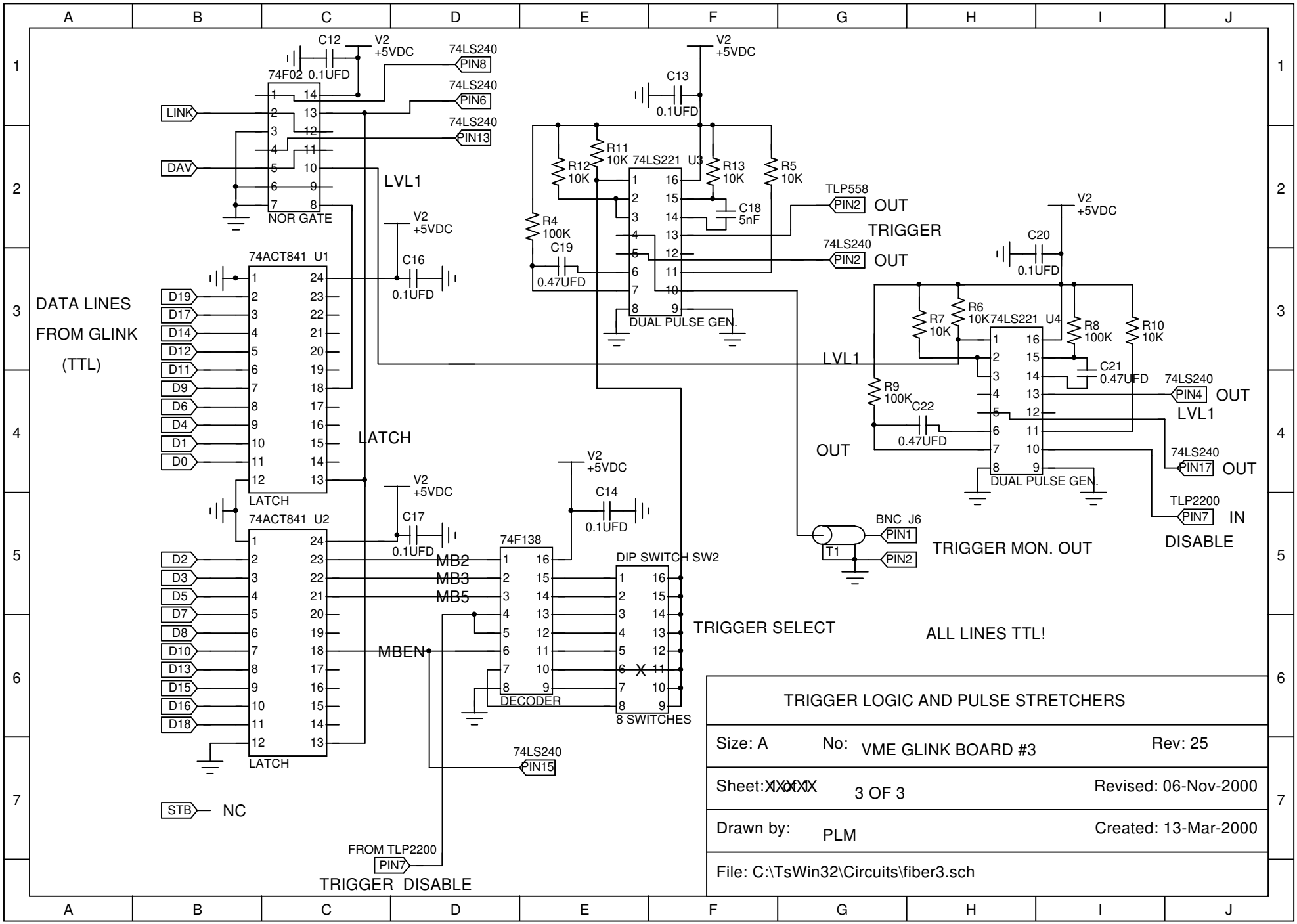
C12
V2
+5VDC
74F02 0.1UFD
74LS240
PIN8
74LS240
PIN6
74LS240
PIN13
LINK
DAV
NOR GATE
LVL1
C13
0.1UFD
R11
10K
R12
10K
74LS221 U3
R13
10K
R5
10K
C18
5nF
R4
100K
C19
0.47UFD
TLP558
PIN2
OUT
TRIGGER
74LS240
PIN2
OUT
DUAL PULSE GEN.
C16
0.1UFD
74ACT841 U1
DATA LINES
FROM GLINK
(TTL)
D19
D17
D14
D12
D11
D9
D6
D4
D1
D0
LATCH
LATCH
C20
0.1UFD
R7
10K
R6
10K
74LS221 U4
R8
100K
R10
10K
C21
0.47UFD
R9
100K
C22
0.47UFD
74LS240
PIN4
OUT
LVL1
OUT
74LS240
PIN17
OUT
DUAL PULSE GEN.
TLP2200
PIN7
IN
DISABLE
C17
0.1UFD
74ACT841 U2
C14
0.1UFD
74F138
DIP SWITCH SW2
D2
D3
D5
D7
D8
D10
D13
D15
D16
D18
MB2
MB3
MB5
MBEN
DECODER
8 SWITCHES
TRIGGER SELECT
BNC J6
PIN1
T1
PIN2
TRIGGER MON. OUT
ALL LINES TTL!
74LS240
PIN15
STB
NC
FROM TLP2200
PIN7
TRIGGER DISABLE
TRIGGER LOGIC AND PULSE STRETCHERS
Size: A
No: VME GLINK BOARD #3
Rev: 25
Sheet: XXofXX
3 OF 3
Revised: 06-Nov-2000
Drawn by: PLM
Created: 13-Mar-2000
File: C:\TsWin32\Circuits\fiber3.sch