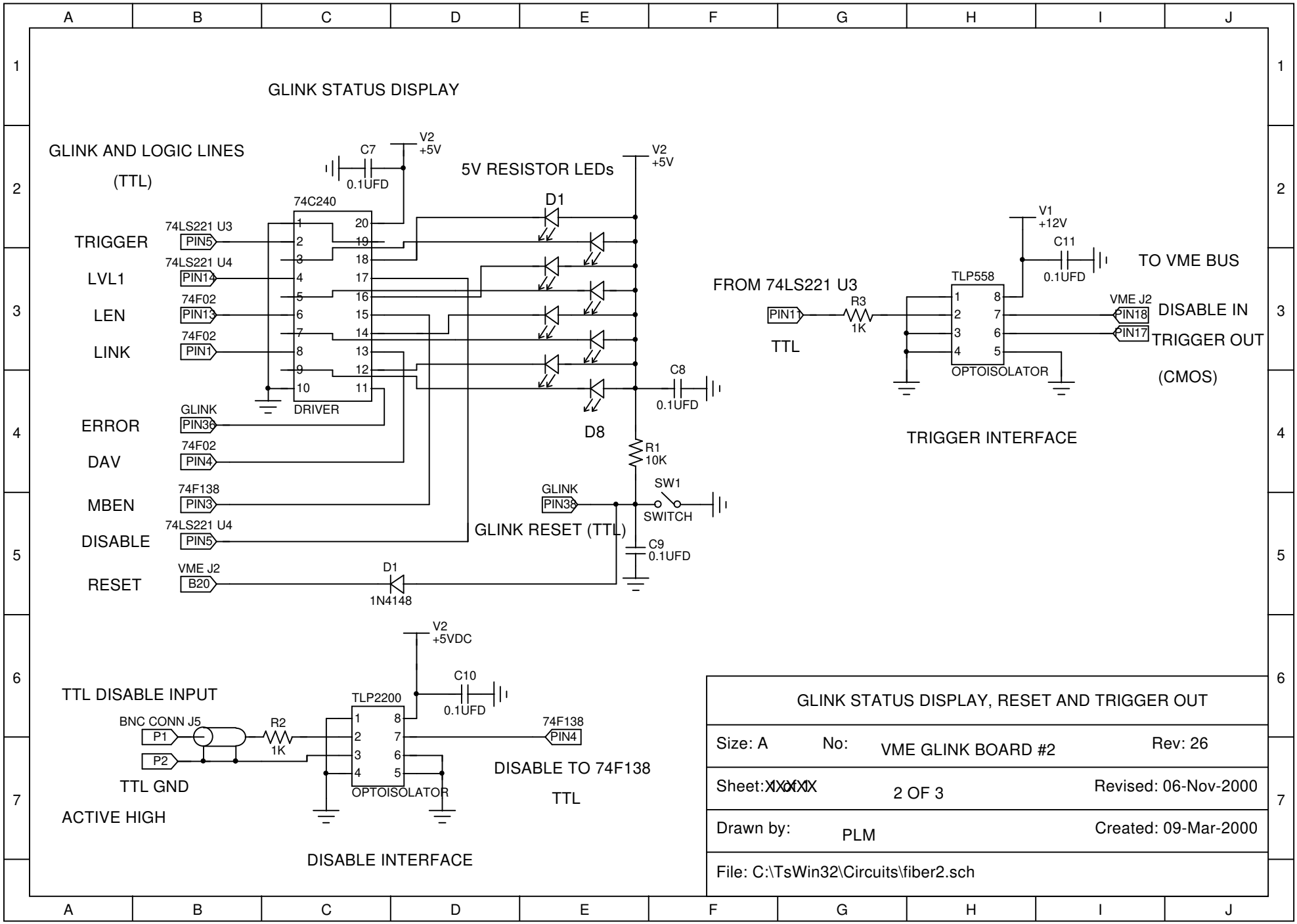
GLINK STATUS DISPLAY
GLINK AND LOGIC LINES
(TTL)
TRIGGER
LVL1
LEN
LINK
ERROR
DAV
MBEN
DISABLE
RESET
74LS221 U3
PIN5
74LS221 U4
PIN14
74F02
PIN13
74F02
PIN1
GLINK
PIN36
74F02
PIN4
74F138
PIN3
74LS221 U4
PIN5
VME J2
B20
74C240
DRIVER
C7
0.1UFD
V2
+5V
5V RESISTOR LEDs
D1
D8
C8
0.1UFD
R1
10K
SW1
SWITCH
GLINK RESET (TTL)
C9
0.1UFD
1N4148
FROM 74LS221 U3
PIN11
TTL
R3
1K
TLP558
OPTOISOLATOR
V1
+12V
C11
0.1UFD
TO VME BUS
VME J2
PIN18
PIN17
DISABLE IN
TRIGGER OUT
(CMOS)
TRIGGER INTERFACE
TTL DISABLE INPUT
BNC CONN J5
P1
P2
TTL GND
ACTIVE HIGH
R2
1K
TLP2200
OPTOISOLATOR
V2
+5VDC
C10
0.1UFD
74F138
PIN4
DISABLE TO 74F138
TTL
DISABLE INTERFACE
GLINK STATUS DISPLAY, RESET AND TRIGGER OUT
Size: A
No:
VME GLINK BOARD #2
Rev: 26
Sheet: XXofXX
2 OF 3
Revised: 06-Nov-2000
Drawn by:
PLM
Created: 09-Mar-2000
File: C:\TsWin32\Circuits\fiber2.sch