Forward Vertex Detector
Cost, Schedule, and Management Plan

- Participating Institutions
- Organizational plan
- Cost Basis
- R&D Costs
- Cost
- Schedule

Participating and Interested Institutions

Los Alamos National Laboratory

LANL coordinate work to procure the silicon sensors, work with FNAL on the development of the PHX chip, with Columbia on development of the interface to PHENIX DAQ, and on the simulation effort with NMSU. Los Alamos is currently leading the mechanical engineering and the integration effort for the barrel detector, VTX, and will continue those efforts for the FVTX.

Columbia University

Columbia University is an acknowledged expert on the PHENIX DAQ system They will work on the interface between the PHX chip and the PHENIX DAQ.

Iowa State University

Iowa State University is currently working on management details with the barrel detector and working on an (funded) SBIR effort for the level one trigger capabilities of the FVTX.

Charles University, Czech Technical University, Institute of Physics, Academy of Sciences, Prague

The Czech groups have been active in the development, testing, assembly, and commissioning of the ATLAS pixel sensors. They will do the same for the FVTX effort and additionally participate in software development.

New Mexico State University

NMSU will work on comprehensive simulations for the FVTX effort and work on the sensor testing.

University of New Mexico

UNM has experience in testing, Q/A and a laboratory for characterization of sensors. They are currently working on the barrel strip sensors and will do the same for the FVTX effort. They may also work on the flex cables.

Ecole Polytechnique, Saclay

Ecole Polytech has contributed to the electronics and software for the muon system has expressed interest in doing the same for the FVTX. Saclay will work on software.

Participating and Interested Institutions

Florida State University

FSU has worked on triggering issues for the VTX and FVTX effort.

Korea University

Korea University has been involved in many aspects of the hardware and software for the Muon system and will do the same for the FVTX.

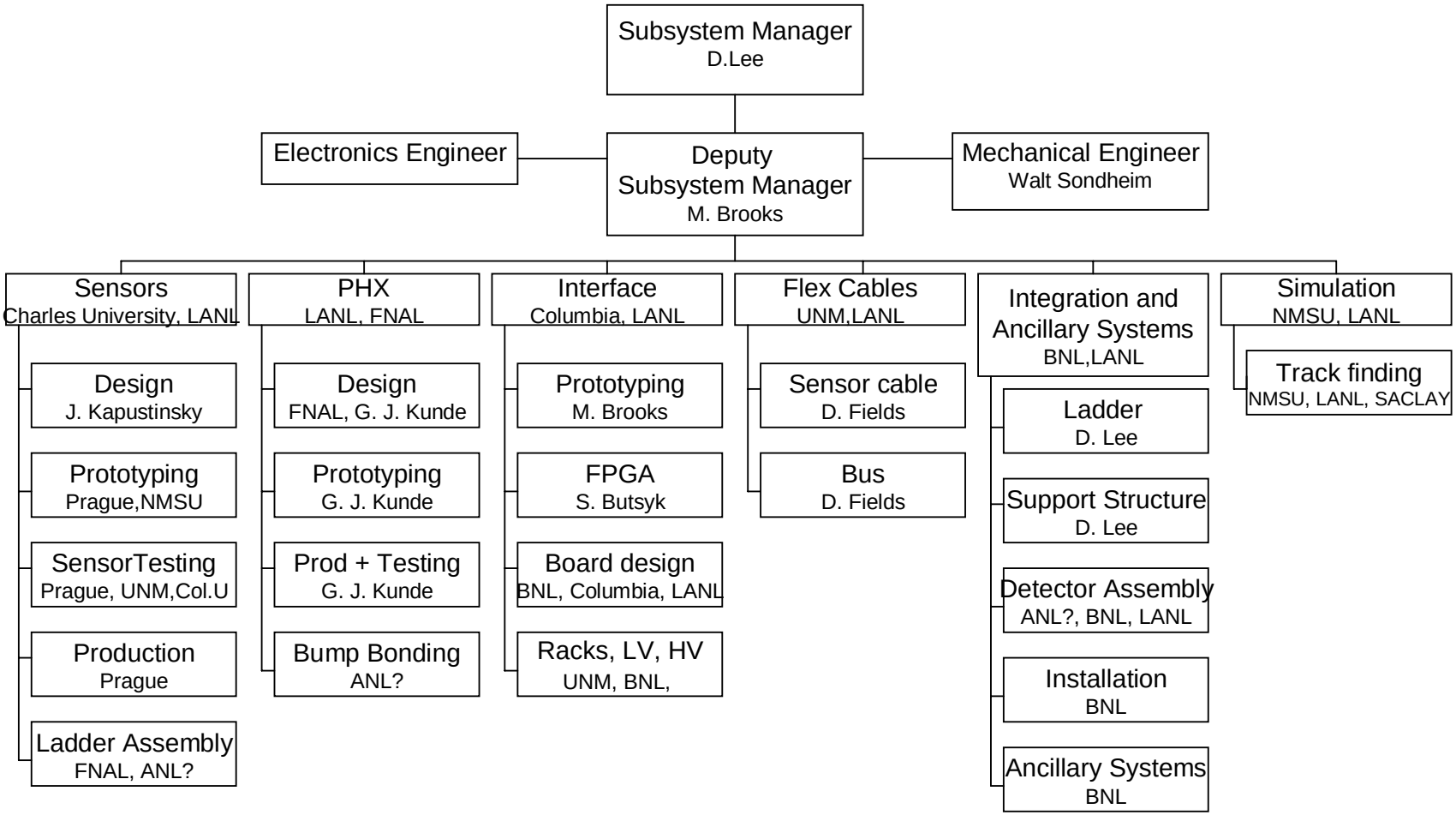
Yonsei University, Seoul, Korea

The Yonsei group has worked on electronics and software for the muon system and will do the same for the FVTX.

Argonne National Laboratory

Argonne National Laboratory is not a member of PHENIX but is considering joining to work on the spin physics program and the FVTX. We will want them to manage and coordinate all activities at FNAL.

Organizational Chart



Cost Basis - Major Items

Mechanical structures – HYTEC estimate based on prior experience

Sensors – Quotes from ON Semiconductor and CIS, Nov 2005

PHX – FNAL estimate based on prior experience

Electronics Interface – estimate based on prior experience with Muon system

Bump Bonding – BTeV experience with pixel chip

DCM,slow controls, etc – Muon system experience

R&D Costs

LANL LDRD-DR - $310k

- $1.2M/year for 3 years (FTE's and M&S)
- Interface Module - $200k
- Mechanics - $50k
- HDI and flex cables $60k

LANL Heavy Ion Program - $50k

- Sensor design - $50k

BNL R&D funds - $495k

- PHX design and Prototype - $440k
- Mechanics - $55k

Contingency – Risk Analysis

Risk Factor	Technical	Cost	Schedule	Design
0	Not used	Not used	Not used	Detail design > 50% done
1	Existing design and off-the-shelf H/W	Off-the-shelf or catalog item	Not used	Not used
2	Minor modifications to an existing design	Vendor quote from established drawings	No schedule impact on any other item	Not used
3	Extensive modifications to an existing design	Vendor quote with some design sketches	Not used	Not used
4	New design; nothing exotic	In-house estimate based on previous similar experience	Delays completion of non-critical subsystem item	Preliminary design >50% done; some analysis done
6	New design; different from established designs or existing technology	In-house estimate for item with minimal experience but related to existing capabilities	Not used	Not used
8	New design; requires some R&D but does not advance the state-of-the-art	In-house estimate for item with minimal experience and minimal in-house capability	Delays completion of critical path subsystem item	Conceptual design phase; some drawings; many sketches
10	New design of new technology; advances state-of-the-art	Top-down estimate from analogous programs	Not used	Not used
15	New design; well beyond current state-of-the-art	Engineering judgment	Not used	Concept only

FVTX Cost Estimate

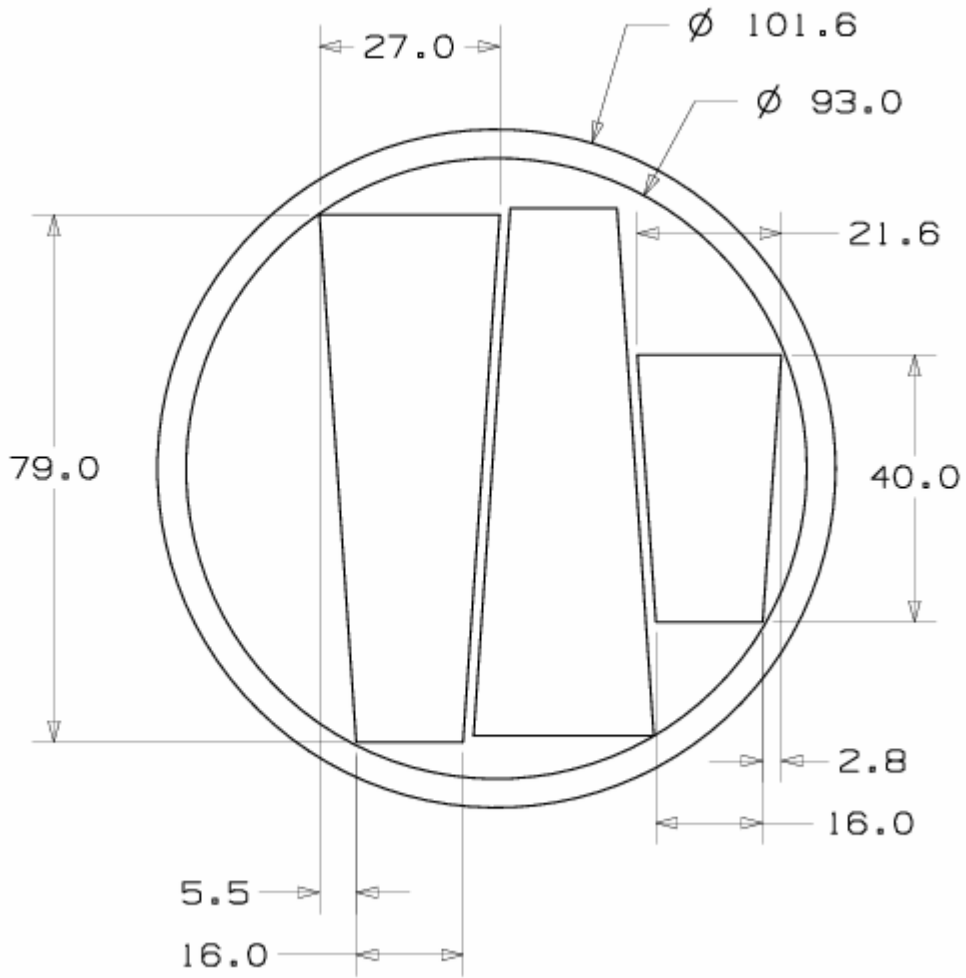
Forward Endcap Cost Estimate - FVTX					Tech	Cost	Schedule	Design	Weight	total	Cost with
2 endcaps	R&D BNL(k$)	R&D LANL(k$)	Construction(k$)	comments	Risk	Risk	Risk	Risk		contin	Continger
Mechanical ladder and support structure	55	50	190	HYTEC Estimate	4	4	4	4	2	0.24	235.6
Assembly jigs			20	engineering estimate	4	4	4	4	1	0.16	23.2
Silicon Sensor		50									
purchase			432	CIS and ON quotes, 20% spare	8	2	8	4	2	0.32	570.24
setup and masks			40	CIS and ON quotes	4	2	4	0	1	0.1	44
dicing			20	$ 100 wafer	4	8	8	0	1	0.2	24
sensor Q/A and testing			50	University students + engineer	4	4	4	0	1	0.12	56
PHX chip, tested	440										
engineering run			295	FNAL estimate	8	4	4	0	2	0.28	377.6
testing			60	FNAL tech	4	4	8	0	1	0.16	69.6
bump bond chip to sensor			420	Btev experience, $100/chip, 20% spares	8	4	8	0	2	0.32	554.4
Inteface - phx to DCM, CHI+MB concept		200	300	$500 for 400 units,arcnet $40k,engineeri	8	6	4	15	2	0.47	441
DCM,fibers,TFC fanout,..			150	existing designs	4	4	4	0	1	0.12	168
slow controls			50	existing designs	4	4	4	0	1	0.12	56
calibration system			20		4	4	4	0	1	0.12	22.4
Assembly and test ladders			200	FNAL techs	4	6	4	0	2	0.24	248
Assemble ladders in frame			100	techs and students	6	6	4	0	1	0.16	116
Electronics Integration			250	Engineer	4	6	4	0	2	0.24	310
Mechanical Integration			250	Engineer	4	6	4	0	2	0.24	310
power supplies, distr. Cards ,cables			100	VTX designs	4	4	2	4	1	0.14	114
bus		20	50	32 flex cables, includes 4 spares	8	6	4	15	2	0.47	73.5
flex cables, sensor to bus		20	160	672 flex cables, $200 each, 20% spares	8	6	4	15	2	0.47	235.2
fibercables, bus to enclosure		20	50	32 -12channel units	8	6	4	15	2	0.47	73.5
Misc cables, etc			150	enclosure to racks, fibers, etc	4	8	4	4	1	0.2	180
lab equipment			100	probe, test equipment	4	4	4	0	1	0.12	112
Management			100		2	4	2	0	1	0.08	108
total	495	360	3557								4522.24

HYTEC Cost Estimate – VTX and FVTX

Item	Engr R&D ($K)	Design ($K)	Mfg Liaison ($K)	Tooling ($K)	Fabrication ($K)	Materials ($K)	Total ($K)
Barrel and End Cap Detector Design	10	10	10				30
Dry Gas Enclosure	10	10	5	5	15	20	65
Suspension System	10	20	10	10	15	20	85
Fixtures for Assembly and Alignment	30	50	10	30	70	30	220
Coolant Circulation and Refrigeration System		50	10			25	85
Outer Structure (2 pieces)	50	35	10	45	50	20	210
End Cap Disks (16 pieces), plus cooling tubes	75	35	25	35	50	20	240
Disk Mounts (64 pieces)	10	15	5	5	15	5	55
Barrel Ladder Staves (~58 pieces)	50	50	20	20	58	20	218
Ladder Support Structure (4 pieces)		45	10	20	25	10	110
Ladder Coolant Tubes (~58 tubes), plus terminations	10	10	2	5	15	5	47
Total	255	330	117	175	313	175	1365

FVTX

FVTX Types 1 & 2 Silicon Wafer Layout



Sensor Needs:

Type 1 192 ea

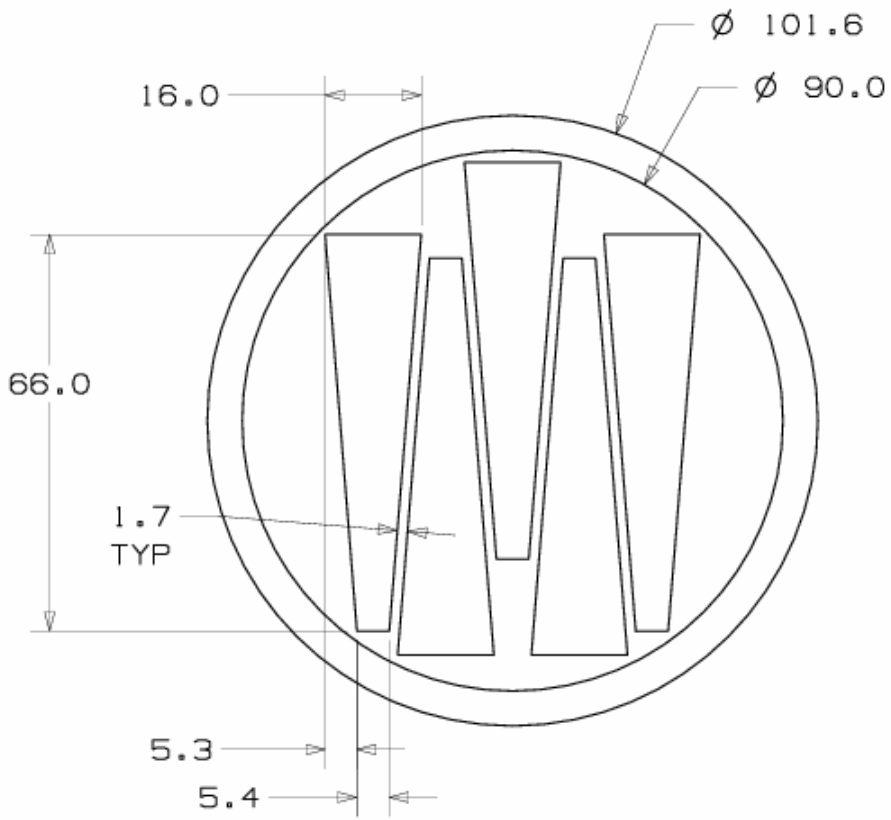
Type 2 96 ea

Wafer needs:

96 x 1.2/.6 = 192

Cost: $240k

FVTX Type 3 Silicon Wafer Layout



Sensor Needs:

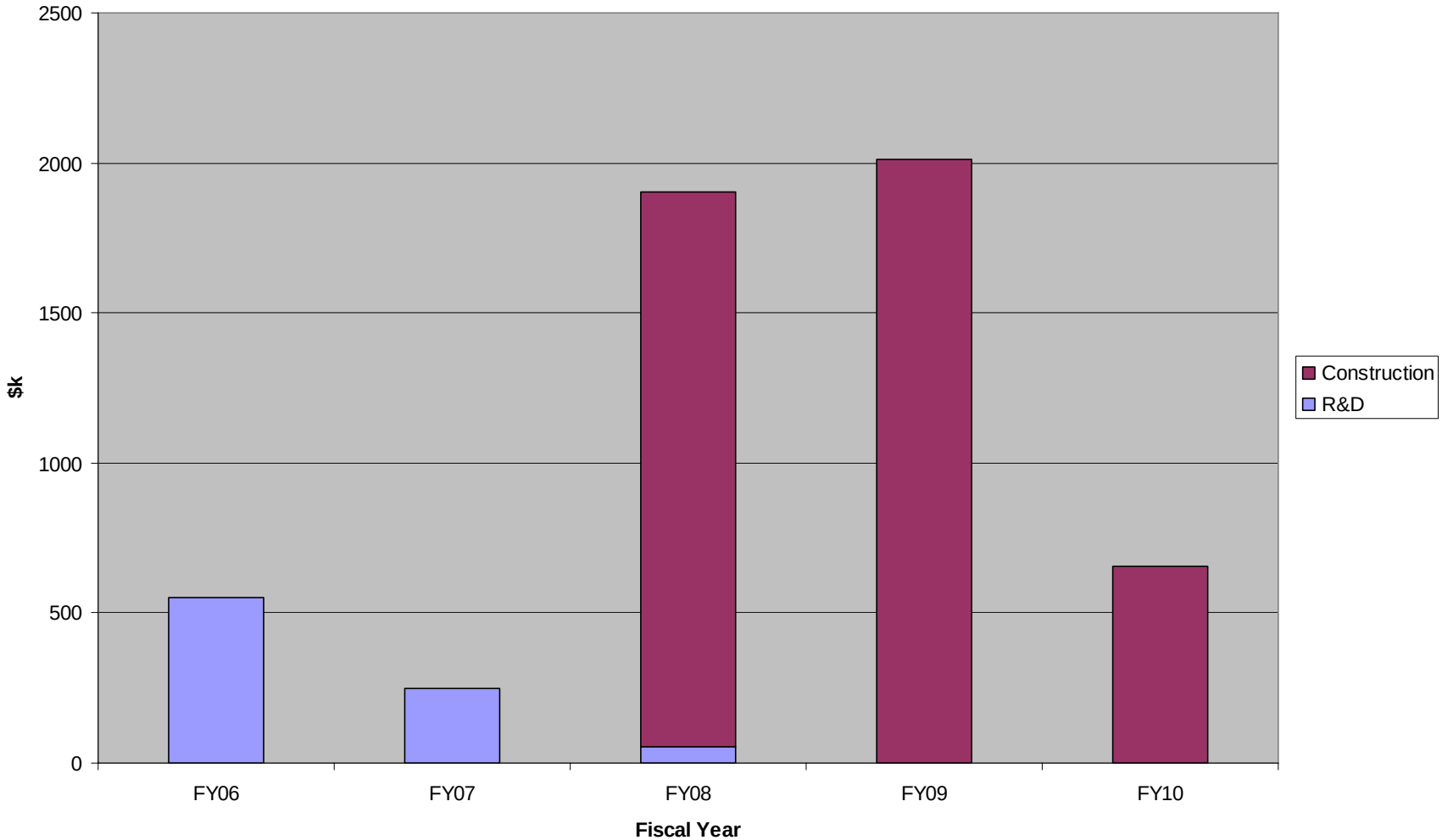
Type 3 384 ea

Wafer Needs:

77 wafers x 1.2/.6 = 154

Cost: $192.5k

Funding Profile

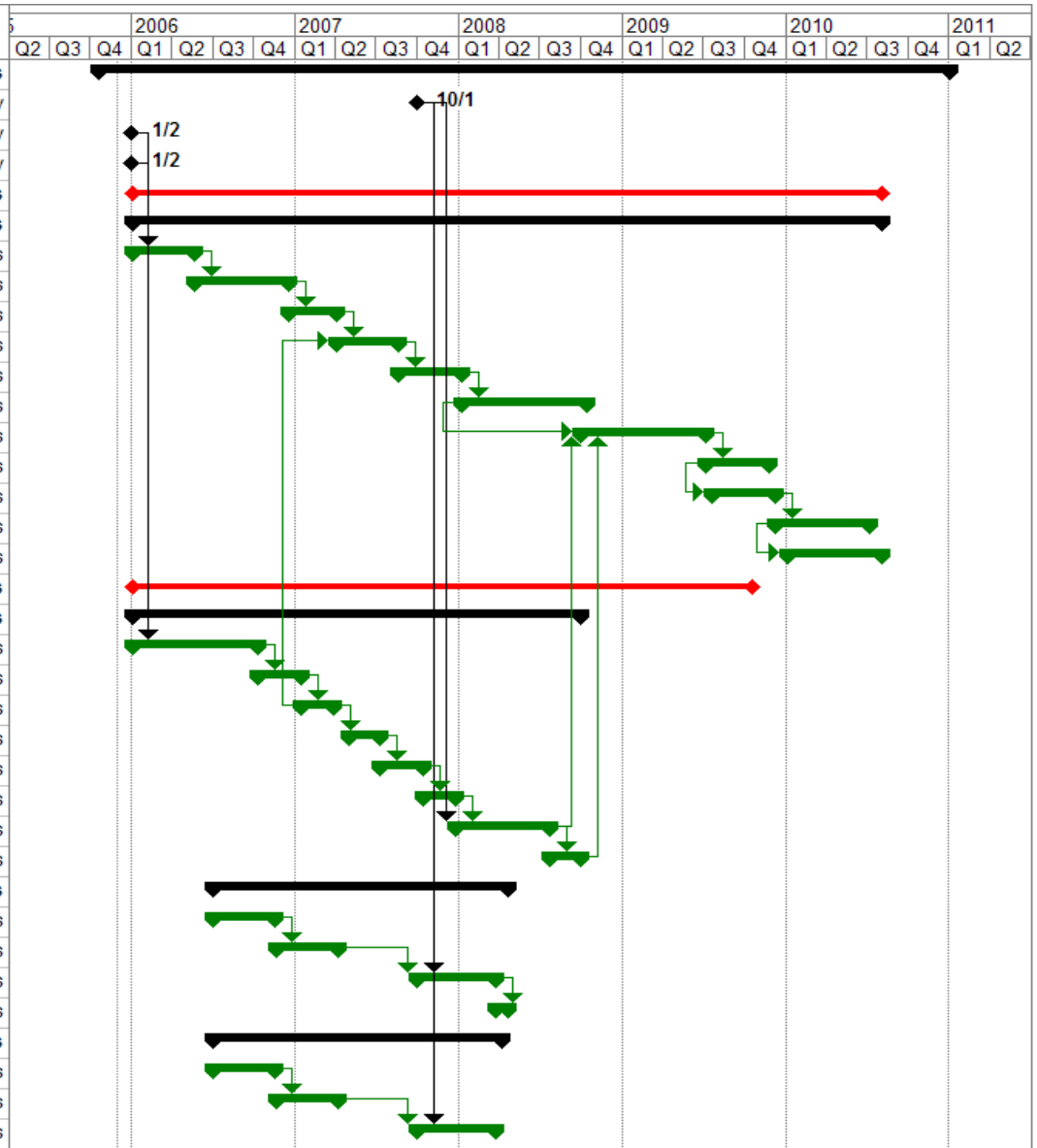


FVTX Schedule Assumptions

- Construction start – October 1, 2007 (FY08)
- LANL R&D start - January 2006
- BNL R&D start – January 2006

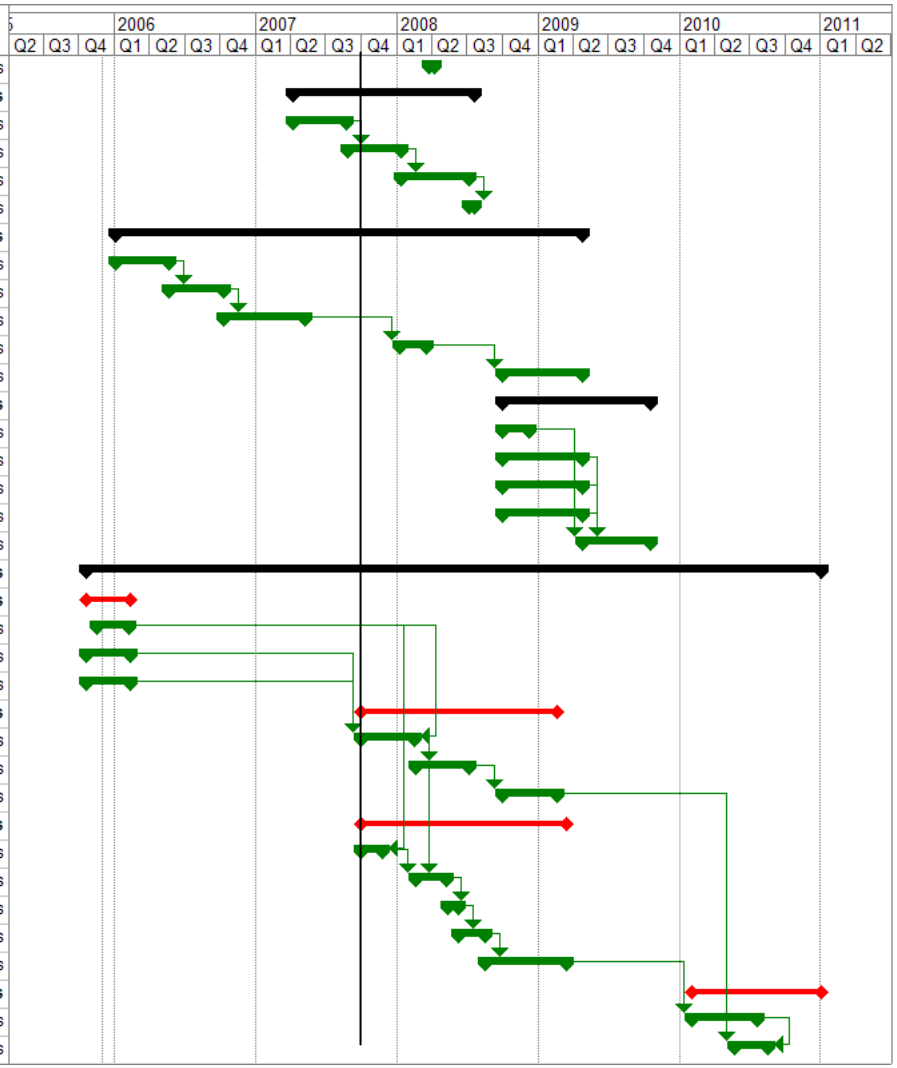
FVTX Schedule

ID	Task Name	Duration
1	**FVTX Project**	**1357 days**
2	**Start Construction**	1 day
3	**Start R&D BNL**	1 day
4	**Start R&D LANL**	1 day
5	**Sensors**	**1195 days**
6	**Wedge sensors**	**1195 days**
7	design sensors	20 wks
8	procure prototype sensor	30 wks
9	test prototype sensor	15 wks
10	bump bond PHX	20 wks
11	test PHX sensor assembly	20 wks
12	procure sensors	40 wks
13	bump bond + flip chip	40 wks
14	Attach flex cable	20 wks
15	Test flip chip + cable assemblie:	20 wks
16	Assemble on ladders	30 wks
17	test ladder assemblies	30 wks
18	**Ministrip electronics**	**989 days**
19	**PHX Chip**	**715 days**
20	design(FNAL)	40 wks
21	submit prototype	14 wks
22	test prototype	10 wks
23	redesign	10 wks
24	resubmit prototype	14 wks
25	test 2nd proto	10 wks
26	engineering run	30 wks
27	test chips(FNAL)	10 wks
28	**Kapton flex cables**	**471 days**
29	design	20 wks
30	prototype	20 wks
31	procure	25 wks
32	test cable	4 wks
33	**Kapton bus**	**461 days**
34	design	20 wks
35	prototype	20 wks
36	procure	25 wks



FVTX Schedule

ID	WBS	Task Name	Duration
37	1.3.3.5	test cable	2 wks
38	**1.3.5**	**fiber output**	**335 days**
39	1.3.5.7	design	20 wks
40	1.3.5.8	prototype	20 wks
41	1.3.5.9	procure	25 wks
42	1.3.5.10	test cable	2 wks
43	**1.3.4**	**Interface electronics**	**864 days**
44	1.3.4.1	design	20 wks
45	1.3.4.2	prototype	20 wks
46	1.3.4.3	2nd prototype	30 wks
47	1.3.4.4	PHENIX system test	10 wks
48	1.3.4.5	production	30 wks
49	**1.3.6**	**Ancillary**	**275 days**
50	1.3.6.1	Racks	10 wks
51	1.3.6.2	LV,HV,etc	30 wks
52	1.3.6.3	Slow controls	30 wks
53	1.3.6.4	calibration	30 wks
54	1.3.6.5	install	25 wks
55	**1.5**	**Mechanics**	**1357 days**
56	**1.5.12**	**specifications**	**80 days**
57	1.5.12.3	endcaps - specify heat load	12 wks
58	1.5.12.4	specify mechanical tolerances/(	4 mons
59	1.5.12.5	specify disassembly/configurati	4 mons
60	**1.5.6**	**support structure**	**362 days**
61	1.5.6.5	design	20 wks
62	1.5.6.6	prototype	20 wks
63	1.5.6.7	procure	20 wks
64	**1.5.7**	**ladders**	**380 days**
65	1.5.7.4	design	8 wks
66	1.5.7.5	prototype	12 wks
67	1.5.7.6	test	4 wks
68	1.5.7.7	final design	10 wks
69	1.5.7.8	procure	30 wks
70	**1.5.8**	**Endcap Assembly**	**240 days**
71	1.5.8.9	Assemble ladders into support	6 mons
72	1.5.8.10	Install into enclosure	3 mons



Summary

- No exotic or state-of-the-art R&D necessary
- LANL LDRD funds very important with BNL R&D funds
- Will design bus and flex cables with conventional line width
- Bump bonding within existing industry standards
- Management Plan is taking shape
- Cost Basis is maturing
- Construction Schedule points to FY 2011 as data run