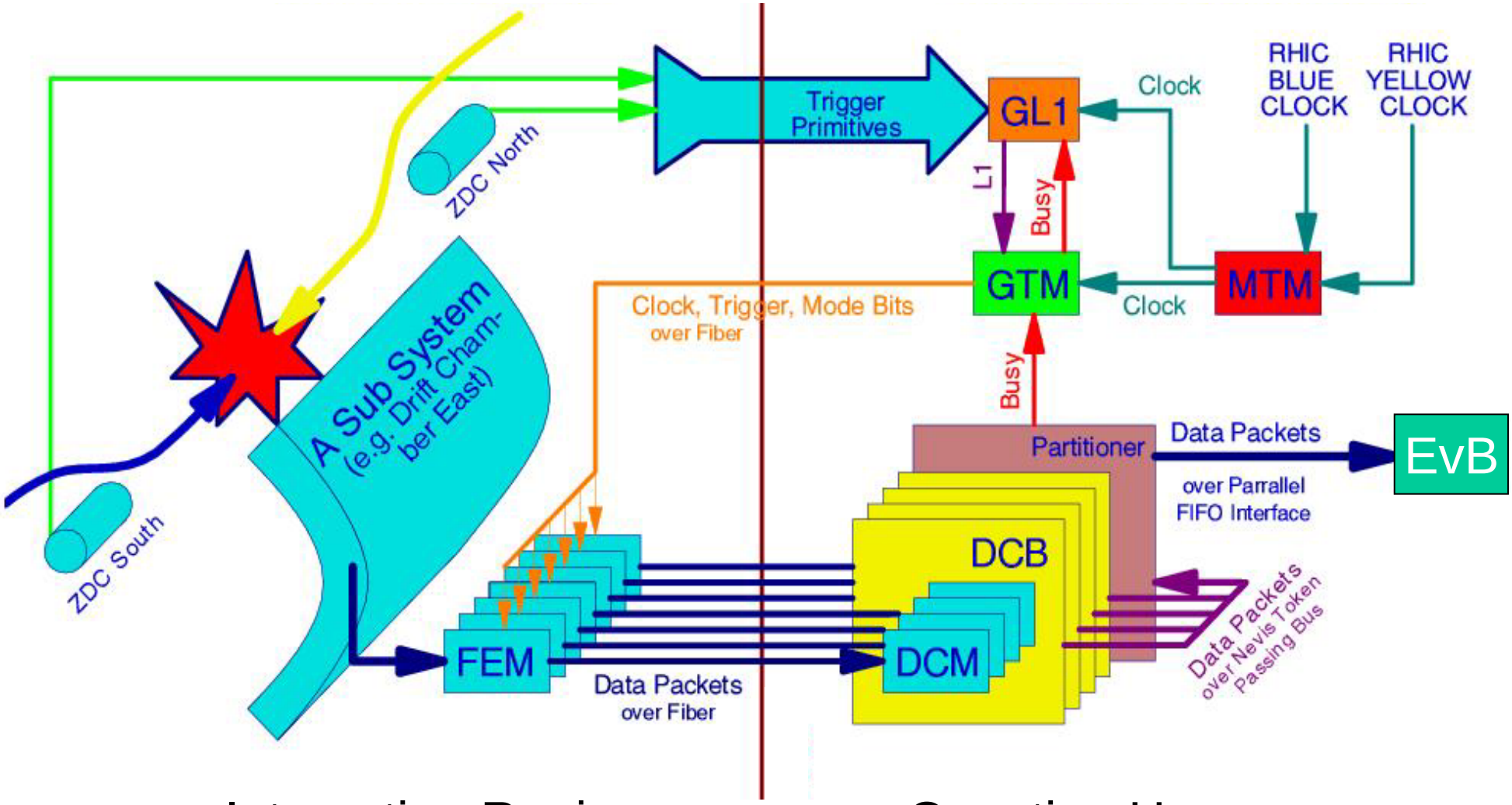
PHENIX DAQ Overview

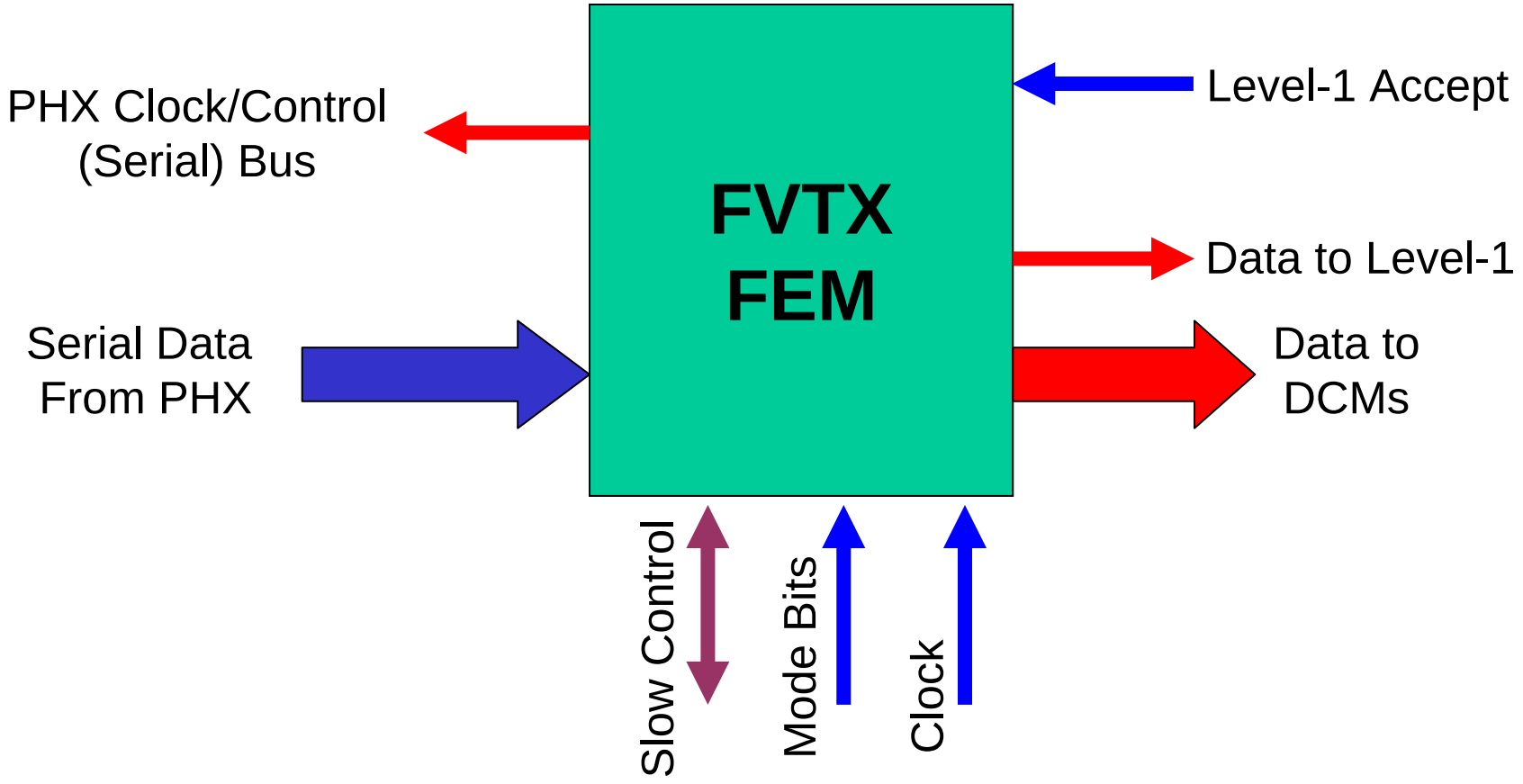


Interaction Region

Counting House

FVTX FEM Overview

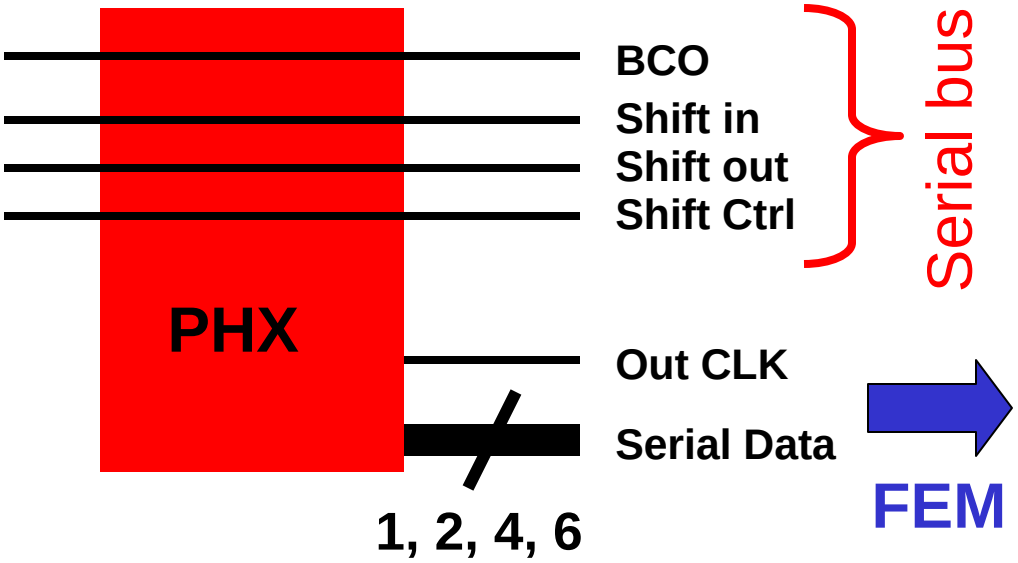
AKA "Electronics Transition Module"



- Primary interface between FVTX and PHENIX DAQ
- Receives **PHX** data, sends to **Level-1** and **DCMs**

PHX Interface

- PHX controlled via serial (LVDS) bus (rd/wr).
- Serial data lines will run @ 170 MHz (nominally)
  - Output clock can be used to latch data.
  - But digital phase follower may suffice.
- Conservatively estimate occupancies with **central Au+Au collisions**
  - ~ 4x Minimum bias
- Goal: read event from PHX in < 4 crossings
  - ⇒ **4 data lines/chip**

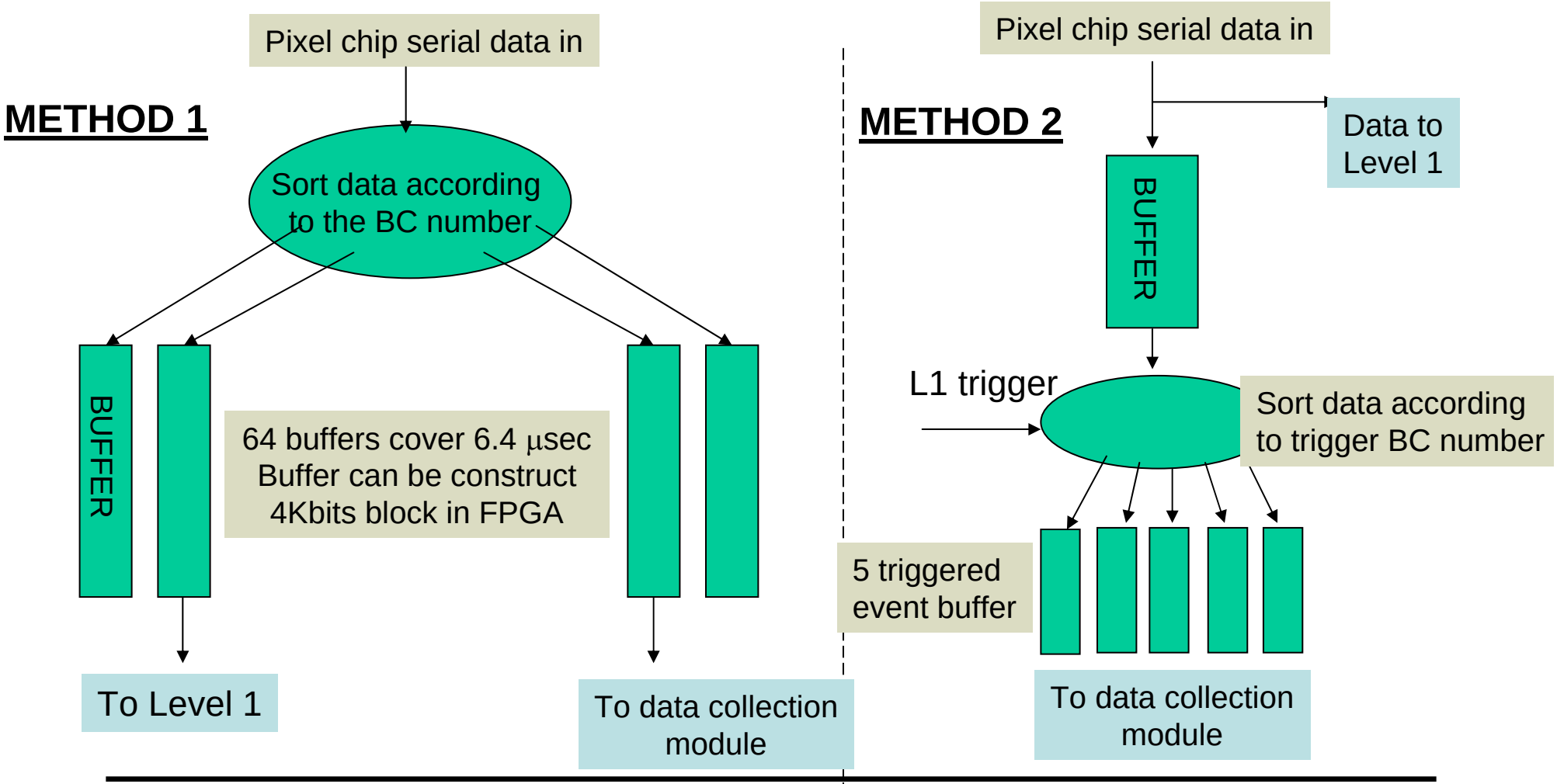


Assumptions:		Serial Data clock	170	MHz
		Avg. occupancy	1.60%	(1.5 hits, 0.1 noise)
		Channels/chip	512	
		Avg. hits/event	9	(rounded up)

# of Serial Bits	Bit Rate (MHz)	Word Rate (MHz)	Words/ Crossing	Avg Readout Time (Crossings)
1	170	7.1	0.75	12.0
2	339	14.1	1.50	6.0
4	679	28.3	3.00	3.0
6	1018	42.4	4.50	2.0

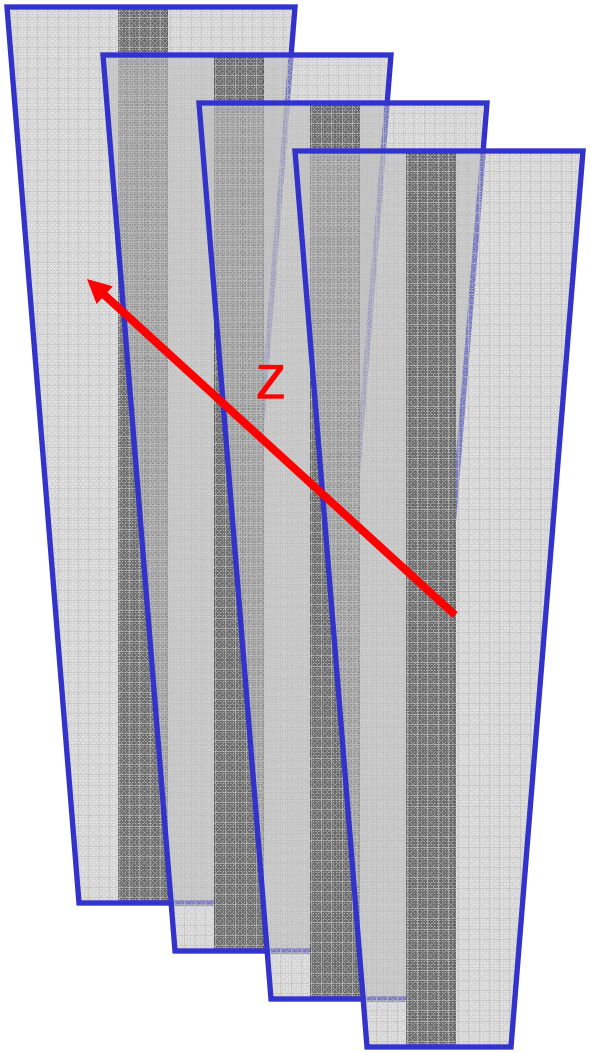
Processing PHX Data

- PHX data may arrive out of order (multiple events in data from single chip) – need to "sort" by crossing.



Strawman FEM Configuration

Tower x 4 Stations



- 35 chips in 1 tower x 4 stations
- Two possible options
  - 9 PHX chips/FEM (**identical FEMs**)
  - Variable # PHX/FEM (**const. occupany/FEM**)
    - ⇒ 5, 8, 11, 11 for ST 1, 2, 3, 4
- Either way, natural geographic mapping of Si readout → FEMs
  - 4 FEMs per tower over 4 stations
- And consistent w/ Level-1 spec
  - "Tile" = 8 towers x 4 stations
  - 1 tile → 1 board w/ 32 fibers
    - ⇒ 1-1 mapping, FEM → Level-1 fibers

FEM Realities: Connector Space

- Assume 9 chips per FEM, no data clock

Copper (LVDS twinax)

- 4 lines per chip ⇒ 9*4 = 36 diff. pairs
- @1 mm/pair in 2 mm HardMetric connector

  ⇒3.6 cm cable space

Fiber (multiplex 4→1)

- 9 chips ⇒ 9 optical input
  - 1.4 cm for dual receiver in SFF package
  - The smallest Altera Stratix GX can de-seralize 4 input in 2.7 cm width
- Either option: **2 FEMs/6U board (23 cm)**

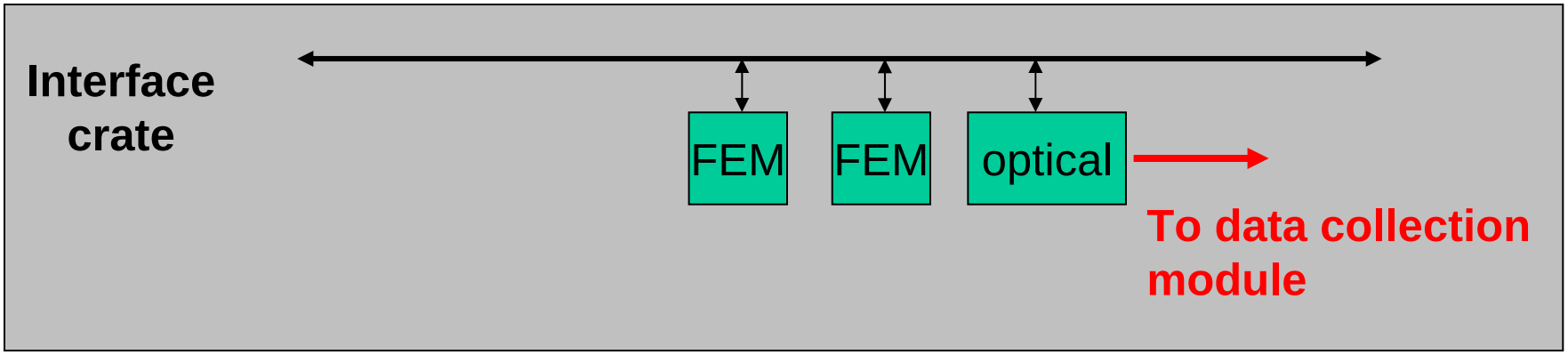
Strawman FEM Numerology

- Assuming 2 FEMs/wedge:
  - 24 Wedges/station, 4 stations/end-cap 2 end-caps

    ⇒384 FEMs in entire system, 192 per end-cap
- Assuming 2 FEMs/board, 16 boards/crate

    ⇒6 (6U) FEM crates per end-cap
- Combine output from multiple FEMs ⇒ DCM
  - Rough estimate: ~ 8 FEM/DCM, 4 DCM/board

    ⇒12 DCM boards (DCB's)



Crates/Clock/Slow Control/...

- Base on PHENIX HBD (Hadron-Blind Detector) FEM system under construction at Nevis.

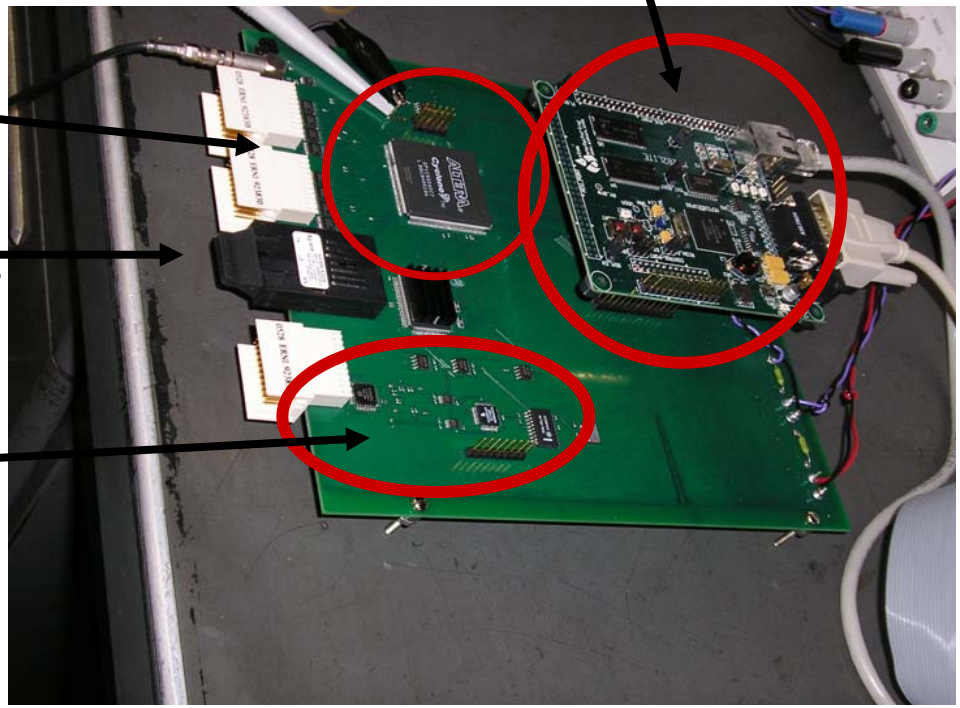
Clock Master Board

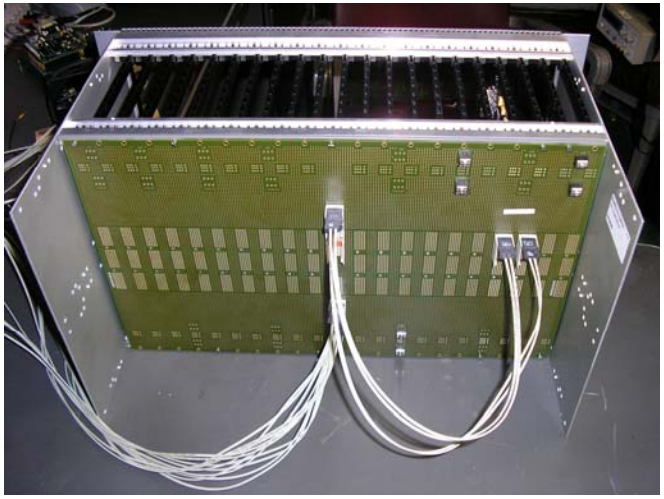
Ethernet interface

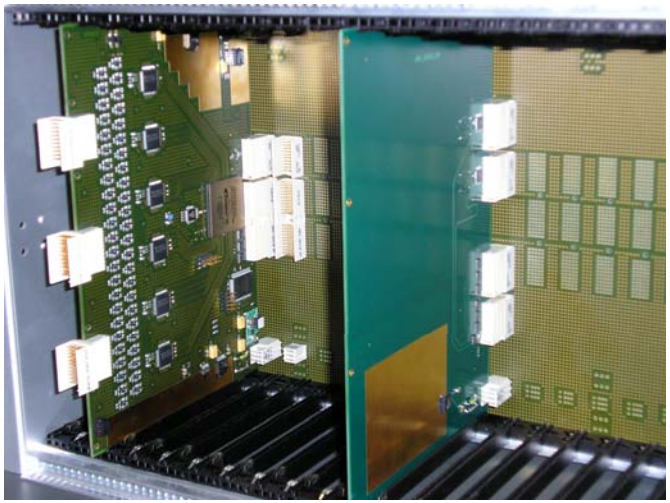
Serial data In/out

GTM Input

Clock Circuits







FVTX FEM Development

Current Status

- Los Alamos group is currrently using FNAL PCI board w/Xilinx FPGA to test FPIX.
  - w/ Xilinx De-serializer and BC-sorting algorithms
    - ⇒ Eventually: full test of FPIX control/readout
- Columbia group currently testing digital phase-follower for clockless readout.
  - Also testing FPIX chip using FPGA+DSP board from another Nevis electronics effort.
  - And testing performance of high-density twinax cables with LVDS drivers.

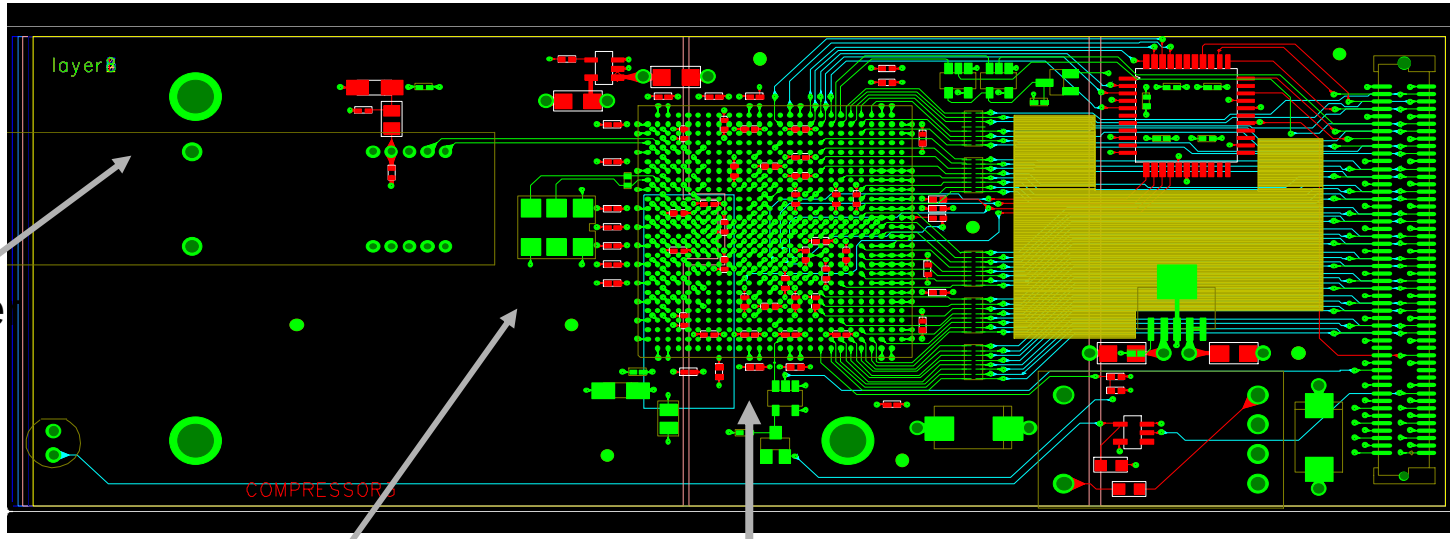
New DCM Daughter-card

Before the new DCM exist, this new DCM daughter card can use to read out new detectors FEM with old DCM Module.

8b/10b encoding on the optics data stream

16 bits raw data

Fix 1.6 Gbits data link



Optical Transceiver

80 MHz optical clock reference

Altera Stratix GX FPGA
(de-serializer, zero suppression, buffer etc)

Data Flow