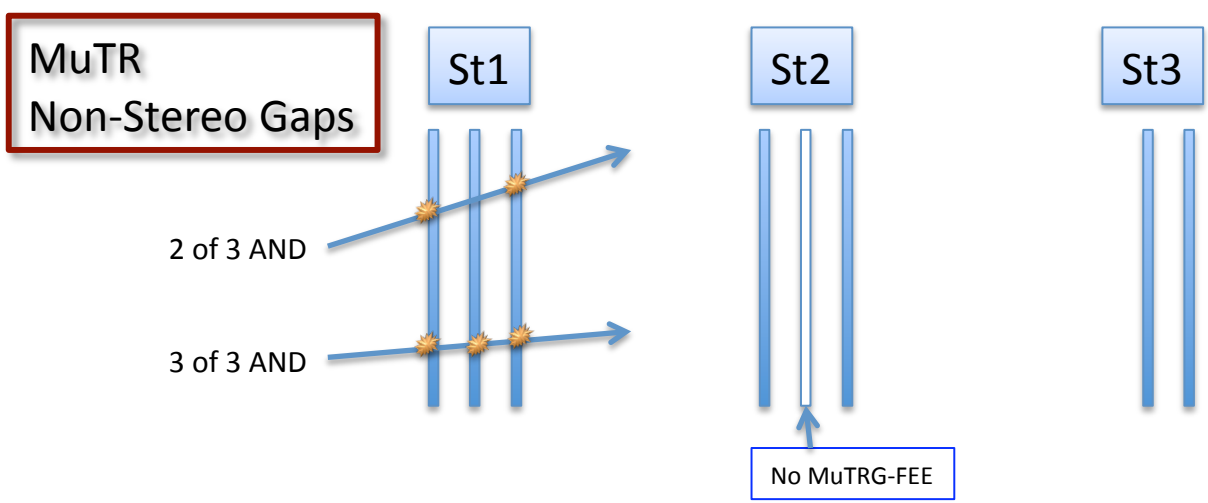
Run11 MuTrig-FEE Summary

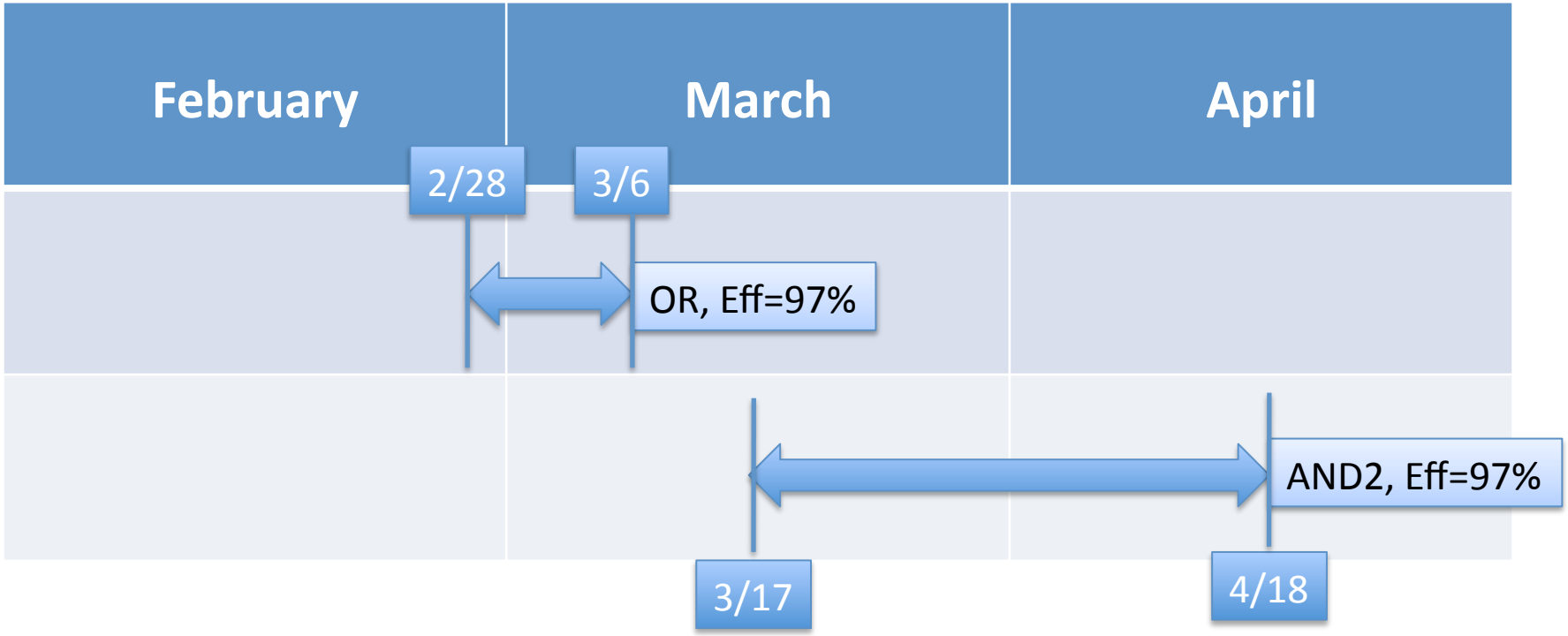
RIKEN/RBRC
Itaru Nakagawa

MuTrig-FEE Parameters

Function	Options		
Discriminator	LED	CFD	
Threshold	0 ~ 100 mV (40,60mV)		
Gap LOGIC	OR	AND	
		2 of 3	3 of 3
LL1 Width	1 ~ 7 (3)		



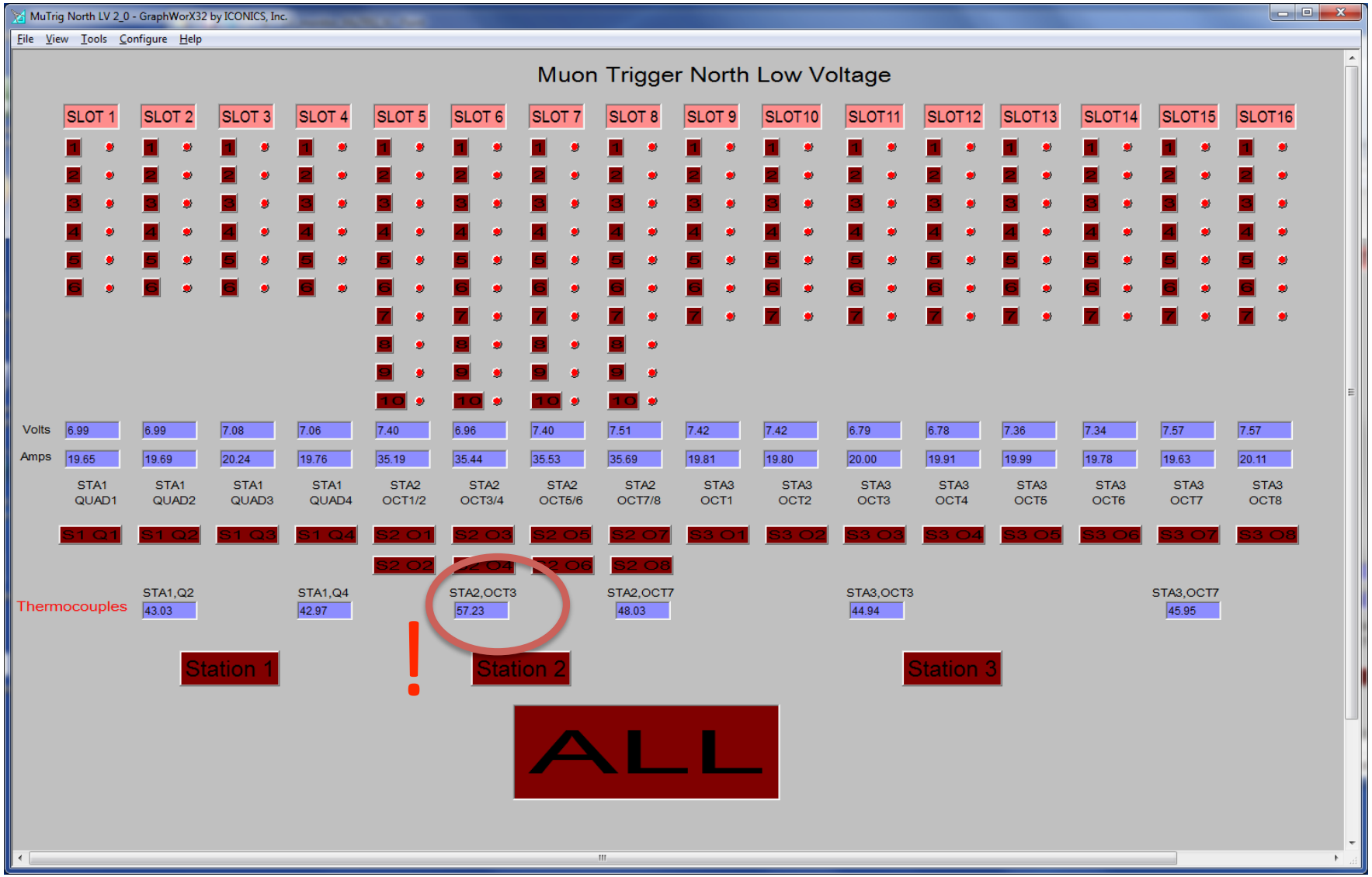
MuTrig-FEE Operation

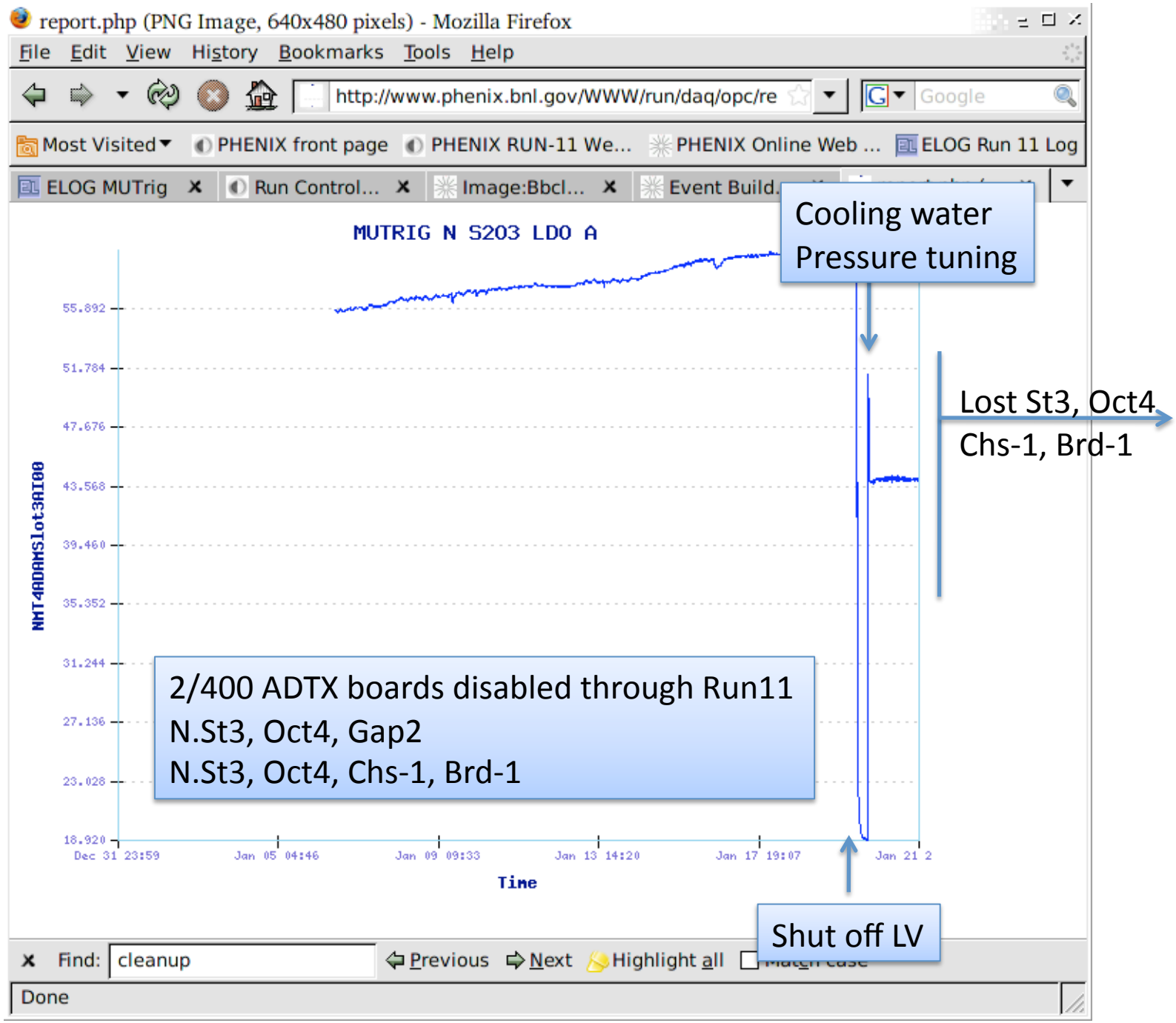


Thresholds are tuned to set efficiency~97% channel-by-channel.

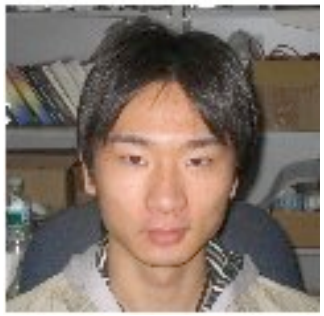
STABILITY

LV North Snapshot Jan.10




report.php (PNG Image, 640x480 pixels) - Mozilla Firefox
File Edit View History Bookmarks Tools Help
http://www.phenix.bnl.gov/WWW/run/daq/opc/re
Most Visited
PHENIX front page
PHENIX RUN-11 We...
PHENIX Online Web ...
ELOG Run 11 Log
ELOG MUTrig
Run Control...
Image:Bbcl...
Event Build...
MUTRIG N S203 LDO A
NMT4ADAMSlot3AI00
55.892
51.784
47.676
43.568
39.460
35.352
31.244
27.136
23.028
18.920
Dec 31 23:59
Jan 05 04:46
Jan 09 09:33
Jan 13 14:20
Jan 17 19:07
Jan 21 2
Time
Cooling water
Pressure tuning
Lost St3, Oct4
Chs-1, Brd-1
2/400 ADTX boards disabled through Run11
N.St3, Oct4, Gap2
N.St3, Oct4, Chs-1, Brd-1
Shut off LV
Find: cleanup
Previous
Next
Highlight all
Done

Katsuro Nakamura

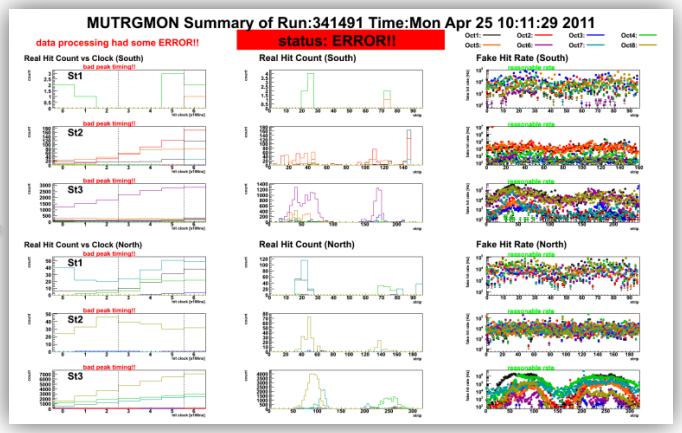


MuTrig-FEE Error Handling

MuTRG-MRG + DCMIF

Data Collecting Module

online monitor



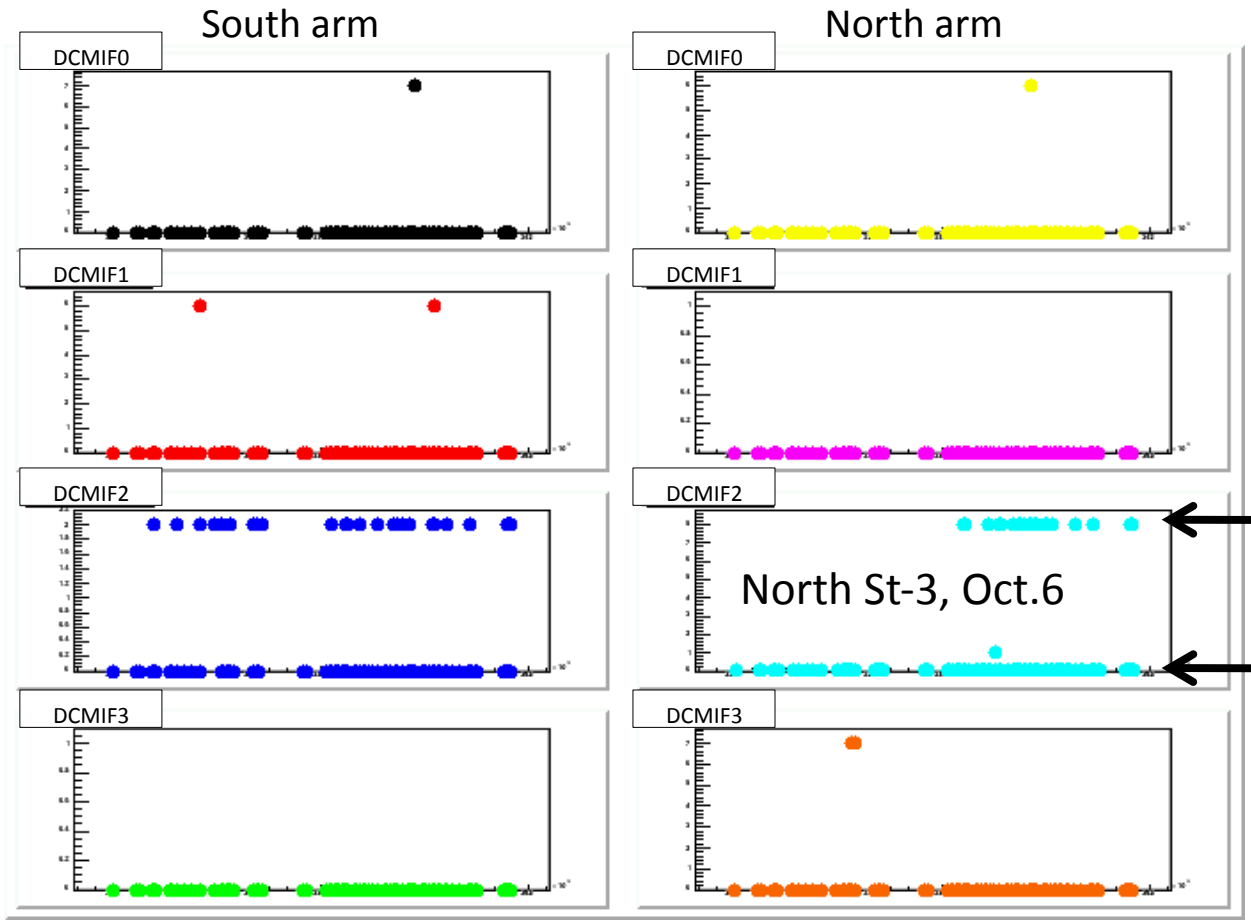
error information is sent to DAQ through data stream.

online monitor notices the error.

- shift crews can find errors through online monitor
  - most of errors can be solved with Reset(“Download”) or Initialization(“Feed”)

Errors in Electronics

All “PHYSICS” data



developed by
K. Nakamura

Y-axis: Channel

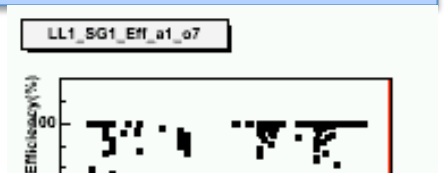
X-axis: Run numbers

Errors

OK!

✓ frequent failure especially for two ADTX boards

Stability Monitored by
Sanghwa Park (SNU)



Errors in Electronics

- Total 419 PHYSICS runs for pp collision
- Total 90 errors observed during PHYSICS data taking

Arm	DCMIF	MRG_CH	Bad runs
South	DCMIF0	MRG_CH6	4
	DCMIF1	MRG_CH5	2
	DCMIF2	MRG_CH1	47
	DCMIF3	No bad runs	
North	DCMIF0	MRG_CH5	1
	DCMIF1	No bad runs	
	DCMIF2	MRG_CH0	1
		MRG_CH7	32
	DCMIF3	MRG_CH6	3

← ~ 11.2 % of total data

← ~ 7.6 % of total data

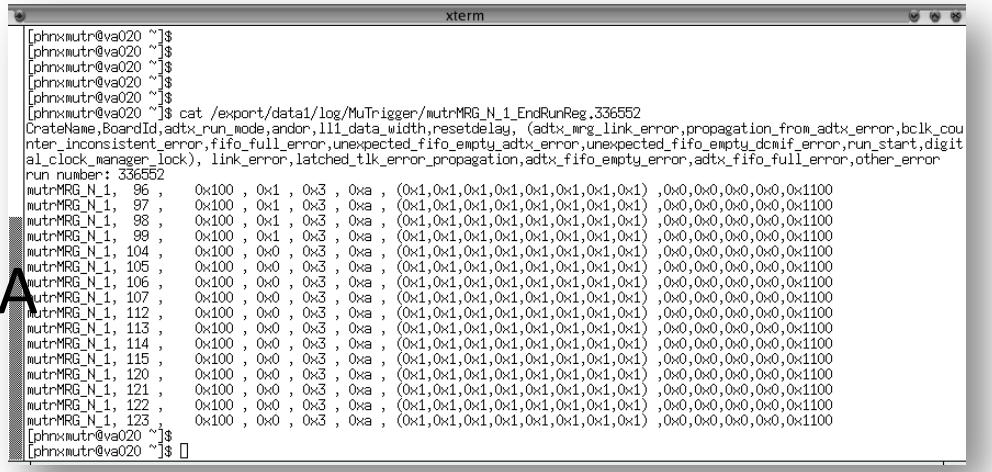
Most likely frequent errors are : beam clock counter mismatch, bad data format from ADTX

Error Log

- Ed Desmond developed status log system
  - read status through VME
  - automatically processed at the end of each run
  - log error information + parameter values
- It's very helpful to investigate the errors
- and recall the parameter setting
- Error analysis to be done
- To be dumped to DB for QA
  -> Spin Festa

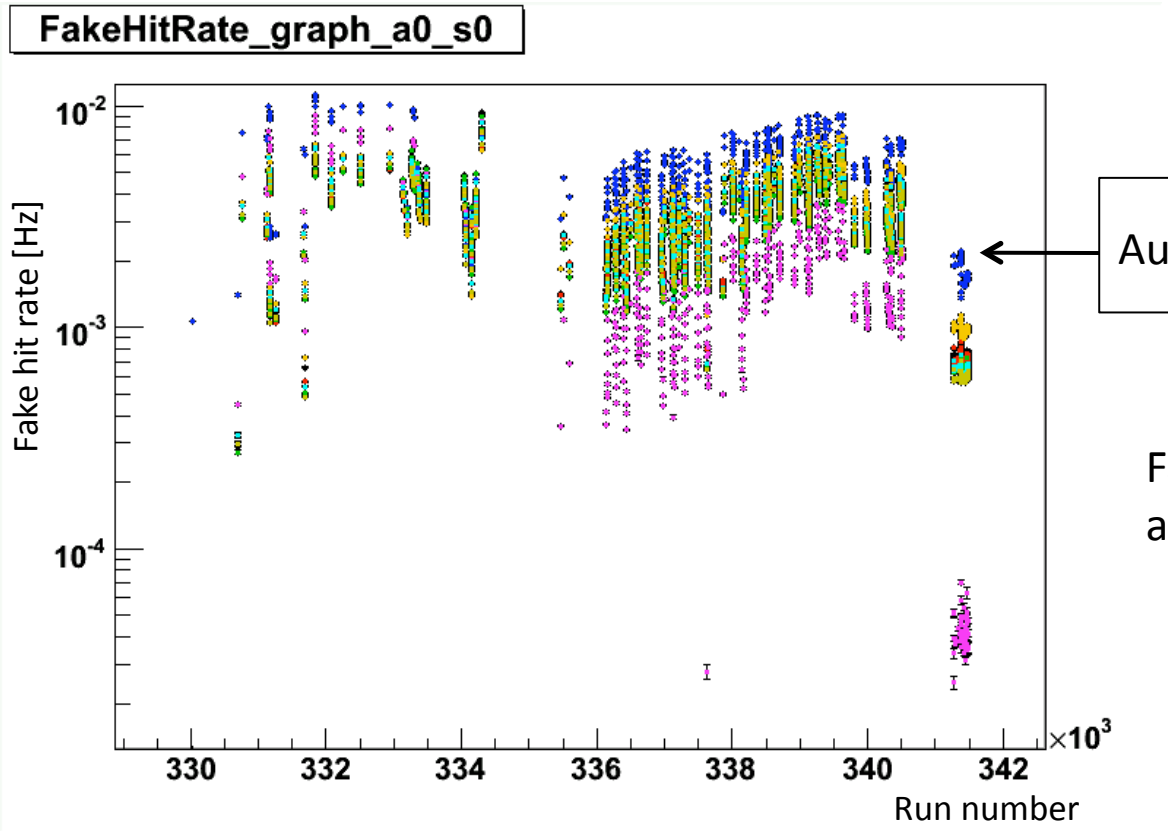
Thanks to Ed Desmond

status log output



```
xterm
[phnxmutr@va020 ~]$
[phnxmutr@va020 ~]$
[phnxmutr@va020 ~]$
[phnxmutr@va020 ~]$
[phnxmutr@va020 ~]$
[phnxmutr@va020 ~]$ cat /export/data1/log/MuTrigger/mutrMRG_N_1_EndRunReg.336552
CrateName,BoardId,adtx_run_mode,andor,lll_data_width,resetdelay, (adtx_mrg_link_error,propagation_from_adtx_error,bclk_cou
nter_inconsistent_error,fifo_full_error,unexpected_fifo_empty_adtx_error,unexpected_fifo_empty_dcmif_error,run_start,digit
al_clock_manager_lock), link_error,latched_tlk_error_propagation,adtx_fifo_empty_error,adtx_fifo_full_error,other_error
run number: 336552
mutrMRG_N_1,  96 ,    0x100 , 0x1 , 0x3 , 0xa , (0x1,0x1,0x1,0x1,0x1,0x1,0x1,0x1) ,0x0,0x0,0x0,0x0,0x0,0x1100
mutrMRG_N_1,  97 ,    0x100 , 0x1 , 0x3 , 0xa , (0x1,0x1,0x1,0x1,0x1,0x1,0x1,0x1) ,0x0,0x0,0x0,0x0,0x0,0x1100
mutrMRG_N_1,  98 ,    0x100 , 0x1 , 0x3 , 0xa , (0x1,0x1,0x1,0x1,0x1,0x1,0x1,0x1) ,0x0,0x0,0x0,0x0,0x0,0x1100
mutrMRG_N_1,  99 ,    0x100 , 0x1 , 0x3 , 0xa , (0x1,0x1,0x1,0x1,0x1,0x1,0x1,0x1) ,0x0,0x0,0x0,0x0,0x0,0x1100
mutrMRG_N_1, 104 ,    0x100 , 0x0 , 0x3 , 0xa , (0x1,0x1,0x1,0x1,0x1,0x1,0x1,0x1) ,0x0,0x0,0x0,0x0,0x0,0x1100
mutrMRG_N_1, 105 ,    0x100 , 0x0 , 0x3 , 0xa , (0x1,0x1,0x1,0x1,0x1,0x1,0x1,0x1) ,0x0,0x0,0x0,0x0,0x0,0x1100
mutrMRG_N_1, 106 ,    0x100 , 0x0 , 0x3 , 0xa , (0x1,0x1,0x1,0x1,0x1,0x1,0x1,0x1) ,0x0,0x0,0x0,0x0,0x0,0x1100
mutrMRG_N_1, 107 ,    0x100 , 0x0 , 0x3 , 0xa , (0x1,0x1,0x1,0x1,0x1,0x1,0x1,0x1) ,0x0,0x0,0x0,0x0,0x0,0x1100
mutrMRG_N_1, 112 ,    0x100 , 0x0 , 0x3 , 0xa , (0x1,0x1,0x1,0x1,0x1,0x1,0x1,0x1) ,0x0,0x0,0x0,0x0,0x0,0x1100
mutrMRG_N_1, 113 ,    0x100 , 0x0 , 0x3 , 0xa , (0x1,0x1,0x1,0x1,0x1,0x1,0x1,0x1) ,0x0,0x0,0x0,0x0,0x0,0x1100
mutrMRG_N_1, 114 ,    0x100 , 0x0 , 0x3 , 0xa , (0x1,0x1,0x1,0x1,0x1,0x1,0x1,0x1) ,0x0,0x0,0x0,0x0,0x0,0x1100
mutrMRG_N_1, 115 ,    0x100 , 0x0 , 0x3 , 0xa , (0x1,0x1,0x1,0x1,0x1,0x1,0x1,0x1) ,0x0,0x0,0x0,0x0,0x0,0x1100
mutrMRG_N_1, 120 ,    0x100 , 0x0 , 0x3 , 0xa , (0x1,0x1,0x1,0x1,0x1,0x1,0x1,0x1) ,0x0,0x0,0x0,0x0,0x0,0x1100
mutrMRG_N_1, 121 ,    0x100 , 0x0 , 0x3 , 0xa , (0x1,0x1,0x1,0x1,0x1,0x1,0x1,0x1) ,0x0,0x0,0x0,0x0,0x0,0x1100
mutrMRG_N_1, 122 ,    0x100 , 0x0 , 0x3 , 0xa , (0x1,0x1,0x1,0x1,0x1,0x1,0x1,0x1) ,0x0,0x0,0x0,0x0,0x0,0x1100
mutrMRG_N_1, 123 ,    0x100 , 0x0 , 0x3 , 0xa , (0x1,0x1,0x1,0x1,0x1,0x1,0x1,0x1) ,0x0,0x0,0x0,0x0,0x0,0x1100
[phnxmutr@va020 ~]$
[phnxmutr@va020 ~]$
```

Noise level (Fake hit rate)

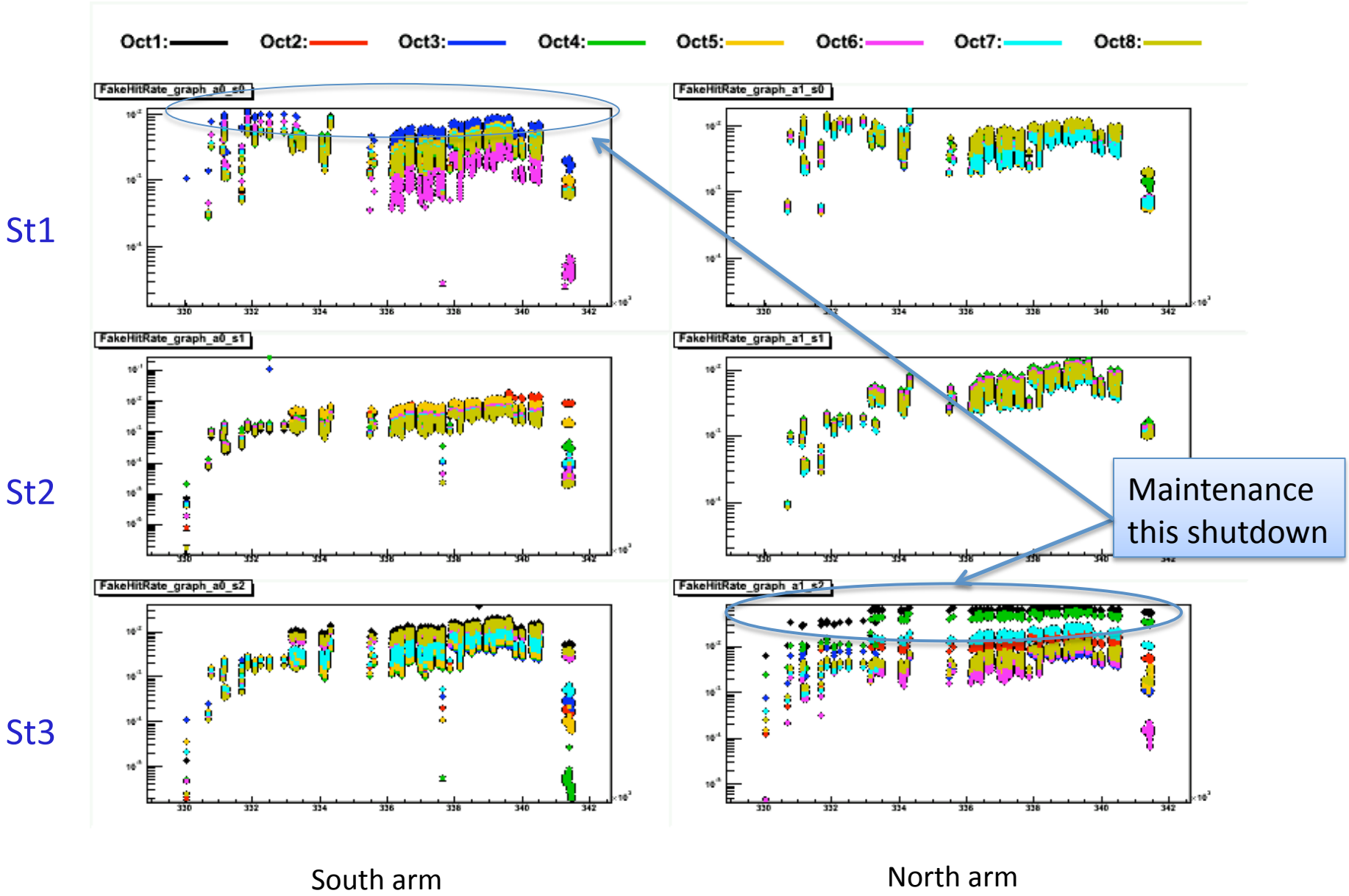


AuAu Run starts

Fake hit rate is sampled from abort gap

- Trigger entry threshold set by 10k → No statistical issues in the plot
- Noise level is negligibly small to form significant accidental coincidence triggers.

Noise level (Fake hit rate)



Trigger timing

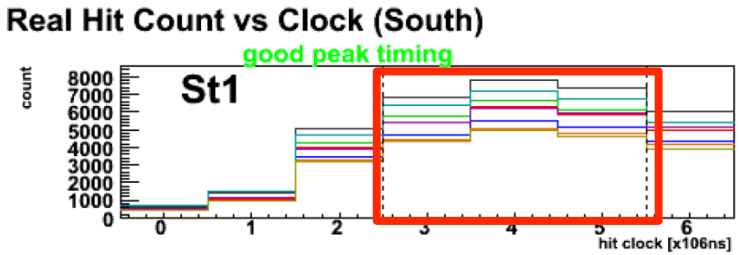
- Non-enough timing resolution of MuTr
- Based on trigger timing study

→ MuTr hit signal(with extended clock width)

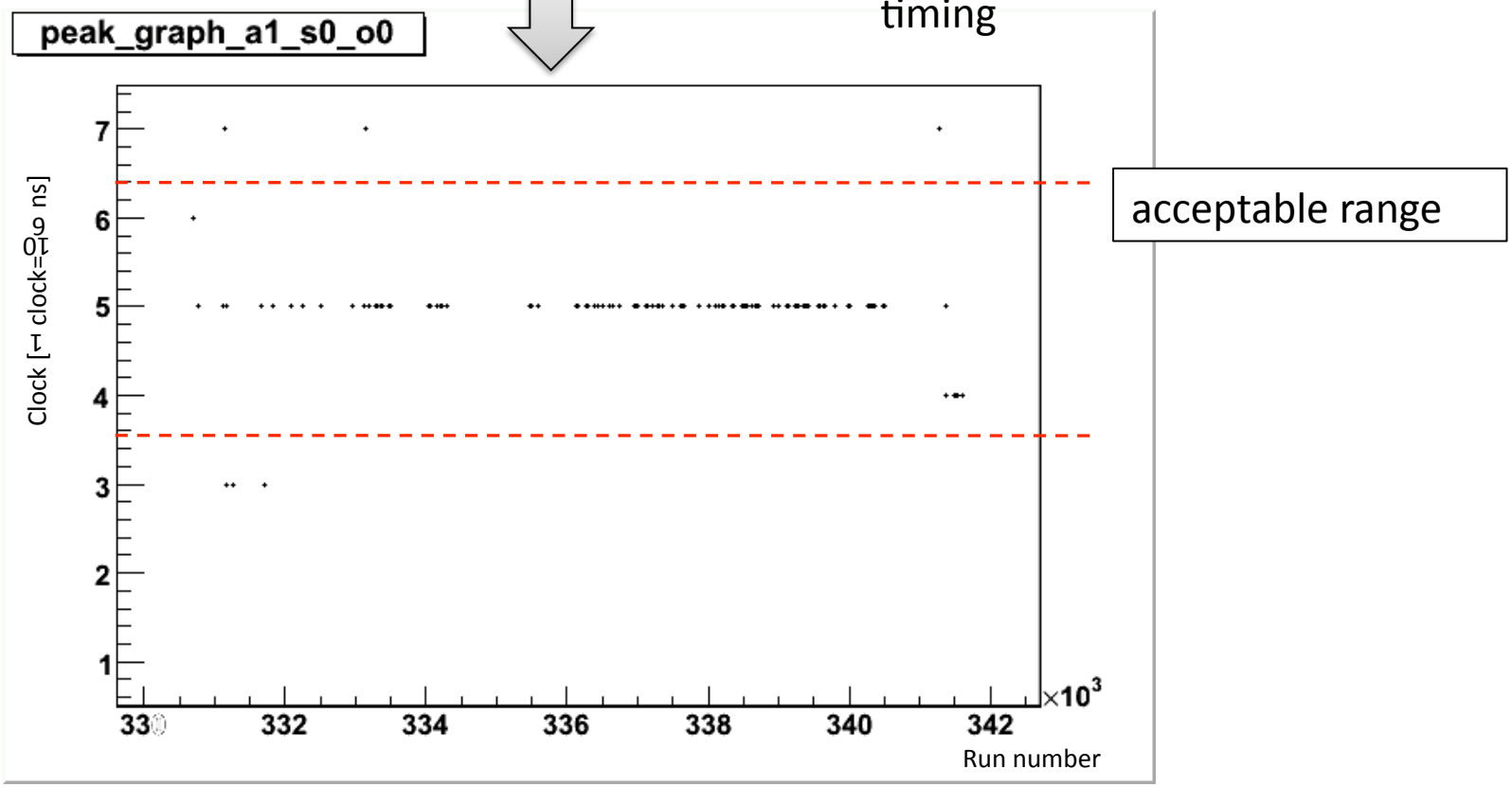
RPC hit signal (good timing resolution)

} **OR logic**

Trigger timing



- Trigger width setting : 3
- stable overall
- Hardware failures or inadequate delay tune can introduce a sloppy timing



Trigger timing

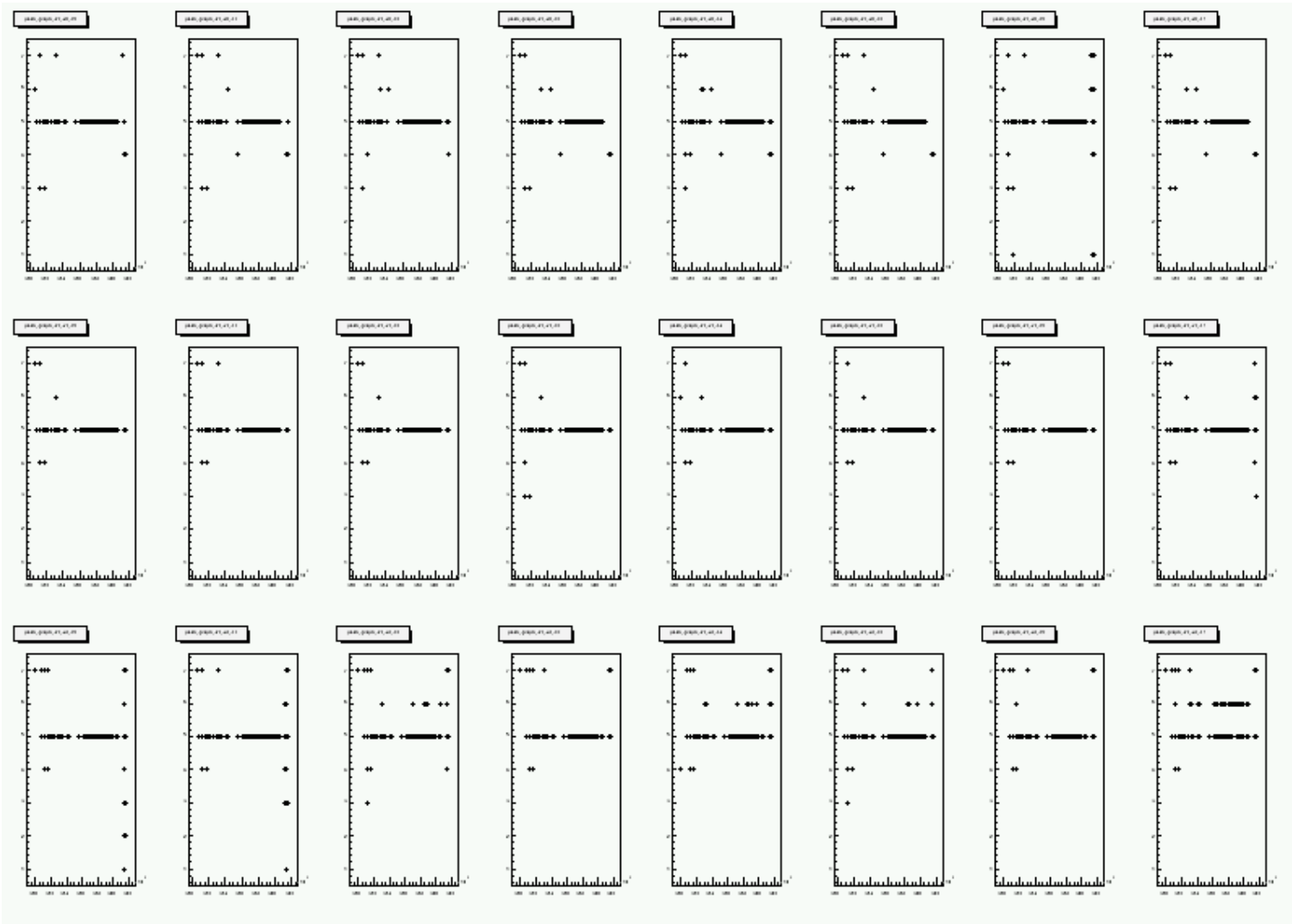
Octant 1~8 →

Same graph for all octants of North arm

St1

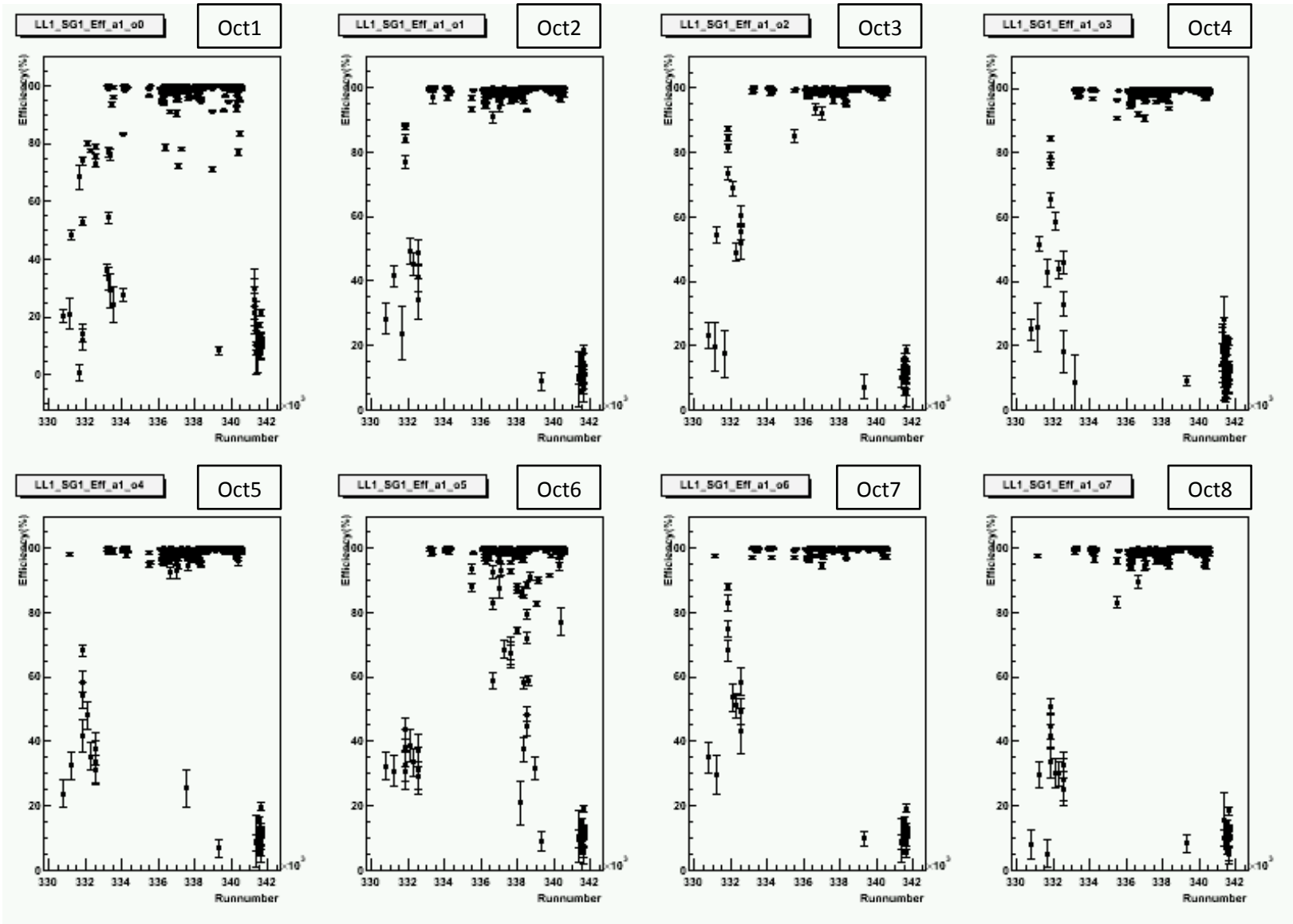
St2

St3



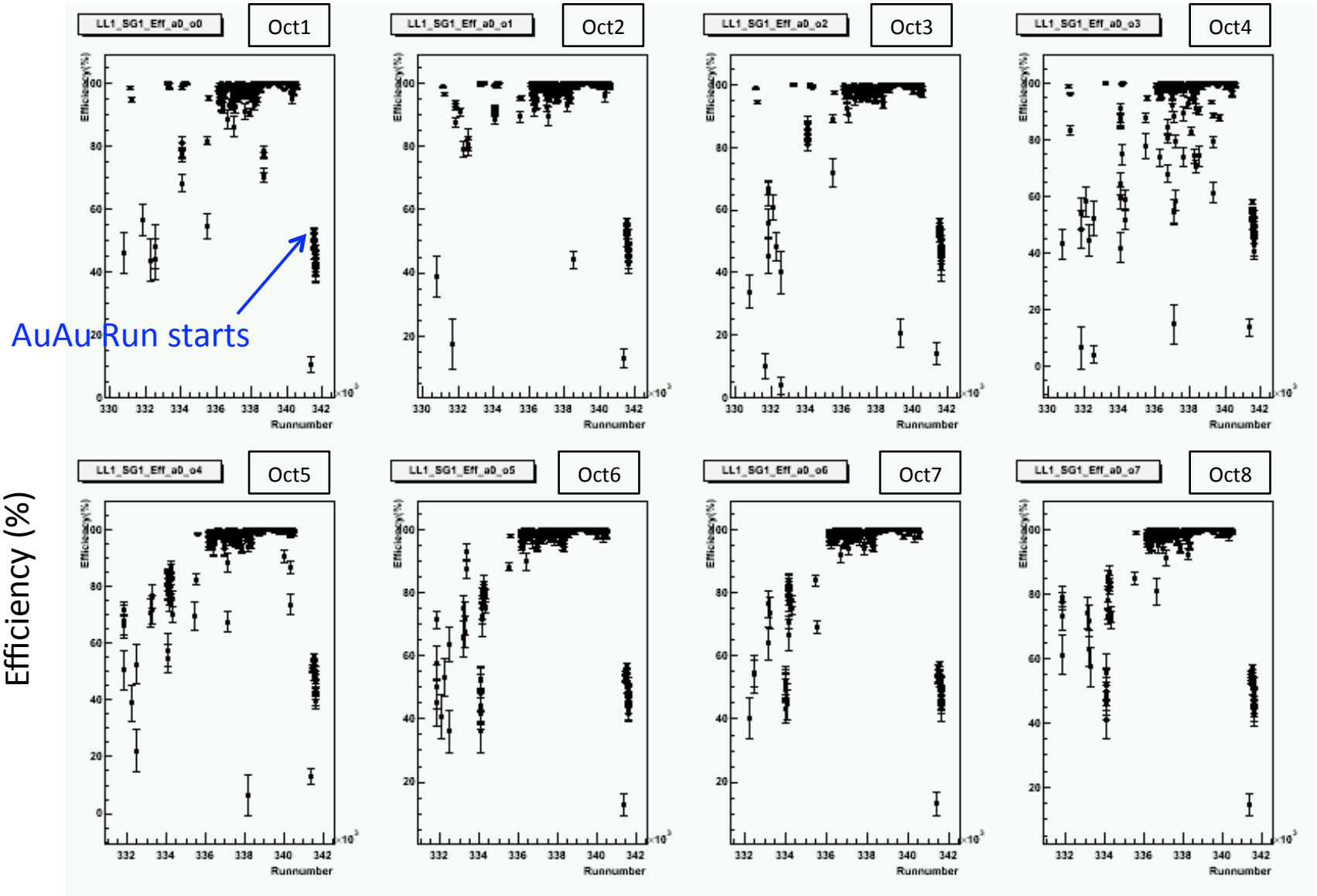
Trigger efficiency - North

Trigger entries threshold: >100



Trigger efficiency – South

Trigger entries threshold: >100

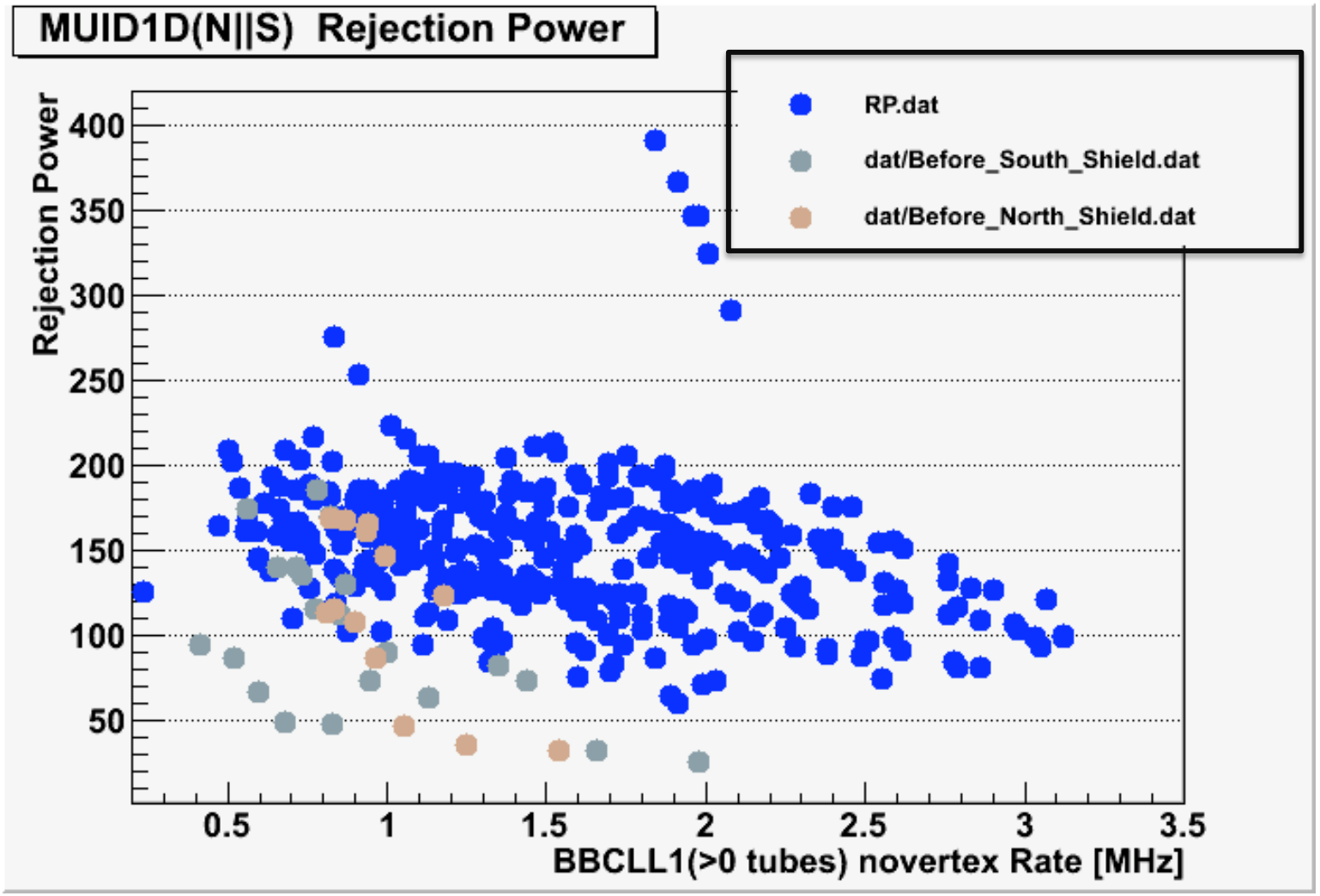


Operation/Stability Summary

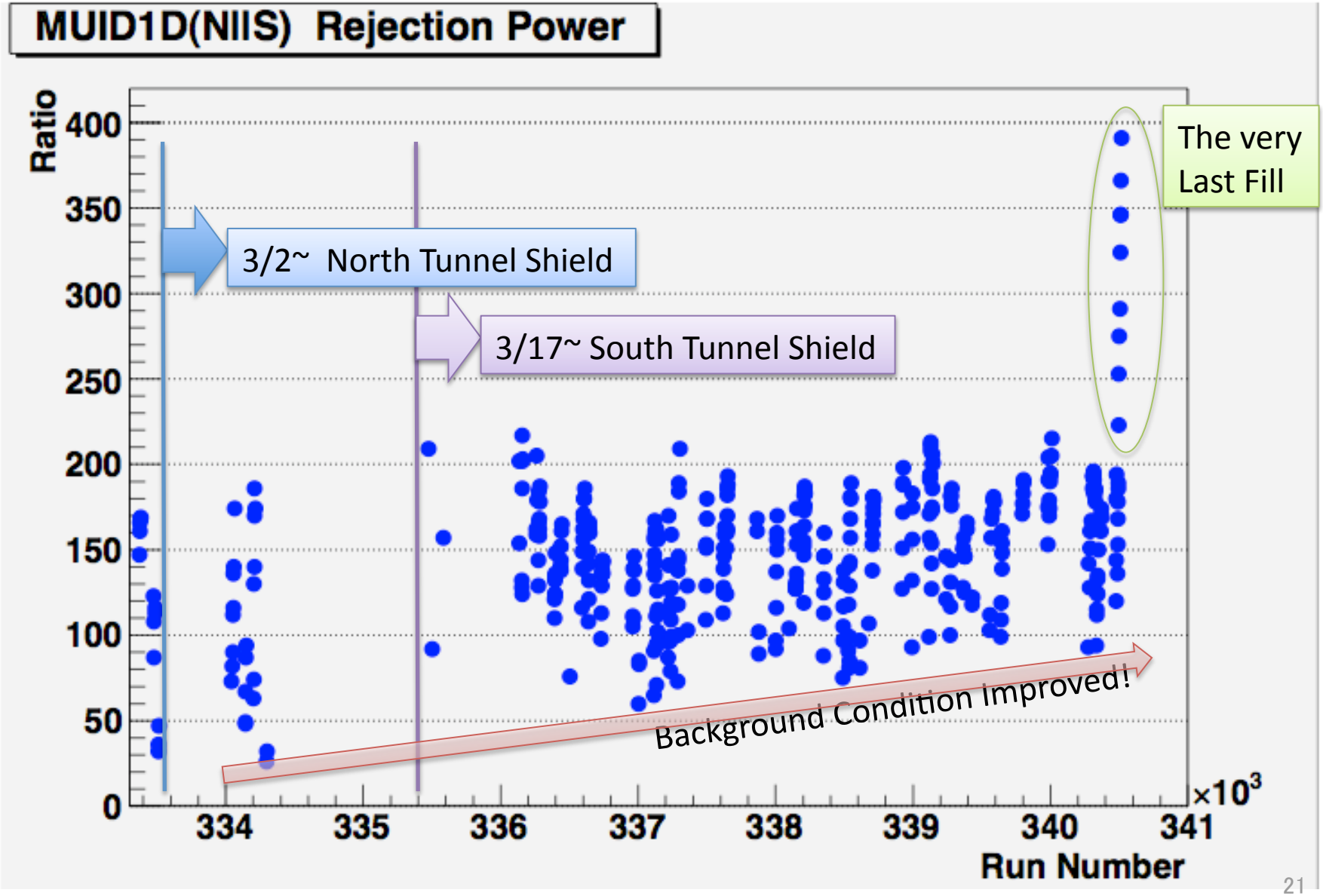
- Disabled ADTX
  - North St-3, Oct-3, Gap-2
  - North St-3, Oct-3, Chs-1, Brd-1
- Frequent Errors
  - Two ADTX boards in South and North (one each)
- High Fake Rates
  - South St-1, Oct-3, Gap-2
  - North St-1, Oct-1, Gap-3
  - North St-1, Oct-8, Gap-1
  - North St-3, Oct-1, Gap-2

Rejection Performance

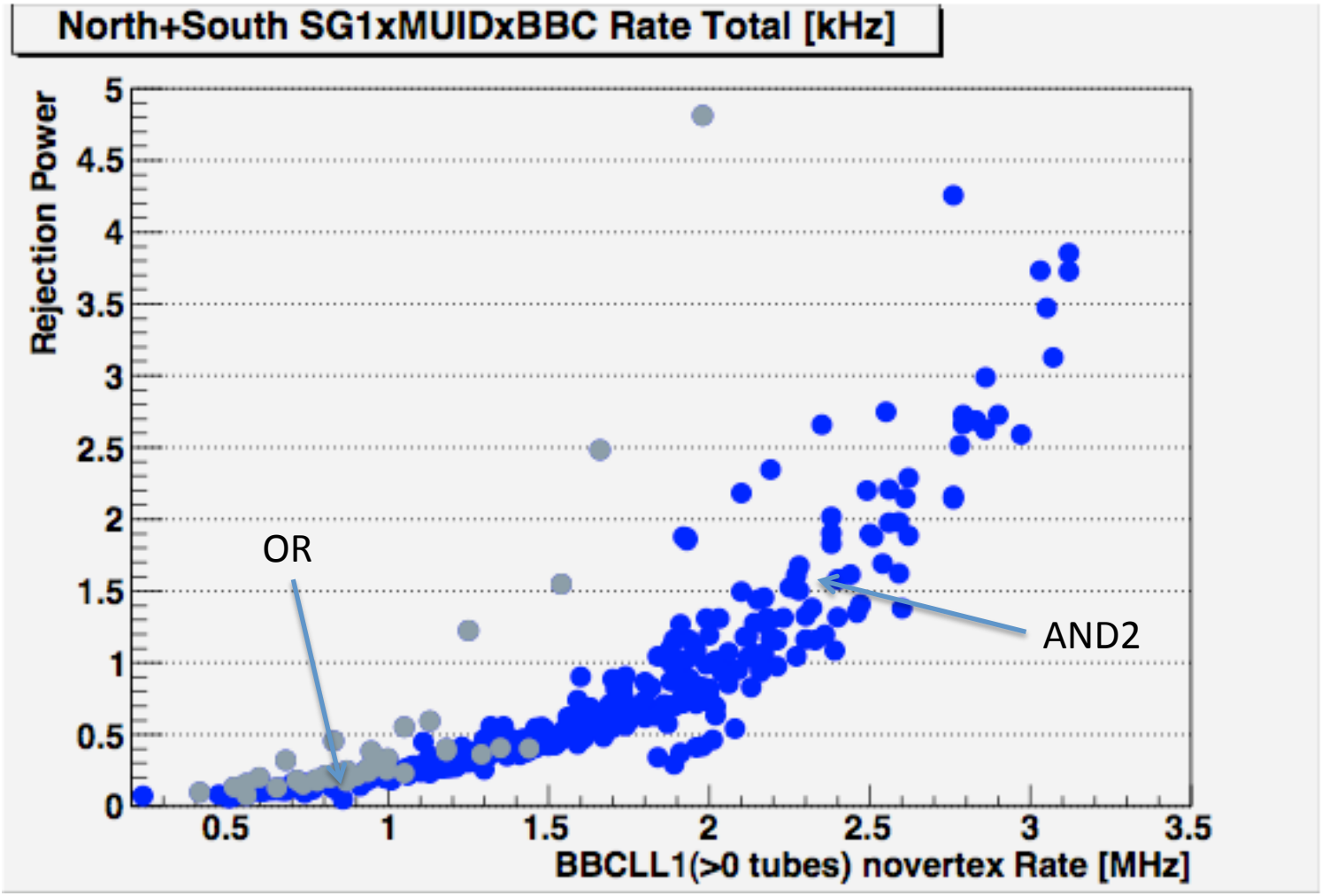
MUID Rejection Performance

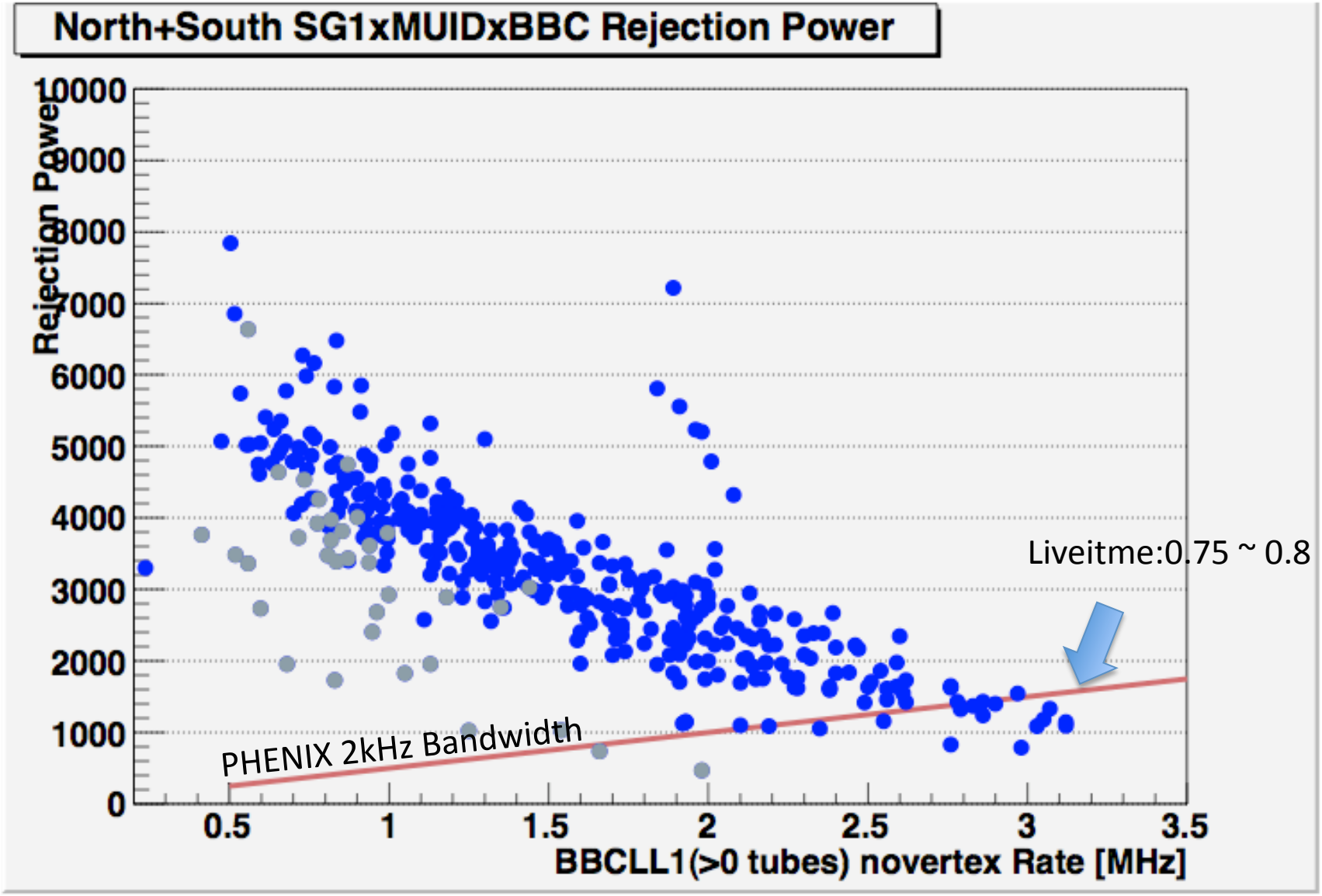


MUID Rejection Power

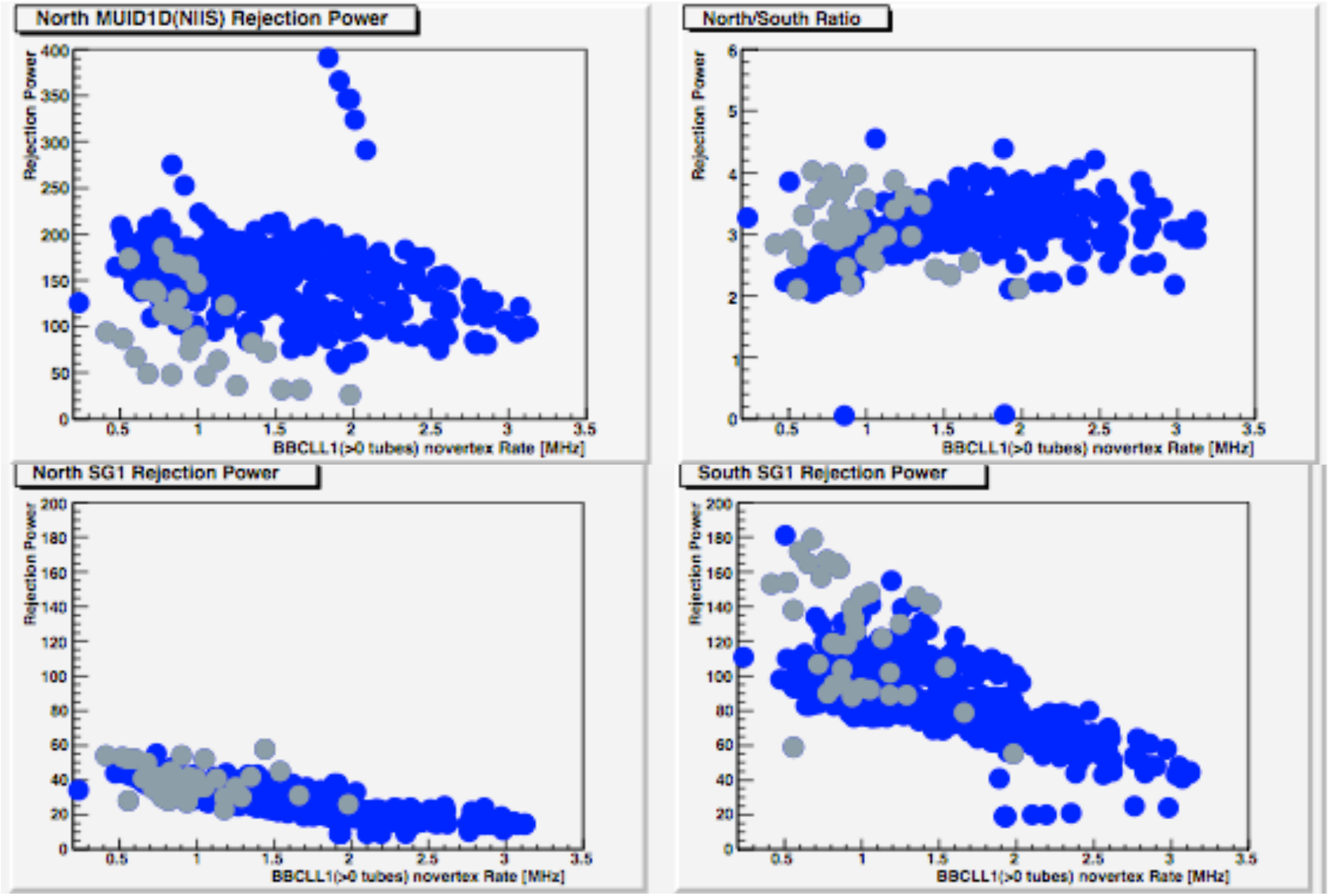


SG1 Raw Trigger Rates




North+South SG1xMUIDxBBC Rejection Power
Rejection Power
10000
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
0.5
1
1.5
2
2.5
3
3.5
BBCLL1(>0 tubes) novertex Rate [MHz]
PHENIX 2kHz Bandwidth
Liveitme:0.75 ~ 0.8

North and South



OR -> AND2 didn't earn much rejection power to SG1

OR vs. AND2 Logic

From Yoshinori Fukao's Run9 Analysis

run	Thre.	BBC (novtx)	MuID (N|S) RP	Δs=0 w/ clus.		Δs=1 w/ clus.	
				Eff.	RP	Eff.	RP
278358	40mV	1.31M	96.1		47.1		18.4
278384	40mV	1.03M	104.4	0.374	86.0	0.790	24.2
278409	40mV	0.70M	112.7		95.4		29.1

OR

run	Thre.	BBC (novtx)	MuID (N|S) RP	Δs=0 w/ clus.		Δs=1 w/ clus.	
				Eff.	RP	Eff.	RP
280043	40mV	1.81M	73.0		139.0		43.9
280075	40mV	1.43M	97.2	0.298	110.9	0.689	32.5
280079	40mV	1.21M	102.6		107.0		45.5

AND2

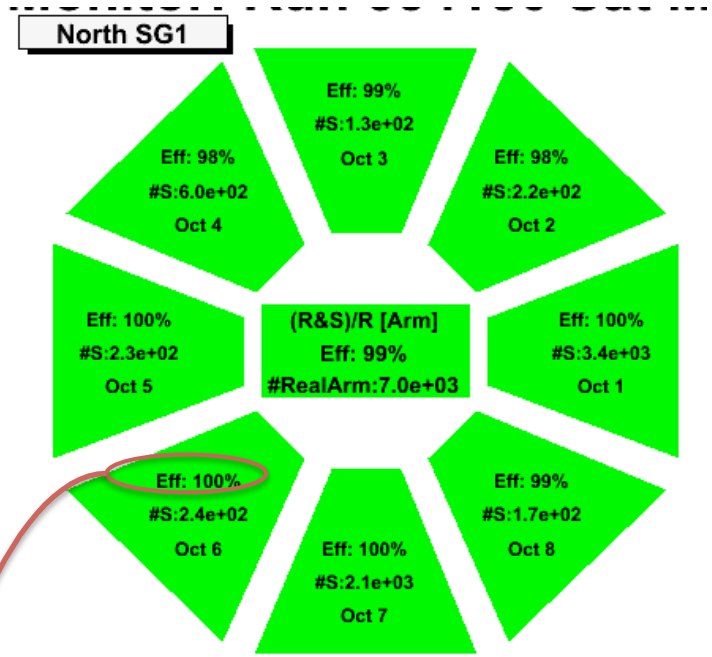
OR .vs AND2 supposed to be non-trivial trade off between efficiency and RP.

Summary

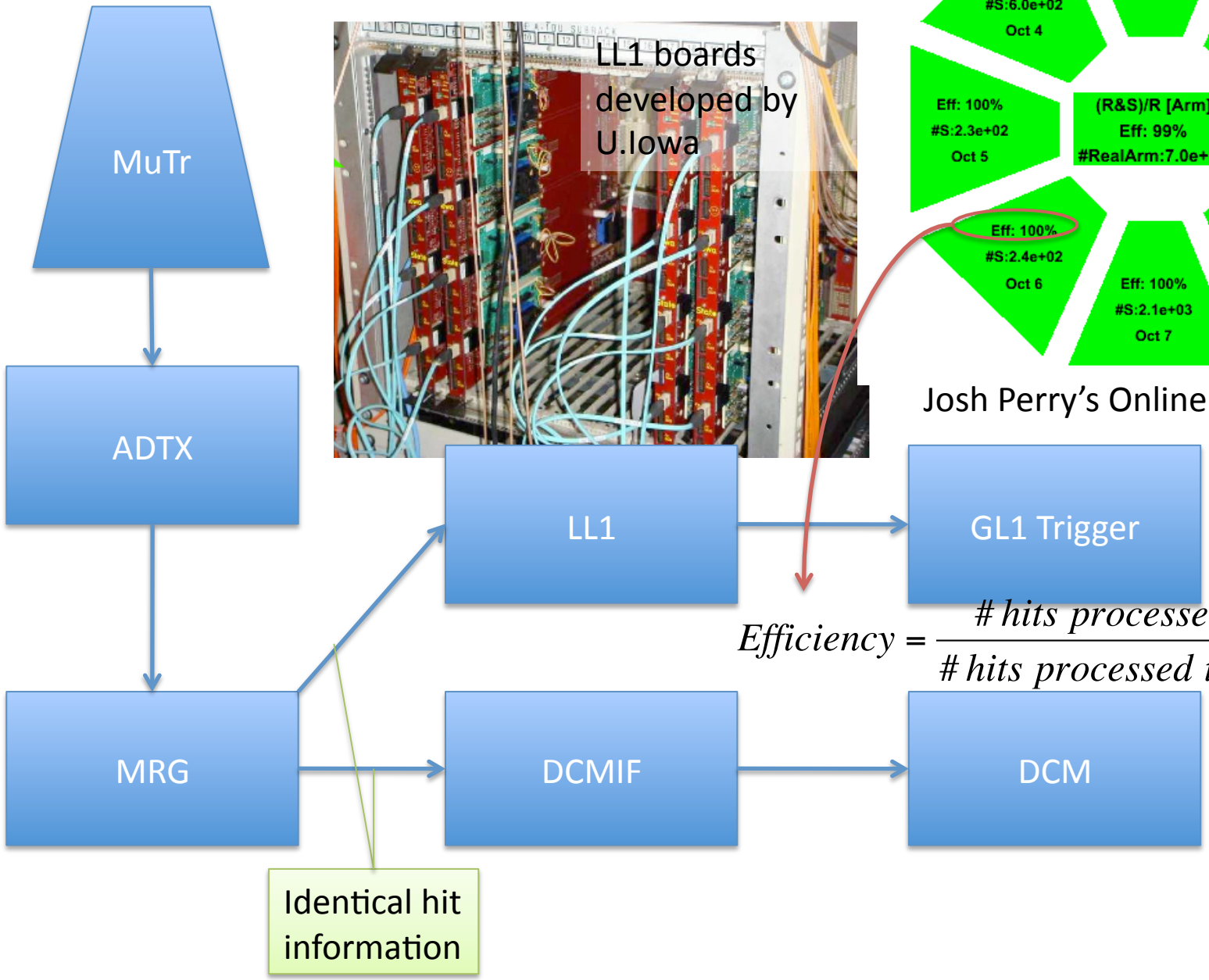
- SG1 trigger has been stably operated thru Run11. Only minor issues are encountered.
- North Rates .vs South Rates needs to be understood.
- OR / AND2 RP looks inconsistent with Run9 expectation.
- Timing alignment between Stations before signals are sent to LL1

backups

LL1 Efficiencies



Josh Perry's Online Monitor



$$Efficiency = \frac{\#\ hits\ processed\ thru\ LL1}{\#\ hits\ processed\ thru\ DCMIF}$$