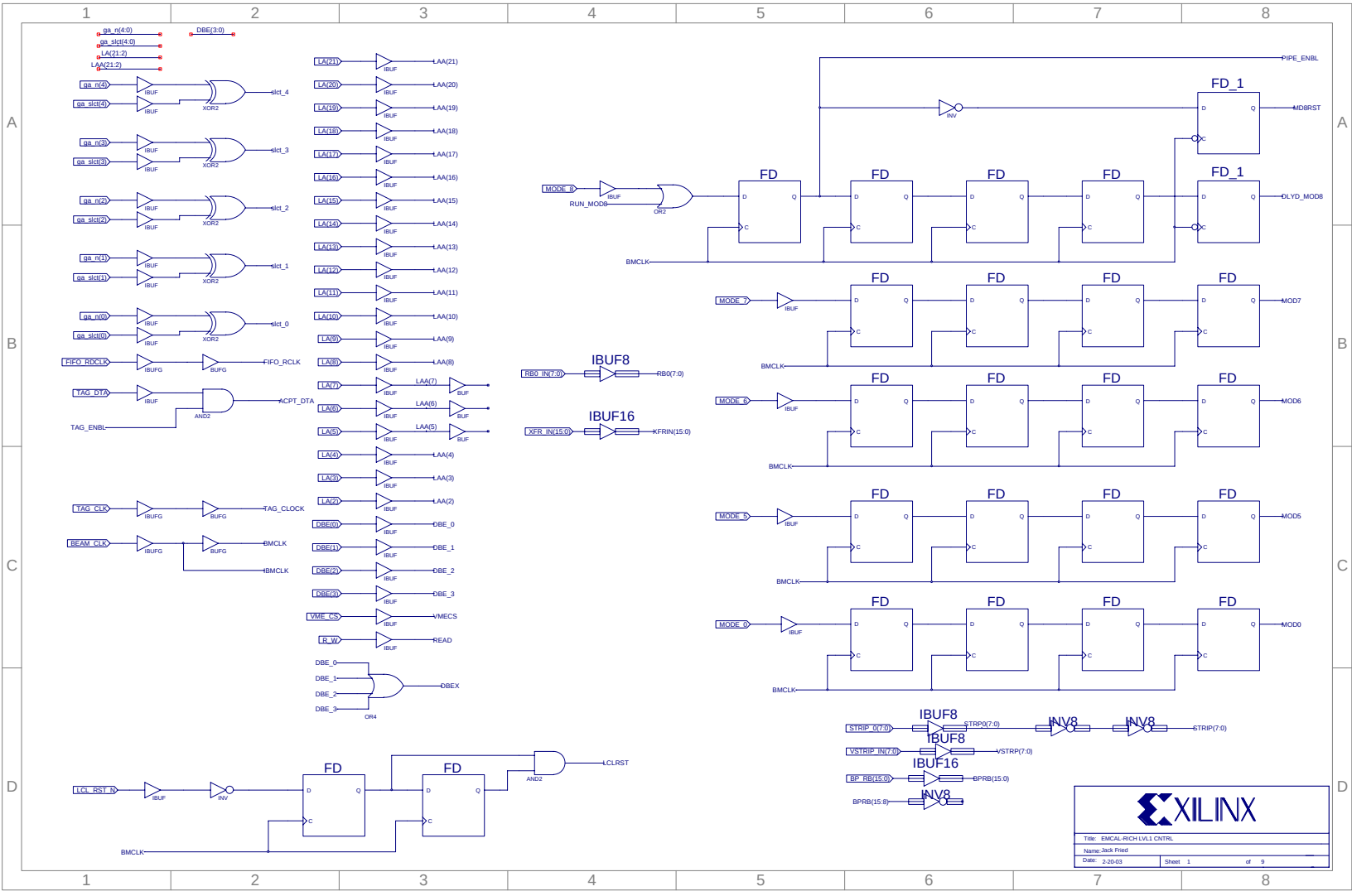
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LAA(21:2)
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ga_n(0)
ga_slct(0)
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XOR2
slct_4
slct_3
slct_2
slct_1
slct_0
FIFO_RDCLK
IBUFG
BUFG
FIFO_RCLK
TAG_DTA
AND2
ACPT_DTA
TAG_ENBL
TAG_CLK
TAG_CLOCK
BEAM_CLK
BMCLK
BMCLK
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LA(20)
LA(19)
LA(18)
LA(17)
LA(16)
LA(15)
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LAA(8)
LAA(7)
LAA(6)
LAA(5)
LAA(4)
LAA(3)
LAA(2)
BUF
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DBE(1)
DBE(2)
DBE(3)
DBE_0
DBE_1
DBE_2
DBE_3
VME_CS
R_W
VMECS
READ
DBE_0
DBE_1
DBE_2
DBE_3
OR4
DBEX
IBUF8
RB0_IN(7:0)
RB0(7:0)
IBUF16
XFR_IN(15:0)
KFRIN(15:0)
PIPE_ENBL
INV
FD_1
MD8RST
MODE_8
RUN_MOD8
OR2
FD
D
Q
C
BMCLK
DLYD_MOD8
MODE_7
MOD7
MODE_6
MOD6
MODE_5
MOD5
MODE_0
MOD0
STRIP_0(7:0)
STRP0(7:0)
INV8
STRIP(7:0)
VSTRIP_IN(7:0)
VSTRP(7:0)
BP_RB(15:0)
BPRB(15:0)
BPRB(15:8)
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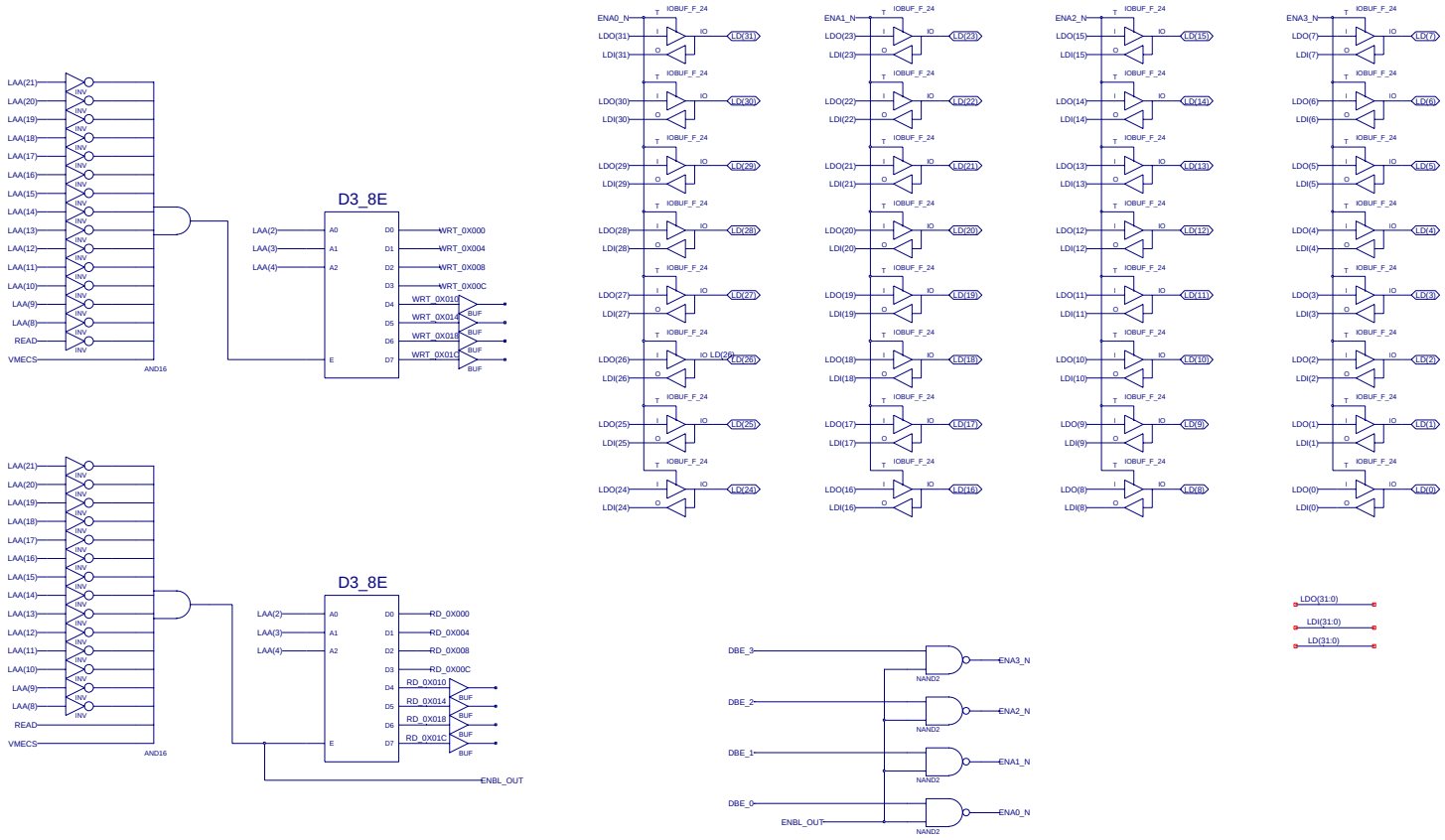
LCLRST
XILINX
Title: EMCAL-RICH LVL1 CNTRL
Name: Jack Fried
Date: 2-20-03
Sheet 1 of 9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LAA(8)
READ
VMECS
INV
AND16
D3_8E
LAA(2)
LAA(3)
LAA(4)
A0
A1
A2
E
D0
D1
D2
D3
D4
D5
D6
D7
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WRT_0X004
WRT_0X008
WRT_0X00C
WRT_0X010
WRT_0X014
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BUF
RD_0X000
RD_0X004
RD_0X008
RD_0X00C
RD_0X010
RD_0X014
RD_0X018
RD_0X01C
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ENA1_N
ENA2_N
ENA3_N
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LD(1)
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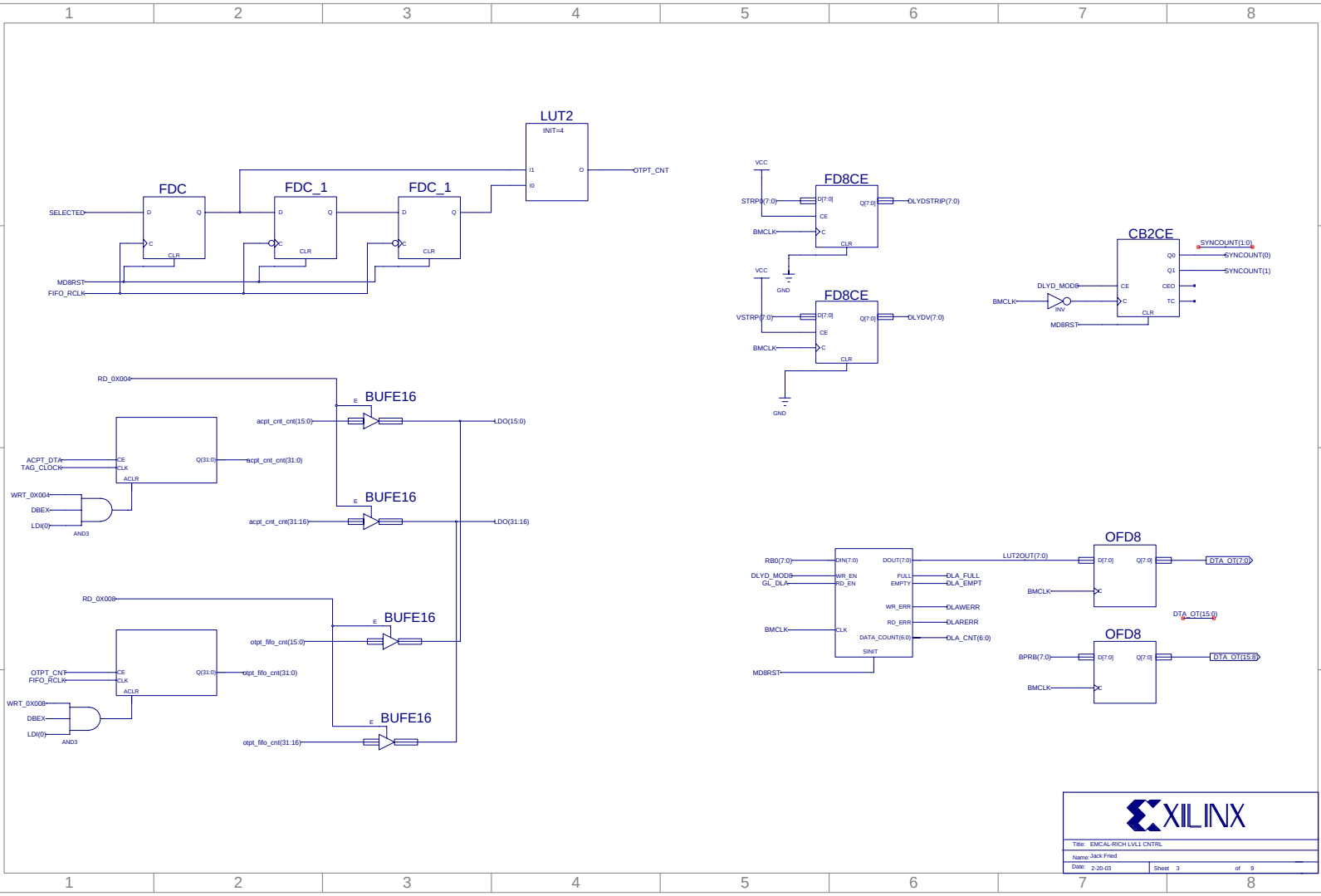
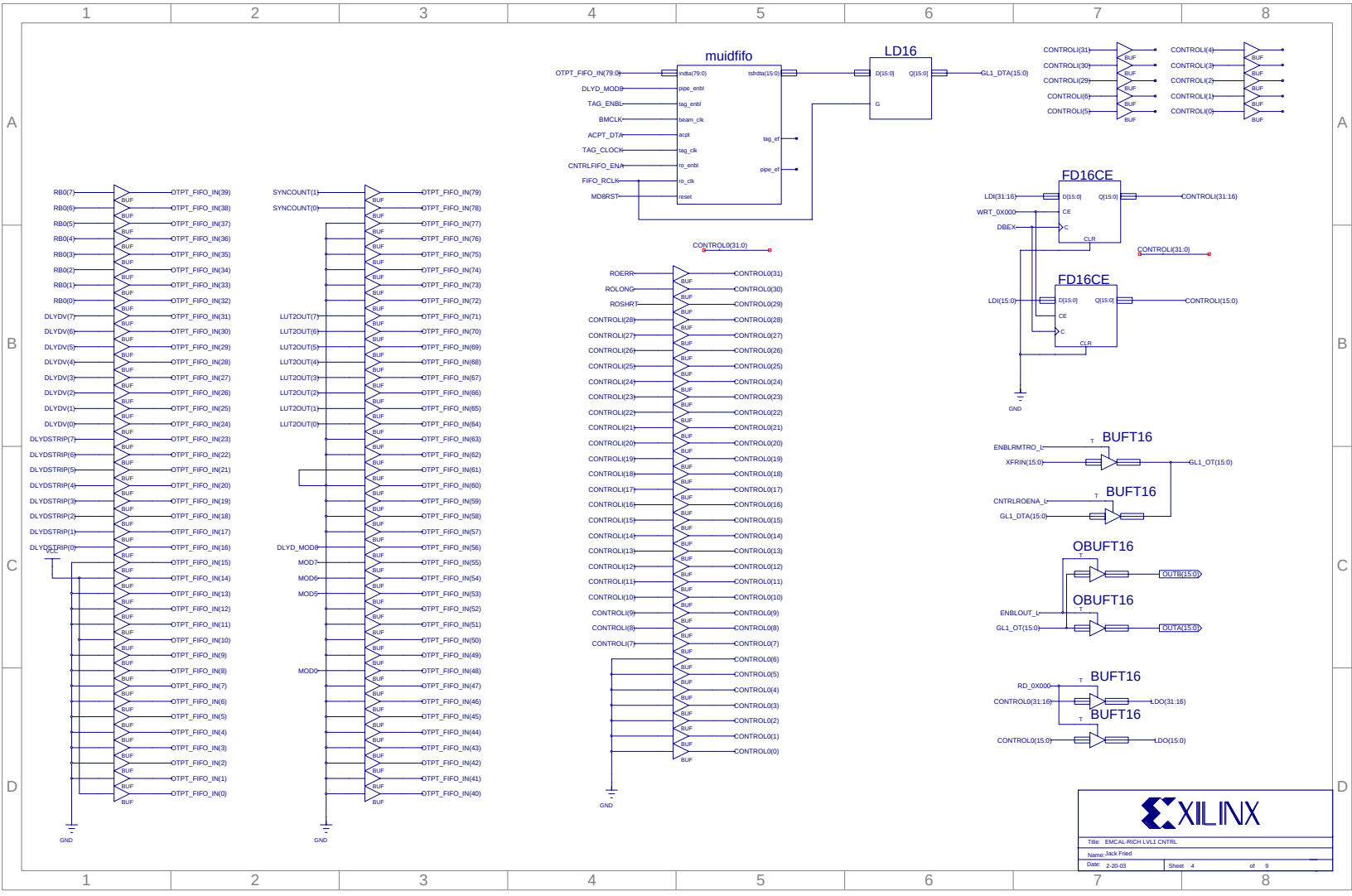
DBE_2
DBE_1
DBE_0
NAND2
XILINX
Title: EMCAL-RICH LVL1 CNTRL
Name: Jack Fried
Date: 2-20-03
Sheet 2 of 9



XILINX

Title:	EMCAL-RICH LVL1 CNTRL
Name:	Jack Fried
Date: 2-20-03	Sheet 3 of 9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indta(79:0)
tsfrdta(15:0)
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TAG_ENBL
tag_enbl
BMCLK
beam_clk
ACPT_DTA
acpt
TAG_CLOCK
tag_clk
CNTRLFIFO_ENA
ro_enbl
FIFO_RCLK
ro_clk
MD8RST
rtcset
tag_ef
pipe_ef
LD16
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Q[15:0]
G
GL1_DTA(15:0)
CONTROLI(31)
CONTROLI(30)
CONTROLI(29)
CONTROLI(6)
CONTROLI(5)
CONTROLI(4)
CONTROLI(3)
CONTROLI(2)
CONTROLI(1)
CONTROLI(0)
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FD16CE
LDI(31:16)
WRT_0X000
DBEX
D[15:0]
Q[15:0]
CE
C
CLR
CONTROLI(31:16)
CONTROLI(31:0)
CONTROL0(31:0)
LDI(15:0)
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GL1_DTA(15:0)
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DLYDV(1)
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DLYDSTRIP(5)
DLYDSTRIP(4)
DLYDSTRIP(3)
DLYDSTRIP(2)
DLYDSTRIP(1)
DLYDSTRIP(0)
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LUT2OUT(4)
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MOD7
MOD6
MOD5
MOD0
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OTPT_FIFO_IN(46)
OTPT_FIFO_IN(45)
OTPT_FIFO_IN(44)
OTPT_FIFO_IN(43)
OTPT_FIFO_IN(42)
OTPT_FIFO_IN(41)
OTPT_FIFO_IN(40)
XILINX
Title: EMCAL-RICH LVL1 CNTRL
Name: Jack Fried
Date: 2-20-03
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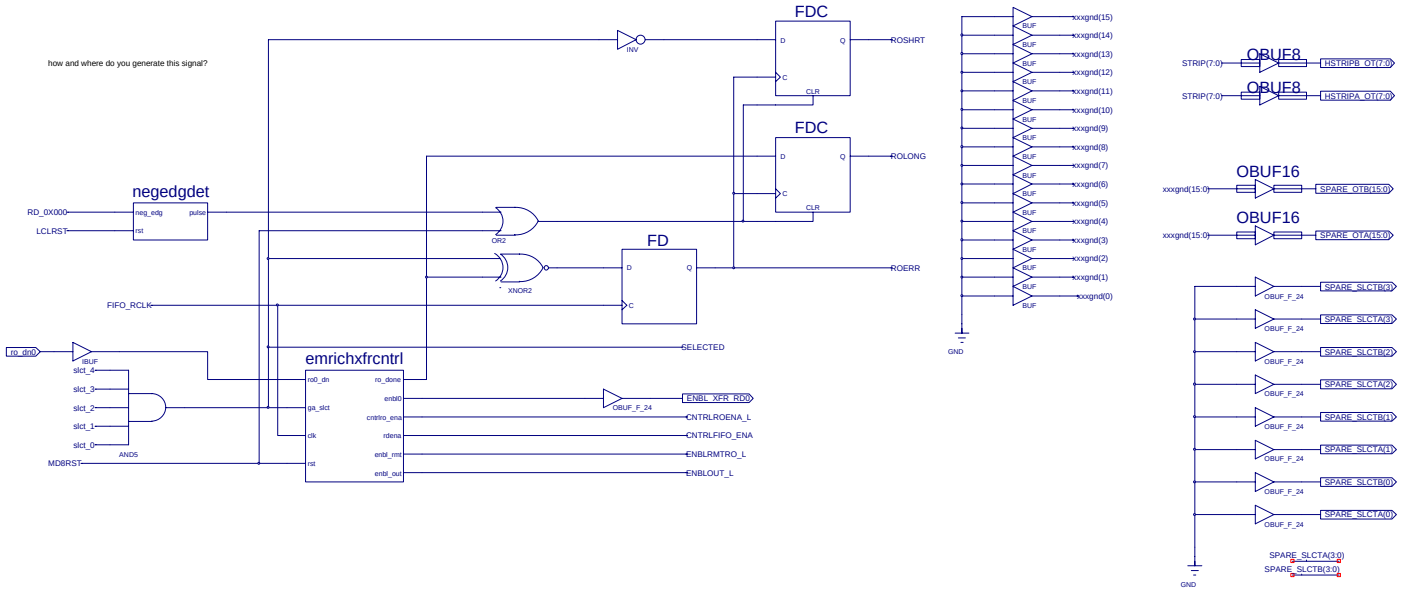

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Title:	EMCAL-RICH LVL1 CNTRL
Name:	Jack Fried
Date:	2-20-03
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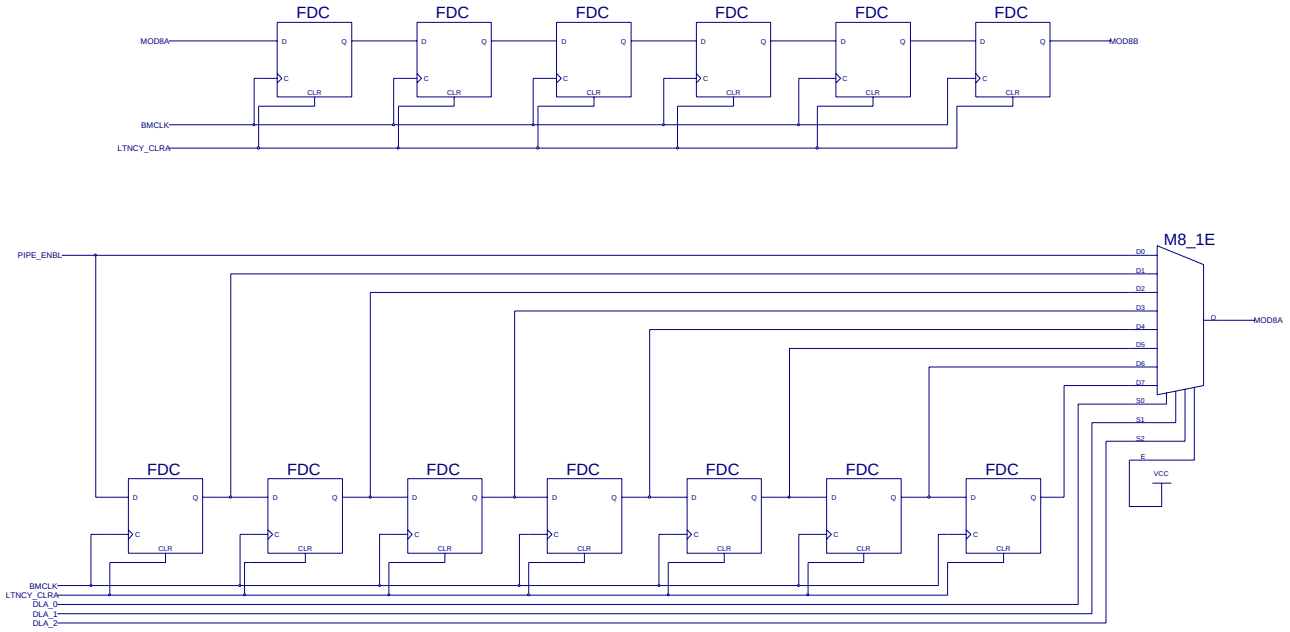
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MOD8B
D
Q
C
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BMCLK
LTNCY_CLRA
M8_1E
PIPE_ENBL
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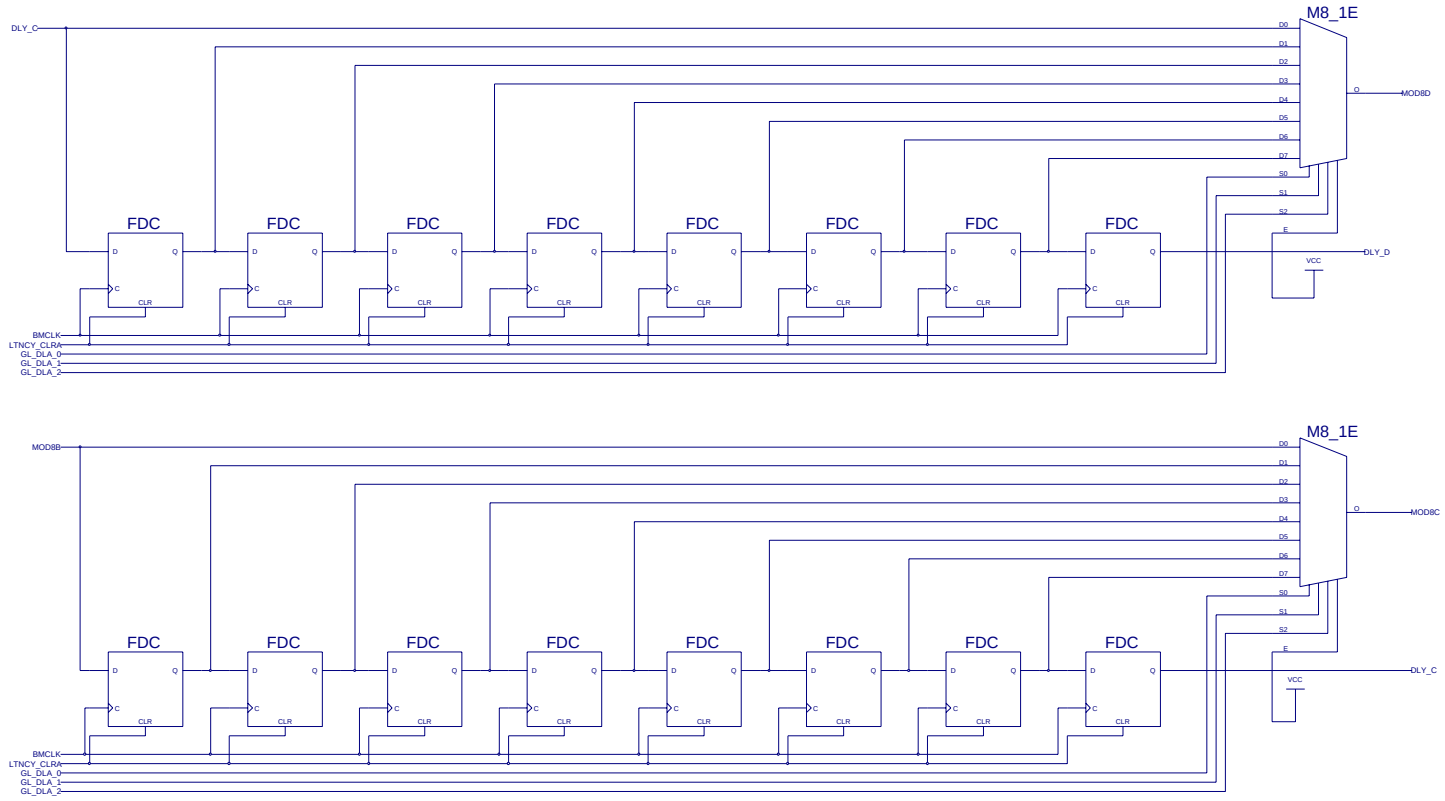
D1
D2
D3
D4
D5
D6
D7
S0
S1
S2
E
O
VCC
DLA_0
DLA_1
DLA_2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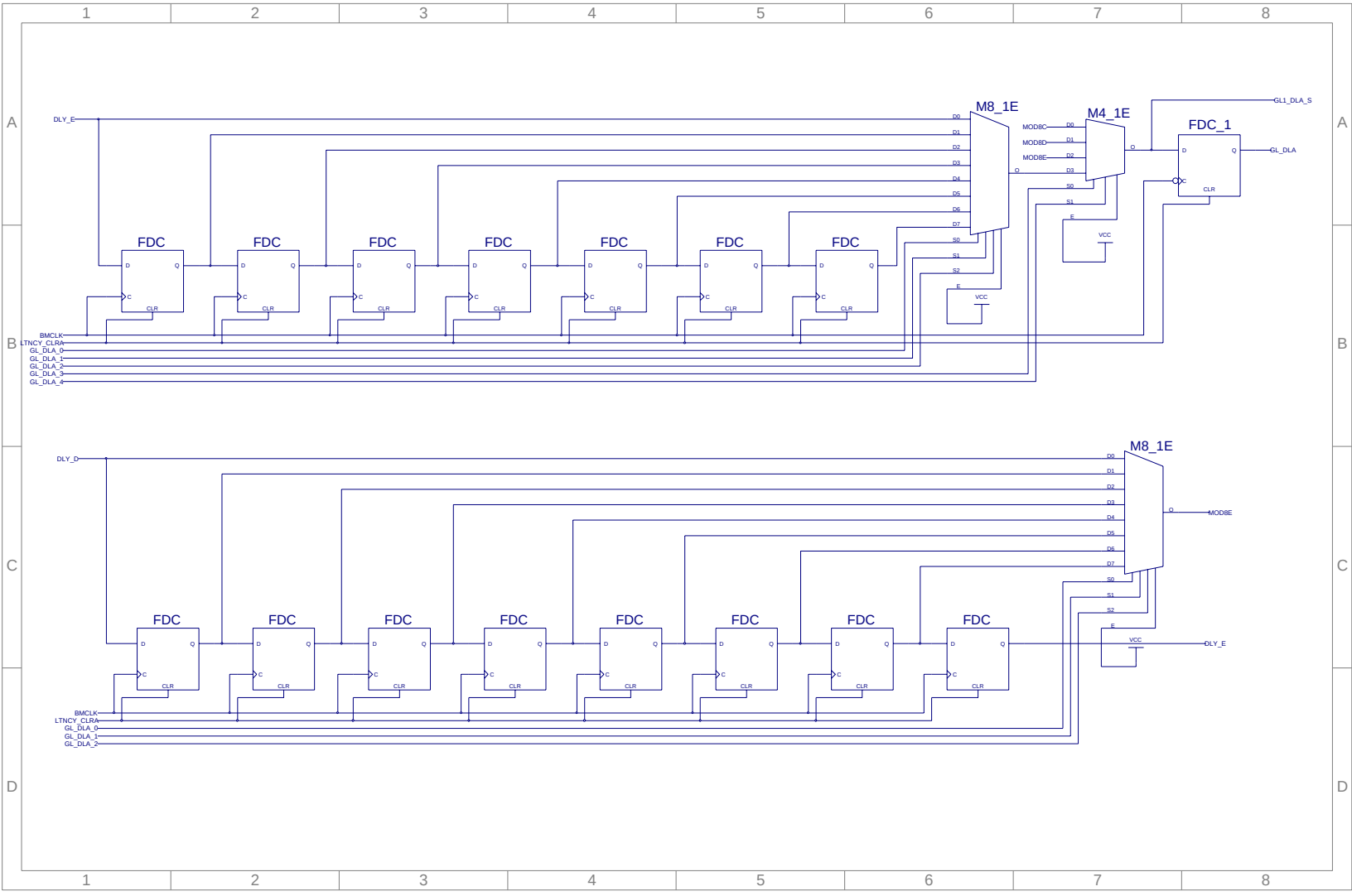
D3
D4
D5
D6
D7
S0
S1
S2
E
O
MOD8D
VCC
FDC
D
Q
C
CLR
DLY_D
BMCLK
LTNCY_CLRA
GL_DLA_0
GL_DLA_1
GL_DLA_2
M8_1E
MOD8B
MOD8C
DLY_C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GL_DLA
MOD8C
MOD8D
MOD8E
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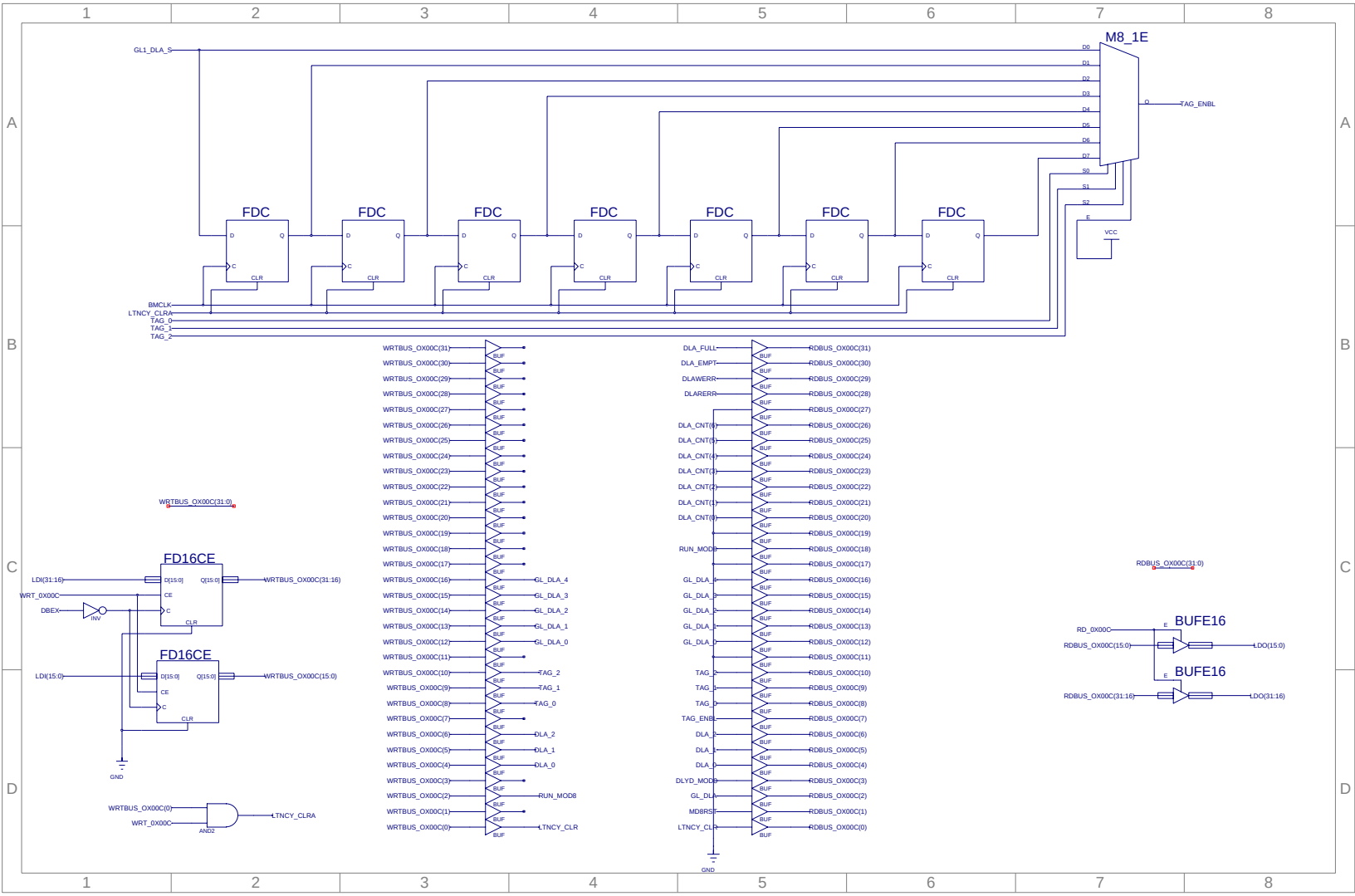
BMCLK
LTNCY_CLRA
GL_DLA_0
GL_DLA_1
GL_DLA_2
GL_DLA_3
GL_DLA_4
VCC
DLY_D
DLY_E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D2
D3
D4
D5
D6
D7
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S1
S2
E
O
TAG_ENBL
VCC
FDC
D
Q
C
CLR
BMCLK
LTNCY_CLRA
TAG_0
TAG_1
TAG_2
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WRTBUS_OX00C(31)
WRTBUS_OX00C(30)
WRTBUS_OX00C(29)
WRTBUS_OX00C(28)
WRTBUS_OX00C(27)
WRTBUS_OX00C(26)
WRTBUS_OX00C(25)
WRTBUS_OX00C(24)
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GL_DLA_2
GL_DLA_1
GL_DLA_0
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TAG_1
TAG_0
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DLA_1
DLA_0
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DLA_1
DLA_0
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RDBUS_OX00C(3)
RDBUS_OX00C(2)
RDBUS_OX00C(1)
RDBUS_OX00C(0)
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Q[15:0]
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C
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LDI(15:0)
WRTBUS_OX00C(15:0)
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WRTBUS_OX00C(0)
WRT_0X00C
AND2
LTNCY_CLRA
RDBUS_OX00C(31:0)
BUFE16
RD_0X00C
RDBUS_OX00C(15:0)
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LDO(31:16)