

**Technical Design Report**  
**on**  
**Amplifier-Discriminator board**  
**and**  
**Data Transfer board**  
**for the MuTr FEE upgrade**

version 3.3

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# Chapter 1

## Overview

This document describes the proposed new trigger using signals from Muon Tracking Chambers (MuTr). In combination with the Resistive Plate Counters (RPCs) to be built with NSF funding, the new trigger will provide momentum sensitive muon trigger. The trigger will be crucial to have the  $W$  measurements where high momentum muon is the key signal. Since current muon trigger will fire with any muon above 2 GeV/ $c$ , it will not provide required rejection factor for 500 GeV running, which is about 10,000. By using the hit information from MuTr chambers online, we will select the high momentum tracks among which we expect to have signal muons from  $W$  decays.

The MuTr chambers are cathode strip chambers with the 5 mm pitch. Every other strip is read out with low noise amplifier-analog memory cell-digitizer chain to obtain position resolution of  $\sim 100 \mu\text{m}$ . We propose to divide the signal into two paths; existing read out path and newly proposed amplifier discriminator board (MuTRG-AD). The discriminated pulses from MuTRG-AD are serialized every 64 channels using asynchronous FI/FO and transformed to optical signals on the data transfer boards (MuTRG-TX) to be sent through optical fibers to the counting house. The serial data are received, deserialized and re-formatted on the data merger board (MuTRG-MRG) then sent to PHENIX DAQ framework including Data Collection Modules (DCMs) and Local Level-1 (LL1) trigger boards. Figure 1.1 displays the schematic diagram of the proposed electronics. Figure 1.2 shows the picture of MuTRG-AD and MuTRG-TX which were installed for the cosmic ray test in summer, 2007.

### Review subjects

While our test is based on the separate boards of MuTRG-AD and MuTRG-TX, we are currently working on the combined board, MuTRG-ADTX. Through out the summer test, we

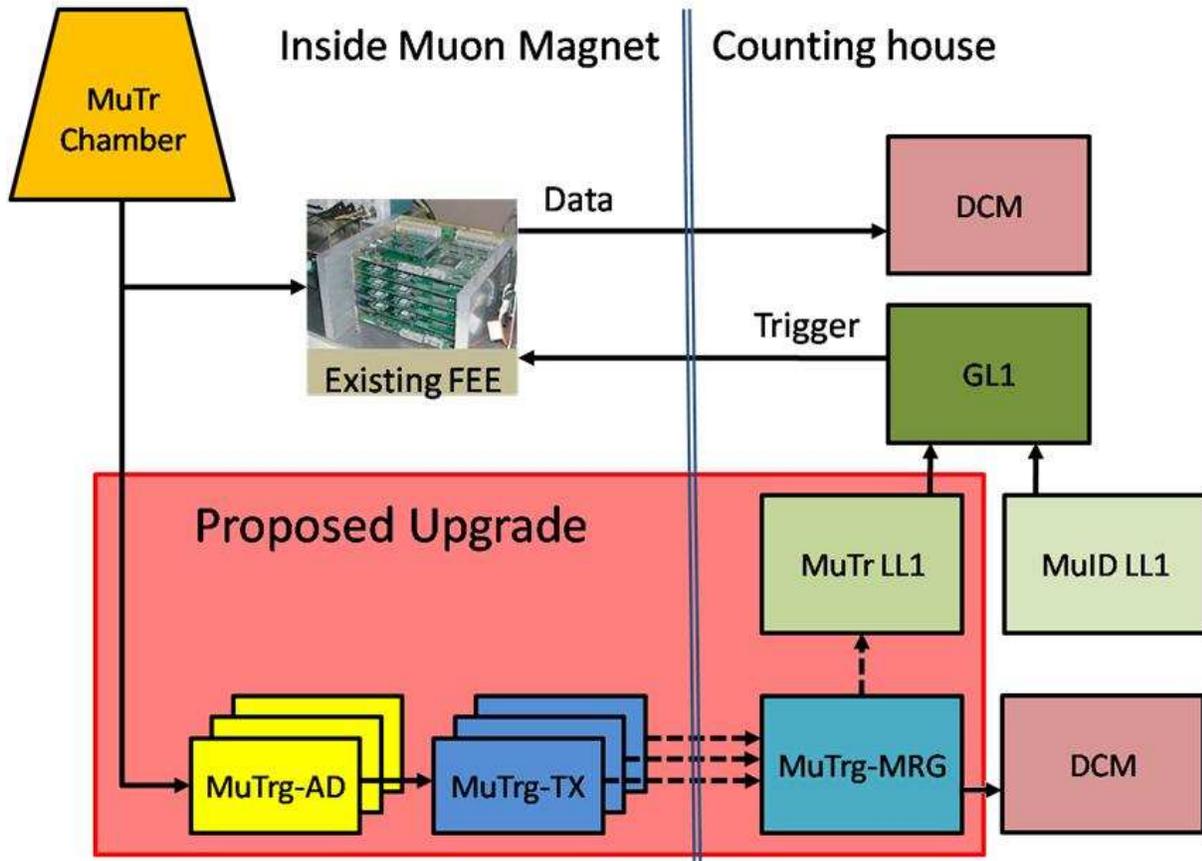


Figure 1.1: Schematic diagram of additional Front-End-Electronics for Muon Trigger.

found that the tight grounding between MuTRG-AD and MuTRG-TX is one of the keys to reduce the noise. Such grounding should be achievable by combining two boards together. In addition, the combined board will simplify the installation process very much. It will also save the cost of cables between MuTRG-AD and MuTRG-TX boards, which is rather significant. Furthermore, the slow control line to the MuTRG-AD and MuTRG-TX boards can be simplified significantly. The test results to be presented in this document are mostly from the separated boards and we expect the same performance with the combined board.

In this review, we would like to ask for an approval for the basic design of the MuTRG-AD and MuTRG-TX with a possible option to combine them together. We are going to provide a supplemental material to demonstrate the performance of the combined boards, when it becomes available. We expect it would happen in a couple of weeks.



Figure 1.2: Additional Front-End-Electronics for Muon Tracking to provide fast signal for new muon trigger. The new modules MuTRG-AD's and MuTRG-TX's were installed for cosmic ray test in summer, 2007.

## 1.1 Requirements for the additional FEE

### 1.1.1 Noise Performance

We propose to split the signal from MuTr chambers roughly 5% to 95% to provide a hit information online using 5% of the signal. One possible concern is an additional noise introduced into the existing read out chain. While currently obtained chamber resolution is about  $300 \mu\text{m}$ , which is assumed to be determined predominantly by the geometrical alignment of the chambers.<sup>1</sup> We have set our goal to stay within  $150 \mu\text{m}$  of chamber resolution so that we

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<sup>1</sup>We have obtained the design value of the chamber resolution  $140 \mu\text{m}$  with both cosmic ray and beam tests. Therefore we believe the current moderate resolution is due to geometrical alignment which still have room for

can still extract the yields of Upsilon substates in the dimuon mass spectrum (see Figure 1.3). This resolution corresponds to a noise level of 1.3% of the typical charge to be induced on the cathode strips by minimum ionizing particle (MIP). Since typical charge after digitization is 140 ADC counts with the existing read out chain, our goal corresponds to a noise level of  $\sim 1.8$  ADC counts.

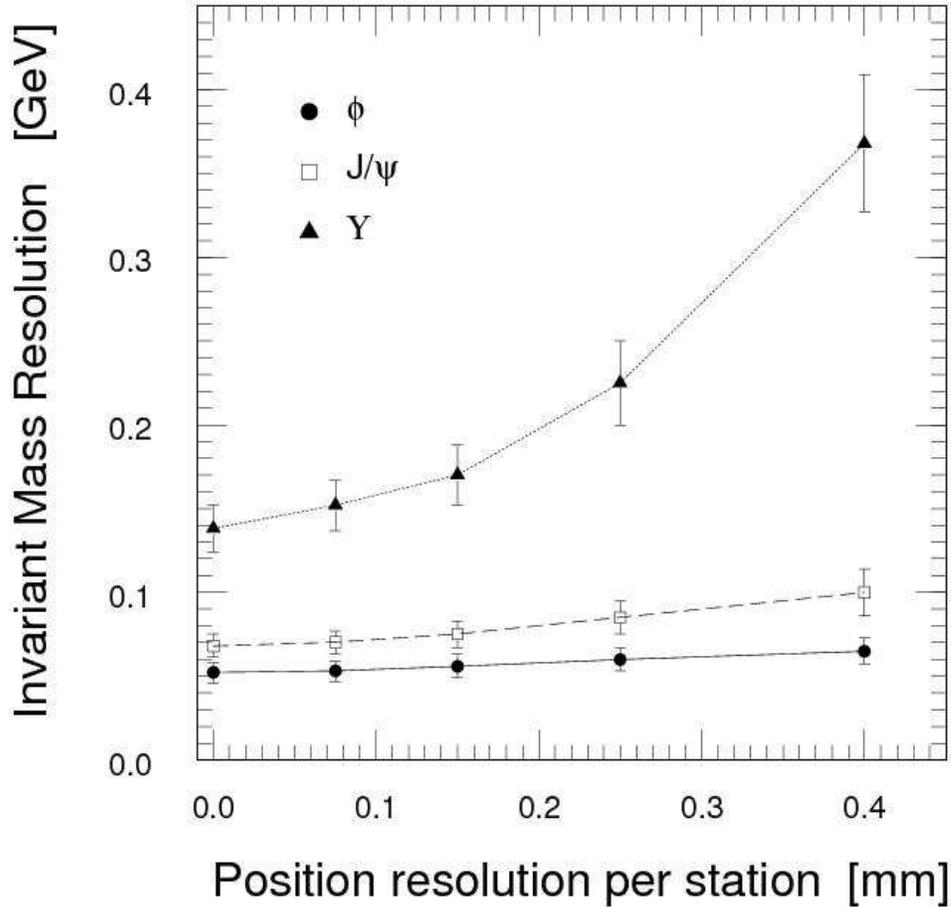


Figure 1.3: Dimuon mass resolution as a function of chamber position resolution.

### 1.1.2 Fake hit rate

A thermal noise on the new electronics is unavoidable and it would produce *fake hit*. The fake hit rate depends on the threshold level to be applied at the MuTRG-AD board. A simulation study by ISU group shows that a fake hit rate above 100 kHz would reduce the rejection factor significantly as shown in Figure 1.4. While the simulation has been done in the PISA <sup>2</sup>

an improvement.

<sup>2</sup>PHENIX Integrated Simulation Application

framework, *i.e.* based on our best knowledge to be realistic, we may have to expect additional background in the real environment. Therefore, we have set our goal to stay within 10 kHz.

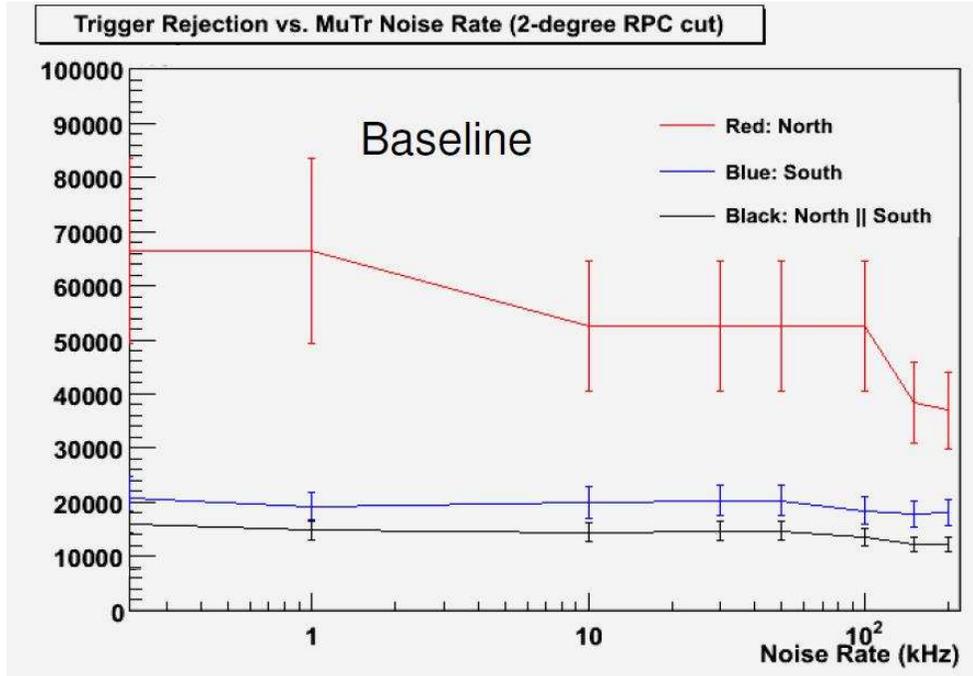


Figure 1.4: Rejection factors of the proposed trigger against minimum bias events as a function of fake hit rate from MuTRG-AD-TX chain.

### 1.1.3 Timing Performance

Ideally the hit information from the newly proposed electronics should be provided within the same beam clock, which means the timing resolution should be better than 106 nsec. However, the drift time alone already inherits the 100 nsec uncertainty. It means that it is going to be hard to identify the beam crossing of the event only with the chamber signal. Therefore, we have decided to utilize other fast counters in coincidence with the chamber signal to formulate the level-1 trigger. It is still true that better timing performance would be helpful in reducing possible accidental coincidence as well as in simplifying the trigger logic to be implemented at the local level-1. Simulation studies by ISU group showed that the required rejection of 10,000 can be obtained without significant degradation ( $\sim 18,000 \pm 2,000$ ), even if MuTr hits are integrated over five beam clocks. Therefore, we set our goal of the timing resolution to be within three beam clocks ( $\sim 318$  nsec) to contain 95% of the signals. This one plane efficiency corresponds to one station efficiency of 99.75%. Even if we have three stations in coincidence in the trigger logic, total efficiency would be 99.25%.

### 1.1.4 Acceptance Loss

The newly proposed electronics has to be implemented very close to the MuTr chambers and existing FEE especially to minimize the excursion of the chamber signal. Therefore we propose to place the MuTRG-AD boards onto the existing FEE chassis. In our current design, the height of the chassis for new boards is 37 mm. Simulation studies with PYTHIA event generator shows that it corresponds to a loss of 3% for  $J/\psi$  yields. Thus we conclude the acceptance loss is minimal.

To summarize the requirements:

- Additional noise to be introduced by the new electronics chain should be less than 30%.
- Fake hit rate should be less than 10 kHz.
- Timing resolution of the MuTRG-AD board should be better than 318 nsec which corresponds to three beam clocks.
- A plane efficiency with the time window above should be more than 95%.
- Acceptance loss for physics signal should be minimized.

## 1.2 Funding

The project is supported by Grant-in-Aid for Creative Scientific Research of Japan Society of Promotion of Science (JSPS). The total funding of \$2.1M is spread over 5 years starting from JFY2006 through JFY2010. The scope of the funding includes followings:

- MuTRG-AD: amplify and discriminate the pulse drawn from the cathode strip,
- MuTRG-TX: serialize digital pulse from MuTRG-AD every 64 channels, then convert to optical signal to be sent to the counting house through G-LINK,
- MuTRG-MRG: receive optical signal from MuTRG-TX, then deserialize and re-format to be sent further to the DCMs and LL-1 trigger boards.

It is already in the second year of the funding and we intend to start mass production of MuTRG-AD and TX boards. We would like to complete the design of MuTRG-AD and MuTRG-TX, while the prototyping of the MuTRG-MRG board is underway. Since the funding profile is peaked at JFY07 and JFY08, we would like to go through mass production process withing these two fiscal years.

JFY06 (Apr.'06-Mar.'07)	JFY07 (Apr.'07-Mar.'08)	JFY08 (Apr.'08-Mar.'09)	JFY09 (Apr.'09-Mar.'10)	JFY10 (Apr.'10-Mar.'11)
\$215,000	\$744,000	\$752,000	\$227,000	\$84,000

Table 1.1: Funding profile of JSPS Grant-in-Aid for Creative Scientific Research for Muon Trigger. The end of the funding coincides with the end of current phase of RIKEN-BNL Collaboration.

### 1.3 Schedule

The intended schedule for installation is shown in Figure 1.5 While the optimization of running time and shutdown is underway at BNL, we assume "regular pattern" just to show when we will be ready for installation.

There are many factors to drive the schedule of the project.

First of all, we would like to follow the master plan of the spin physics as closely as possible. While the master plan is not to promise the physics delivery in the proposed time line, a significant delay in the schedule would be harmful for the entire RHIC physics program.

Secondly, the funding profile is assuming that physics delivery on JFY2010, which is consistent with the master plan as well as PHENIX beam use proposal.

Basing on the current level of achievement in the entire Muon Trigger project, which includes both Upgrade of Muon Tracking electronics and RPC Installation, we are confident to follow.

We also confirm that the accelerator group is ready for 500 GeV commissioning followed by physics production run starting from Run 9. Therefore our plan is also consistent with the RHIC accelerator readiness.

We would like to add one more issue here. Since RIKEN-BNL collaboration for the spin physics should go through the review process for its extension of next 5 years. Current 5-year phase will end in the end of March, 2011, which coincides with the end of JSPS funding. To be ready for the review, we should have the physics results out of 500 GeV run before October, 2010 at the latest. Timely completion of the project will help to meet the goal of the current five-year plan of RIKEN-BNL collaboration, which will strengthen our proposal to extend the RIKEN-BNL collaboration for another five years.

## 1.4 Nomenclature - excerpt from Muon Tracking Design Book

Information is given on the nomenclature used in the Muon Tracker. The Muon Tracker consists of three Cathode Strip Chamber (CSC) stations in each of the two Muon Magnets. Stations 1 and 2 consist of three CSC chambers (called gaps) and Station 3 has two gaps. Each gap has two cathode planes which are read out. The "perpendicular" cathode planes provide high resolution "" measurements and the "stereo" cathode planes provide poorer resolution measurements but add stereo views which enable you to reject ghost intersections of cathode strips.

Numbering scheme are displayed in Figure 1.6.

## 1.5 Outline of the Document

In the next two chapters, the design principle and the test results in the test bench and with the beam test at Tohoku University are shown.

Full system test done in the summer 2007 are described in Chapter 4-6.

Installation issues including the possible acceptance loss are described in Chapter 7. Chapter 8 describes the interface with the PHENIX DAQ system, especially the Data Collection Module (DCM) and Local-Level-1 (LL-1).

Conclusion follows in Chapter 9.

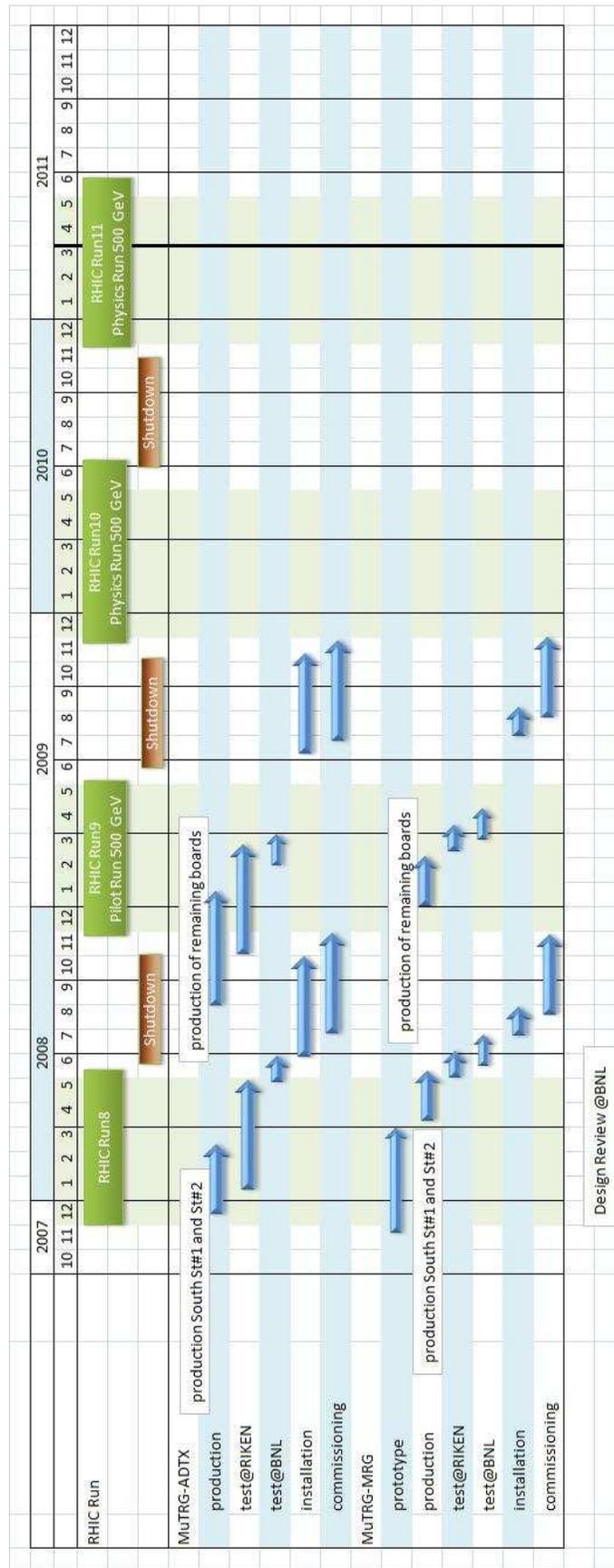


Figure 1.5: Proposed schedule of the Muon Tracking FEE Upgrade.

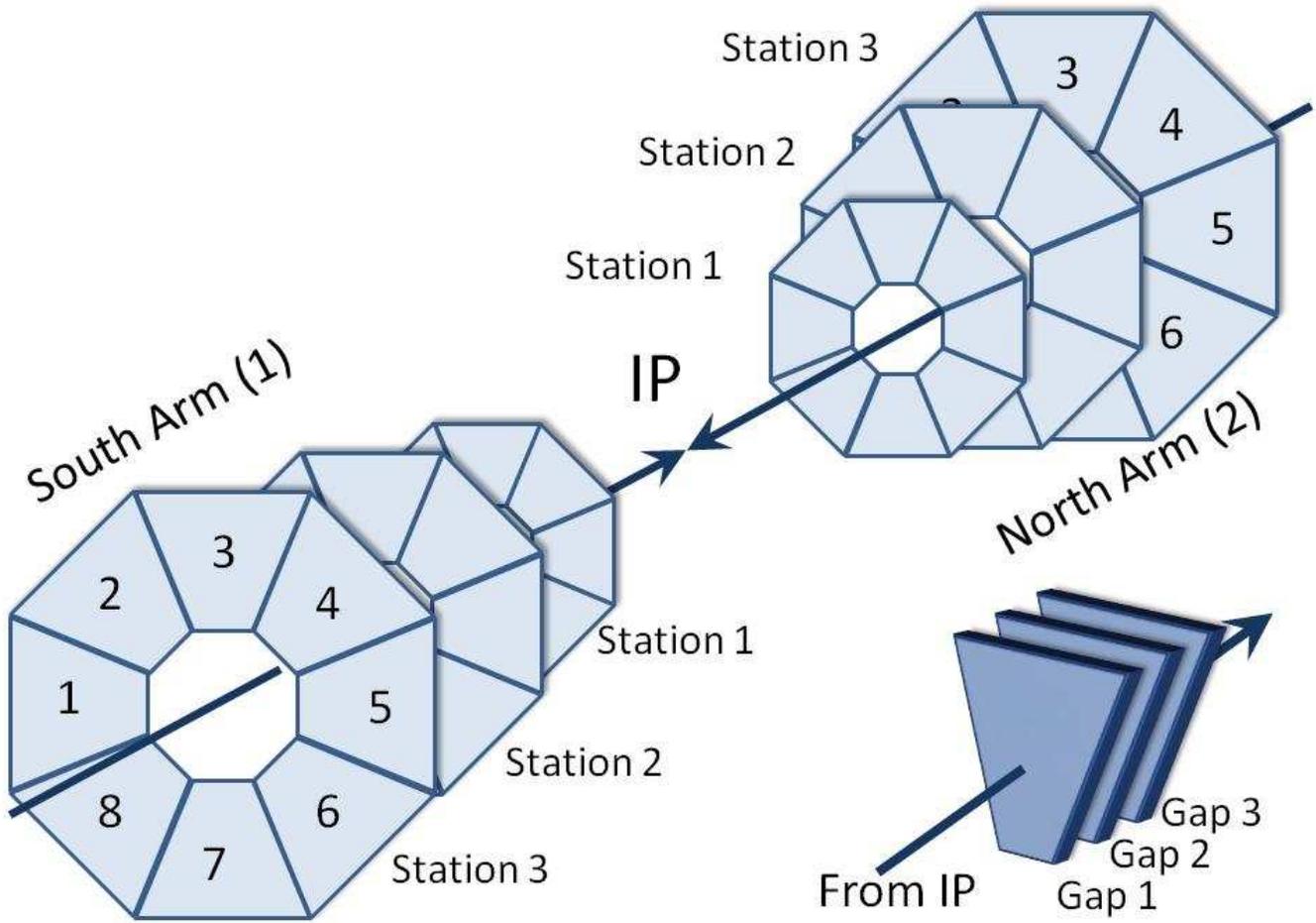


Figure 1.6: Nomenclature used for the number of the South and North Muon Arms, tracking stations within each arm and CSC planes within each tracking station.

# Chapter 2

## MuTRG-AD board

### 2.1 Design principle

The main function of the Amplifier Discriminator (MuTRG-AD) board is to provide strip hit information of the MuTr chamber. The outputs of MuTRG-AD board are sent to the transmitter board for further processing of the trigger decision.

Currently, the signal of the MuTr chamber is read out with Front End Electronics (FEE) which are designed to precisely measure the amount of charge induced on strips. These data are used to determine the passage point of the particle by offline analysis. The design value is 100  $\mu\text{m}$  position resolution. A 1 % noise level for a typical charge is required to achieve this resolution.

To obtain strip hit information at online level, we propose to split the raw signal line from the chamber as shown in Figure 2.1. One goes to the Cathode PreAmplifier (CPA) on the current FEE as before and the other one connects to the MuTRG-AD board to provide strip hit information. Then the signal is amplified and discriminated to provide one bit information. The 64 channel parallel outputs are sent to a data transfer (MuTRG-TX) board which serializes strip hit information and transmit with optical cable. The actual connection of MuTRG-AD and MuTRG-TX boards is shown in Figure 2.2. The signal lines are split on the backplane of MuTRG-AD.

The splitting ratio of the charge can be controlled by inserting the capacitor  $C_{\text{split}}$  shown in Figure 2.1. The ratio of the charge that flows into the FEE and the MuTRG-AD board is equal to the ratio of the CPA effective capacitance ( $\sim 900$  pF) and  $C_{\text{split}}$ . The typical amount of the induced charge is 100 fC. Therefore, if we choose 100 pF as  $C_{\text{split}}$ , the expected typical charge that flows into the MuTRG-AD board is 10 fC. Figure 2.3 shows that the FEE output

depends on the capacitance of  $C_{\text{split}}$ . Quite a low noise level, the design value of 1 %, should be achieved on the FEE to produce the required position resolution so using only a small fraction of the raw signal can be allowed. Moreover, adding the  $C_{\text{split}}$  means increasing the input capacitance and results in a worse noise level. However, we need enough charge for the MuTRG-AD board to create an efficient trigger. As another effect on the existing FEE, a delay of the peak position of the FEE output is expected because of the introduced capacitance by  $C_{\text{split}}$ . In view of these factors, we should determine the  $C_{\text{split}}$  value with extreme caution.

In the discriminator part, we use a cable-less Constant Fraction Discriminator (CFD), which is modeled after the MuID readout system[1], which we call pseudo-CFD, to minimize the time jitter due to pulse height variation. The fact that the pseudo-CFD technique requires no delay cable, which helps us with respect to space and channel density. We also use a Leading Edge Discriminator (LED) whose threshold voltage is programable for each channel. By requiring a logical AND of LED and the pseudo-CFD, the MuTRG-AD board is resistant to noise and the timing of the outputs is well defined. Figure 2.4 is a simple illustration which shows the effect of pseudo-CFD. The outputs of the LED could delay depending on the pulse height. The delay will be as long as the integration time at maximum. On the other hand, the pseudo-CFD, which outputs at the crossing point of the high pass filtered signal and the low pass filtered signal, shows a small time jitter from pulse height variation. Here one of the points is that the pseudo-CFD outputs are always late to LED outputs so the timing is determined by the pseudo-CFD by taking a logical AND of the LED and the pseudo-CFD.

Figure 2.5 shows the TDC distributions of CFD and LED with the ADC counts measured using the test bench at Kyoto University. It seems that the CFD works especially for the pulses near the threshold voltage. Unfortunately, the outputs broadens more than one beam clock (106 nsec). However, it is not the problem of the CFD circuit because it is confirmed that the jitter caused by electrical noise is  $\sim 11$ nsec (RMS) for the pulses around 150 ADC counts ( $\sim$  MPV for MIP) (see Fig. 2.6). It means that there are events which delays more than 100 nsec from particle passage while the longest drift path is 5 mm.

## 2.2 Specification

The MuTRG-AD board manipulates 64 channels on a 6 U size card and consists of operational amplifiers and comparators. Figure 2.7 shows the prototype of the MuTRG-AD board. It requires 6 V power supply at minimum and consumes the current of 1.5 A, then the power

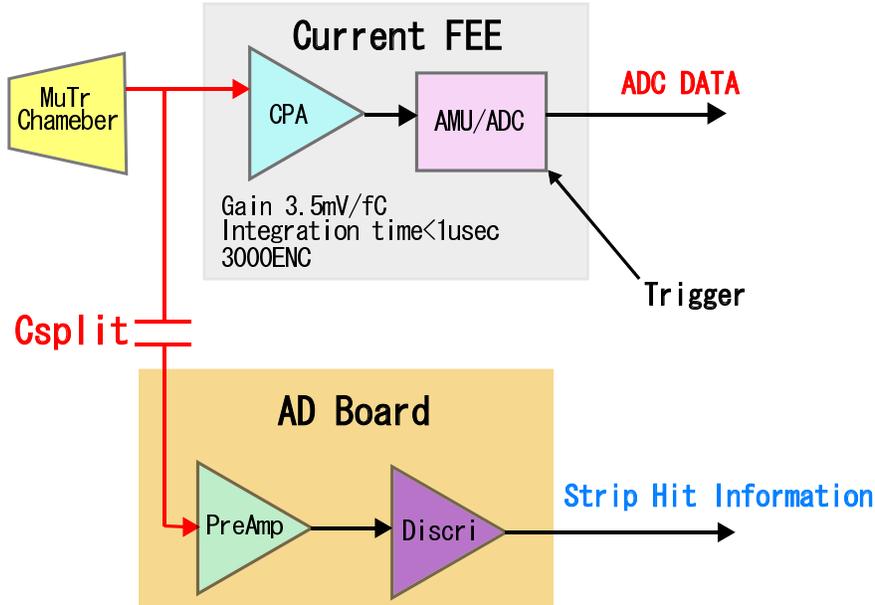


Figure 2.1: The new configuration of chamber readout.

dissipation is 9 W per board. The charge that flows into MuTRG-AD board is amplified with the gain of 10 mV/fC and shaped. The measured RMS noise at the amplifier output is 15 mV.

Figure 2.8 shows the response of both FEE and MuTRG-AD board to the test pulse input. The pulse of MuTRG-AD board returns to the base line within  $\sim 3 \mu\text{sec}$  while the amplifier output of the FEE has long shaping time to measure the induced charge precisely.

The output of the MuTRG-AD board is LVDS signal which delays about 300 nsec from the input. This delay is due to the pseudo-CFD. For the leading edge discriminator, channel by channel setting of the threshold voltage is capable to get the tolerability to the noise using Digital to Analog Converters (DACs). They are programmed from the MuTRG-TX board and can be set up to 512 mV with 2 mV step (8-bit)

The chassis in which the MuTRG-AD board is installed has two slots and one power supply connector. The width and length of the chassis is almost the same as FEE's chassis and the height is less than 5 cm. It has the capability of the water cooling and the air drying.

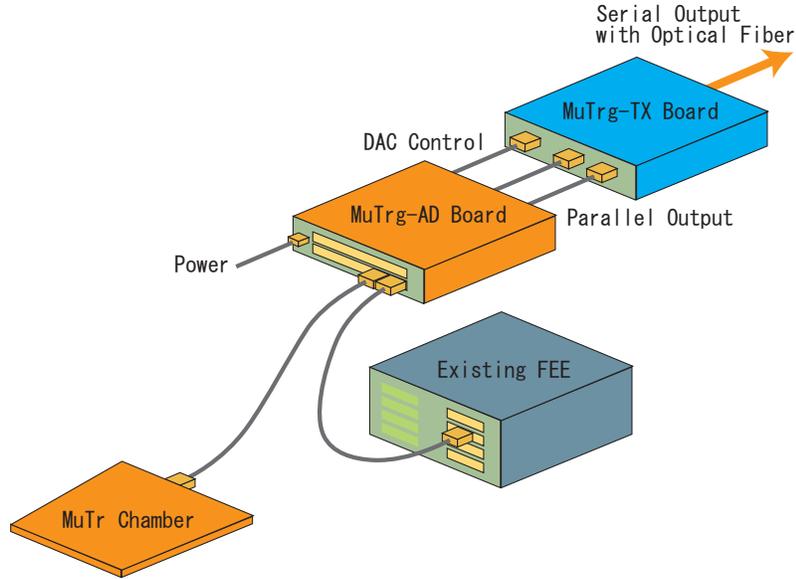


Figure 2.2: The connection of MuTRG-AD and MuTRG-TX to the existing system.

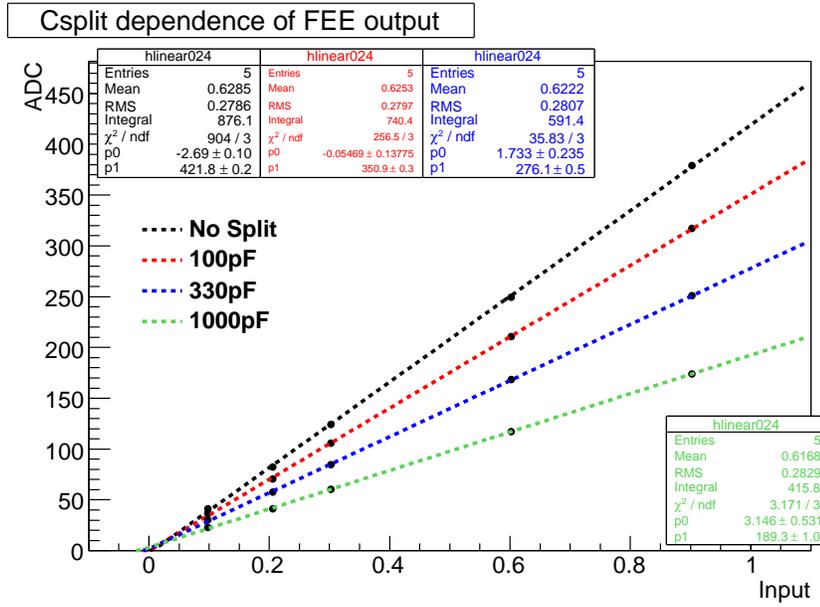


Figure 2.3:  $C_{\text{split}}$  dependence of the FEE output. Vertical axis is the output of the FEE with ADC. Horizontal axis is the value proportional to the input pulse height.

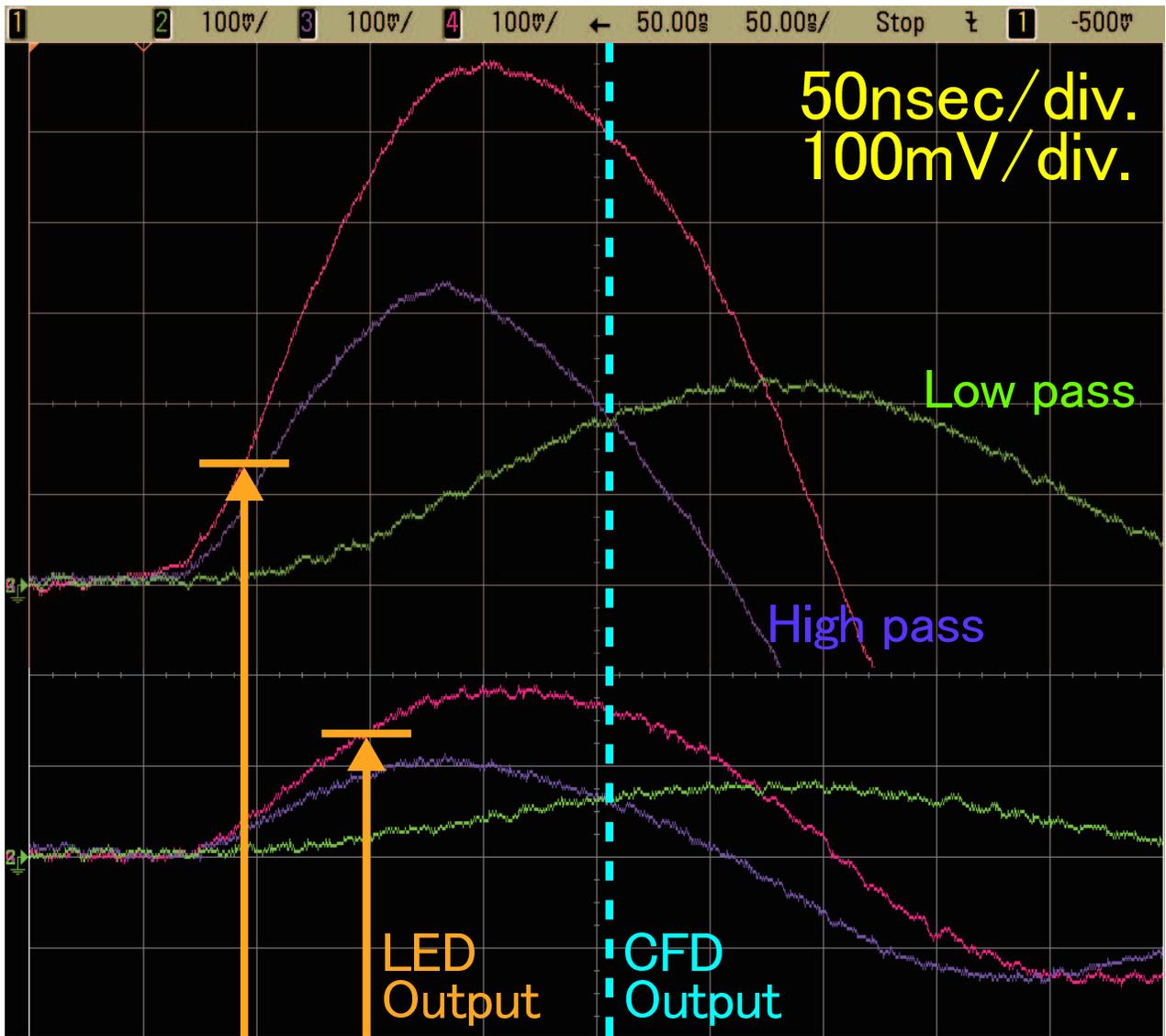


Figure 2.4: The illustration of the pseudo-CFD effect. The pseudo-CFD compares the high pass filtered signal and the low pass filtered signal. The output timing has small dependence on the pulse amplitude while the timing of LED outputs can vary up to its rise time.

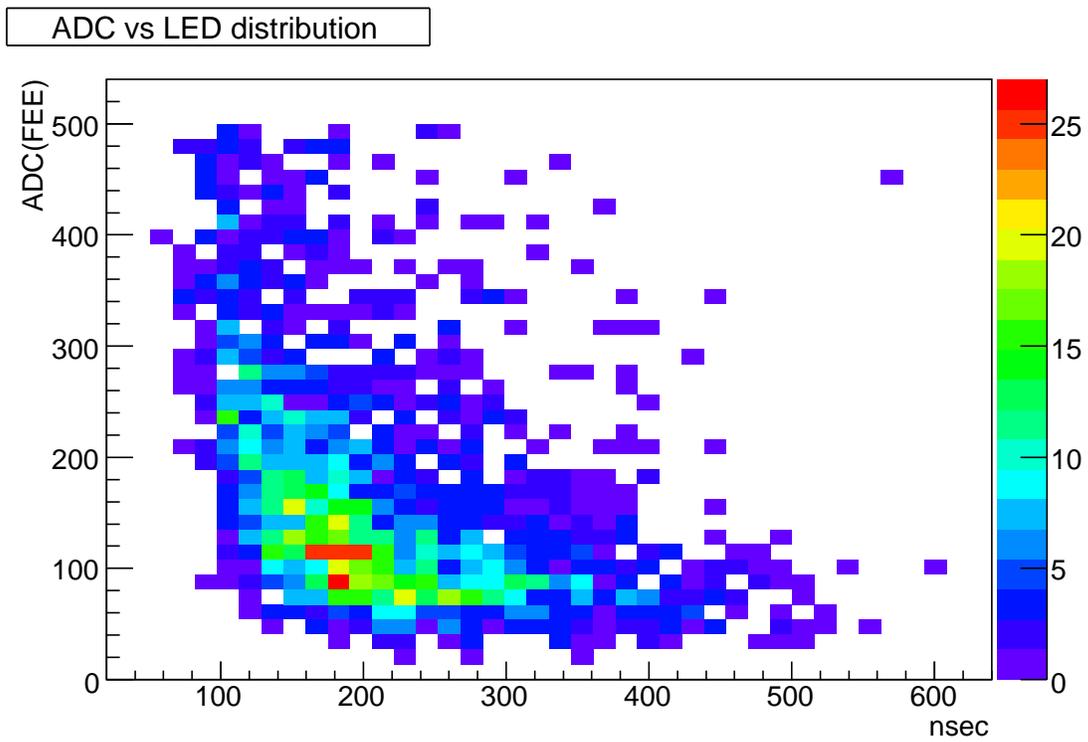
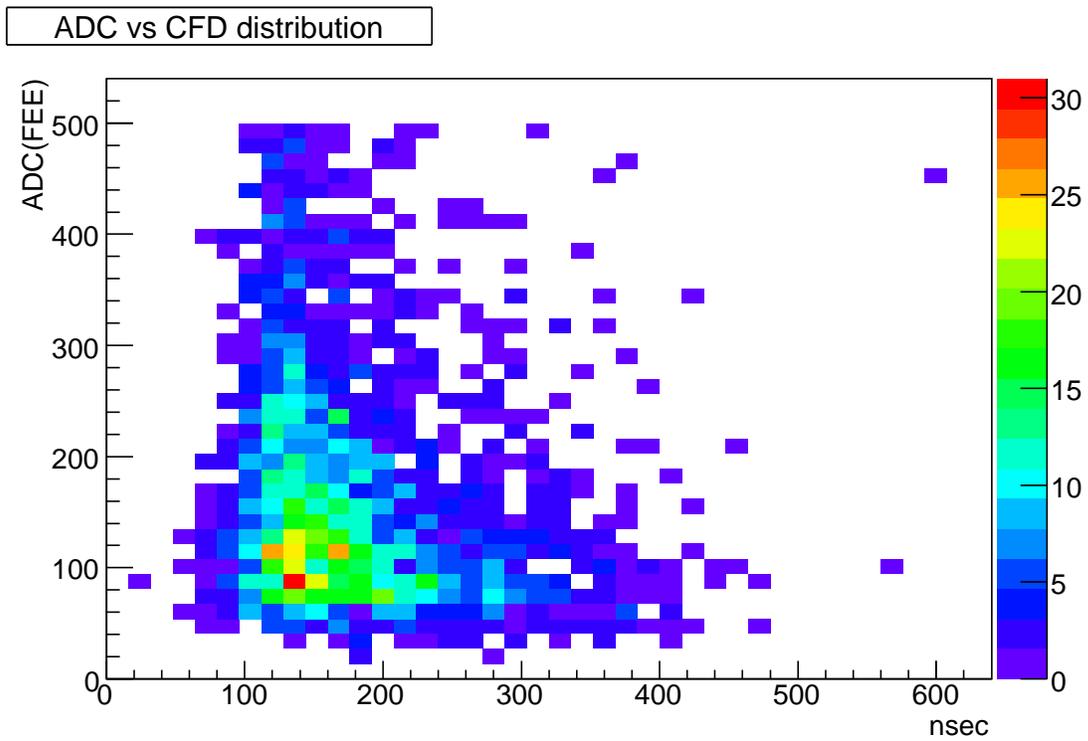


Figure 2.5: TDC distribution of CFD(top) and LED(bottom) with ADC counts. CFD circuit shows small time jitter compared to LED circuit.

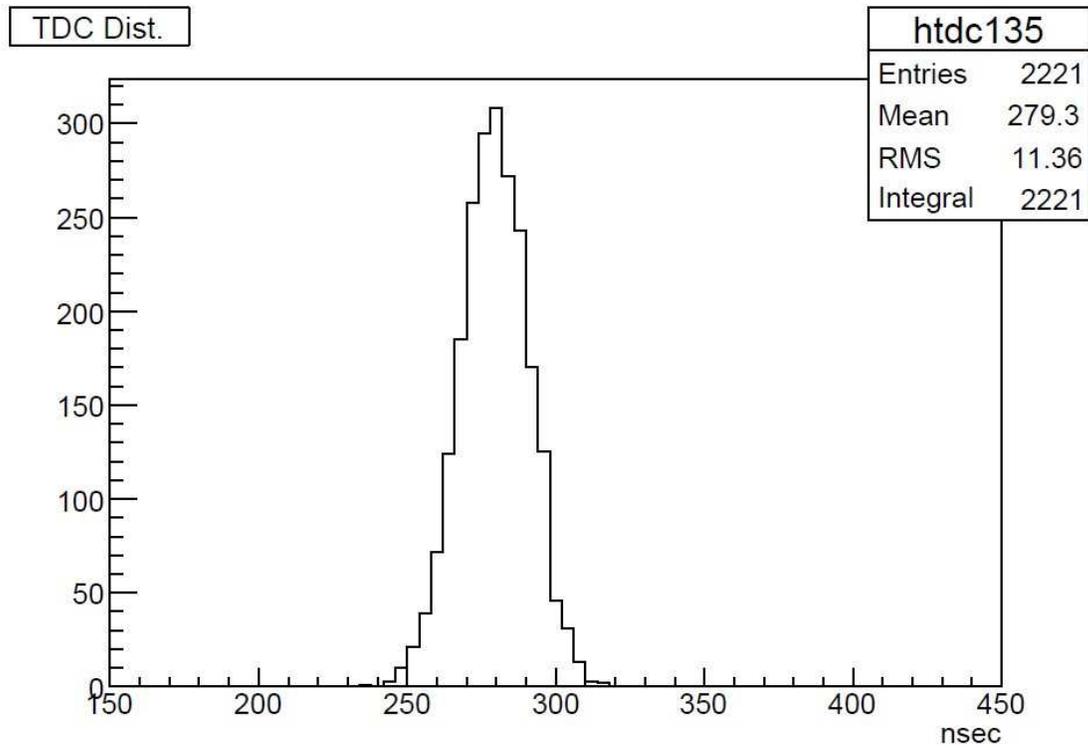


Figure 2.6: Timing distribution of the MuTRG-AD output for the calibration pulse at around MPV for the minimum ionizing particle.

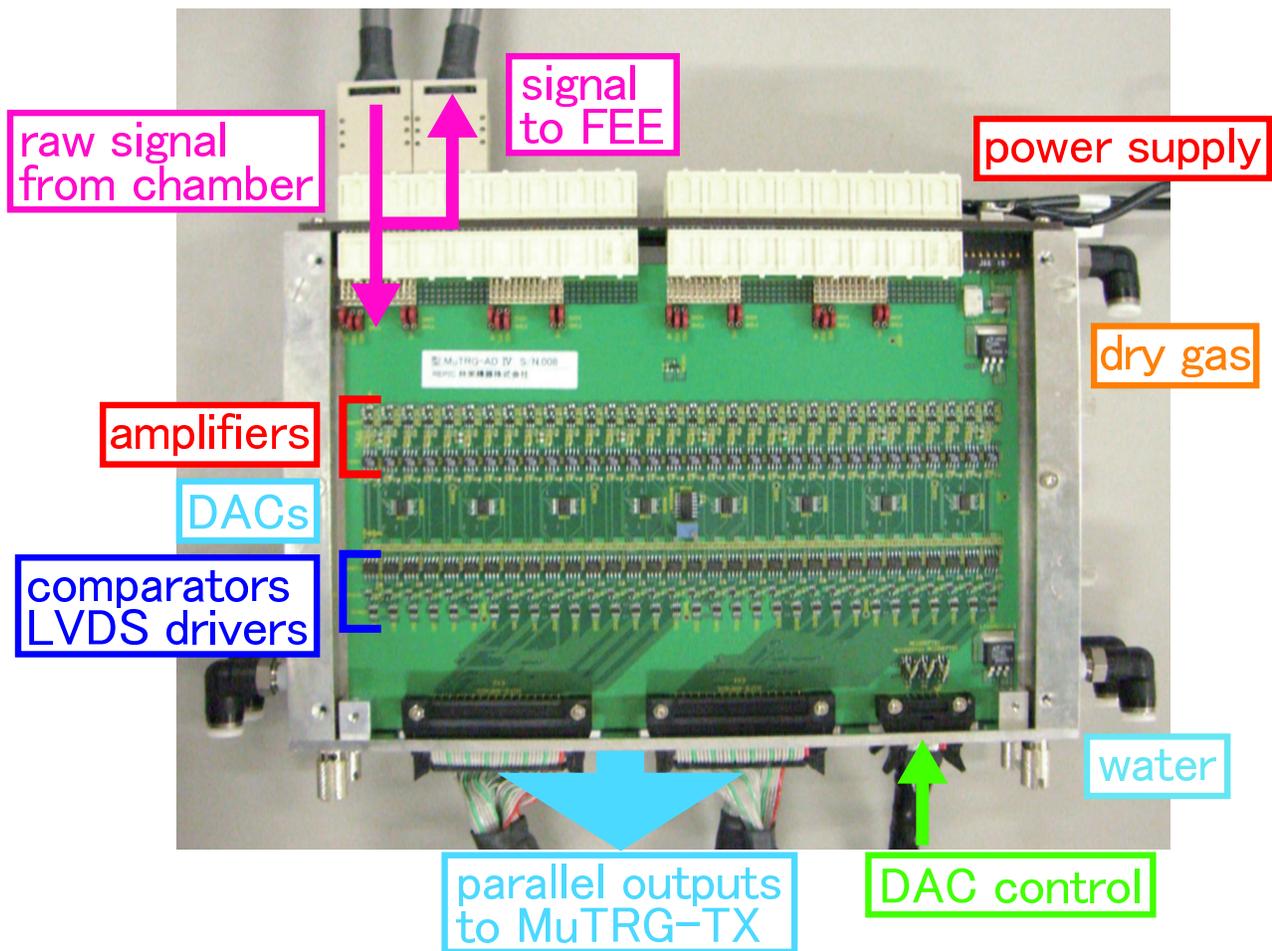


Figure 2.7: Prototype MuTRG-AD board.

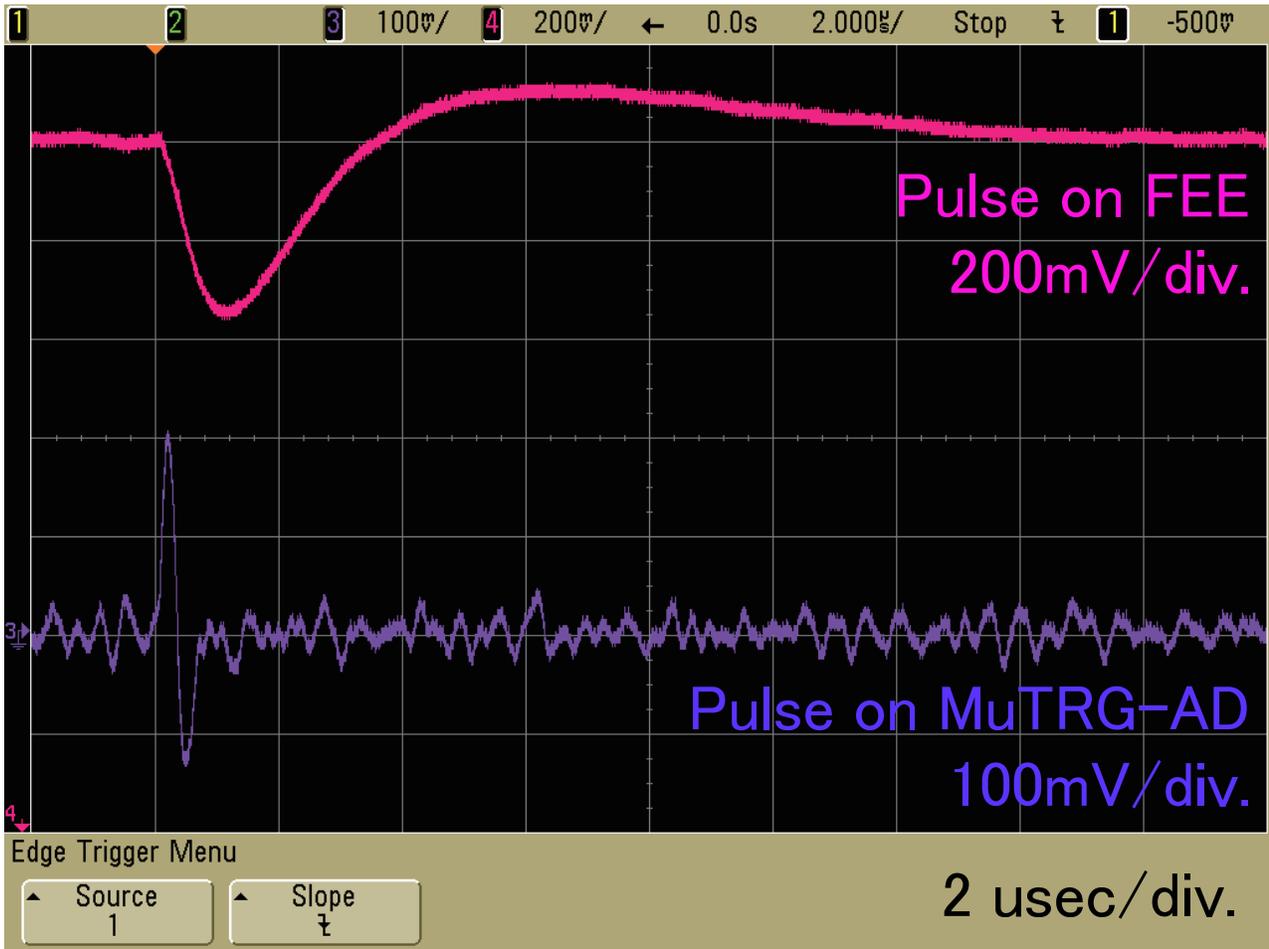


Figure 2.8: The snapshot of the amplifier output

# Chapter 3

## MuTRG-TX board

In this chapter, we described about the data transfer board (MuTRG-TX board). Section 3.1 is about the specification of it and the procedure of testing it is represented in section 3.2.

### 3.1 Specification

The main role of the MuTRG-TX board is a data transfer. The MuTRG-TX board is placed near the MuTRG-AD (Amplifier Discriminator) board. It receives parallel 64-bit outputs (LVDS level) from the MuTRG-AD board and serializes them, then transmits serialized data to the counting house by a optical fiber. The other role of the MuTRG-TX board is setting the threshold value of the discriminator on the MuTRG-AD board.

Figure3.1 represents a brief diagram of the MuTRG-TX board. Major chips which have great responsibility for the function of the MuTRG-TX board are FPGA (Xilinx Co., Spartan3, XC3S1000, FG456), TLK1501 (TI Co.) and optical transceiver (AVAGO Co., AFBR5710LZ).

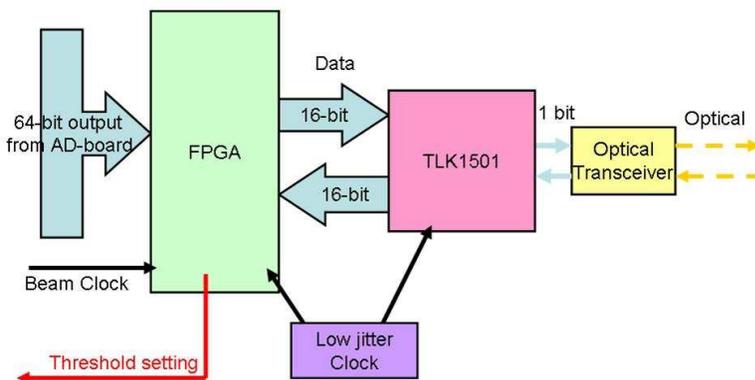


Figure 3.1: Block diagram of the MuTRG-TX board.

The FPGA is used as a data formatting module as well as a threshold controller of the MuTRG-AD board. It converts 64-bit paralleled signals into 16 bits data sequence. Beam clock counter (16 bits) and carrier extend (16 bits) are also added to original 64-bit data inside the FPGA. Figure 3.2 shows the block diagram of the logic of the FPGA. This data-formatting is necessary since the TLK1501, which is a serialize&deserialize device, has only 16-pin to input. In the FPGA, an asynchronous FIFO is implemented in order to switch its operation clock. The operation clock is switched from beam clock to 60MHz low jitter clock. The reason why the operation clock is switched is the jitter requirement of the TLK chip. The jitter of the beam clock (BCLK) is 25ps (rms) and the requirement jitter of the TLK is 40ps (peak to peak).

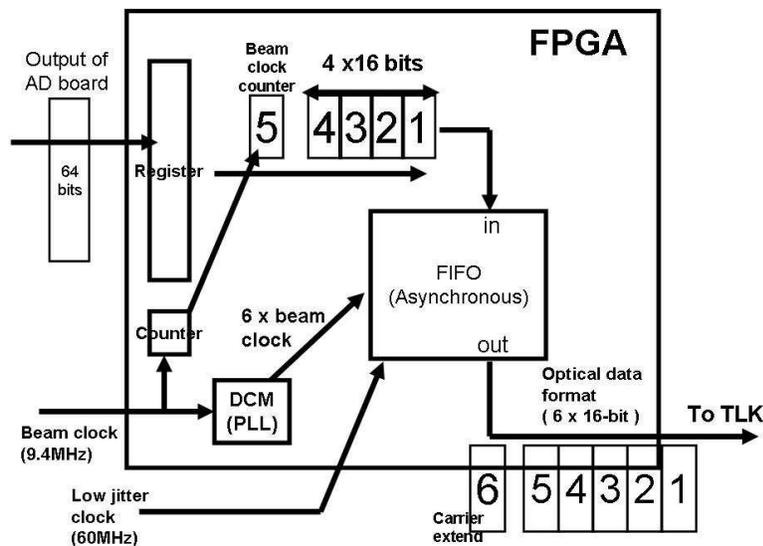


Figure 3.2: The FPGA logic of the MuTRG-TX board.

The TLK1501 is a serialize&deserialize device. It serialize 16 bits into 1 bit and output to optical transmitter which converts electrical 1 bit signal into optical signal. Since the TLK1501 has TX (transfer) and RX (receive) function, it can work as the receiver as well as the transmitter. This function is important because the data transmitting and the slow control from the counting house can be achieved with only one TLK chip. The 8b/10b data encoding is processed by the TLK. So, the data transmitting rate of the MuTRG-TX board is  $16\text{bits} \times 60\text{MHz} \times 10/8 = 1.2 \text{ [Gbps]}$ . The optical transmitter AFBR5710 can cover this data rate.

Although it is still in the development stage, a CPLD will be also mounted on the MuTRG-TX board for slow control. Figure 3.3 is the block diagram of the MuTRG-TX board including

a CPLD. The slow control includes "Download the design of the FPGA", "Initialize", "Reset" etc. Since the CPLD will be placed between the FPGA and the TLK, it can control all the signal to/from FPGA. This provides us the versatility for the slow control.

The CPLD was not mounted on the MuTRG-TX board in the summer test experiment, since the slow control method was not fully developed at that time.

Figure 3.4 is a picture of the MuTRG-TX board and table 3.1 is the detail of the MuTRG-TX board & its chassis.

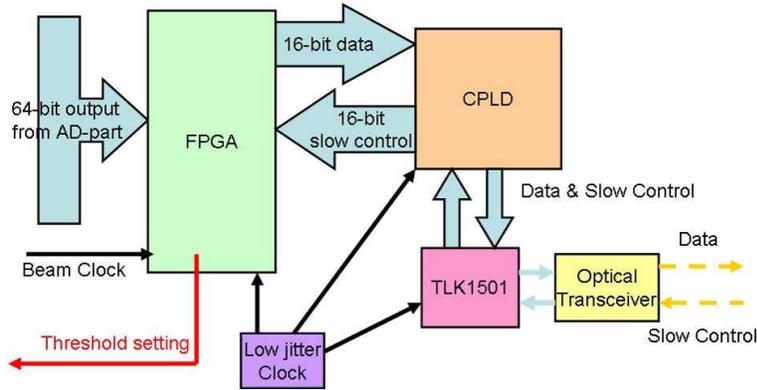


Figure 3.3: Block diagram of the MuTRG-TX board including CPLD. Slow control can be processed with this design.

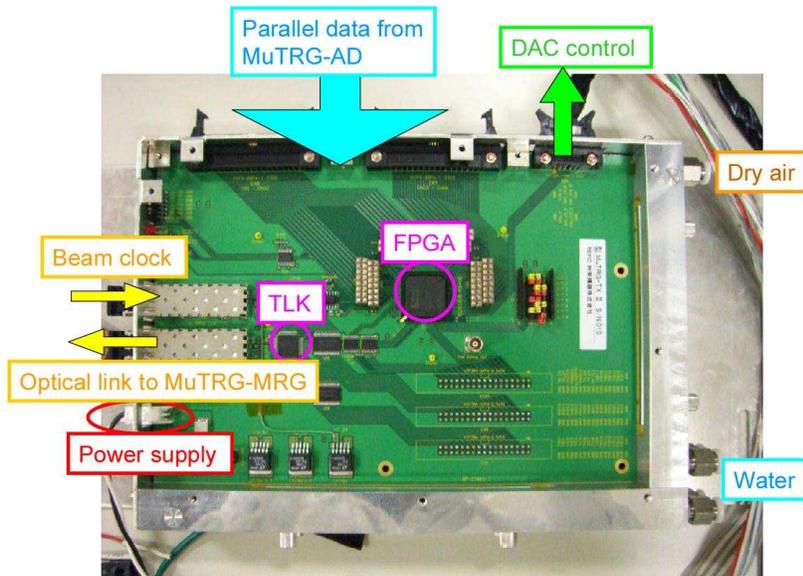


Figure 3.4: Picture of the MuTRG-TX board used in the summer test experiment.

About board	
board size	6U
power requirement	6V (3.3, 2.5, 1.2V are actual voltages supplied by the regulators on the board)
power consumption	~3W (0.4~0.6A)
input to output delay	2~3 BCLK (212~318 nsec)
About chassis	
chassis size ( breadth × width × height)	170mm × 245mm × 50mm
number of slots	2
cooling capability	capable of water cooling and air drying

Table 3.1: detail of the MuTRG-TX board and its chassis.

## 3.2 Performance test in the test bench

The R&D of the MuTRG-TX board was carried out using 2 boards. One of them was used as transmitter and another was as receiver. Figure 3.5 is a picture of the set up and figure 3.6 represents the block diagram of the test set up.

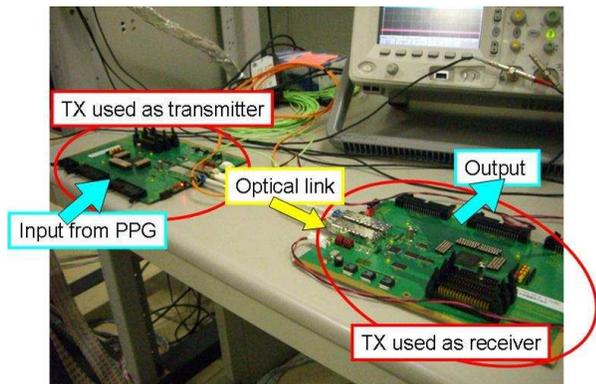


Figure 3.5: Picture of the set up.

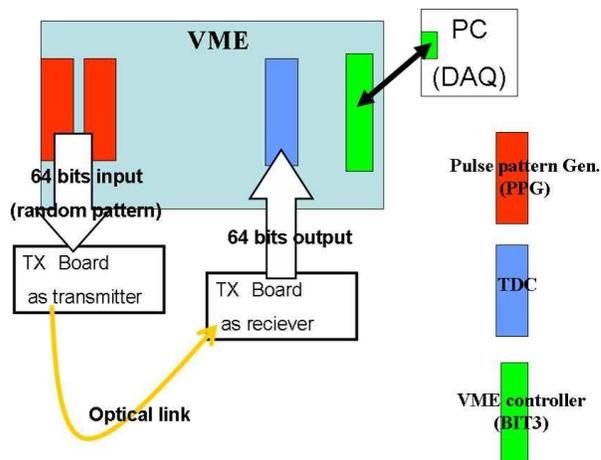


Figure 3.6: Block diagram of the test bench for the MuTRG-TX board.

We used a VME module, called pulse pattern generator (PPG), to generate random 64-bit pulse. Random pulse was controlled so that only one of 64 bits become high state. The generated pulse were input to the MuTRG-TX board and it transmitted them to the receiver in the manner described in section 3.1. The MuTRG-TX board used as a receiver converted the serial data to 64-bit paralleled data. The recovered data was then transferred to TDC and collected by the DAQ (data acquisition) PC.

The performance of the MuTRG-TX board was confirmed by comparing the random input data with the collected data. Figure 3.7 shows the result of the test. In the left plot, the horizontal axis is the channel of the recovered data and the vertical axis denotes the channel of the input data. It is clear that the transferred data are recovered at the receiver. The right plot of the figure 3.7 is the efficiency of each channel. Again, we can also be convinced that the MuTRG-TX board work appropriately. However, a channel where no signal was observed exists around 60th. This dead-like channel error doesn't come from the MuTRG-TX board. This is because the software defect occurred in the process of generating the random pattern. So, the dead-like channel differs every time taking the data.

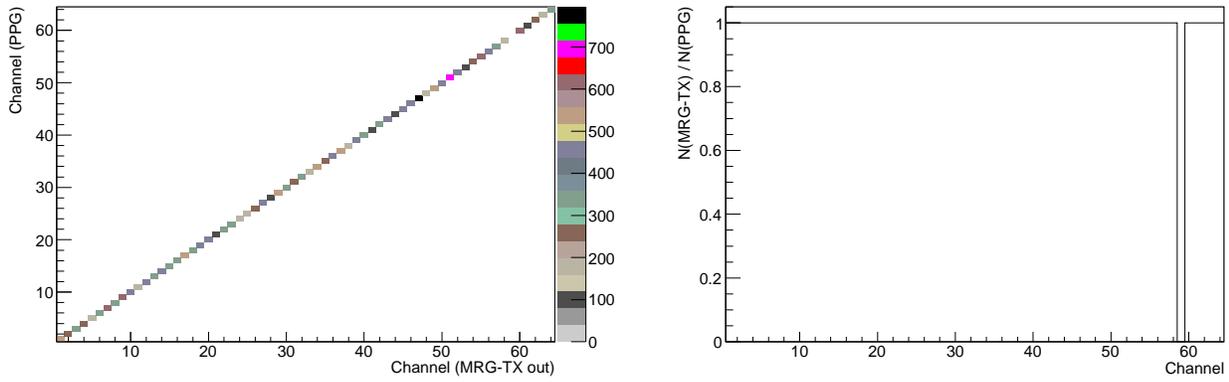


Figure 3.7: left: The plot of output channel (horizontal axis) versus input channel (vertical axis). It can be noticed that the transmitted data were completely recovered at the receiver side. right; The efficiency of each channel.

# Chapter 4

## Test of MuTRG-AD and MuTRG-TX with cosmic ray at IR

### 4.1 Overview

The prototype boards were installed at the bottom octant of the MuTr North station 1 and 2. Infrastructures for the test were prepared by the PHENIX technical support group. Prior to the full installation, a single MuTRG-AD was installed and tested in station 2. The MuTr gain and the noise performance were studied by using the test data taken with a calibration pulse and pedestal data. After establishing proper grounding and shielding procedures, other MuTRG-ADs as well as MuTRG-TXs were installed in both station 2 and station 1, one non-stereo plane each. Data from MuTRG-TXs were collected by the MuID ROC to record the digitized data with PHENIX DAQ. A fake hit rate at the MuTRG-AD was measured with several MuTRG-AD threshold settings. MuTr signals from cosmic rays, as well as signals from MuID and RxNP, were measured by triggering on the MuID Local Level 1 trigger (LL1) or the MuID Blue Logic Trigger (BLT). See Fig. 4.1 for the overview of the detector setup. Several sets of data were taken by changing the read-out latency, the MuTr high voltage, and the MuTRG-AD threshold. The time line of the test measurements is shown in Fig. 4.2.

Details of preparations and installation procedure are given in following sections.

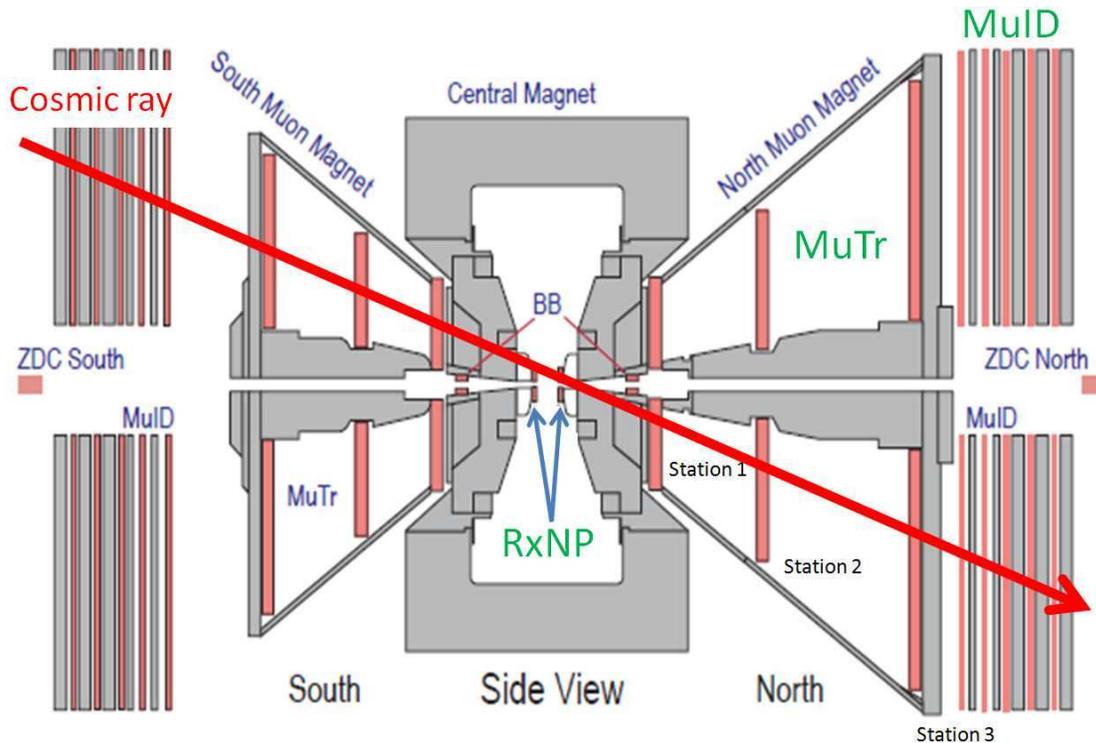


Figure 4.1: The PHENIX detector

## 4.2 Preparations

### 4.2.1 Infrastructures

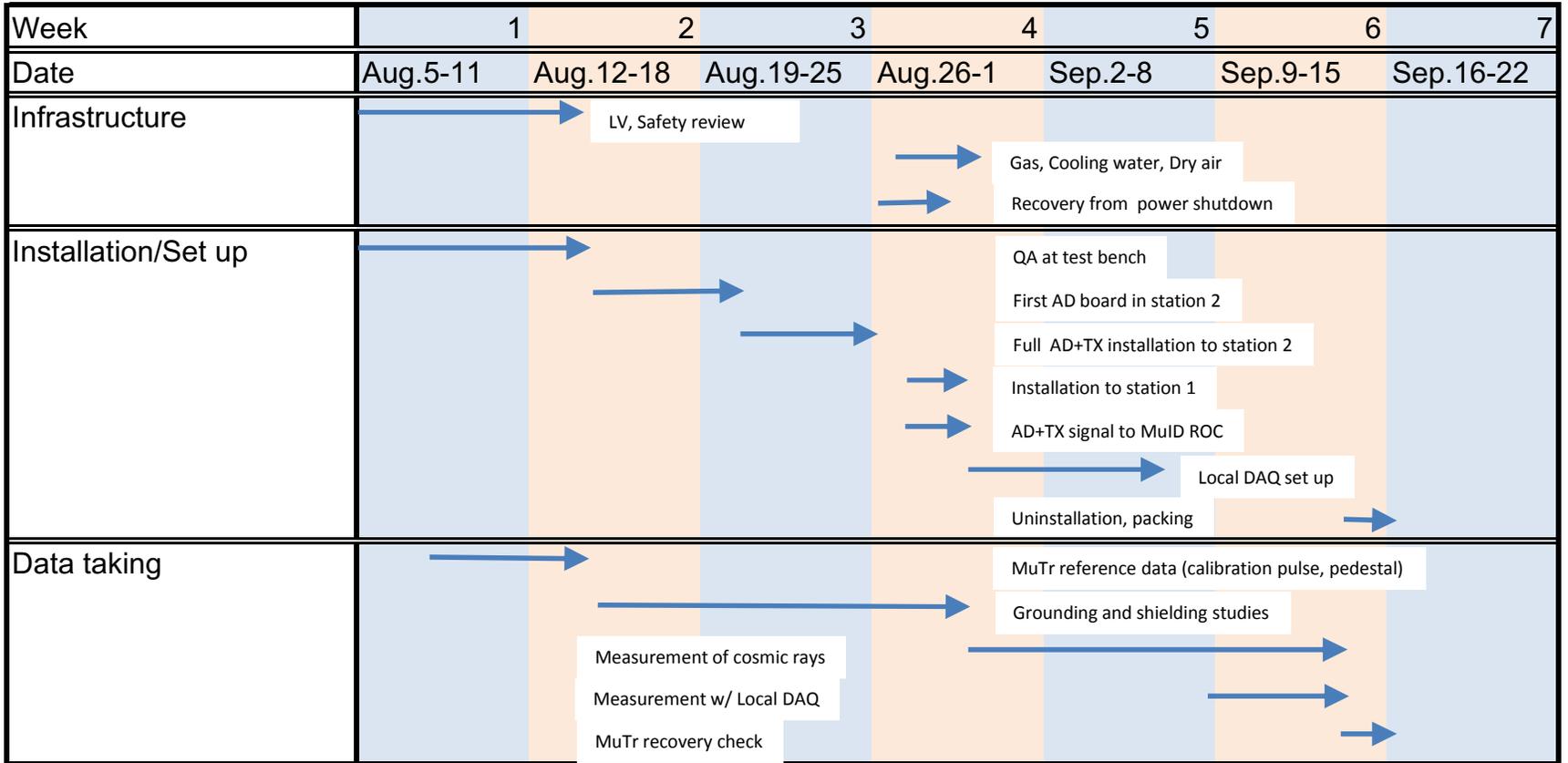
#### LV supply

The low voltage (LV) for the MuTRG-AD and MuTRG-TX were supplied from the PHENIX LV power supplies through the 10-ch LV distribution cards located on the platform (2nd floor) in the North arm. Those LV distribution cards were originally used for the MuTr North FEE. However there were some empty channels. Ten empty channels from four LV distribution cards were used to power the MuTRG-AD and MuTRG-TXs. The LV cables were routed on cable trays and they entered the MuTr inner volume through the corner of the lampshade at station 3. The nominal supplied voltage is 7.5 V (30 W) per channel with a 4 A fuse. Enabling and disabling of each LV channel was controlled by a GUI from the counting room.

In a default operation of the test set up, a MuTRG-AD chassis (with one MuTRG-AD,  $\sim 1.6$  A) and a MuTRG-TX ( $\sim 0.6$  A) were powered by a single LV line. The power consumption for each chassis was about  $(1.6+0.6) = 2.2$  A. <sup>1</sup>

<sup>1</sup>There was one chassis in which two MuTRG-ADs were mounted. The drawing current for this particular

Figure 4.2: Timeline of the test.  
30



## Gas system

The nominal operation gas for the MuTr is a mixture of Ar, CO<sub>2</sub> and CF<sub>4</sub> with a mixing ratio of 50 : 30 : 20. CF<sub>4</sub> gas had been turned off before the cosmic ray measurement since the CF<sub>4</sub> gas was not necessary for the earlier works on noise and gain studies. Supply of CF<sub>4</sub> gas was started on August 29. Since then, the nominal operation gas was used until the end of the measurement. On September 4th, we switched to a recirculation mode to save the gas consumption.

The nominal operation gas for the MuID is a mixture of CO<sub>2</sub> and iso-butane (i-C<sub>4</sub>H<sub>10</sub>) with a mixing ratio of 92 : 8. The C<sub>4</sub>H<sub>10</sub> gas was not flown before the cosmic ray measurement since the MuTr noise and gain studies and installation did not require the MuID information. The C<sub>4</sub>H<sub>10</sub> gas flow was started on August 30. A safety document for the operation of flammable gas was prepared and approved by the C-AD department. The trigger rate on the MuID Local level 1 trigger and blue-logic trigger increased by about a factor of two after the C<sub>4</sub>H<sub>10</sub> gas flow. Since the level-1 latency for the MuID trigger may depend on the gas condition, optimization of the level-1 latency for the MuTr digitized signals were done with the nominal gas mixture.

The status of the gas system for MuTr and MuID was monitored every four hours throughout the cosmic ray data taking based on a check list [2]. There was no major system failure during the data taking, except some minor disturbances such as empty gas bottles etc.. which were promptly taken care by the gas system experts.

## Cooling water and dry air

Cooling water was used to stabilize the temperature of MuTRG-AD and MuTRG-TX, thus the MuTRG-AD temperature, during the measurements. In addition, dry air swept surface of the MuTRG-AD and MuTRG-TXs to keep it dry against ambient humidity in the chassis. The MuTRG-AD chassis had cooling water inlets and outlets at each side of the chassis. It was designed that the largest heat source on voltage regulators on the MuTRG-AD edges were efficiently removed by cooling water. The MuTRG-AD and MuTRG-TX chassis had a dry air inlet connector. The dry air was allowed to escape from chassis through the signal connectors and other openings. Ad-Hoc cooling water and dry air lines were prepared from manifolds under the north-arm lampshade (see Fig. 4.3) in station 2. There is no water leakage from the

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MuTRG-AD and MuTRG-TX chassis was about  $(1.6 \times 2 + 0.6 = 3.8$  A which was close to the maximum current per LV line was 4 A. The solution was to use an alternative standalone LV supply (Matsusada PLE-18-5) to power that particular MuTRG-ADs.

MuTRG-AD chassis during the data taking.

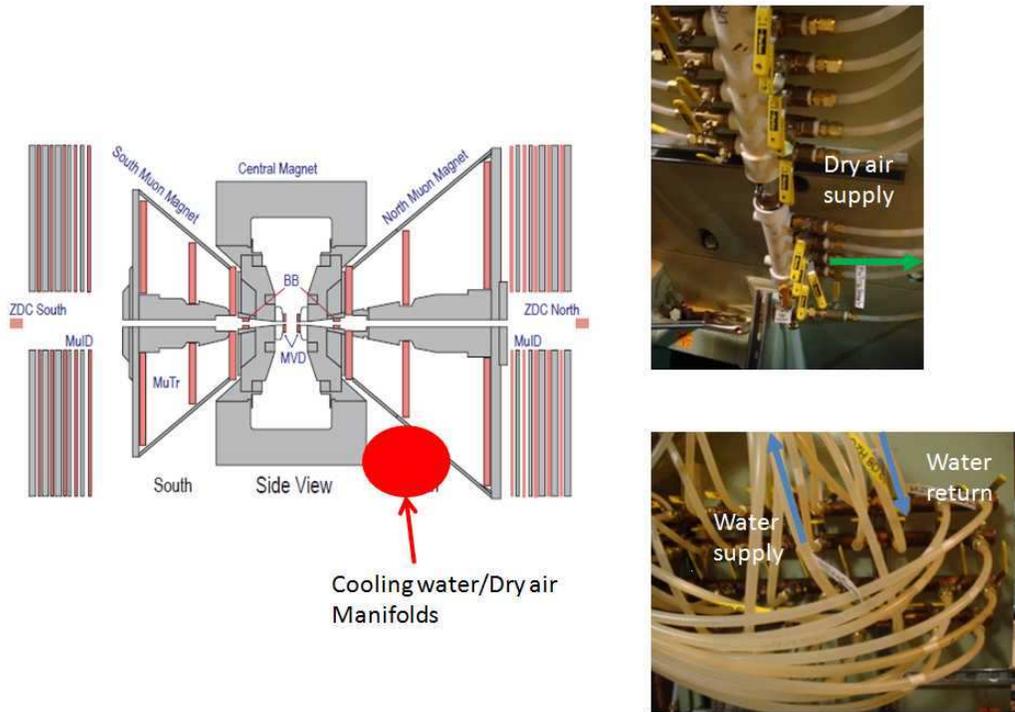


Figure 4.3: Cooling water manifold (right) and dry air manifold (left) under the MuTr north lampshade. Lines with white tags were used for the test.

## 4.2.2 PHENIX subsystems

### MuTr

The MuTr North bottom octant (octant 7) was operated with the nominal conditions during the test. HV for peripheral octants were also turned on during a part of data taking period. The high voltage (HV) for our test was set to the nominal value, i.e. 1875 V for station 1, 1900 V for station 2, and 1925 V for station 3. There was a certain period when the HV had to be lowered by -25 V due to high trip rate and high current, presumably because of higher humidity in IR. The HV values were set to nominal value when these unfavorable conditions were cleared by increasing the pressure for the dry air to the chamber surface by 20 %. Another data set was taken at +25 V higher HV values in the last few days to investigate the HV dependence of the performance. Figure. 4.4 shows the HV currents for some of selected HV chains. Most of HV currents became stable after about 24 hours of operation. An exception was that the HV chain N371(8) was disabled in Sep. 10th since it drew current as high as  $\sim 50 \mu\text{A}$ . It was

not clear what triggered the higher current in this HV chain. However, it was known that the MuTr HV current is sensitive to settle change in local humidity which we were not able to monitor during the test. Note that this HV chain is for station 3 where the MuTRG-AD was not installed.

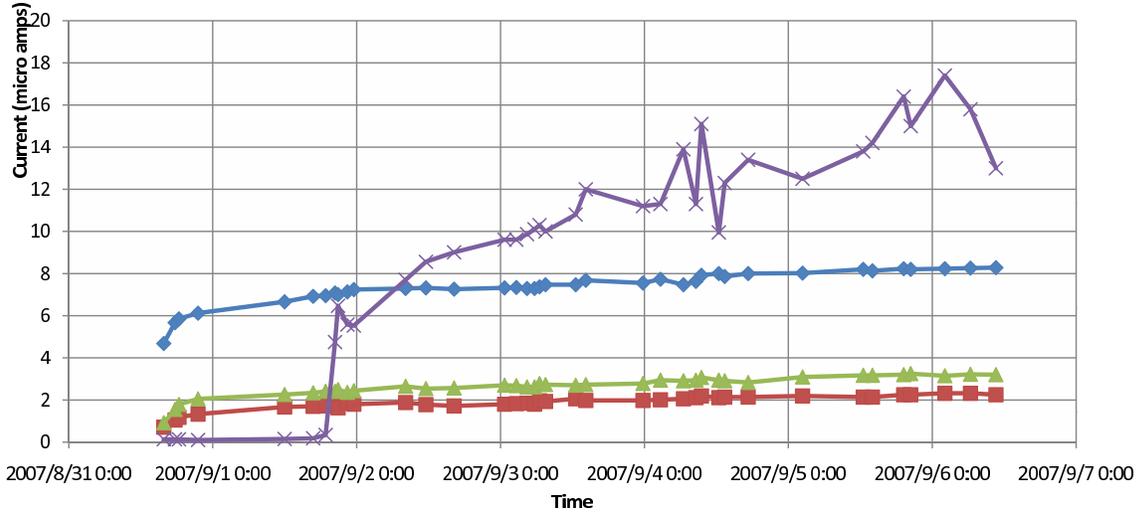


Figure 4.4: Monitored HV currents for selected HV chains for MuTr North. Blue, red, green and magenta points are the current for the HV chain N171(2), N271(7), N371(6) and N371(8), respectively.

Decapacitor work by the LANL group had been in progress in the mid. August and mid. September. Thanks to those efforts, we were able to recover some of disabled channels in the later part of the measurements. For convenience, all LV for MuTr north FEE were turned on so that no modification is necessary in configuration scripts and PHENIX DAQ to take MuTr data. See also Section 4.2.1 for the condition of the operation gas.

The hit occupancy, estimated multiplicity, charge distribution, and pulse shape distribution were monitored throughout the data taking by using the PHENIX standard online monitor framework (*onlmon*). Examples of monitoring histograms from the cosmic ray data are shown in Fig. 4.5. Here, no huge spike was observed in hit occupancy and multiplicity distributions. Empty bins in the multiplicity distribution is due to the fact that only bottom octant(s) were operated. A MIP peak was observed in the charge distribution for the cluster peak strip. The measurements of pulse amplitude at four beam clock tics indicated that the MuTr pulse was peaked at around 6th beam clock where there were three successive measurement to increase the accuracy of the total charge measurement. As long as one can see from these histogram, no major change in the MuTr performance was observed throughout the data taking period.

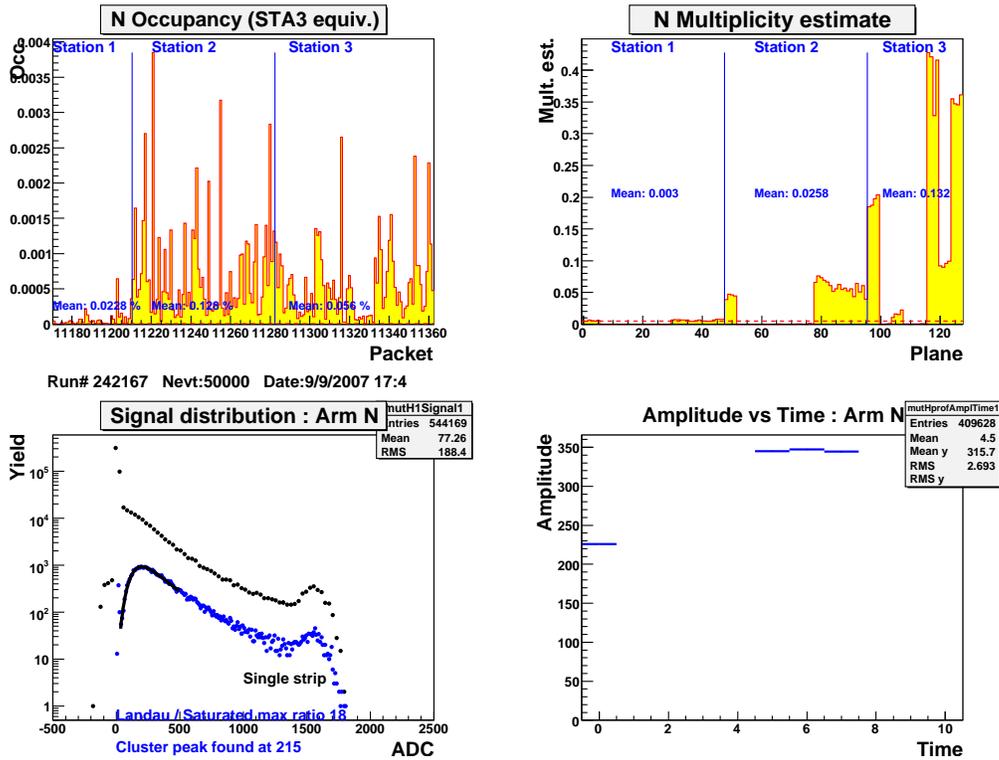


Figure 4.5: MuTr monitoring histograms for cosmic ray data (run 242167).

## MuID

The MuID provided a trigger signal for the cosmic ray measurement. The bottom half of the MuID panels in North arm was operated during the measurement to select cosmic rays which hit both the MuTr octant 7 and the MuID. After the nominal gas is supplied to the MuID, HV was set to nominal value of 4400 V. See also Section 4.2.1 for the condition of the operation gas.

The relative yield as a function of ROC, HV chain, signal cable number were routinely monitored with the *onlmon* framework. Figure 4.6 shows examples of monitoring histograms for cosmic ray data. Here, a ratio of the yield relative to the reference data were plotted as a function of ROC, HV cables, signal cables. The variation of the yield ratio was within tolerance range (horizontal lines in those plots) over about two weeks of measurements.

## RxNP

The reaction plane detector (RxNP) was turned on during the cosmic ray measurement. Bird's eye view of the RxNP detector is shown in Fig. 4.7. We expect that fast signals from the RxNP would be useful to identify the cosmic ray timing with an accuracy of one beam clock tic. Note

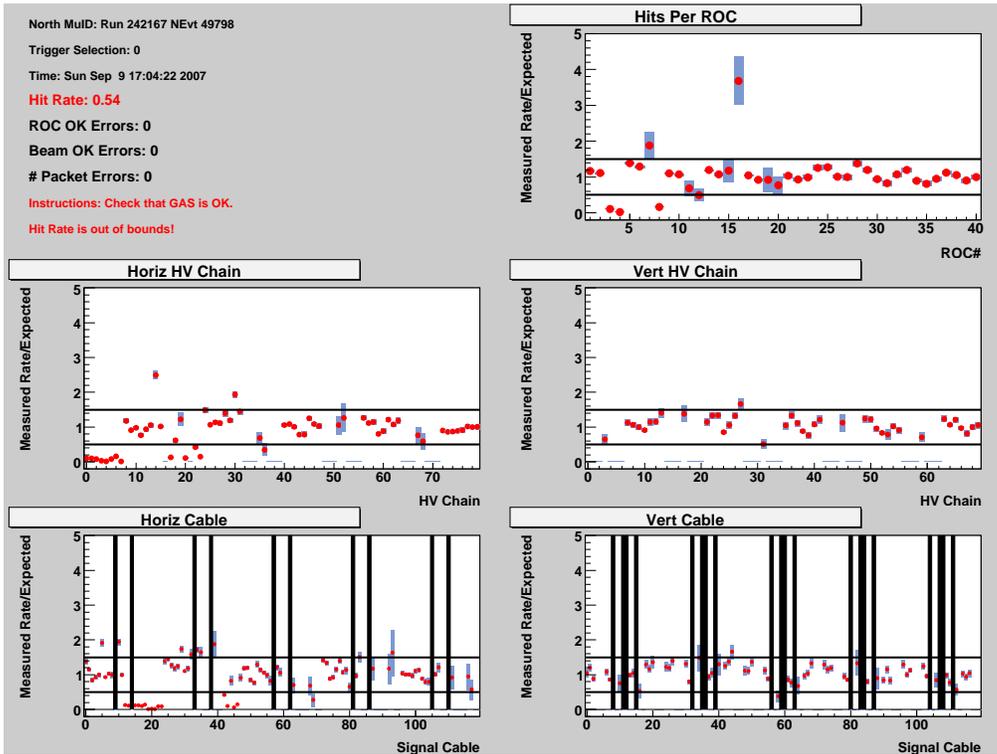


Figure 4.6: MuID monitoring histograms for cosmic ray data (run 242167). Note that only bottom three panels were powered.

that trigger timing by MuID is no better than a few beam clock. The HV for the RxNP in the north arm was tuned based on the cosmic ray data taken in this summer. The HV values were set at +300 V higher than the Run 7 values.

### 4.2.3 PHENIX DAQ configuration

The cosmic ray data consisted of data from MuTr(North), MuID(North), RxNP, and digitized signals from MuTr MuTRG-AD/MuTRG-TXs. To operate the PHENIX DAQ system with the desired configuration, a new partition (P0) and a trigger configuration (MuTrFEE\_test) were prepared for this purpose. Granules used were MUTR.N, MUID.N, and FCAL. The trigger requirements were trigger signal(s) from MuID deep BLT (North) or MuID(North) LL1.

### 4.2.4 Local DAQ system

The local DAQ system was set up underneath the north-arm lampshade for testing, debugging AD and MuTRG-TXs, and a high resolution measurement of timing distributions for digitized MuTr signals and PHENIX trigger signals. The local DAQ system consists of a trigger plastic

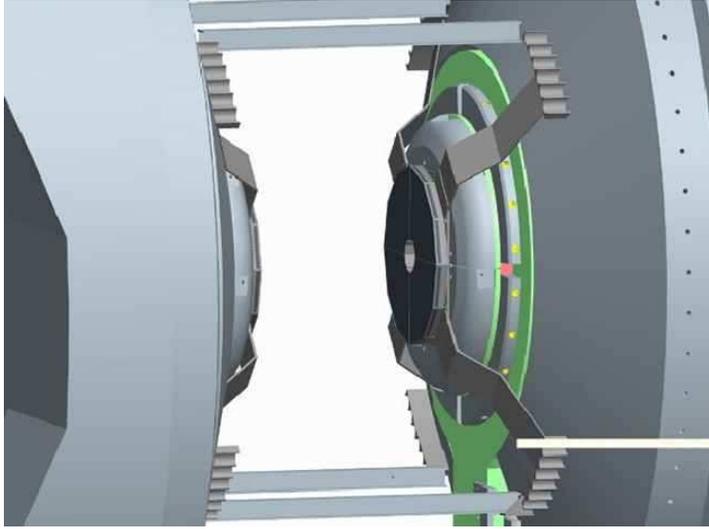


Figure 4.7: Bird's eye view of the RxNP detector.

scintillator (10 cm wide and 52 cm long), NIM logic modules and a VME interrupt register and a 128ch multi-hit TDC (CAEN V1190A) and an on-board computer. Figure 4.8 shows a block diagram of the local DAQ system. The local DAQ system was controlled by a standalone data acquisition package (*nagidaq*) on a linux PC.

The trigger plastic scintillator was installed in parallel to the cathode strips in station 2, octant 7. Later, it was moved to in station 1, quadrant 4 (see Fig. 4.9). The outputs from a MuTRG-AD as well as the trigger signal for the PHENIX DAQ (MuID LL1 || MuID BLT) was fed to the TDC inputs. The timing distributions relative to the plastic scintillator were measured by the multi-hit TDC.

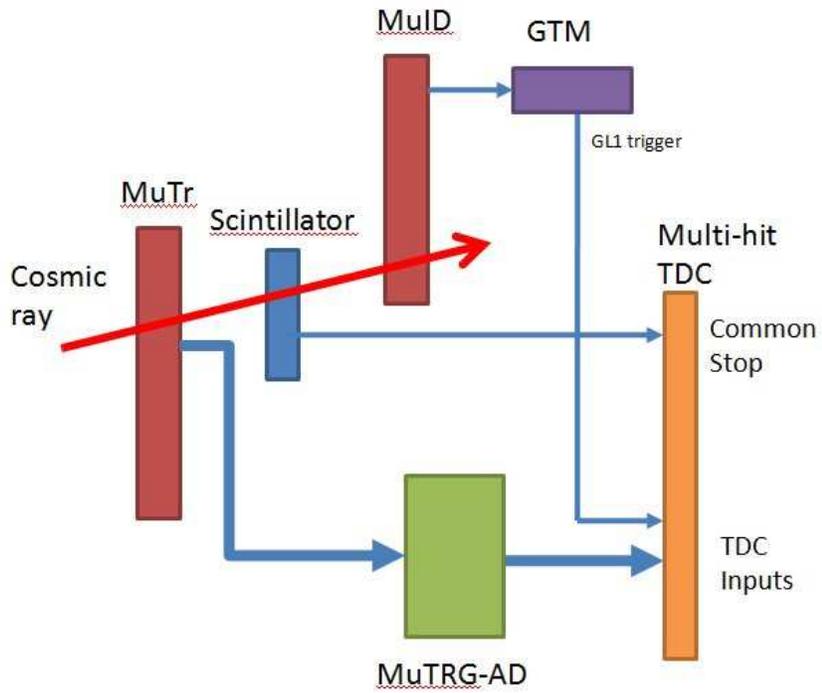


Figure 4.8: Block diagram of the local DAQ system.

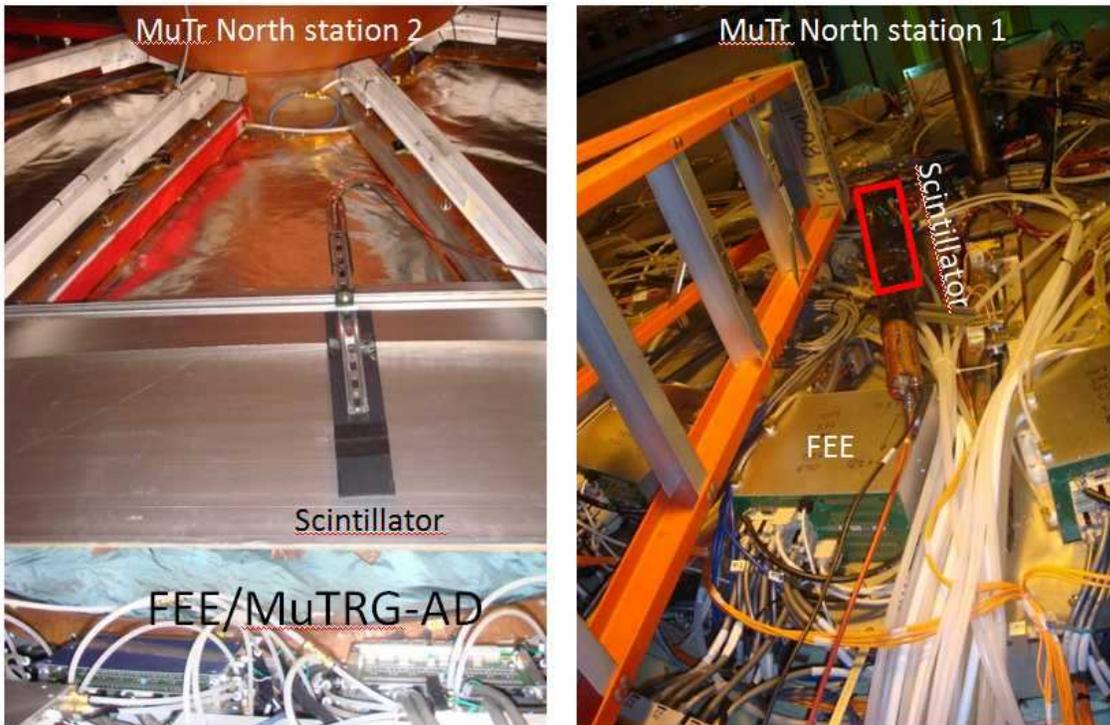


Figure 4.9: The trigger plastic scintillator for the local DAQ at MuTr north arm when it was installed at station 2, octant 7 (left) and at station 1, quadrant 4 (right).

## 4.3 Installation

### 4.3.1 MuTRG-AD and MuTRG-TX

All MuTRG-ADs and MuTRG-TXs were pretested at RIKEN test bench before they were shipped to BNL. Basic property of the MuTRG-AD and MuTRG-TX, such as dead channel, fake hit rates, threshold setting, signal transmission were inspected. A water leak test of the MuTRG-AD chassis was performed both at RIKEN and BNL.

Prior to the installation, pedestal data and calibration of existing FEEs were measured. These data were used as references to compare with the data after new boards were installed. The pedestal and gain of the MuTr signals was measured by the MuTr calibration system. The calibration system distributed a pulse with a preset pulse height to all cathode strips. The pedestal distribution was measured when a pulse height was set to zero. Figure 4.10 shows the MuTr FEEs at station 2 before the installation.



Figure 4.10: MuTr FEE at station 2, octant 7 before installation

One MuTr octant consists of three gaps. Each gap contains two planes of cathode strips. Total number of cathode strips per plane is 192 at station 2. MuTRG-ADs were installed in station 2, octant 7, gap 2, plane 1 (non-stereo cathode strips). There are five FEE chassis per octant in station 2. The MuTRG-AD chassis was installed on top of existing FEE chassis. Each FEE receives 1 – 3 read-out cables for the corresponding group of strips from the plane (16 strips per cable). The read-out cables were removed from the FEE backplane and connected to the MuTRG-AD backplane. Another short cables were added from MuTRG-AD chassis to FEE to pass the analog signal after the  $C_{\text{split}}$ .

The first MuTRG-AD chassis was installed for the strip #113-128. Figure 4.11 shows details of MuTRG-AD and FEE backplanes. Here, black cables were connected to the chamber, and a gray cable connects between MuTRG-AD and FEE (30 cm-long with FSI connectors). After installation of the MuTRG-AD, changes in pedestal RMS and gain were measured by the calibration system under various conditions of grounding and shielding (See section ?? for more discussions).

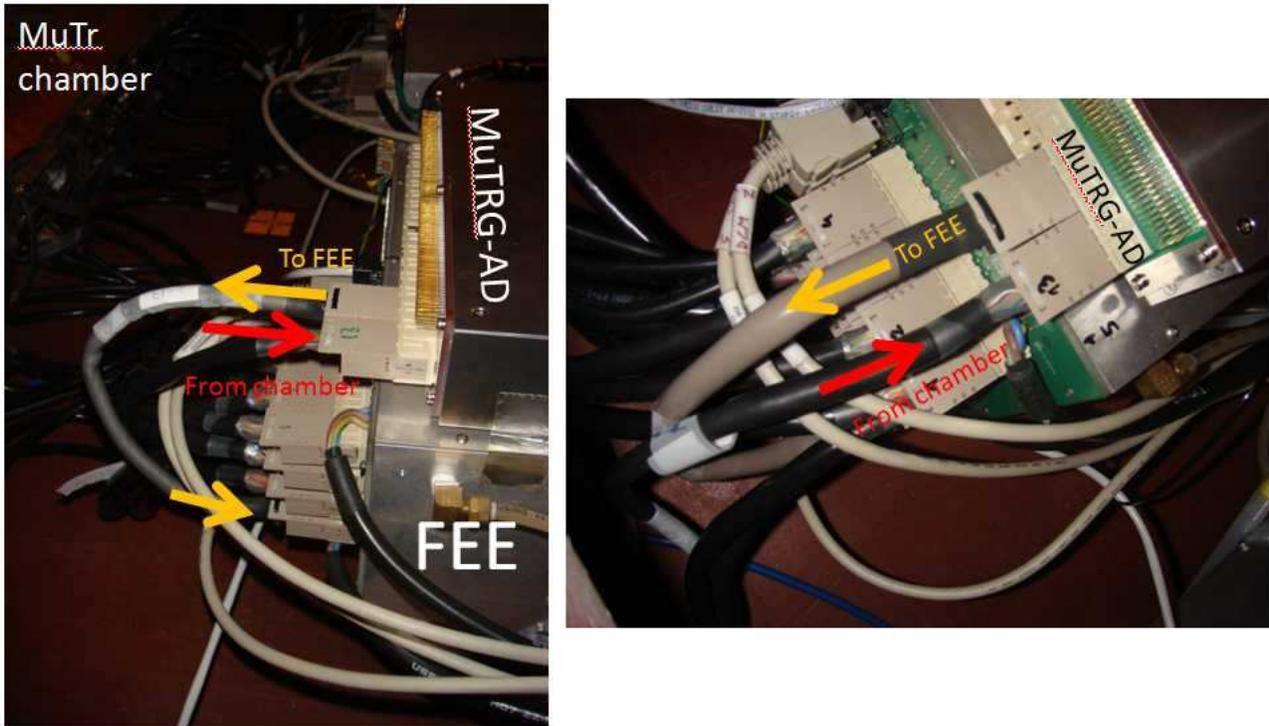


Figure 4.11: MuTr FEE and MuTRG-AD connections at station 2, octant 7, chassis 2 when the first cable was connected. Black cables connects the chamber and readout electronics. MuTRG-AD and FEE are connected by a gray cable.

After we identified the optimal grounding and shielding conditions of the MuTRG-AD and chassis, the MuTRG-TX and its chassis were installed at downstream of the MuTRG-AD (see Fig. 4.13). The PHENIX beam clock fan-out board was installed in the NIM bin for the local DAQ. The beam clock signals to the MuTRG-TXs were provided from here. The MuTRG-TX chassis was attached to the MuTr support structure “spider” with a unistrut. The connection between the MuTRG-TX chassis and the spider was electrically insulated. Here, two MuTRG-TXs were mounted in a MuTRG-TX chassis. Data from MuTRG-AD was sent to MuTRG-TX by two 150 cm-long twist cables. Again, grounding and shielding conditions for the MuTRG-TXs, MuTRG-TX chassis, and cables were investigated by checking the pedestal RMS for

various grounding conditions.

The optimal grounding and shielding conditions are summarized in Fig. 4.12. The strategy for the grounding of MuTRG-AD and MuTRG-TX was to obtain the ground from the MuTr chamber. The grounds for the MuTr chamber and chamber frame were tightly connected to the FEE and FEE chassis. The MuTRG-AD's chassis was tightly connected to the FEE's chassis. The noise performance was better when the ground for MuTRG-AD and that for MuTRG-AD's chassis was common, and the grounding for the MuTRG-AD and MuTRG-TX were the same. The grounding for the LV lines for the MuTRG-AD and MuTRG-TX were also common. More discussion on the noise performance will be given in next chapter.

Following successful installation of the first MuTRG-AD and MuTRG-TX chassis, remaining chassis were installed in station 2. Cooling water and dry air tubes were installed accordingly. Figure 4.14 shows a picture of station 2, octant 7 after full installation. In total, five MuTRG-AD chassis (five MuTRG-ADs) and three MuTRG-TX chassis (three MuTRG-TXs) were installed.

As for station 1, three MuTRG-ADs and three MuTRG-TXs were installed in quadrant 4, gap 2, plane 2 (non-stereo, 96 strips). The installation to station 1 required an additional mechanical structure to hold MuTRG-AD chassis since there was not enough space to temporarily locate the chassis near the FEE on the MuTr tea cup. It is desirable to make the distance between the MuTRG-AD chassis and FEE as short as possible to the best noise performance. The solution was to install a support structure made by unistruts below the bottom quadrant of station 1. The MuTRG-AD chassis were installed to the support structure using a ladder. An extra care was needed to disconnect cable from FEE since the cable connection at the chamber-side was known to be fragile. Figure. 4.15 shows a set up after full installation to station 1. MuTRG-TXs were located on top of the rack under the station 1. No cooling water nor dry air were installed to MuTRG-AD chassis at station 1.

In the last week of the test, the local DAQ became available. One more MuTRG-AD was installed at station 2, octant 7, gap 3, plane 1, strip 112–159. The outputs of the MuTRG-AD were fed into the multi-hit TDC module in the local DAQ system for the high resolution measurement of the timing jitter.

A list of MuTRG-AD and MuTRG-TXs installed in North arm are summarized in Table 4.1.

2

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<sup>2</sup>The convention of strip numbering in this report follows from the MuTr naming convention, but the strip number is not reset to zero when the strip enters the second half-octant.

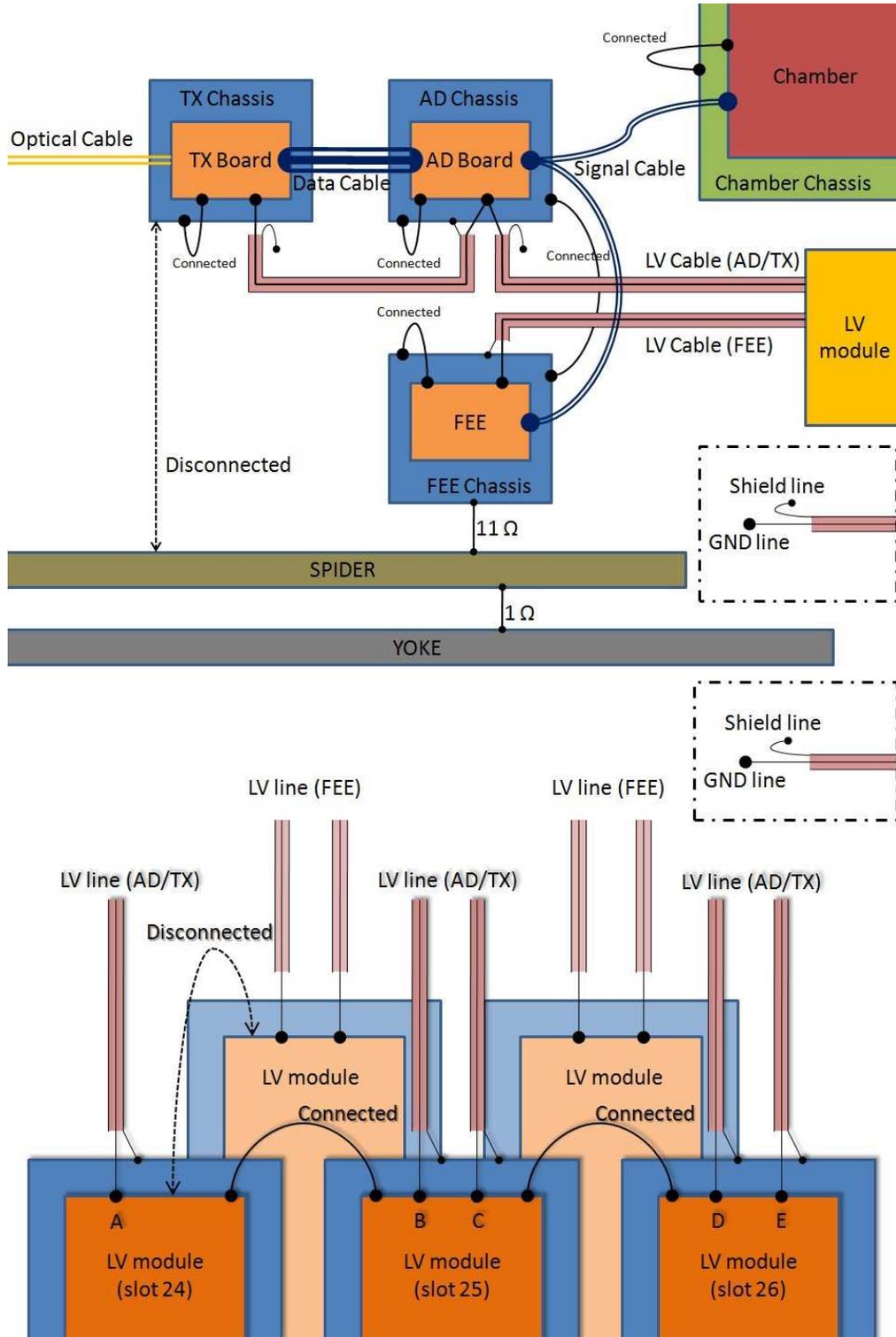


Figure 4.12: Schematic diagram of grounding and shielding at station 2

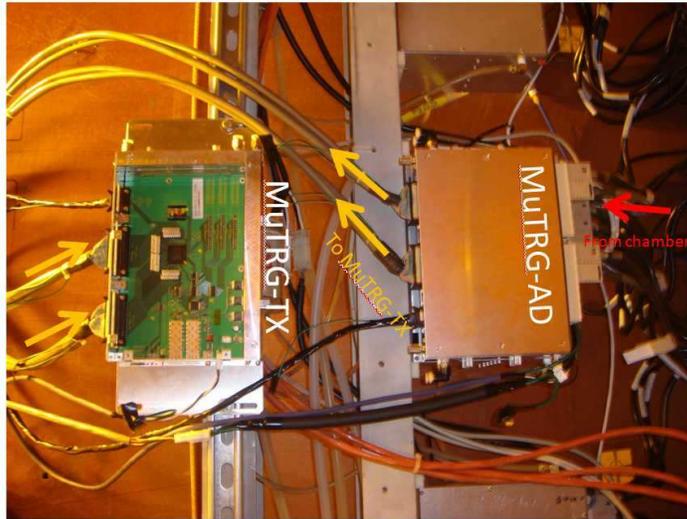


Figure 4.13: First MuTRG-AD/TX chassis installation at station 2, octant 7, chassis 2. Cooling water and dry air lines were not installed yet.



Figure 4.14: After full installation in station 2, octant 7. Five MuTRG-AD chassis (five MuTRG-ADs) and three MuTRG-TX chassis (five MuTRG-TXs) were installed. Tubes are for cooling water and dry air.



Figure 4.15: After full installation in station 1, quadrant 4

### 4.3.2 Feeding digitized signals to PHENIX DAQ

Cosmic ray data was taken for the studies of efficiency, resolution and timing jitter. MuTr digitized signals from MuTRG-TXs triggered by cosmic rays were recorded in the PHENIX data stream. Figure 4.16 shows a schematic diagram for the read-out of the digitized signals.

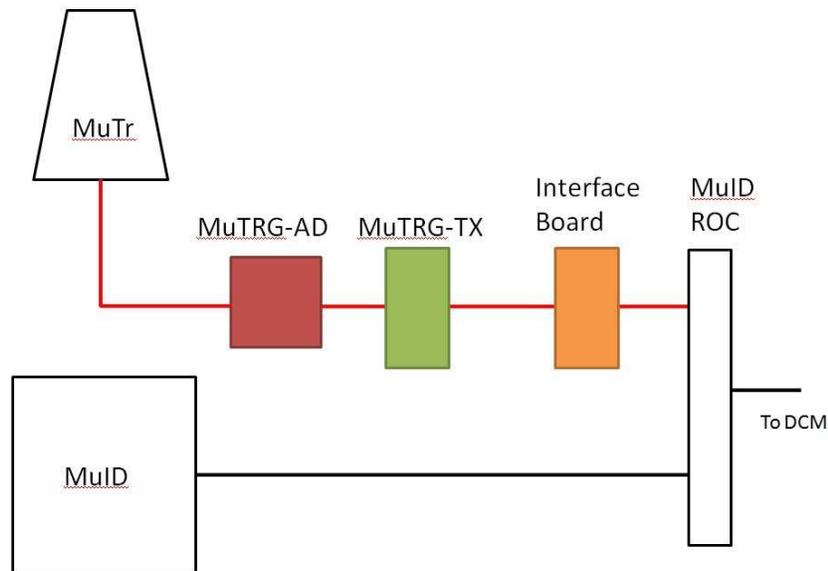


Figure 4.16: Schematic diagram for the read-out of the digitized signals.

The MuTr signals were digitized by the MuTRG-ADs. The MuTRG-TXs transmitted the digitized data to an interface board to the MuID ROC. The block diagram of the interface board is shown in Fig. 4.17

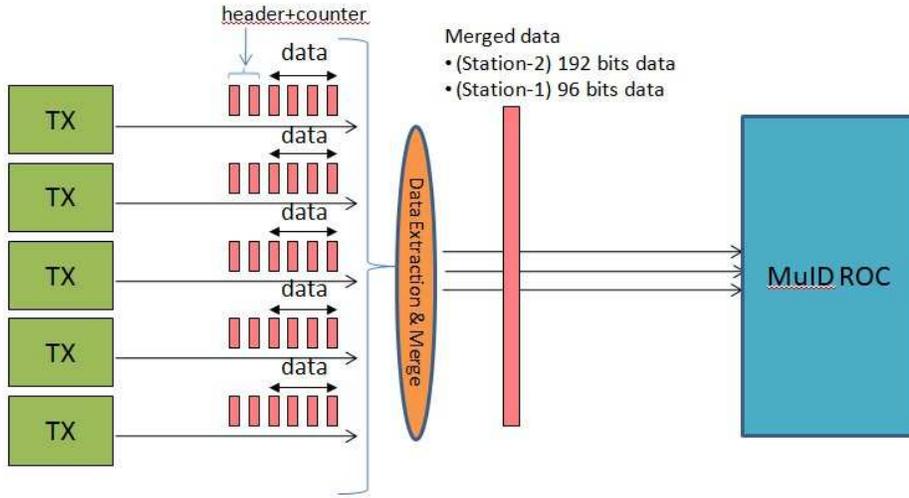


Figure 4.17: Block diagram of interface board to MuID ROC.

Two interface boards were used in the test experiment. Each interface board collects serial data via optical fibers from all MuTRG-TXs in each MuTr station. The interface board reformatted a set of MuTRG-TX data to an array of the hit bits ordered by strip number, and send them to the MuID ROC. A pictures of the interface board is shown in Fig. 4.18. The MuID ROC recognizes the hit pattern of an array of input data in the two beam clock period, and send it to DCM. The MuID signal cables for the upper MuID panels were temporary removed from two MuID ROC modules since upper MuID panels were not used in the test. The signal from the interface board were then connected to those MuID ROCs.



Figure 4.18: Interface board to MuID ROC

The latency of the signal from the MuTRG-AD input to output of the interface board was 1.2  $\mu$ sec, while MuID signals came to the MuID ROC right away (within a few beam clocks). The read-out timing relative to GL1 (level 1 latency) was different from that for the MuID. Several sets of cosmic ray data were taken by scanning the level 1 latency for the MuTr digitized signal to find the optimum latency which maximize the efficiency and determination of the timing jitter.

The fake hit rate of the digitized signal was measured from the data taken when the level 1 latency was set far from the optimum. A dependence of fake hit rate on MuTRG-AD threshold was studied for each strip. Based on the fake hit rate and the charge distribution for the cosmic ray, the strip-by-strip threshold was obtained for the fake hit rate at 1kHz which corresponds to about 50–60 percent of the MPV for the MIP.

## **4.4 Acquired data**

### **4.4.1 Calibration/pedestal data**

The calibration data and pedestal data were taken under various conditions of grounding and shielding. Once set up conditions were fixed, gain and pedestal RMS were monitored daily for about two weeks until the end of test experiment.

### **4.4.2 Cosmic ray data**

The base data of the cosmic ray was taken with PHENIX DAQ at a nominal MuTr HV and threshold at less-than 1kHz and at 1kHz. A small fraction of time was spent to take data at higher HV values (+25 V) or lower threshold values at 10kHz. For each given setup, the level 1 latency was scanned over about 5–10 beam clock range at around the optimum latency. In total, about 340 M triggers were accumulated.

A complementary set of data on the timing information was taken with the local DAQ. The data on the timing distributions of signals from the MuTRG-AD and GL1 trigger were taken at station 2 as well as station 1.

Table 4.1: List of MuTRG-AD and MuTRG-TXs installed in North arm

MuTRG-AD (chassis)	TX (chassis)	Station	Oct/Quad	Gap	Plane	FEE chassis	Strip
1 (1)	1 (1)	2	7	2	1	5	0–47
2 (2)	2 (1)	2	7	2	1	4	48–95
3 (3)	3 (2)	2	7	2	1	3	96–111
4 (4)	4 (3)	2	7	2	1	2	112–159
5 (5)	5 (3)	2	7	2	1	1	160–191
6 (6)	6 (4)	1	4	2	2	3	80–95
7 (7)	7 (4)	1	4	2	2	4	48–79
8 (8)	8 (5)	1	4	2	2	5	0–47
9 (2)	–	2	7	3	1	2	112–159

Table 4.2: Summary of acquired data

Data	Trigger	Conditions	Amounts
MuTr pedestal	Calibration system	various grounding conditions	~1 k events per setting
MuTr calibration	Calibration system	standard MuTr calibration run	one run per day
Cosmic ray	MuID LL1    BLT	threshold less than 1 kHz	266 M events
Cosmic ray	MuID LL1    BLT	threshold at 1 kHz (~ 28 mV)	12 M events
Cosmic ray	MuID LL1    BLT	threshold at 10 kHz(~ 25 mV)	16 M events
Cosmic ray	MuID LL1    BLT	threshold at 25 mV)	16 M events
Cosmic ray	MuID LL1    BLT	HV +50 V	30 M events

# Chapter 5

## Impact on the existing readout system

### 5.1 Overview

This chapter describes the effect of the new readout electronics on the existing Front End Electronics (FEE) of MuTr chamber. As the design value, a 1 % noise level for a typical charge is required on the FEE to realize 100  $\mu\text{m}$  position resolution. Therefore the concerns are how much the new electronics increase the noise and decrease the signal on the FEE.

A clear correlation between the position resolution and the noise level is measured from test experiment using 600 MeV/c electron beam at Laboratory of Nuclear Science (LNS), Tohoku University. Figure 5.1 shows the position resolution measured before installing MuTRG-AD board and after installing MuTRG-AD with  $C_{\text{split}}$  of 30 pF and 100 pF. No unpreferable effect is observed by adding the MuTRG-AD board other than increasing the noise and decreasing the signal on the FEE. Based on these results, this chapter is focused on the noise level as the effect on the current system.

The  $C_{\text{split}}$  of 56 pF was used for summer test experiment. The beam test at LNS shows that the H.V. gain of 50 V is needed to recover the MuTr chamber performance when the  $C_{\text{split}}$  of 100 pF is used. However, it is not desirable to gain the H.V. by 50 V because it makes the chamber operation unstable. On the other hand, the large fake hit rate is expected to obtain the good efficiency by selecting the  $C_{\text{split}}$  of 30 pF, which corresponds to split  $\sim 3$  % of signal. Then we chose the intermediate value of 56 pF ( $\sim 6$  % of signal) as  $C_{\text{split}}$ .

### 5.2 Noise

The noise on the FEE is discussed in terms of the root mean square (RMS) value of the pedestal. A sample of the pedestal distribution is shown at Figure 5.2 and Figure 5.3 shows

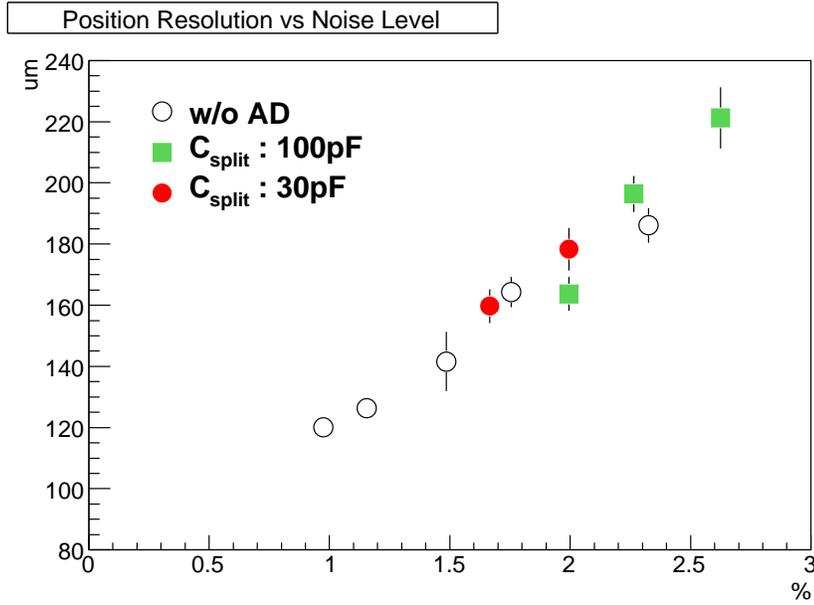


Figure 5.1: Position resolution vs Noise level. The definition of the noise level is the ratio of pedestal RMS to most probable value of the signal on peak strip. The position resolution includes the ambiguity of the reference  $\sim 50 \mu\text{m}$ .

the RMS values before (black) and after (red) installing MuTRG-AD and MuTRG-TX boards. Generally the noise on the FEE depends on the input capacitance which the chamber strip has. Then the channels connected to the longer strips shows the larger RMS values. Consequently the noise at station 2 is larger than station 1 on an average. The ratio of the RMS value after installing MuTRG-AD and MuTRG-TX boards to that before installing is shown at Figure 5.4. Adding MuTRG-AD boards means providing further input capacitance to the FEE. As the results, the RMS values increase 35 % for station 1 and 22 % for station 2 on average. Again the ununiformity of noise increase is caused by strip length.  $C_{\text{split}}$  is small compared to longer strip capacitance therefore the effect of adding MuTRG-AD boards is small for the channels of longer strip. The noise level which is the ratio of the RMS value to the typical signal value is discussed later.

### 5.3 Pulse height

Because MuTRG-AD steals a part of the charge induced in MuTr, the charge provided to the analog readout on FEE is reduced. The gain of FEE is calibrated by inputting the pulse to anode wires of MuTr[3]. The decrease of the gain by installing MuTRG-AD can be measured

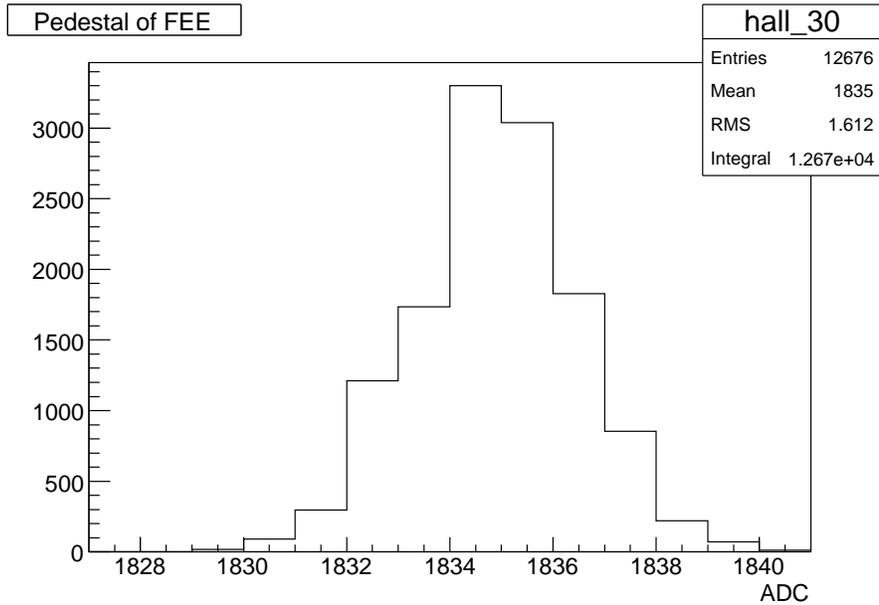


Figure 5.2: Pedestal distribution of a sample channel.

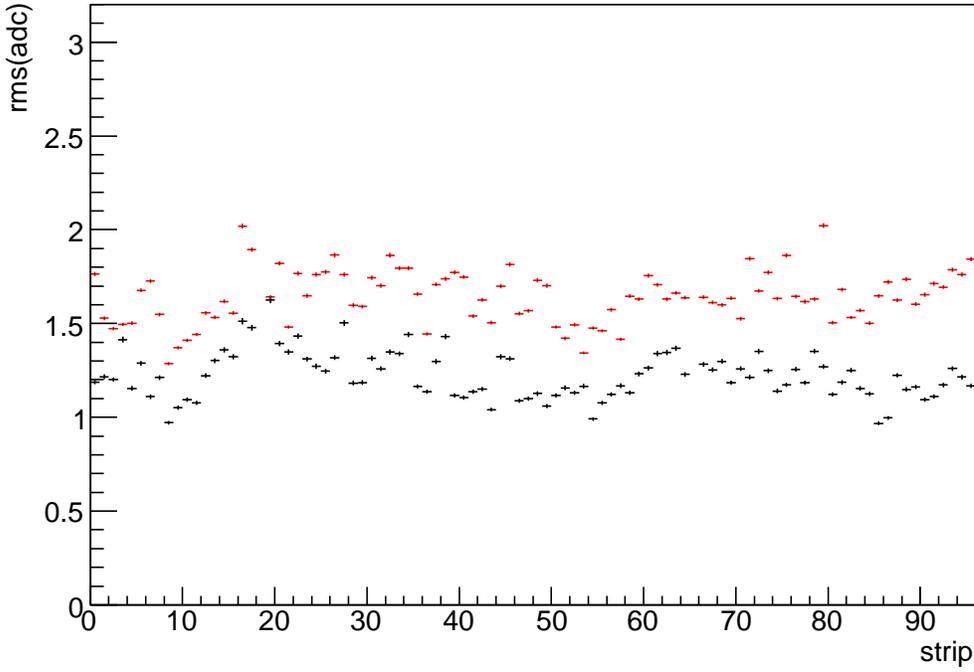
using calibration pulse by comparing the pulse height with and without MuTRG-AD. Figure 5.5 displays the ratio of the pulse height for the cathodes where we installed MuTRG-AD. The charge on FEE decreases to  $\sim 90\%$  after installing the MuTRG-AD boards.

The decrease of the gain is also studied using MPV measured by cosmic ray data. Figure 5.6 displays “q” value distribution for station 1, gap 2, cathode 2, and station 2, gap 2, cathode 1. In these cathodes, MuTRG-ADs were installed. The distribution for other cathodes has similar shape and MPV. The “q” is calibrated ADC value with gain coefficient of  $\sim 0.05$  in station 1 and  $\sim 0.1$  in station 2,  $q \sim \text{gain} \times \text{ADC}$ . MPV is obtained by fitting “q” distribution to the Landau function. The fitting function is also drawn in the figure.

To evaluate the decrease of the gain, some bad strips were removed in the analysis. MPV and “q” distribution are utilized to find bad strips. Figure 5.7 displays MPV as a function of strip number for station 1 (left) and station 2 (right). MPV for some strips are clearly lower than other strips. Such strips are discarded in the analysis.

In the test experiment, we took cosmic ray data with and without MuTRG-AD installed into station 2, half octant 2, gap 3 and cathode 1. (Though we also installed MuTRG-ADs into other cathodes as described above, they were installed throughout the data taking period and no MPV change can be measured.) We extracted MPV for these data set and compared them. Figure 5.8(left) displays the ratio of MPV of the data set, MPV with MuTRG-AD

Pedestal RMS Station 1



Pedestal RMS Station 2

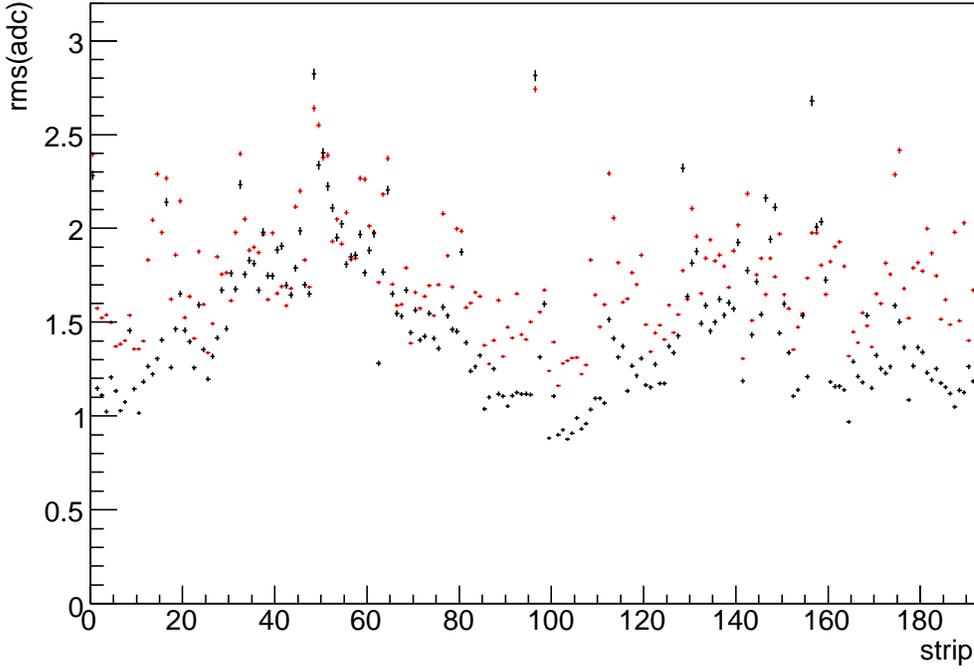
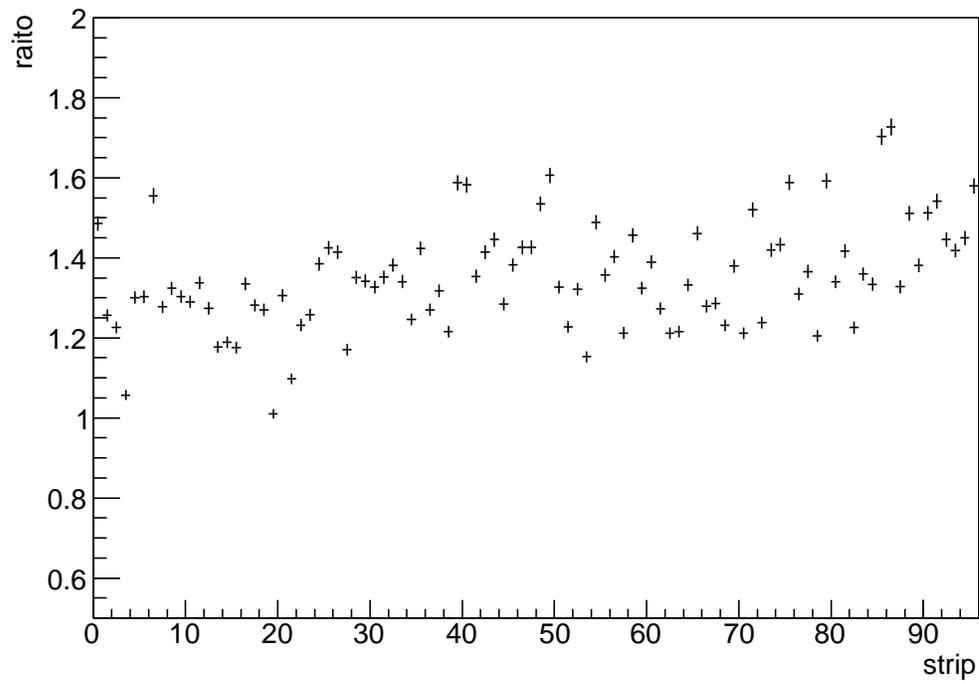


Figure 5.3: The RMS noise on the FEE for station 1 (top) and 2 (bottom). Black points shows the noise before installing MuTRG-AD board and red points are that after install.

Ratio of Pedestal RMS Station 1



Ratio of Pedestal RMS Station 2

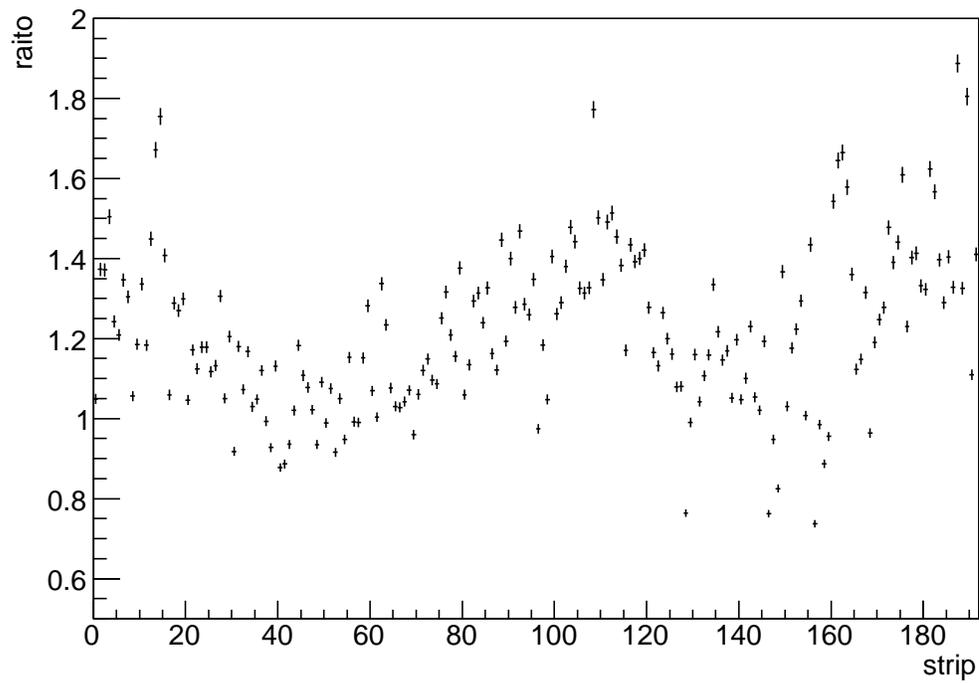
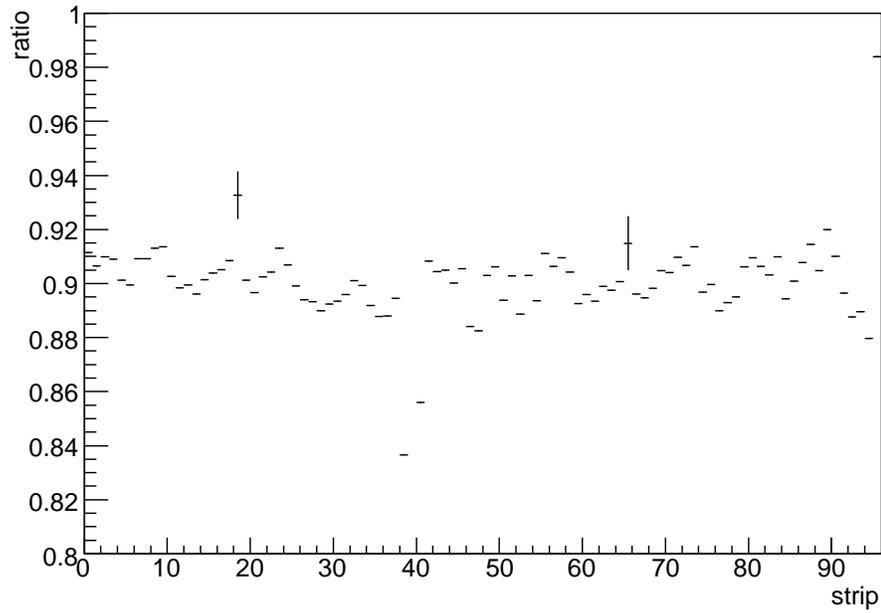


Figure 5.4: The RMS noise ratio of the noise after install to that before install.

Peak Ratio Station 1



Peak Ratio Station 2

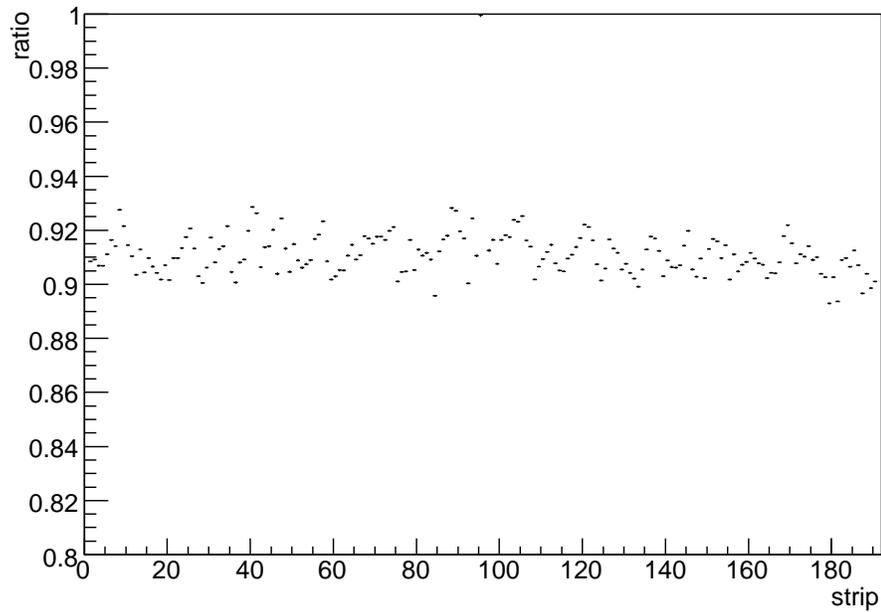


Figure 5.5: The ratio of the calibration pulse, the pulse height with MuTRG-AD divided by that without MuTRG-AD. The top plot is for station 1, gap 2, cathode 2 (strip 0 – 44 is in half octant 1 and strip 45 – 95 is in half octant 2). The bottom plot is for station 2, gap 2, cathode 1 (strip 0 – 95 is in half octant 1 and strip 96 – 191 is in half octant 2). MuTRG-AD was installed into these cathodes.

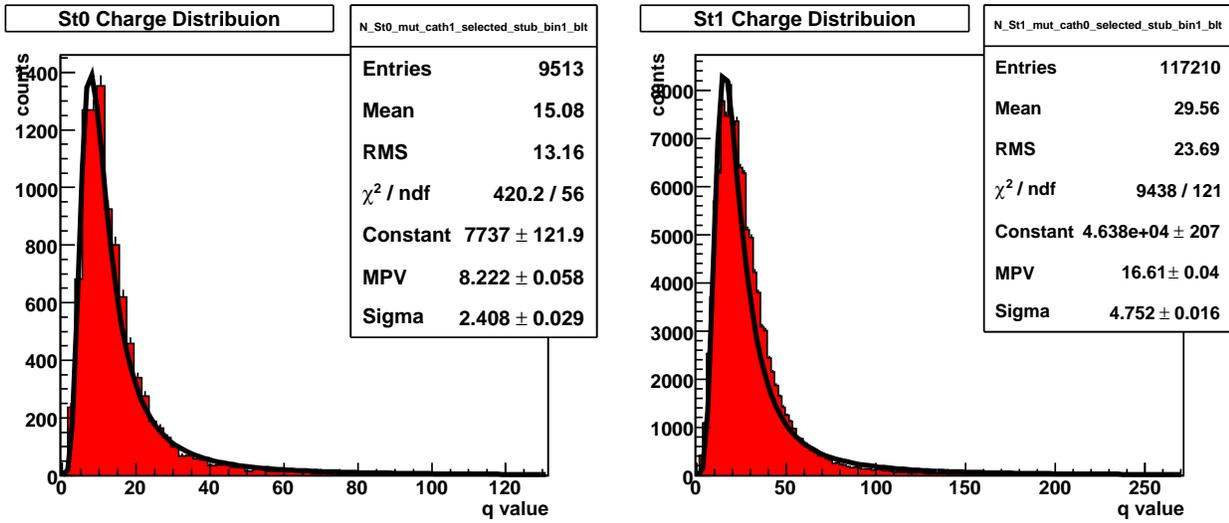


Figure 5.6: “q” distribution for station 1, gap 2, cathode 2 (left) and station 2, gap 2, cathode 1 (right). The distribution is fitted to the Landau function.

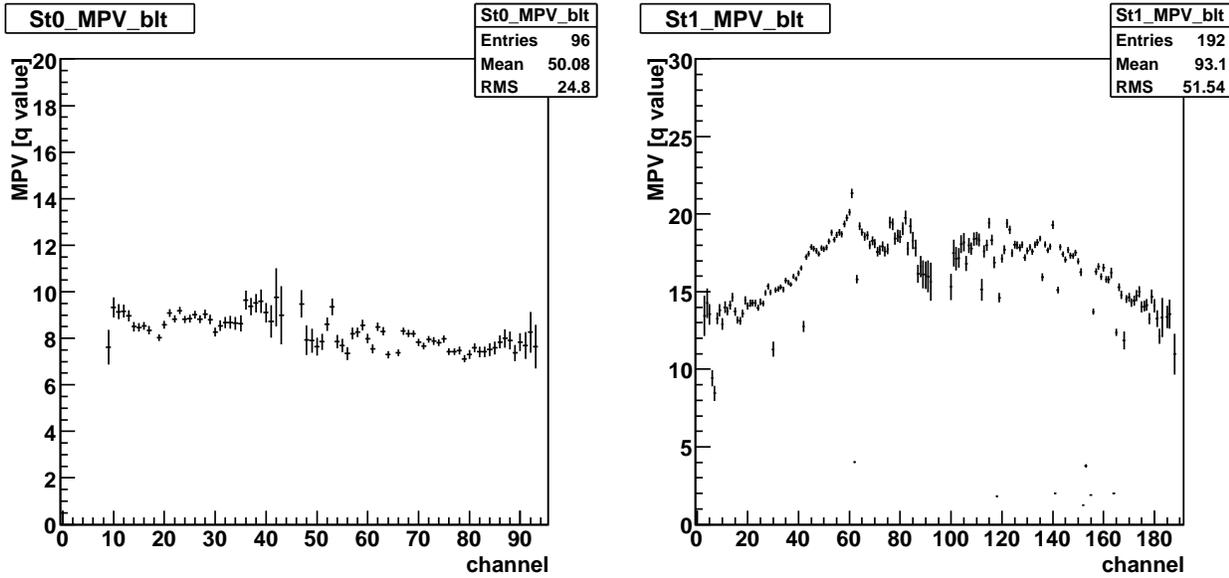


Figure 5.7: channel by channel MPV distribution of station 1, gap 2, cathode 2 (left), and station 2, gap 2, cathode 1 (right). In station 1, channel 0 – 44 is in half octant 1 and 45 – 95 is in half octant 2. In station 2, channel 0 – 95 is in half octant 1 and 96 – 191 is in half octant 2. MuTRG-ADs were installed these cathodes.

divided by that without MuTRG-AD, as a function of the strip number for station 2, gap 3 and cathode 1. MuTRG-AD was installed for the strips between two blue lines. Clearly, MPV at the region becomes low after installing MuTRG-AD compared to the other strips. Figure 5.8(right) displays the cathode-by-cathode average of the MPV ratio for station 2. Each point corresponds to one cathode in a half octant. For the cathode of Figure 5.8(left), strips between blue lines were used to calculate the average. The ratio of the cathode with MuTRG-AD is about 0.97, while it is  $\sim 1.03$  at the other cathodes. The fact that the ratio is not 1.0 for the other cathode indicates that the gain of MuTr is shifted during the data taking. Assuming the same size of the gain drift in the cathode with MuTRG-AD, the gain decrease by installing MuTRG-AD is evaluated to be  $(94.2 \pm 0.4) \%$ . The error is obtained considering the statistics and both strip-by-strip and cathode-by-cathode variations. As shown in Figure 5.5, the gain becomes  $\sim 90 \%$  for the calibration pulse and slightly different from the case of the cosmic ray signal. This difference is presumed to be due to the frequency dependence of the amplifier of MuTRG-AD. Because the signal of the cosmic ray and the calibration pulse have different frequency components, the response of MuTRG-AD could be different.

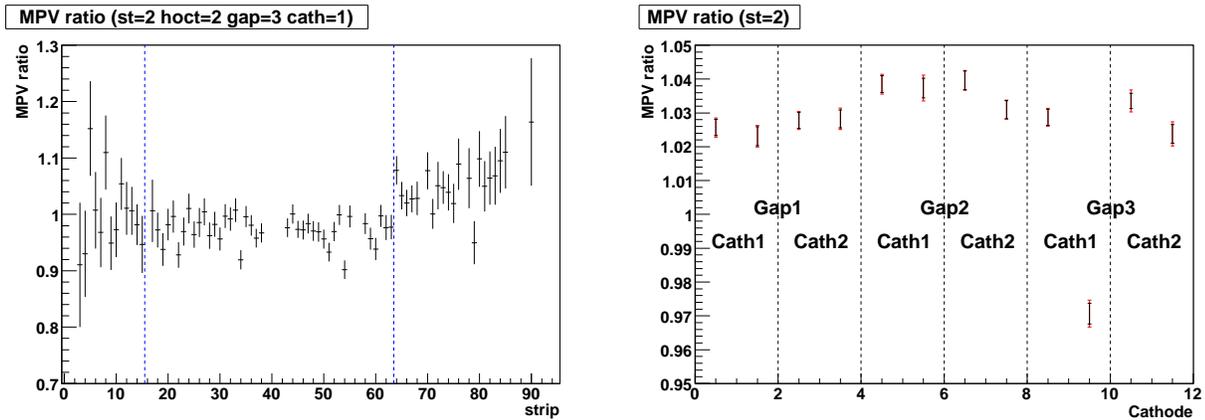


Figure 5.8: The MPV ratio with and without MuTRG-AD installed, MPV with MuTRG-AD divided by that without MuTRG-AD. (Left) The MPV ratio as a function of the strip number for the cathode where we installed MuTRG-AD. MuTRG-AD was installed for the strips between blue lines. Several strips are removed in the figure due to dead channel or too small statistics. (Right) The MPV ratio averaged over the strips in one cathode as a function of the cathodes in station 2. Two points in the same cathode, 0th and 1st bins for example, corresponds to half octant 1 (left point) and 2 (right point). For the cathode with MuTRG-AD, strips between blue lines are used to extract the average.

## 5.4 Noise level

The noise level means the ratio of the pedestal RMS value to the most probable value (MPV) of the charge distribution for the cosmic ray signal. A 1% noise level is the design value of MuTr chamber and should be achieved to realize the position resolution of  $100\ \mu\text{m}$ . Figure 5.9 and 5.10 display the noise level for station 1 and 2, respectively. MuTRG-ADs were installed into cathode 2 (non-stereo strips) at gap 2 for station 1 and cathode 1 (non-stereo strips) at gap 2 for station 2. The right middle two plots in Figure 5.9 corresponds to the place we installed for station 1, while the left middle plots in Figure 5.10 are the place for station 2. The red points in Figure 5.10 is obtained by the data with HV raised by 25 V. Black points are for the normal HV values.

The noise level is about 1 % of MPV except for gap 3 in station 1.<sup>1</sup> Though the ratio of MPV and pedestal RMS varied cathode by cathode, it is larger by  $\sim 30\%$  in the cathode where MuTRG-ADs were installed compared with other cathodes. This is consistent with our expectation in the test at Kyoto and RIKEN. As displayed in Figure 5.10, the noise level becomes smaller by about 30 % when HV was raised by 25 V. This implies that if HV is increased by 25 V, degradation of the position resolution will recover. Based on study of the noise level and position resolution as shown in Figure 5.1, 1.3 % (1.0 %) noise level results in the position resolution of  $120\ \mu\text{m}$  ( $100\ \mu\text{m}$ ). For this reason, we conclude that the degradation of the position resolution by installing the MuTRG boards is acceptable.

## 5.5 Timing of signal

As described in Section 2.1, installing MuTRG-AD changes the timing of the signal for the chamber. We compare the timing before and after installing MuTRG-AD. The timing of each signal is obtained by fitting four ADC samples in each signal to a quadratic function as displayed in Figure 5.11. The four ADC samples are set to 1.5, 6.5, 7.5, and 8.5 clock. The peak position of the fit function is used as the timing of the signal, we call it peak time. Figure 5.12 is a sample of the peak time distribution with and without MuTRG-AD. The peak time delays after installing MuTRG-AD. Figure 5.13 displays difference of the mean of the peak time as a function of the strip number. MuTRG-AD is installed into the strips between two blue lines. The delay is about 0.9 beak clocks.

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<sup>1</sup>Large noise level in station 1, gap 3 is presumed to be due to reasons which are unrelated to the MuTRG circuit.

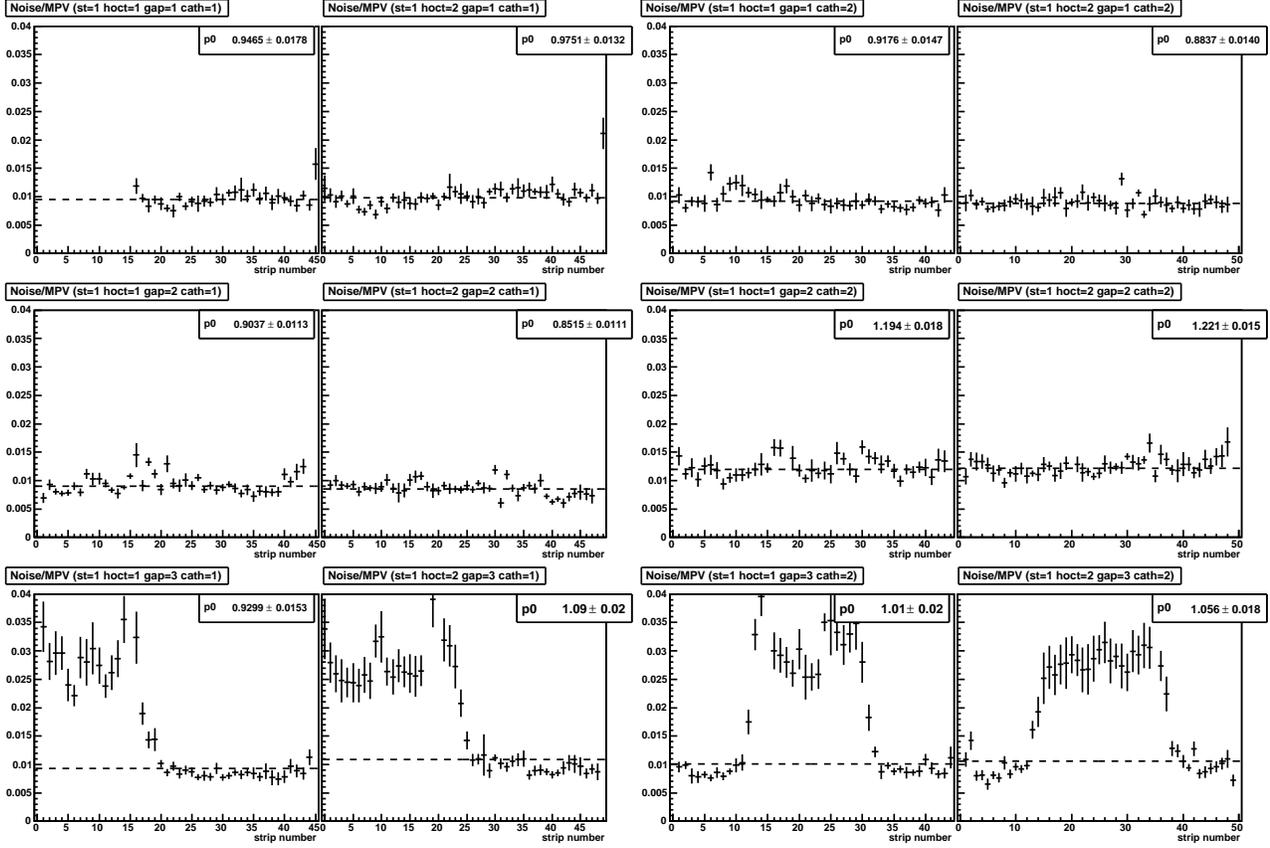


Figure 5.9: Noise level for station 1. A set of two histograms corresponds to one cathode plane. Left one of the set is for half octant 1 and right is for half octant 2. Gap number 1, 2 and 3 are from top to bottom. Left sets are for cathode 1 (stereo plane), and the right side is for cathode 2 (non-stereo plane). Channel 0 – 15 in cathode 1, gap 1, half octant 1 were disabled during the data taking. The average over each cathode is obtained by fitting the data to constant and the fit line is shown in the plot. The average value in % is displayed in the right top corner of each plot.

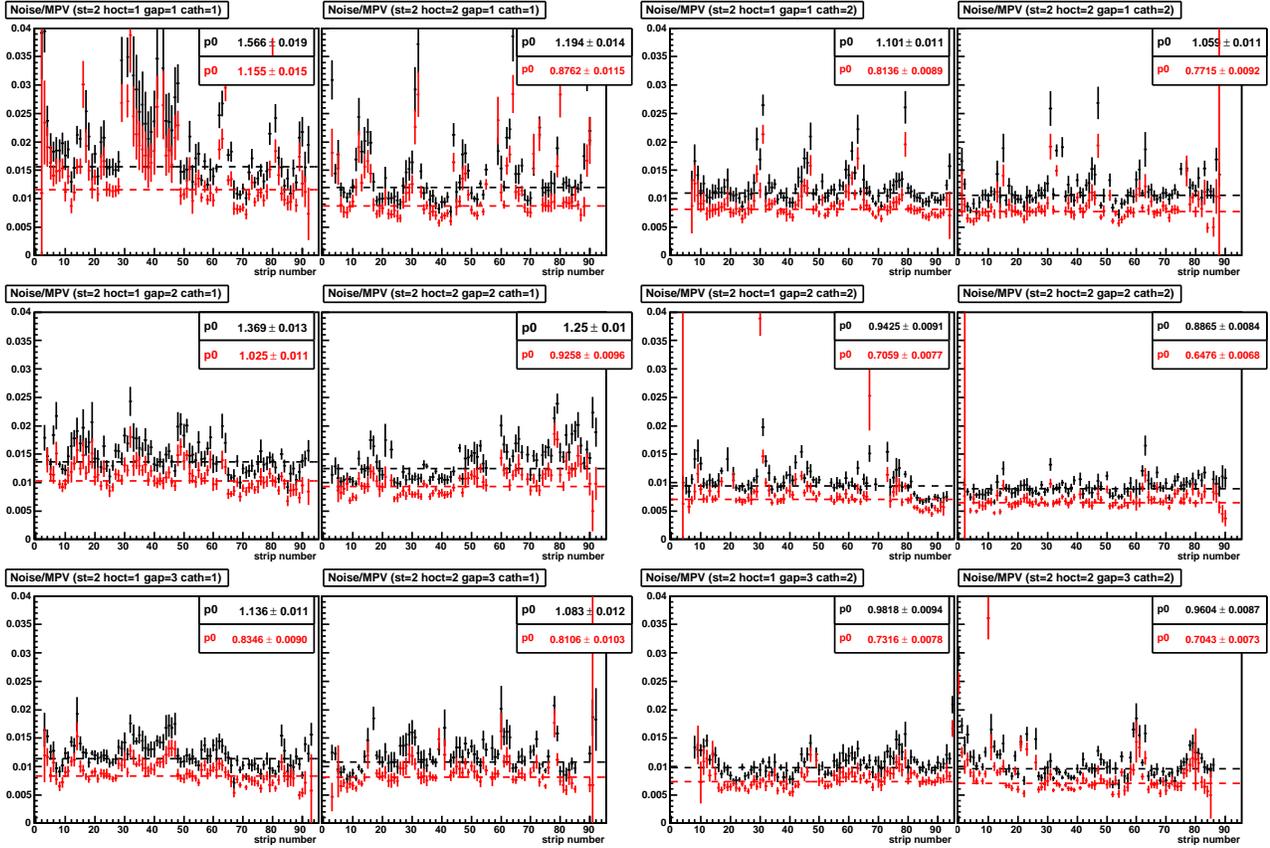


Figure 5.10: Noise level for station 2. A set of two histograms corresponds to one cathode plane. Left one of the set is for half octant 1 and right is for half octant 2. Gap number 1, 2 and 3 are from top to bottom. Left sets are for cathode 1 (non-stereo plane), and the right side is for cathode 2 (stereo plane). Red points are the case of HV=1925 V (The normal is 1900 V as black points.) The average over each cathode is obtained by fitting the data to constant and the fit line is shown in the plot. The average value in % is displayed in the right top corner of each plot.

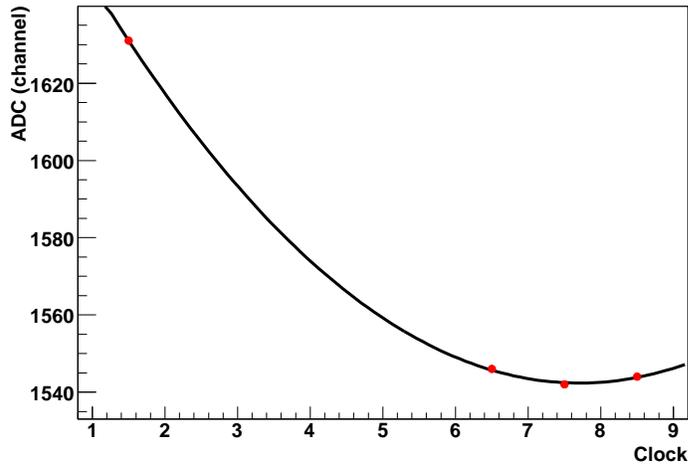


Figure 5.11: Example of four ADC samples. The samples are set to 1.5, 6.5, 7.5 and 8.5 clock. The samples are fitted to a quadratic function and the peak position of the fit function is used as a timing of the signal, which is called peak time.

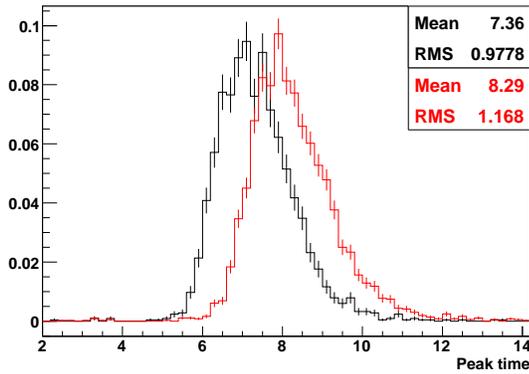


Figure 5.12: The peak time distribution for station 2, half octant 2, gap 2, cathode 1, strip 50. The black histogram is the peak time without MuTRG-AD and the red one is with MuTRG-AD.

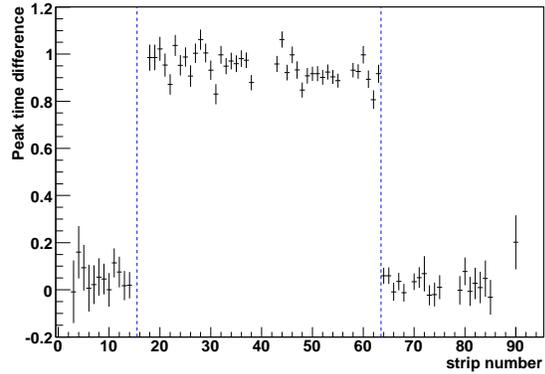


Figure 5.13: The mean of the peak time distribution as a function of strip number. This is for station 2, half octant 2, gap 2, cathode 1. MuTRG-AD was installed into the strips between two blue lines.

Based on this measurement, we will need to change the timing of the signal with MuTRG-AD. One concern is that the delay of MuTr FEE can not be set cathode by cathode. We plan to install MuTRG board into only two cathodes per station. Therefore, the timing of the signal becomes different by  $\sim 1$  clock between cathodes with MuTRG-AD and without MuTRG-AD in the same station. In study using calibration pulse, the shift of the timing by 1 clock changed the amplitude of the signal by 1 % as shown in Figure 5.14. However, in terms of the amplitude relative to the next strip, the difference is much small. For this reason, it is expected that keeping the position resolution is possible. To derive this results, we extracted the amplitude of the signal by fitting four ADC sample to a quadratic function.

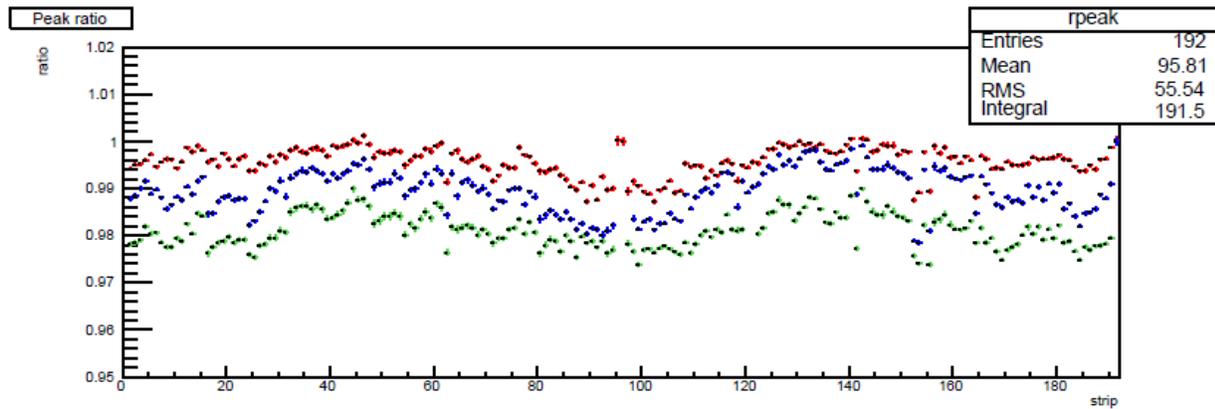


Figure 5.14: Dependence of the calibration pulse height on the timing of the signal. The points are the ratio of the pulse height relative to the optimal timing as a function of the strip number. These are for station 2, gap 2, cathode 1. Strip number 0 – 95 is in half octant 1 and strip number 96 – 191 is in half octant 2. Red, blue and green points are the cases that GL1 delayed by 1, 2 and 3 clocks (The peak time position becomes interpolation between four ADC samples).

## 5.6 Efficiency

One of the concerns in installing MuTRG-AD is the effect to the MuTr efficiency because MuTRG-AD steals the charge from the existing FEE. We also checked the cluster size to confirm that the number of valid clusters does not change with MuTRG-AD.

### 5.6.1 Efficiency

Figure 5.15 and 5.16 display “efficiency” of MuTr for gap 2. We installed MuTRG-AD into non-stereo cathodes in gap 2 in both station 1 and 2. The “efficiency” was evaluated as follows.

At the first step, stubs are detected using 4 cathodes without gap 2 in each station. The point where the cosmic ray passed is estimated using the stub at the second step. Then, at the last step, we examined whether there was a peak strip of any clusters at the point. We allowed the shift of  $\pm 1$  strips to find the peak strip at the last step because we did not confirm that the track is normal to the cathode plane or not.<sup>2</sup> Typically, the “efficiency” was 95 % in station 1 and 99 % in station 2. Significant difference of the “efficiency” is not observed between two cathodes in gap 2. This indicates that installing MuTRG-AD does not increase inefficiency of MuTr.

### 5.6.2 Cluster size

It is important to confirm that MuTRG-AD does not decrease the clusters with valid size. Because the position of MuTr is obtained by looking at the charge sharing between strips in the cluster. Figure 5.17 and 5.18 display number of strips which belong to a cluster (cluster size) for station 1 and 2, respectively. The distributions with red or green line correspond to the cathode where MuTRG-AD installed. In all cathodes, the cluster size has a maximum at 2. However, the size is slightly larger in the cathodes with MuTRG-ADs than others. This is because the cluster size depends on the timing of the signal from the chamber. (Though, we can’t find out the reason of the correlation.)

Figure 5.19 displays the correlation between the mean cluster size and mean peak time. The peak time is explained in Section 5.5. Each point in Figure 5.19 corresponds to a certain strip of MuTr and the mean of the cluster size and the peak time is for the strip. The black points in Figure 5.19 indicate strips without MuTRG-AD, while red and green points are with MuTRG-AD. MuTRG-AD delays the timing of the signal by  $\sim 1$  clock and the cluster size becomes larger therewith. As shown in Figure 5.19, the strips with MuTRG-AD look to have the same correlation as those without MuTRG-AD. Therefore, It is expected that there is no significant difference in the cluster size between strips with and without MuTRG-AD.

## 5.7 Summary of this chapter

In this chapter, we examined the impact on the existing readout system. The items we checked are the noise level, the pulse height (the gain decrease), the signal timing, the efficiency of

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<sup>2</sup>The “efficiency” is also evaluated for gap 1 and 3 using same method. However, it is much worse than gap 2 because identification of good track is more difficult by this method.

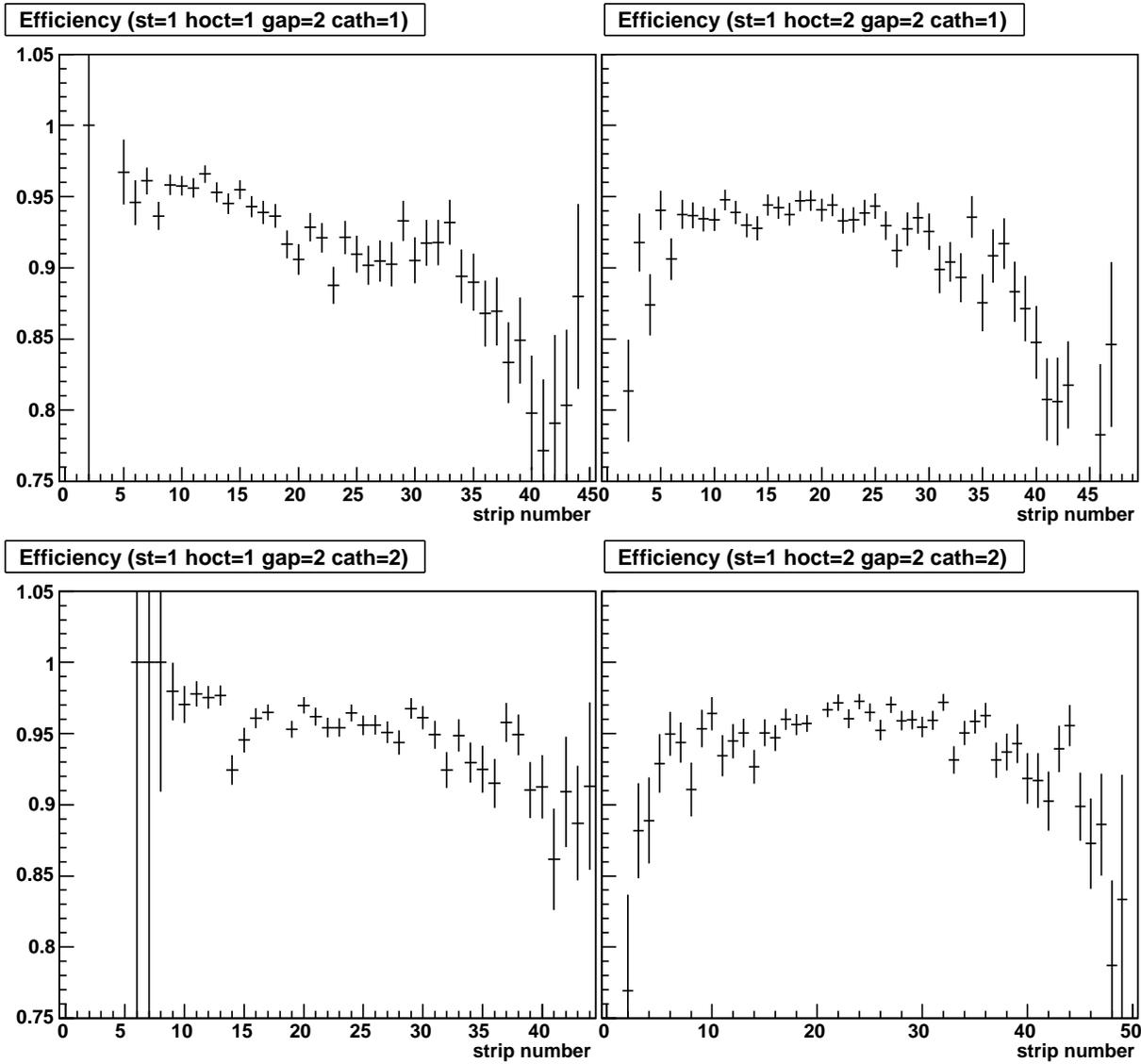


Figure 5.15: Efficiency of MuTr for gap 2, station 1 as a function of the strip number. The top two plots are for cathode 1, while the bottom two are for cathode 2. The left side is for half octant 1 and the right side is for half octant 2. MuTRG-ADs were installed into cathode 2. The strips with small number in the half octant 1 is because near strips in gap 1 were disabled in the data taking.

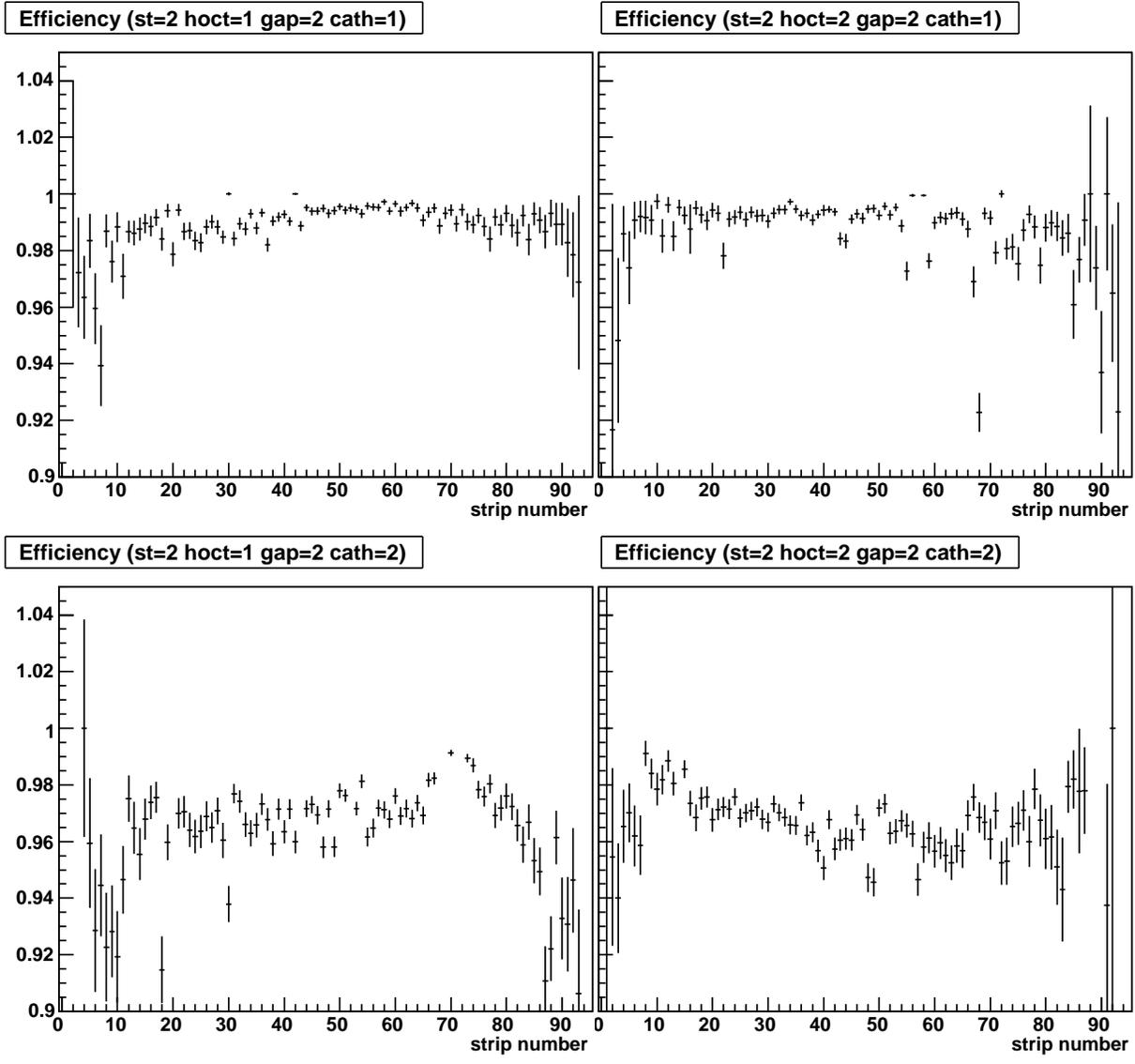


Figure 5.16: Efficiency of MuTr for gap 2, station 2 as a function of the strip number. The top two plots are for cathode 1, while the bottom two are for cathode 2. The left side is for half octant 1 and the right side is for half octant 2. MuTRG-ADs were installed into cathode 1.

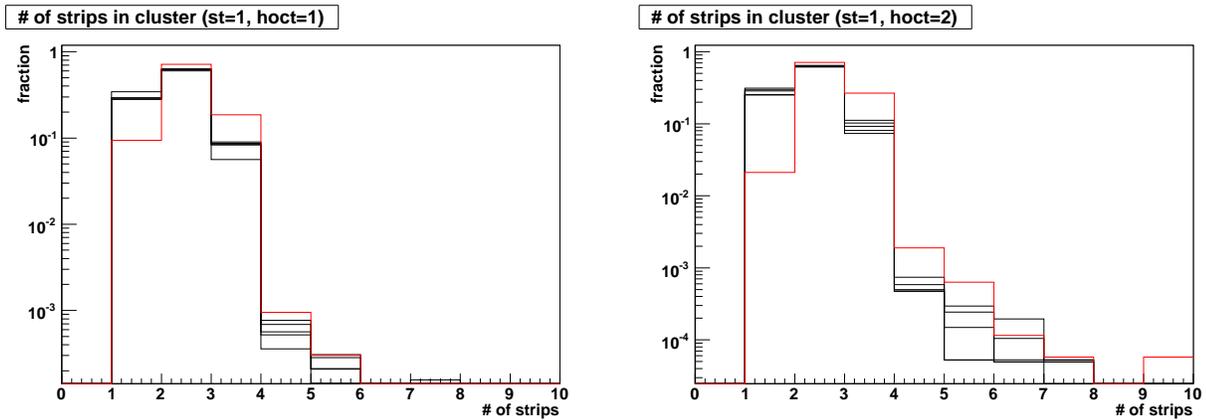


Figure 5.17: Number of strips in a cluster for station 1. The left plot is for half octant 1 and the right plot is for half octant 2. Six histograms for six cathodes are superposed. The distribution with red line (gap 2, cathode 2) is for the cathode with MuTRG-AD.

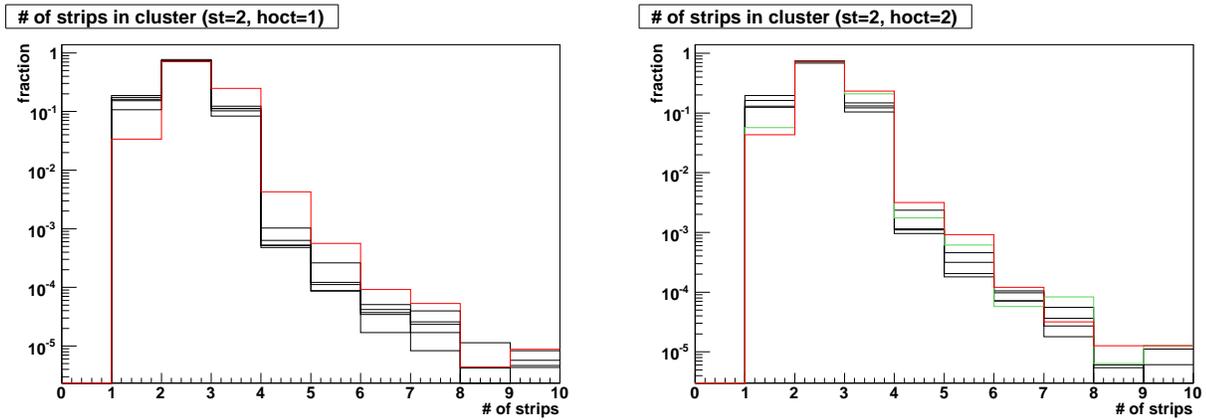


Figure 5.18: Number of strips in a cluster for station 2. The left plot is for half octant 1 and the right plot is for half octant 2. Six histograms for six cathodes are superposed. The distributions with red (gap 2, cathode 1) and green (gap 3, cathode 1) line are for the cathode with MuTRG-AD.

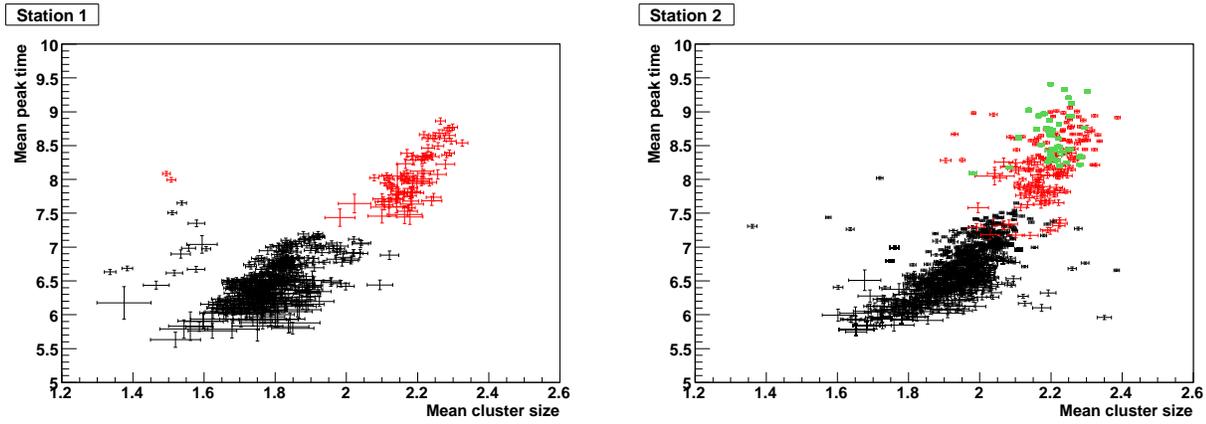


Figure 5.19: Correlation between mean cluster size and mean peak time of the signal. The left plot is for station 1 and the right plot is for station 2. Each point corresponds to a strip. Strips which MuTRG-ADs installed into are colored by red (gap 2, cathode 2 for station 1, and gap 2, cathode 1 for station 2) and green (gap 3, cathode 1 for station 2).

MuTr. Degradation of the position resolution of MuTr was evaluated base on the noise level. It turns out that the position resolution becomes  $120 \mu\text{m}$  when MuTRG-AD is installed. The degradation will recover by raising HV by 25 V. From the study of the efficiency and the cluster size, no inefficiency is expected to be provided by installing MuTRG-AD. Another impact is that MuTRG-AD delay the timing of the signal. As far as the measurement of calibration pulse, we found that the delay will not make the position resolution worse. Finally, we conclude that the impact on the existing readout system by MuTRG-AD is acceptable.

# Chapter 6

## Performance of MuTRG-AD and MuTRG-TX boards

In this chapter, we would like to discuss the performance of digitized signal. In the summer experiment, the digitized signal is created on the MuTRG-AD board using the signal from MuTr chamber, serialized and transmitted by the MuTRG-TX board to the interface board. The interface board deserialized the data and output to the MuID ROC, which we temporarily used for the data read out module of the summer test experiment. The data of our electronics was then transmitted to the PHENIX DAQ system.

In section 6.1, how to control the fake hit rate of our electronics is described, the efficiency of our boards is evaluated in section 6.2, and time jitter, which is intrinsic property of our electronics, is discussed in section 6.3.

### 6.1 Fake hit rate

At the beginning of the summer test, we measured the fake hit rate to determine the reasonable threshold for the MuTRG-AD boards. The fake hit rate can be calculated with the following equation.

$$(\text{fake hit rate}) = \frac{(\text{number of hits})}{(\text{number of triggers}) \times (\text{gate width})} [Hz]$$

Since the gate width of the MuID ROC is 212nsec (2 beam clock wide), the term of "gate width" equals 212nsec in the above equation.

We measured the fake hit rate at out of the timing (latency), therefore, most of the hit data from our electronics can be considered as the data caused by the noise. This means we really measured the fake hit rate and didn't count any real hit data from the MuTr.

The procedure of determination of the threshold for each channel is as following.

1. measure the fake hit rate channel by channel when the threshold of all channels are the same value. we measured at the threshold value of 20, 30 and 34 mV.
2. fit the fake hit rate with an exponential function,

$$y = p_0 \exp(p_1 x)$$

here,  $y$  and  $x$  denote the fake hit rate and the threshold, respectively. Figure6.1 shows the typical fit.

3. from the fitting function of each channel, calculate the threshold with which the fake hit rate of each channel would be the value we want.
4. implement the calculated threshold to the MuTRG-AD boards. Figure6.2 shows the fake hit rate of the St2. we can notice that, except a few channels, we successfully control the fake hit rate by setting the threshold channel by channel. Here, there was no event observed in which several strips fired at once by fake hit.

In the summer test experiment, our trigger board was operated with the threshold at which the fake hit rate would be around 1kHz and 10kHz.

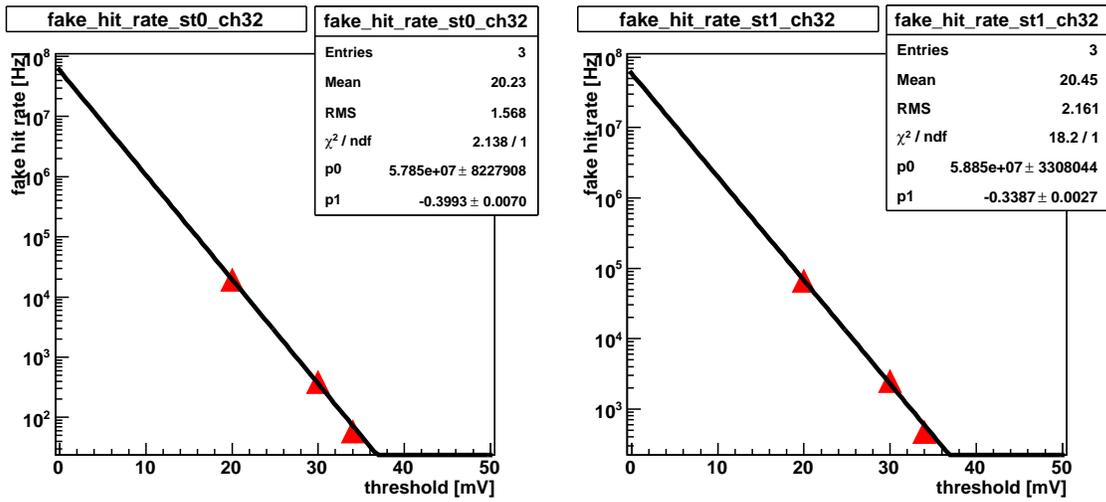


Figure 6.1: Fit the fake hit rate with exponential function at the point 20, 30 and 34 mV of the threshold. These plots shows the typical fit. (left:33ch of the St1, right:33ch of the St2)

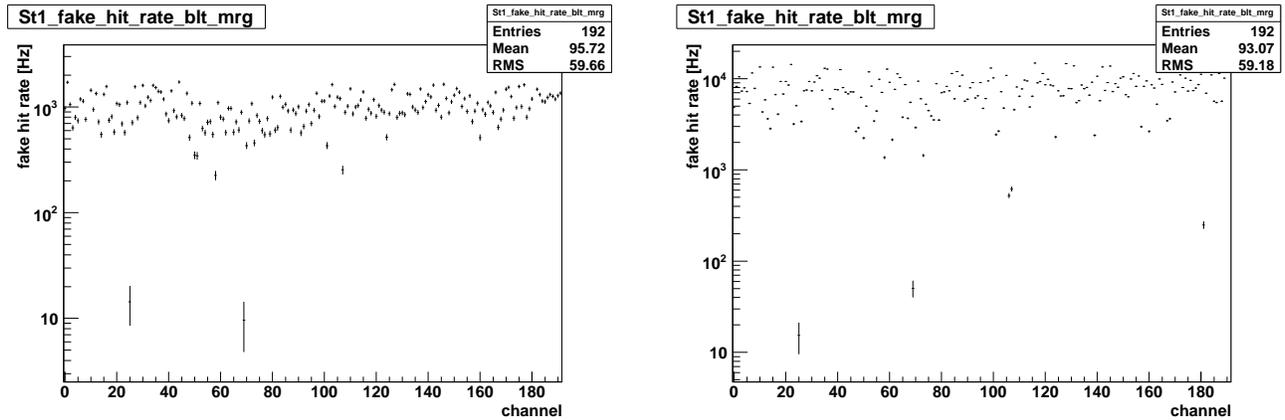


Figure 6.2: Fake hit rate of the trigger board in station2. The threshold was set to make the fake hit rate at around 1kHz (left) and 10kHz (right).

## 6.2 Efficiency

The one of main goals of the summer test experiment is to measure the efficiency of our electronics with infinite gate width. In this section, we discuss about the efficiency of our electronics.

### 6.2.1 Efficiency evaluation

In this subsection, the procedure of evaluating the efficiency is described.

First of all, bad channels of the MuTr should be took away. This is a reasonable cut because

we would like to sort out whether the problem, if it occurred, is caused by our electronics or by the MuTr itself. In order to determine bad channels, the most probable value (MPV) of the charge distribution for each strip was investigated. (see figure 5.6 and 5.7) Figure 5.7 shows the MPV values of St1 and 2 of the MuTr. The MPV for some strips are clearly lower than the peripheral strips. These channels were taken away because this would indicate that they are either broken/dead strips or problematic calibration constants.

Secondly, the "q value", which is the calibrated ADC value, dependence of the efficiency (turn on curve) of St1 and St2 was derived and fitted (Fig 6.3). The fitting function is

$$f(x) = \frac{p_2}{2} \left( 1 + \frac{2}{\sqrt{\pi}} \int_0^x dx' \exp\left(-\frac{(x' - p_0)^2}{2p_1^2}\right) \right). \quad (6.1)$$

The value of the plateau ( $p_2$ ) of the turn on curve achieves almost 1.0 at both St1 and St2. Taking account of the MPV value from Fig 5.7 (St1: 8~10, St2: 14~19), it can be claimed that the efficiency of our trigger board against the minimum ionization particle (MIP) is almost 100%.

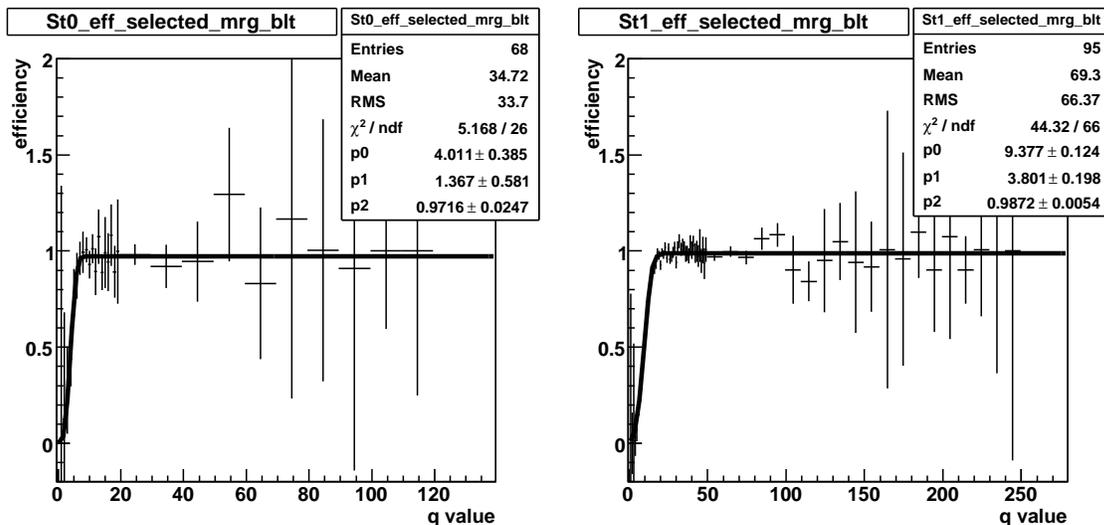


Figure 6.3: The efficiency curve of our electronics. (left: St1, right: St2) The horizontal axis denotes the q value.

Finally, we calculate the efficiency against the peak strip. In order to calculate, it is necessary to extract the fitting function. Since the plateau of the turn on curve is consistent with 1.0 within uncertainty in figure 6.3, we assume it, in other words, fix  $p_2 = 1.0$  in equation (6.1), and then refit the turn on curve (top row of figure 6.4). In Fig 6.4, the charge distribution

of the peak strip is also represented. Here, x axis denotes q value. In those figures, the charge distribution times the fitting function is also over-plotted. The efficiency against the peak strip is evaluated by following expression,

$$(\text{efficiency of the peak strip}) = \frac{(\text{Integral of the charge distribution times the turn of curve})}{(\text{Integral of the charge distribution})}$$

As a result, the efficiency against the peak strip achieved to 94% at St1 and 91% at St2.

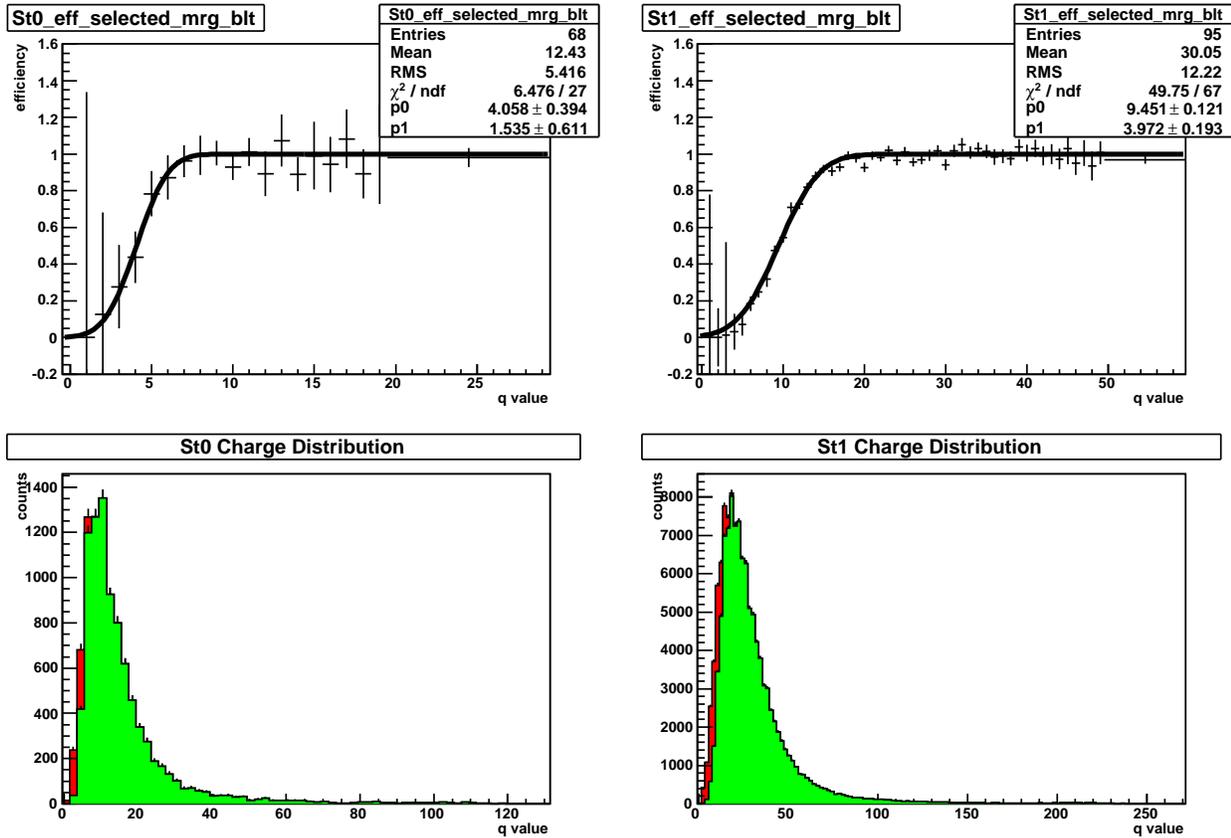


Figure 6.4: top row: The turn on curve of St1 (left) and St2 (right) fitted by equation (6.1) ( $p_2$  is fixed to 1.0). We can easily notice that the q value of the rising edge is below/equal to the MPV (St1: 8~10, St2: 14~19). bottom row: The charge distribution of St1 (left) and St2 (right). The red is the charge distribution of the peak strip and the green histogram represents the distribution of (the charge distribution) × (the turn on curve).

## 6.2.2 Efficiency value when the HV of the MuTR are raised 25V

The normal operation high voltage value of the station2 of the MuTr is 1900V. Since our trigger board get about 5 percent of the signal from the MuTr, it will be necessary to operate the MuTr with the higher voltage to recover its performance when our electronics is fully installed to the PHENIX. This subsection is about the efficiency value which is calculated from the data set acquired when the HV of the MuTR was raised 25V (only station2) in the summer test.

Figure 6.5 is the charge distribution of the peak strip of cluster. The left histogram is the distribution when the HV is 1900V and the right is when the HV is 1925V. The major transition is the MPV. It changes 17 to 22. While the MPV converts, the shape of the turn on curve doesn't change (figure 6.6) because the data set of HV=1900V and 1925V were taken at the same threshold, which is controlled to make the fake hit rate become 1kHz (see section6.1). This means the efficiency value of the HV=1925V become higher than it of the HV=1900V. The same procedure as the section 6.2.1 has been done (figure 6.7), and the efficiency against the peak strip increased to 95%.

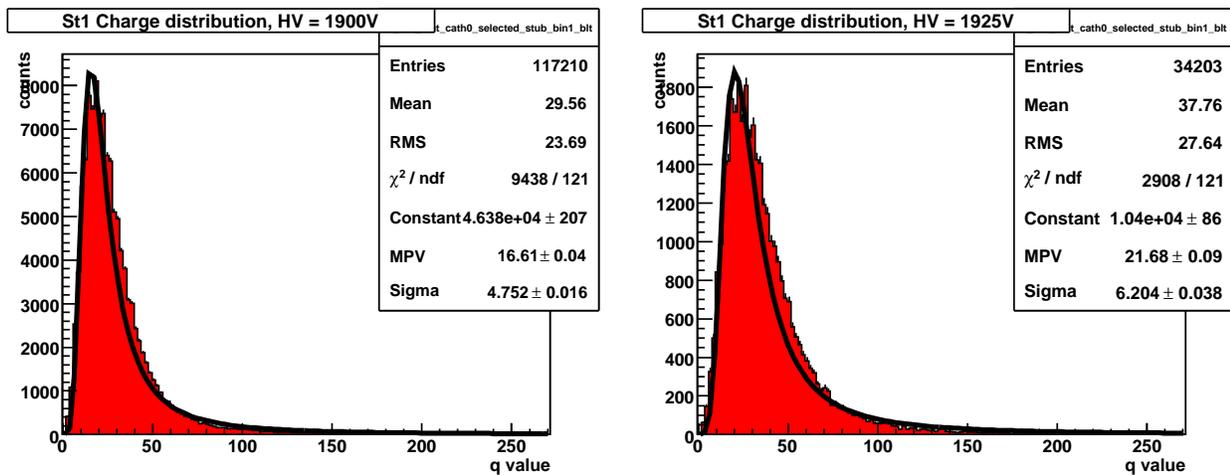


Figure 6.5: The charge distributions with different high voltage value. (left:1900V, right:1925V) The fitting function (landau function) is also drawn.

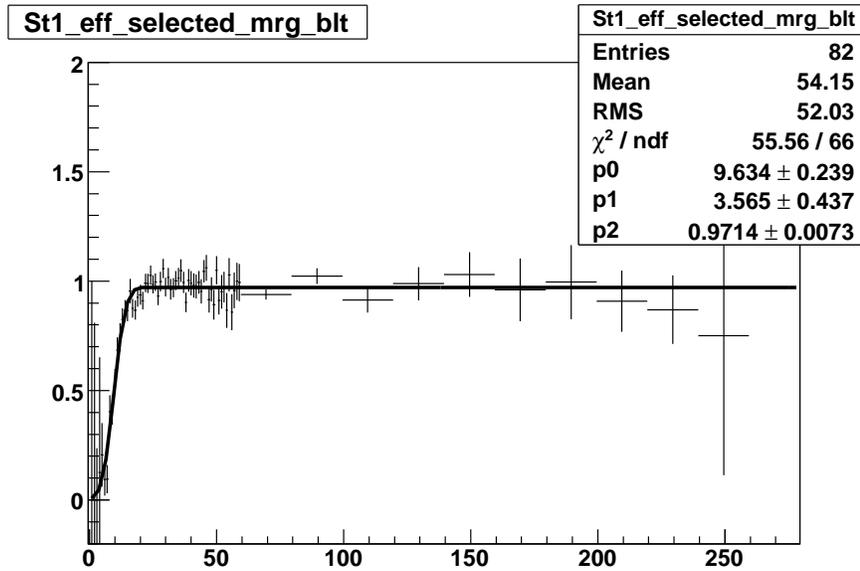


Figure 6.6: The efficiency curve for the HV=1925V (St2) fitted by equation (6.1) ( $p_2$  is not fixed). Compared to the right plot of figure 6.3 (HV=1900V), we can claim that the shape of the turn on curve doesn't change in different high voltages if threshold doesn't change.

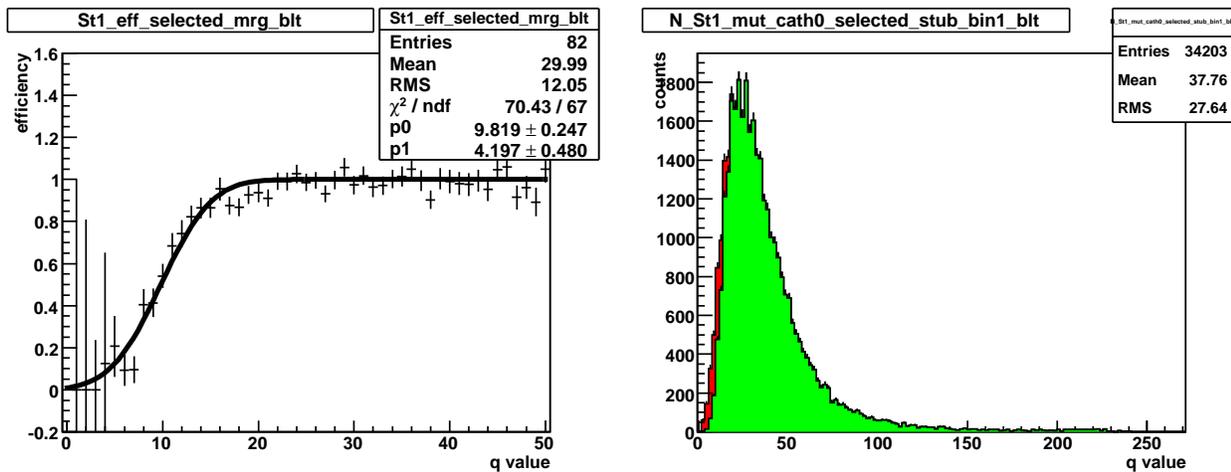


Figure 6.7: right: The turn on curve of the HV=1925V fitted by equation (6.1) ( $p_2$  is fixed to 1.0). left: The charge distribution of the HV=1925V. The red is the charge distribution of the peak strip and the green histogram represents the distribution of (the charge distribution)  $\times$  (the turn on curve).

### 6.2.3 Threshold dependence of the turn on curve

Threshold dependence of the efficiency curve of the MuTr St2 is represented in this subsection.

It is natural for the rising edge of the turn on curve to change with different threshold. However, the rising width doesn't change with different threshold. To confirm this, the turn on curves of the St2 with the threshold value of  $\sim 28\text{mV}$ ,  $\sim 25\text{mV}$  and  $20\text{mV}$  were studied. The turn on curve was fitted by equation (6.1), and the result was compared. Table 6.1 is the result of the fitting of each efficiency curve shown in figure 6.8. Here, the efficiency against the peak strip is also shown. These efficiencies are extracted by the same procedure explained in the section 6.2.1. The parameter  $p_0$  and  $p_1$  indicate the rising edge and the rising width of the turn on curve, respectively. The parameter  $p_2$  is the value of the plateau. From the table 6.1, it can be claimed that the rising width ( $p_1$ ) does not change while the rising edge ( $p_0$ ) differs in different threshold. Since the MPV is not affected by the threshold value, lower the threshold is set, higher the efficiency can be achieved. This result means the reasonable performance of our trigger board.

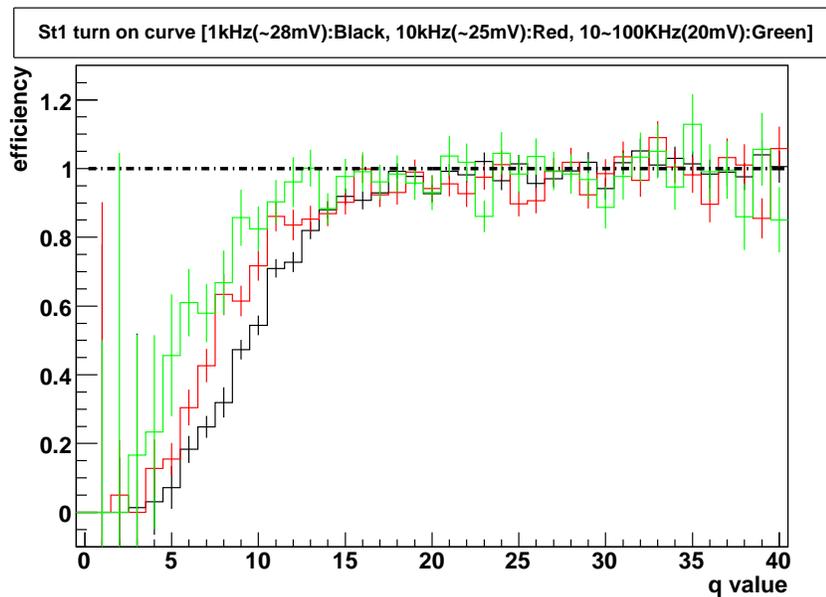


Figure 6.8: St2 efficiency curve of each threshold. The dashed line indicates the value of 1.0. black: the threshold where the fake hit rate become 1kHz ( $\sim 28\text{mV}$ ), red: the threshold where the fake hit rate become 10kHz ( $\sim 25\text{mV}$ ), green: the threshold equals to 20mV (with this threshold, the fake hit rate become 20kHz $\sim$ 100kHz)

parameter	Black( $\sim 28\text{mV}$ )	Red( $\sim 25\text{mV}$ )	Green( $20\text{mV}$ )
$p_0$ (mean)	$9.4 \pm 0.1$	$7.7 \pm 0.2$	$5.5 \pm 0.7$
$p_1$ (sigma)	$3.8 \pm 0.2$	$3.5 \pm 0.3$	$4.0 \pm 0.9$
$p_2$ (plateau)	$0.99 \pm 0.01$	$0.96 \pm 0.01$	$0.98 \pm 0.01$
efficiency	91%	93%	96%

Table 6.1: Table of fitting parameters.  $p_0$  is the rising edge,  $p_1$  is the rising width and  $p_2$  is the plateau. The last column is the efficiency value against the peak strip.

## 6.3 Time jitter

In the summer test experiment, we took the data at various latencies. This is because we know our trigger board have time jitter more than 1 beam clock (106 nsec) and we couldn't decide the best latency. This fact means that the efficiency of our electronics become lower than 1.0 with 1 beam clock (BCLK) gate width though it is achieved with infinite width. In this section, we would like to estimate how much efficiency our trigger board can achieve with various gate width.

### 6.3.1 Timing scan

The time information we can get from the data set taken by the PHENIX data acquisition (DAQ) system is only the timing scan plot. This is a plot of the efficiency versus the latency. The efficiency value is extracted from the  $p_2$  (plateau) of the equation (6.1) which is used to fit the turn on curve. Because the MuID ROC, which we temporarily used as our data acquisition module in the PHENIX DAQ System, can take the data at a particular latency, the efficiency doesn't achieve 1.0. In fact, the efficiency value ( $\sim 1.0$ ) of section 6.2.1 is calculated with adding data sets acquired at various latencies.

We took the data at various latencies. The timing scan plot is figure 6.9. Since the gate width of the MuID ROC is 2BCLK (212 nsec), the integration value of the timing scan plot is about 2.0.

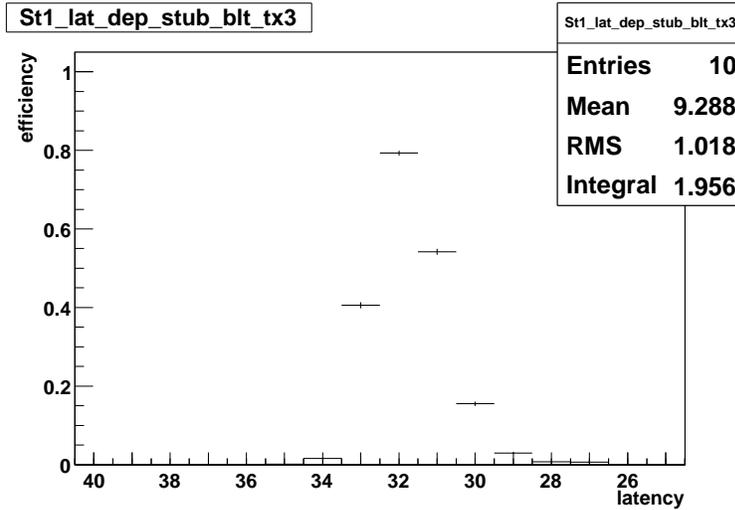


Figure 6.9: Timing scan plot. the data point is where the latency is 40, 35, 34, 33, 32, 31, 30, 29, 28 and 27.

### 6.3.2 Data from Local DAQ

As the gate width of the MuID ROC is  $2\text{BCLK}$  and  $\text{BCLK}$  is not synchronous to cosmic ray, it is quite complicate to evaluate the efficiency with various gate width from the timing scan plot. In order to estimate the efficiency with various gate width correctly, the accurate time distribution of the output signal of our trigger board should be acquired. This data is what we can't get with the PHENIX DAQ system since it is operated synchronously with the  $\text{BCLK}$  and can't have the resolution smaller than the  $\text{BCLK}$  range (106 nsec). To compensate this problem, we installed one MuTRG-AD board into the gap3 of the MuTr St2 as well as the gap2 and took data with a PC which was temporarily placed near the MuTR (Local DAQ) in the summer test experiment. In this subsection, data from the Local DAQ system is reported.

We took the data not only from our electronics but also from the GL1 trigger with a TDC module. This GL1 trigger data enables us to treat the data from our electronics as if it is acquired by the PHENIX DAQ. Figure 6.10 is the TDC distribution, normalized appropriately, of the GL1 trigger. There are two peaks because we took the data with the LL1 and the BLT during the summer test. The left and right peak of the figure 6.10 are considered to be the distribution of the LL1 and the BLT trigger, respectively. In fact, figure 6.10 implies that the LL1 and the BLT have different timing and the best latency setting against each trigger should be differed. Therefore, data analysis should be done separately.

Figure 6.11 is the distribution of the MuTRG-AD board. It is also normalized appropriately.

The black line shows the distribution with no requirement (w/o GL1 distribution), and the red line indicates the distribution with the requirement of the coincidence of the GL1 trigger (with GL1 distribution). From figure 6.11, we can notice that the "with GL1 distribution" is broadening compared to the "w/o GL1 distribution".

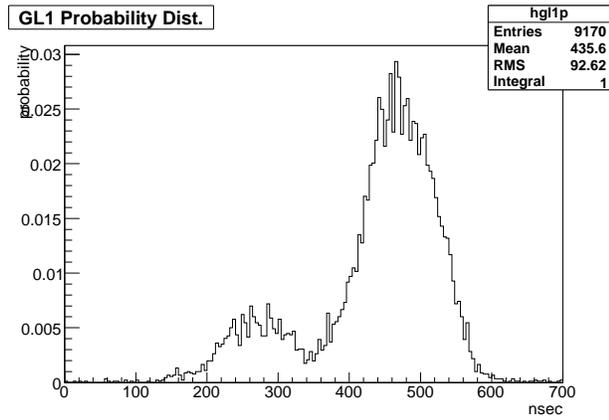


Figure 6.10: GL1 trigger distribution.

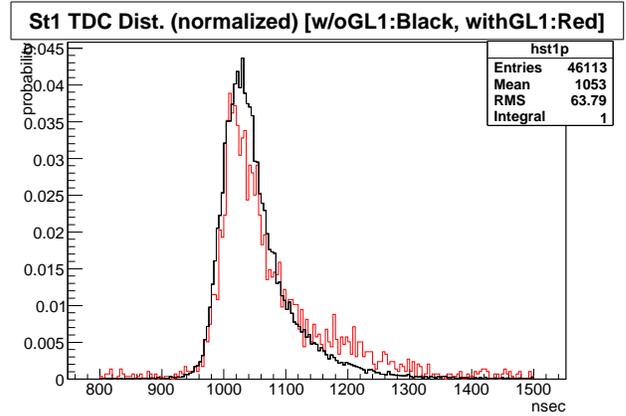


Figure 6.11: TDC distribution of St2 taken by the Local DAQ system. the black is the "w/o GL1 distribution" and the red is the "with GL1 distribution".

### 6.3.3 Simulation of timing scan & Fit

Although the data from Local DAQ gives us the accurate time information of our electronics, doubts against the data remains since it is not refined compared to the data taken by the PHENIX DAQ. For example, we never know the ADC distribution of the data from the Local DAQ and, therefore, can't execute appropriate cuts except setting the proper threshold. To extend the credit of the data taken by the Local DAQ, we reconstruct the timing scan plot from it and fit the real timing scan plot by the reconstructed ones. In this subsection, the procedure of the simulation and the fitting are described.

In order to simulate the timing scan plot, it is necessary to calculate the efficiency value of each latency. It is calculated from following expression,

$$(\text{efficiency}) = \int_{t_{\text{offset}}+t_{\text{trig-min}}}^{t_{\text{offset}}+t_{\text{trig-max}}} dt [G_{\text{trig}}(t - t_{\text{offset}}) \times \int_t^{t+2BCLK} dt' F_{\text{tdc}}(t')].$$

Here, each character indicates as following list.

- $G_{\text{trig}}$ ; Probability distribution of the trigger. It is the normalized TDC distribution of LL1 or BLT. (refer Figure 6.10)<sup>1</sup>
- $F_{\text{tdc}}$ ; Probability distribution of the output signal from the MuTRG-AD board. It is also normalized appropriately. (Figure 6.11)
- $t_{\text{offset}}$ ; (latency)  $\times$  (BCLK=106nsec) + (phase difference between the clock on the MuTRG-TX board and the MuID ROC)
- $t_{\text{trig-min}}/t_{\text{trig-max}}$ ; Minimum/Maximum value of the horizontal axis of the  $G_{\text{trig}}$  distribution.

In the simulation, the term of "phase difference between .." (Phase Diff, its range is 0~105 nsec) in the  $t_{\text{offset}}$  is an important parameter and the simulation plot with different value of the "Phase Diff" results in different shape. Figure 6.12 and 6.13 are the example of the simulated timing scan plot. In these figures, simulated plots with "Phase Diff" value of 0, 35, 70 and 105 nsec are represented. Figure 6.12 is resulted from the "with GL1 distribution" (see section 6.3.2) as the term of  $F_{\text{tdc}}$ , and figure 6.13 is simulated from the "w/o GL1 distribution" (see section 6.3.2). The term of  $G_{\text{trig}}$  is the BLT distribution in both figures. Since the range of the "Phase Diff" is 0 nsec to 105 nsec, 106 simulation plots can be created and they are used when we fit the real timing scan plot.

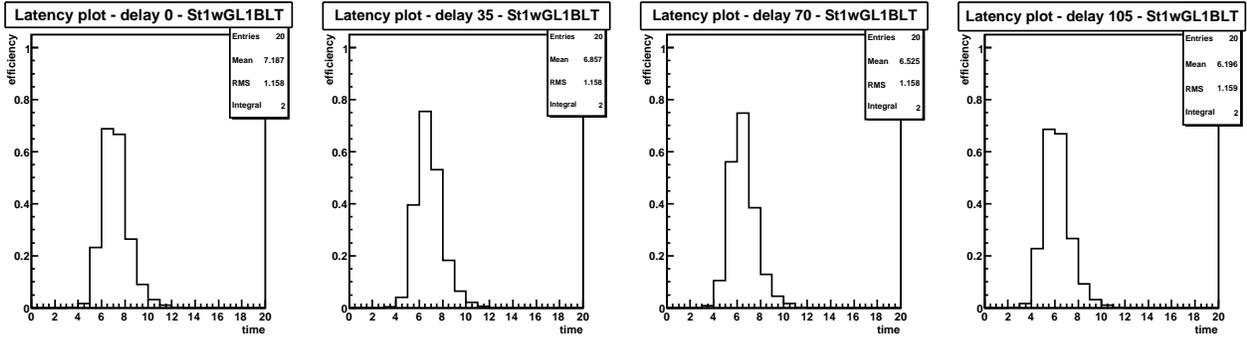


Figure 6.12: Simulation plots when  $G_{trig}$  is the BLT distribution,  $F_{tdc}$  is the "with GL1 distribution" and the "Phase Diff" is 0, 35, 70 and 105 nsec (left to right).

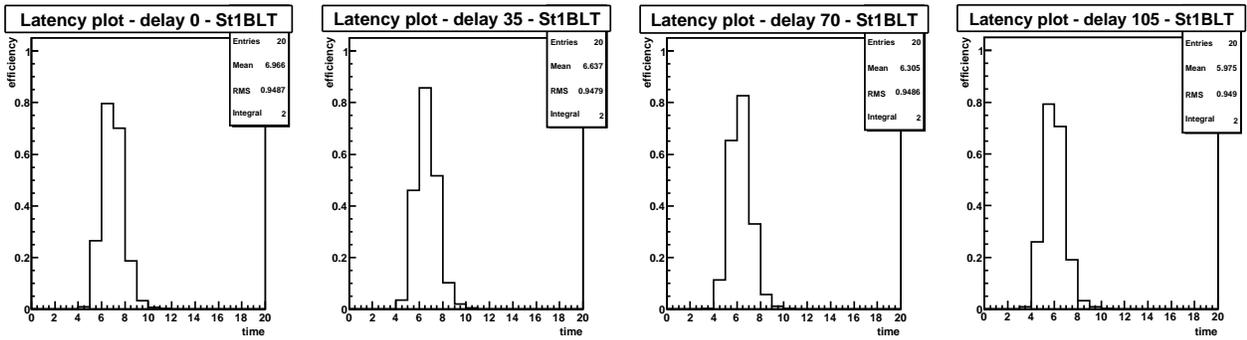


Figure 6.13: Simulation plots when  $G_{trig}$  is the BLT distribution,  $F_{tdc}$  is the "w/o GL1 distribution" and the "Phase Diff" is 0, 35, 70 and 105 nsec (left to right).

With 106 simulation plots, we fit figure 6.9. Figure 6.14 show the result of the fitting. The left is fitted by the series plots of figure 6.12 (with GL1 simulation) and the right is by the series of figure 6.13 (w/o GL1 simulation). Unfortunately, we cannot conclude easily which fit (by with GL1 or w/o GL1) is better. However, considering the results of fitting, it seems that the timing scan plot can be well reconstructed from the data acquired by the Local DAQ. This fact encourages us to use the data of the Local DAQ to evaluate the efficiency value with various gate width. This is calculated in the next subsection.

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<sup>1</sup>In this histogram, LL1 and BLT distribution are not separated. However,  $G_{trig}$  is a separated distribution in actual.

### 6.3.4 Efficiency with various gate width

Since the fitting of section 6.3.3 has been done quite successfully, it can be claimed that the data of the Local DAQ is reasonable. So, it is time to evaluate the efficiency value with the various gate width. This is done by integrating the figure 6.11 with a certain gate width. Figure 6.15 is the result of the calculation. The maximum efficiencies of each plot in figure 6.15 are summarized in table 6.2. As a result, it can be claimed that the efficiency with 3BCLK gate width achieves to 94~98%. Note that this efficiency is against the BCLK width and different from the efficiency described at section 6.2 where it is against the cluster peak strip.

Gate width [Beam Clock]	with GL1	w/o GL1
1	64%	76%
2	84%	94%
3	94%	98%

Table 6.2: The efficiency value with various gate width. The results of integrating both the with GL1 and "w/o GL1 distribution" are represented.

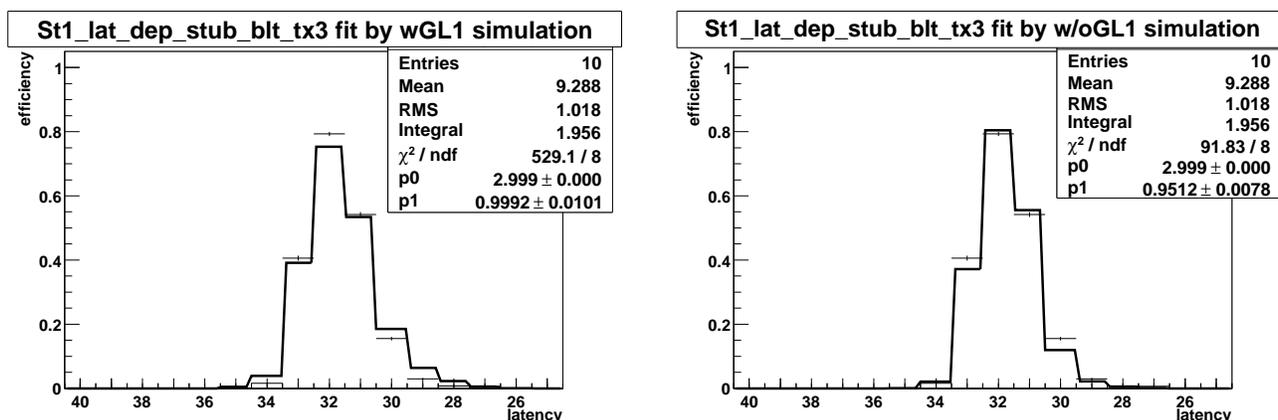


Figure 6.14: left: fitted by the "with GL1 simulation". The value of the "Phase Diff" become 34 nsec. right: fitted by the "w/o GL1 simulation". The value of the "Phase Diff" become 23 nsec.

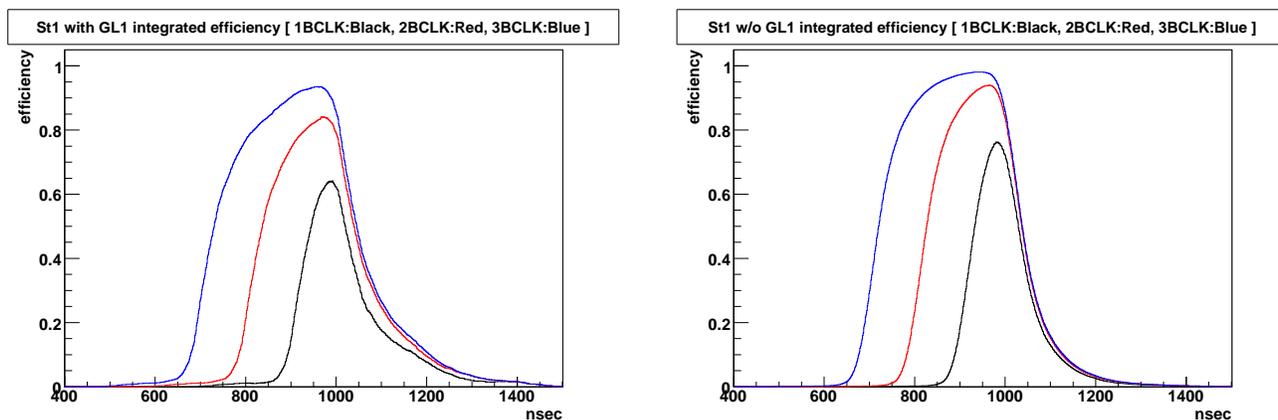


Figure 6.15: left: The distribution of the integration of the "with GL1 distribution" (see section 6.3.2). Black, Red and Blue line indicates the gate width equals to 1BCLK (106 nsec), 2BCLK (212 nsec) and 3BCLK (318 nsec), respectively. right: The distribution of the integration of the "w/o GL1 distribution" (see section 6.3.2). Black, Red and Blue line indicates the gate width equals to 1BCLK (106 nsec), 2BCLK (212 nsec) and 3BCLK (318 nsec), respectively.

# Chapter 7

## Assembly and mechanical integration

### 7.1 Installation plan

The installation locations of the new electronics chassis are strictly constrained by following concerns:

1. Minimum modification to the present working system.
2. Cable length from the MuTr chambers.
3. Aggression into the MuTr acceptance volume.
4. Geometrical interference with existing devices, cables, and frames.
5. Keep the design for all new chassis, no customization depending on installation location.

1) Any modifications to the present working system for the installation could raise the potential risk to deteriorate the present performance of MuTr system. For instance, the substitution of the cables, re-arranging the existing FEE mounting position could easily alter the grounding condition and noise performance of the existing system. The installation of the new electronics needs to be carefully planned to avoid such a risk.

2) The length of the signal cables from the MuTr chambers is approximately 40 cm. Due to the stiffness of the cable, it is also constrained on the magnitude of the angle can be twisted without introducing extra stress on connection parts. Thus the installation position is constrained not only the distance from the chamber connector, but also the orientation of connectors due to such a short and stiff cables.

3) In station-2, due to the short length of the cables from the MuTr, there are bare spaces left to install new electronics outside the acceptance. Therefore there is only one practical

position to install, i.e. on top of the existing FEE chassis cutting into the MuTr acceptance. The chassis of the new electronics is designed to make the volume in the acceptance as small as possible. As for station-1, there are possible spaces outside the acceptance.

4) For the station-1, there are limited space between the station-1 MuTr chambers and the central magnet. The spacing between the lampshade and the central magnet is not uniform for all octants. The details are discussed in the section 7.1.2.

5) The available spaces for installation are not necessarily always identical for all stations, octants and all chassis. For instance, finite space is available between adjacent chassis of present FEEs, while not available for chassis between adjacent octants because of the separation by the support spider frame in station-2. It is not impossible to install new chassis for those channels which have available spaces, but the others need to be treated exceptionally, which requires customized hardware setup including re-designing the circuit to fit into the space or employing different cable lengths, for instance. We avoid such a solution as much as possible.

### 7.1.1 Station 2 and 3 Install

There are no possible installation locations which satisfies all constraints presented at the beginning of this section simultaneously. The most feasible locations for the new electronics to be installed for the station-2 and 3 are on top of the existing FEE chassis as illustrated in Fig. 7.1. This location certainly cuts into the present MuTr acceptance volume though, any other locations requires either significant re-arrangement of the existing FEE locations, or replacing all signal cables from MuTr chambers with longer ones. Since the impact of the acceptance is relatively minor as studied details in the subsection 7.1.3, it seems better solution rather than another option which jeopardize the present performance of existing FEEs.

In the summer test, the MuTRG-TX board was mounted on the spider frame following the MuTRG-AD board chassis to the downstream of the collision point. The station-2 and station-3 MuTr chambers are separated far enough to mount AD and TX boards chassis separately in North Arm. However, this is not the case for the south arm. Once TX board chassis are mounted on the spider frame, they will block the access entry on the side of the lampshade as can be seen Fig. 7.2. Thus it is necessary to combine both AD and TX functions into the same board and accommodate in a single chassis.

There are 192 cathode strips per plane in the north MuTr station-2 chambers. Our plan is to install new electronics to cover two non-stereo planes. The total strip channels to be covered

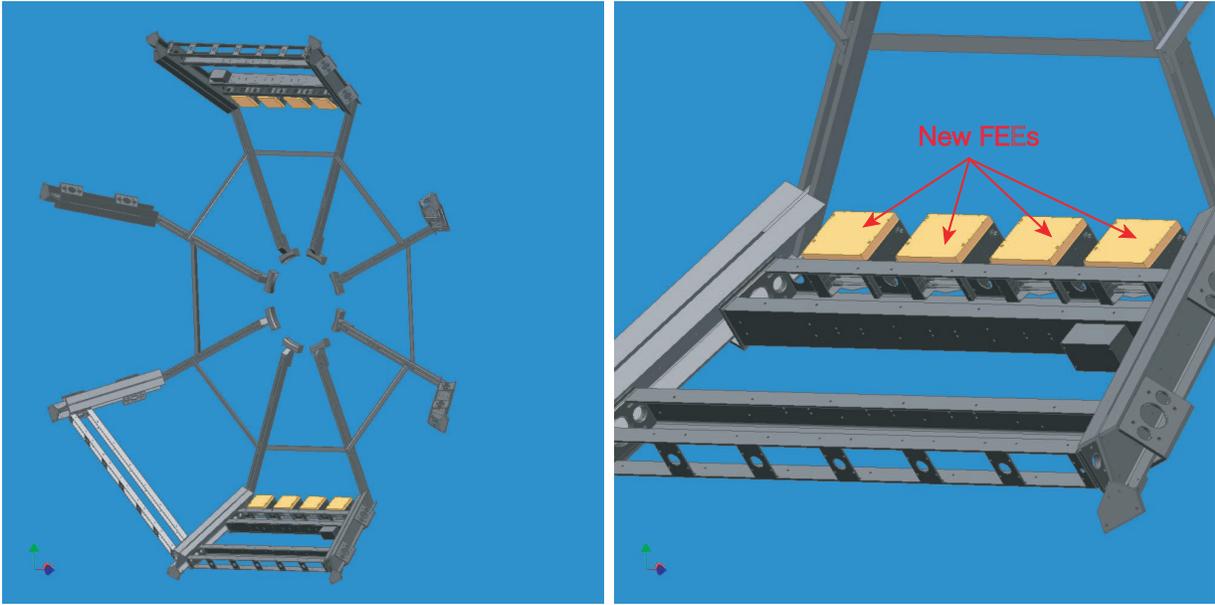


Figure 7.1: CAD drawings of the mounting position of the new chassis on top of the existing FEE chassis in octant 3 and 7 at station-2 (left), The octant 6 is zoomed up in the right panel.

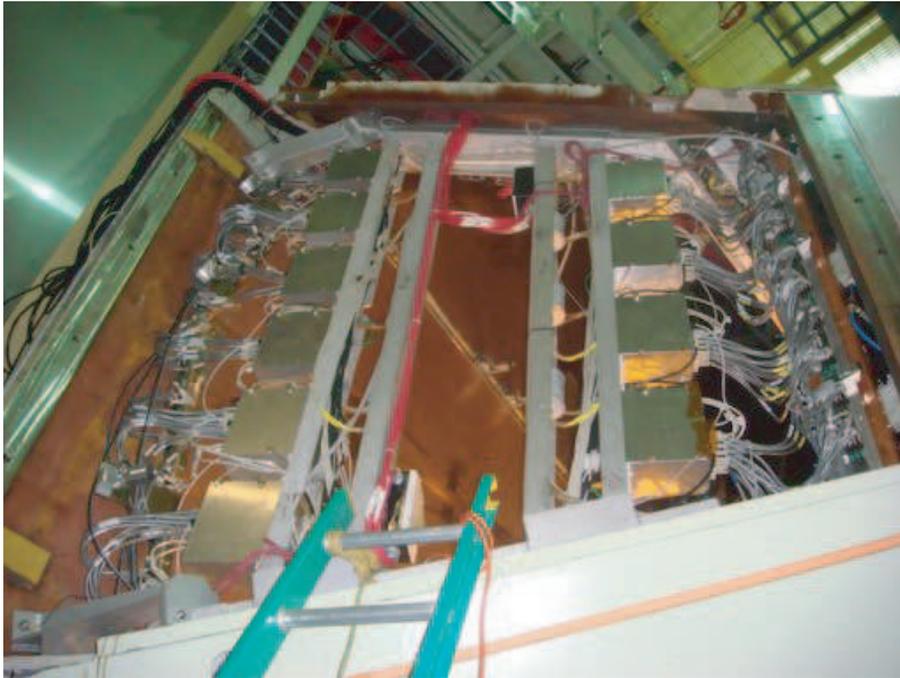


Figure 7.2: A view of station-2 and 3 chassis in South arm. The open space between spider frames are the access entry to the MuTr.

is 384 per octant. This requires minimum of 6 boards per octant (64 channels per board). Because of the constraint of short cables connect between chambers to FEE, we will install additional boards which allow us to avoid extra stress to the cables and connectors by making reckless connections. This is how the existing FEE cabling is done and we inherit the policy. Thus in addition to 6 boards, extra 4 boards (total 10 boards) will be prepared per octant which are enough to make easy connections between MuTr chambers and new electronics. Each chassis are designed to accommodate 2 MuTRG-ADTX boards and thus total of 5 chassis will be installed per octant in the north station-2. The south arm has 160 cathode strips per plane in station-2 chambers. From the same reason, total of 8 boards are prepared (2 extra boards in addition to the minimum requirement). As a consequence, total 4 chassis per octant are installed. The numbers of chassis per octant are exactly consistent with those of existing FEEs in both north and south arm MuTr station-2. The total number of MuTRG-ADTX boards are 80 and chassis are 40 to cover all octants. The number of boards, chassis are summarized in Table 7.1.

Similarly for station-3, extra numbers of boards are installed to avoid tight cable connections and they are tabulated in Table 7.3.

Table 7.1: Number of strips per plane, numbers of MuTRG-ADTX boards and chassis to be installed in station-2. The number in bracket is the minimum number of MuTRG-ADTX boards to cover all strips in two planes.

Arm	plane	2-planes	octant total		station total	
	strip	strips	MuTRG-ADTX boards	chassis	MuTRG-ADTX boards	chassis
South	160	320	8 (6)	4	64 (48)	32
North	192	384	10 (6)	5	80 (48)	40

### 7.1.2 Station 1 Install

Constraints:

In contrast to station-2, there are possible space to mount new chassis outside of the acceptance. As shown in Fig. 7.3, The new chassis are mounted at the upstream tip of the lampshade towards the collision point. The space between the lampshade and the return yoke of the central magnet is confirmed to be at least greater than 2" when the central magnet is

Table 7.2: Number of strips per plane, numbers of MuTRG-ADTX boards and chassis to be installed in station-3. The number in bracket is the minimum number of MuTRG-ADTX boards to cover all strips in two planes.

Arm	plane	2-planes	octant total		station total	
	strip	strips	MuTRG-ADTX boards	chassis	MuTRG-ADTX boards	chassis
South	256	512	12 (8)	6	96 (64)	48
North	320	640	14 (10)	7	112 (80)	56

at the closed position. This is enough for the new chassis whose height is 37 mm to fit in the space. The mock-up test is discussed later in this section.

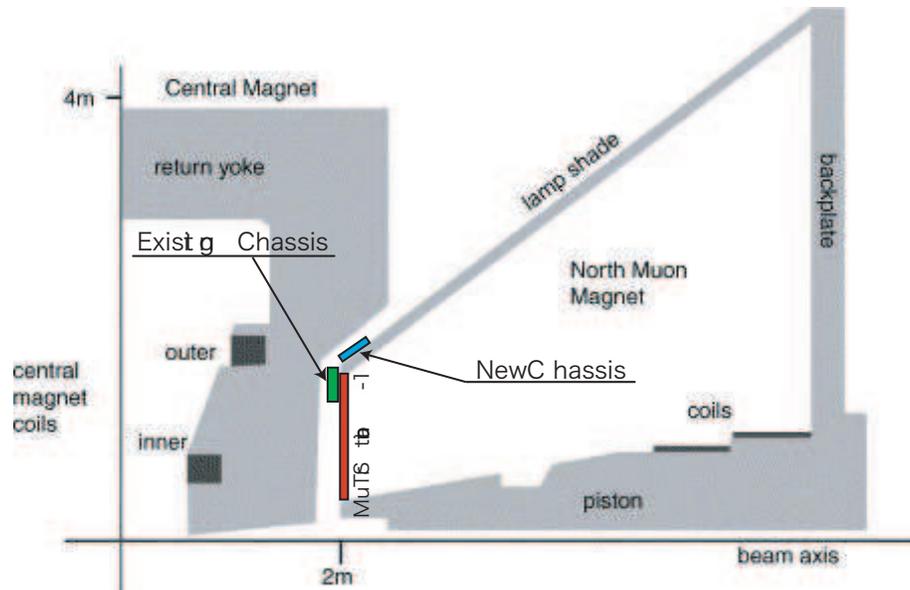


Figure 7.3: A side view of the new chassis install location on the lampshade for station-1.

The choice of this mounting position satisfies most of constraints presented at the beginning of this section, it may require some modifications to existing cabling and cooling water lines as can be seen in Fig. 7.4. However the re-arrangement work will be minor.

The total number of strips per plane in station-1 chambers are the same between the south and the north arms, and it is 96. The number of boards to be installed per octant is 5, 2 extra boards in addition to the minimum requirement 3 boards. The number of chassis is 3 and one of the chassis is shared by the board in adjacent octant and therefore the total number of chassis is 5 per quadrant.

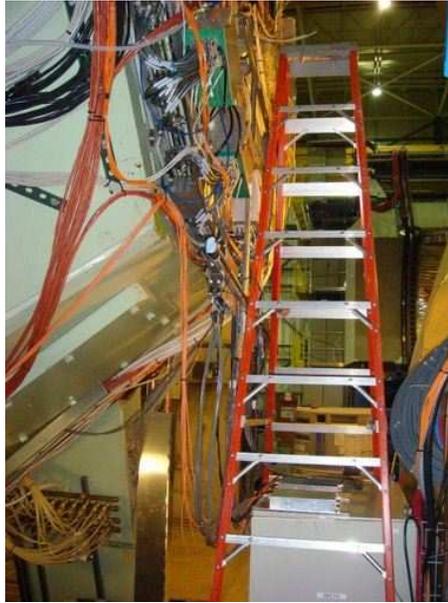


Figure 7.4: The upstream tip of the lampshade of north arm. Some cables and cooling water lines need to be re-arranged to make space for the new chassis on the lampshade.

Table 7.3: Number of strips per plane, numbers of MuTRG-ADTX boards and chassis to be installed in station-1. The number in bracket is the minimum number of MuTRG-ADTX boards to cover all strips in two planes.

Arm	plane	2-planes	octant total		station total	
	strip	strips	MuTRG-ADTX boards	chassis	MuTRG-ADTX boards	chassis
South	96	192	5(3)	2.5	40 (24)	20
North						

The mock up test was done with north muon magnet. The picture of the mounted box is shown in Fig. 7.5. The box is mounted on the unistrut rails. The box size is 6" \* 2" \* 10" is emulate size of AD-TX chasis. After mounting the box, the central magnet was moved to the designated postion for the run. We cofirmed that the box not having any space conflict with the central magnet and its attachments.

Some concern for the existing atachment such cooling water pipe, dry N2 tubing, optpical fibers, copper cables may conflict in some octants. But it can be relocated with some efforts.

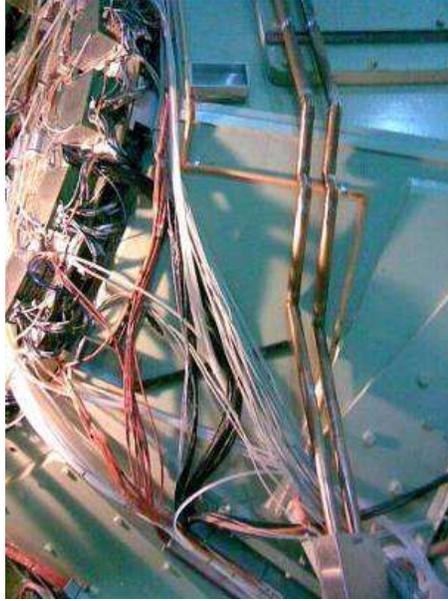


Figure 7.5: The mock up test of AD-TX chassis on the north muon magnet. Mockup box is shown with red circle.

### 7.1.3 Acceptance loss due to AD/TX chassis

For the new chassis for the AD boards are going to be installed on the top of the existing MuTr FEE chassis in station-2 and 3, its influence on the muon detection acceptance needs to be examined. Indeed, the box height of the new chassis is tried to be minimized considering this issue. In this section, estimation results on the influence on mechanical acceptance and also on  $J/\Psi$  detection acceptance is described for new chassis with several centimeters heights.

#### Mechanical Acceptance

PHENIX Muon arm covers rapidity range of  $|\eta| < 1.2 \sim 2.4$ , which corresponds to  $|\theta| = 10.4^\circ \sim 33.5^\circ$  coverage. By adding the new chassis, largest  $\theta$  angle  $\theta_{\max}$  is possible to be modified. Before then, it needs to be described that how original is determined. Most trivial mechanical object limiting the acceptance is the chamber frames.

As drawn in Fig 7.6, station-2 chamber frames have circular shaped outer edges. There are two types of station-2 chambers, front and rear chambers. They are located mutually one-by-one in order to minimize the dead region by superimposing the radial frames. In this location, rear side edge of the front chambers have smallest  $\theta$  coverage. Corresponding  $\theta_{\max}$  is  $34.16^\circ$ . In the followings, geometrical information of the south arm is used.

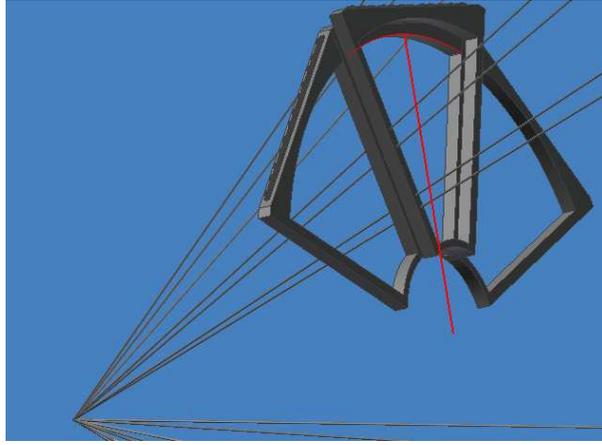


Figure 7.6: The station-2 chamber frames limiting the acceptance of MuTr acceptance volume.

Actually, some existing materials are located inside the prime fiducial region of  $\theta_{\max}$   $34.16^\circ$ , i.e. defined by the chamber frames. As shown in Fig 7.7, existing MuTr FEE chassis are located slightly inside the fiducial region. Indeed, corresponding  $\theta$  angle of the smallest distance between beam axis and the edge line of the FEE chassis is  $34.00^\circ$ , which is smaller than  $34.16^\circ$  determined by the chamber frames. Therefore, if new chassis boxes are added on the existing FEE chassis which is already inside the fiducial region, muon detection acceptance must be influenced.

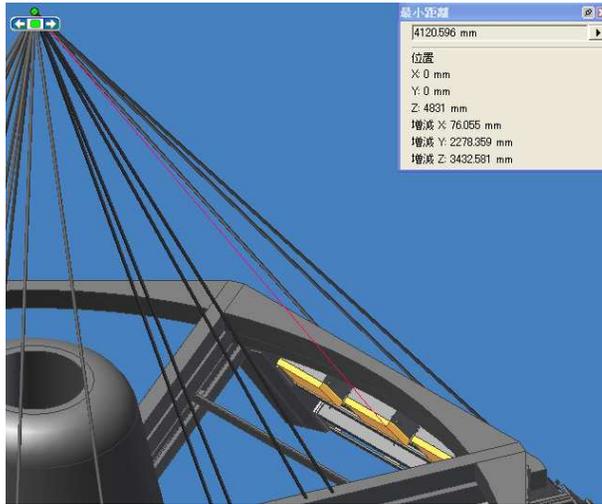


Figure 7.7: The interference with the new FEEs mounted on the existing FEEs and the acceptance in station-2.

Relative acceptance region is illustrated in Fig. 7.8, which shows the  $\theta_{\max}$  positions for

chamber frame, existing FEE chassis and the new acceptance limited by adding the new chassis for  $\theta_{\max} = 33.46^\circ$ , for example. It can be noticed that the acceptance influence is negligible in the existing FEE chassis only, however, the superimposed region cannot be ignored for the case of installing new chassis. It cannot be avoided to reduce the original fiducial region.

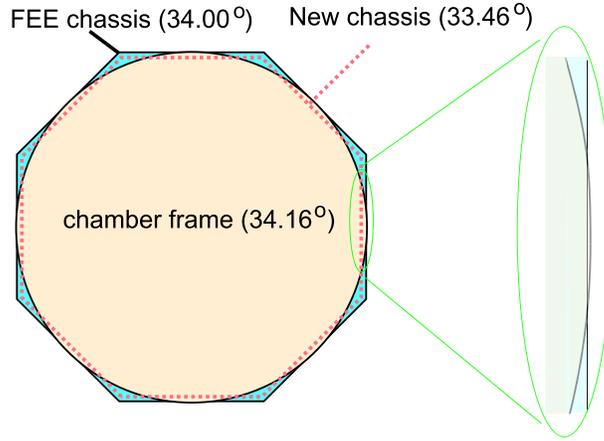


Figure 7.8: The maximum acceptance  $\theta_{\max}$  defined by chamber frames, existing FEE chassis, and new FEE chassis assuming with 40 mm tall.

For different box height of the new chassis,  $\theta_{\max}$  is calculated as shown in Fig. 7.9. For example, estimated value is  $33.46^\circ$  for 40mm height chassis.  $\theta_{\max}$  is also estimated for the vertex position varying. In Fig. 7.9, dotted lines indicate the  $\theta_{\max}$  position limited by the chamber frame. It can be noticed that the acceptance is reduced by adding the new chassis for almost all the cases.

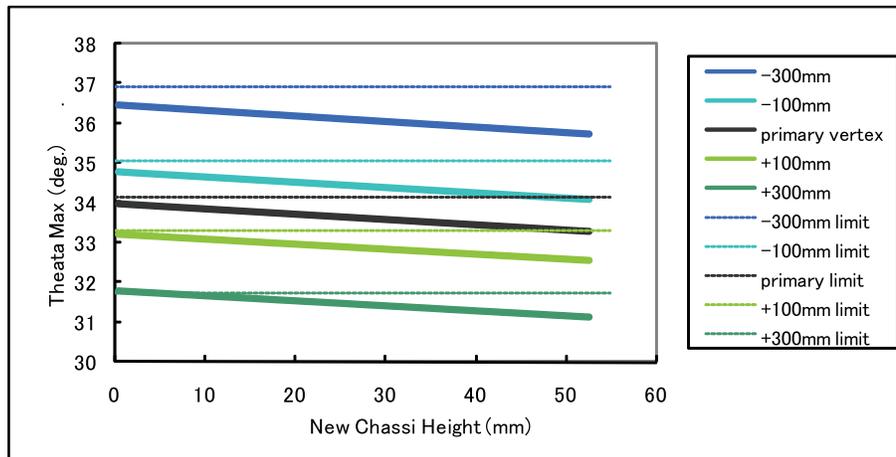


Figure 7.9: The  $\theta_{\max}$  dependence on the height of the new chassis.

## J/ $\Psi$ Yield Acceptance

To see the yield reduction effect by adding the new chassis, a Monte-Carlo simulation is performed. In this study, J/ $\Psi$  particles are produced by using PYTHIA6.4 for the case of  $\sqrt{s} = 500$  GeV p+p collisions. 85000 events are analyzed. In Fig. 7.14, dimuon emission angler correlation is plotted.  $d^2N/d\theta_{\mu^+}d\theta_{\mu^-}$  is plotted as functions of  $\theta_{\mu^+}$  and  $\theta_{\mu^-}$ . Here, polar angle  $\theta$  originated from the beam axis is plotted for  $\mu^+$  and  $\mu^-$ . Black boxes indicate original acceptances of south and north muon arm. As described before, north-south symmetry is supposed in this first order estimation. In addition, although the new fiducial region limited by the FEE and new chassis has a octagonal shape (see Fig. 7.8, axial symmetry is supposed. In the following studies, muons detected inside the  $\phi$ -symmetric acceptance defined as  $\theta_{\min} < \theta < \theta_{\max}$  are counted and the total yield is estimated as a function of  $\theta_{\max}$ . The corresponding  $\theta_{\max}$  is defined as smallest  $\theta$  angle of the edge of the chassis, i.e., polar angle defined with the middle side of the octagon. For the real acceptance is defined with superimpose of the octagonal-shaped chassis spider-frame and the chamber frame, and the estimation should always overestimates the acceptance loss. The effect of axial symmetry assumption is almost negligible at around  $\theta \sim 32$  degrees, however, in contrast, the ratio between real acceptance loss and the current results based on the axial symmetry become over ten at around  $\theta \sim 34^\circ$ . It means that the current estimation is very conservative. However, as described below, the absolute value of the acceptance loss at  $\theta$  around  $34^\circ$  are very small, therefore, the axial symmetry assumption is good enough for the current purpose.

Number of dimuon events are counted if both  $\mu^+$  and  $\mu^-$  are hit inside the acceptance box shown in the Fig. 7.14.

$$Yield_{\text{accept}}(\theta_{\max}) = \int_{\theta_{\min}}^{\theta_{\max}} \int_{\theta_{\min}}^{\theta_{\max}} d\theta_{\mu^+} d\theta_{\mu^-} \frac{d^2N}{d\theta_{\mu^+} d\theta_{\mu^-}} \quad (7.1)$$

The red box lines indicate the modified acceptance by adding the new chassis, which corresponds to the value  $\theta_{\max}$  in Eq. 7.1. In this estimation,  $\theta_{\min}$  value of  $10.37^\circ$ , which obtained from  $\eta = 2.4$ , is used. The obtained yield is compared with the value with original  $\theta_{\max}$  value of  $34.00^\circ$ . In Fig. 7.11, relative yield defined as

$$\frac{Yield_{\text{accept}}(\theta_{\max})}{Yield_{\text{accept}}(\theta_{\max} = 34.00^\circ)} \quad (7.2)$$

is plotted as a function modified  $\theta_{\max}$  values. The blue line indicate the Monte-Carlo events and the red line denotes a simple geometrical acceptance

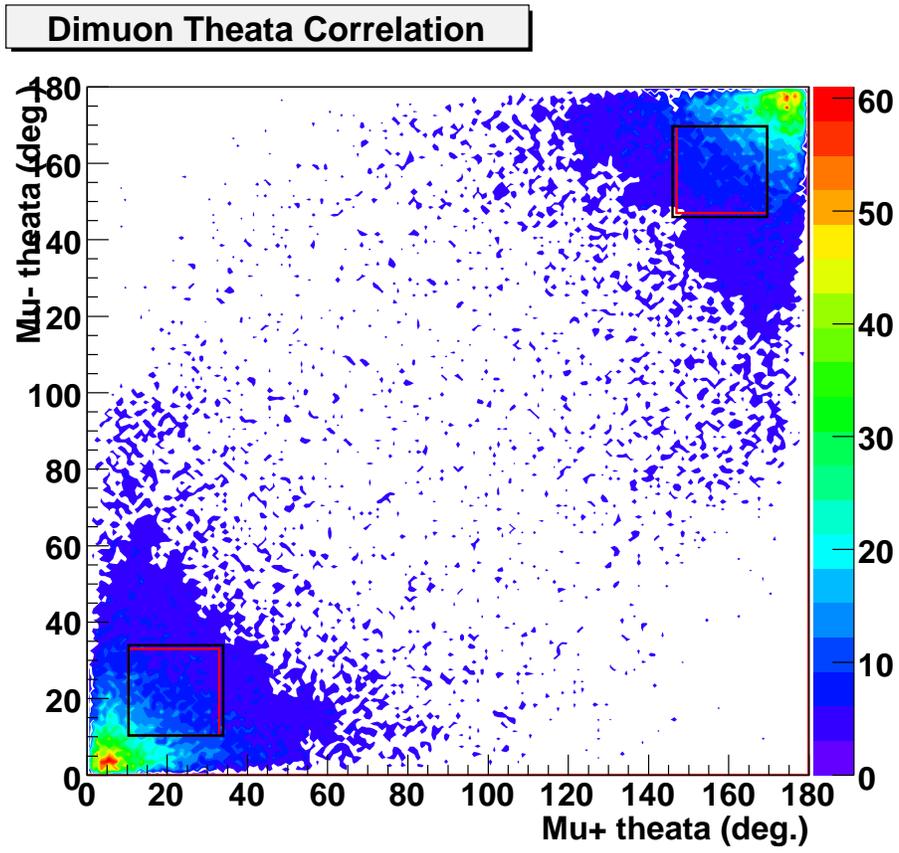


Figure 7.10: The angular correlation of dimuons through the decay  $J/\Psi \rightarrow \mu^+\mu^-$ .

$$Acc = \int_0^{2\pi} d\phi \int_{\theta_{\min}}^{\theta_{\max}} \sin \theta d\theta \quad (7.3)$$

$$= 2\pi(-\cos \theta_{\max} + \cos \theta_{\min}) \quad (7.4)$$

as a reference, which is also normalized at the value of 34.00°.

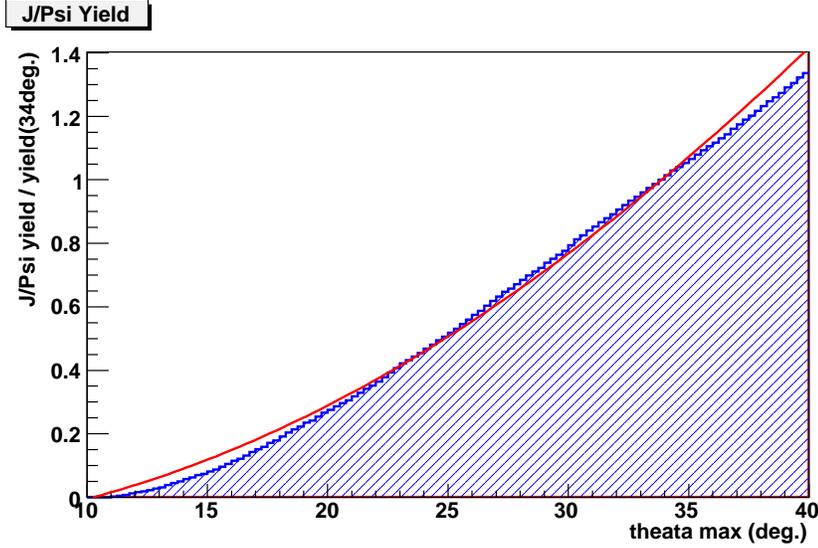


Figure 7.11: J/Ψ yield predicted by Monte Carlo normalized at the yield at  $\theta_{\max} = 34.00^\circ$  is plotted as a function of the modified  $\theta_{\max}$  values. The red line shows a simple geometrical acceptance defined by the Eq. 7.4.

From Fig. 7.11, we can estimate the acceptance varying. Fig. 7.12 is same but enlarging the results around  $\theta_{\max} = 34^\circ$ . For the function shape of the J/Ψ yield line can be assumed as a linear function of  $\theta_{\max}$  around  $34^\circ$ , results of a linear fitting can be used for the J/Ψ yield estimation.

The result of the linear fitting is

$$\frac{Yield_{J/\Psi}(\theta_{\max})}{Yield_{J/\Psi}(\theta_{\max} = 34.00^\circ)} = -0.80 + 0.053 \times \theta_{\max}/\text{deg.}, \quad (7.5)$$

so now we can estimate yield modification at any  $\theta_{\max}$  around  $34^\circ$  using Eq. 7.5. Yield ratio Eq. 7.2 for several new box height are then obtained using Eq. 7.5. The results are listed in Table 7.4.

For example, we can see that the yield ratio is 97% for 40mm height new chassis. It should be noticed that the obtained results listed here is assuming axial symmetry, therefore, realistic value would be even better than the obtained results.

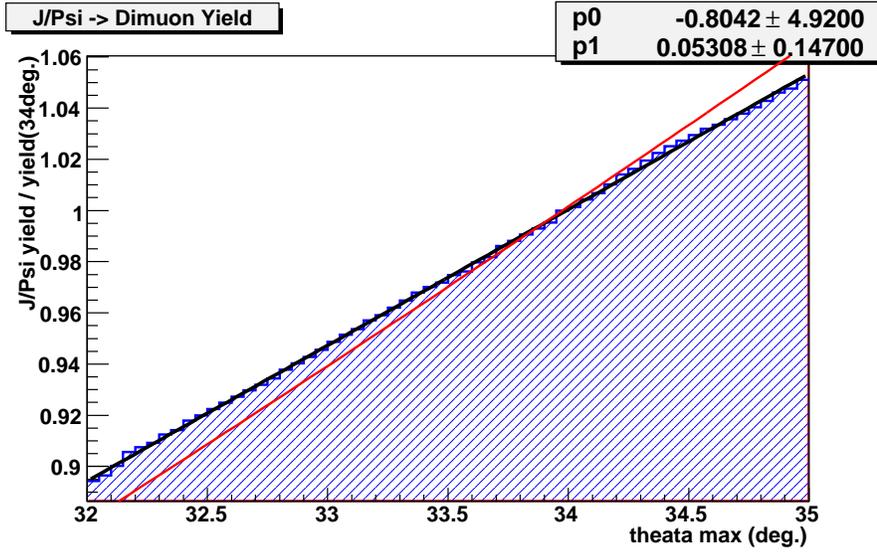


Figure 7.12: ibid of Fig. 7.11, but the scale is zoomed in around  $\theta_{\max} \approx 34$ .

Table 7.4: J/ $\Psi$  events yield ratio with respect to the yield at  $\theta_{\max} = 34.00^\circ$  for various height of the new chassis.

New Chassis Height [mm]	$\theta_{\max}$	Yield Ratio
0	34.00°	1.000
10	33.87°	0.993
20	33.72°	0.985
30	33.59°	0.978
40	33.46°	0.971
50	33.32°	0.964

### Single Muon Acceptance

In addition to the dimuon events, single muon yield evaluation for J/ $\Psi$  events are also examined here.

$$Yield_{\text{accept}}^{\mu^+}(\theta_{\max}) = \int_{\theta_{\min}}^{\theta_{\max}} d\theta_{\mu^+} \frac{dN}{d\theta_{\mu^+}} \quad (7.6)$$

is counted and plotted in Fig. 7.13. The linear fitting result is

$$\frac{Yield_{\mu^+}(\theta_{\max})}{Yield_{\mu^+}(\theta_{\max} = 34.00^\circ)} = -0.10 + 0.032 \times \theta_{\max}/\text{deg.} \quad (7.7)$$

Similar results of relative yield are listed for single muon acceptance in Table 7.5. In this

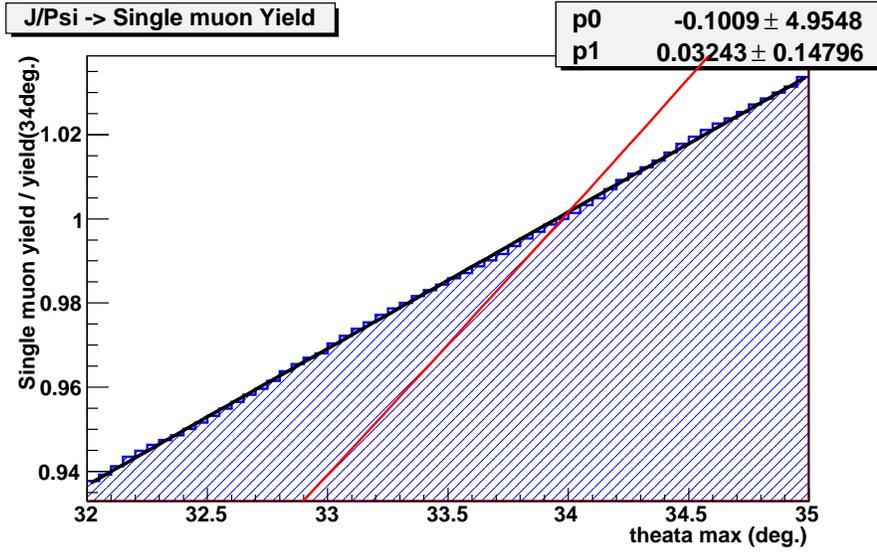


Figure 7.13: Single muon from  $J/\Psi$  yield predicted by Monte Carlo normalized at the yield  $\theta_{\max} = 34.00^\circ$  is plotted as a function of the modified  $\theta_{\max}$  values. The red line shows a simple geometrical acceptance defined by the Eq. 7.4.

case, for example, at least 98% acceptance can be expected to be kept for the new chassis with 40mm tall.

Table 7.5: Single muon from  $J/\Psi$  events yield ratio with respect to the yield at  $\theta_{\max} = 34.00^\circ$  for various height of the new chassis.

New Chassis Height [mm]	$\theta_{\max}$	Yield Ratio
0	$34.00^\circ$	1.000
10	$33.87^\circ$	0.996
20	$33.72^\circ$	0.991
30	$33.59^\circ$	0.987
40	$33.46^\circ$	0.983
50	$33.32^\circ$	0.978

### Prime Vertex Position Dependence

Prime vertex position is varying event-by-event. The corresponding  $\theta_{\max}$  is distributed from about  $32^\circ$  to  $37^\circ$ . As shown in Fig. 7.12 and Fig. 7.13, the yield ratio can be regarded as linear function of  $\theta_{\max}$ , therefore, same fitting results of Eq. 7.5 can be used. Obtained evaluation results for dimuon acceptance is summarized in Tables 7.6, 7.7 7.8.

Table 7.6: J/ $\Psi$  events yield ratio with respect to the yield at  $\theta_{\max} = 34.00^\circ$  for the primary vertex of  $\pm 0$  mm as tabulated in Table 7.4.

New Chassis Height [mm]	$\theta_{\max}$	Yield Ratio	Relative Ratio
0	31.80°	1.000	1.000
10	31.67°	0.993	0.993
20	31.55°	0.985	0.985
30	31.42°	0.978	0.978
40	31.30°	0.971	0.971
50	31.18°	0.964	0.964

Table 7.7: J/ $\Psi$  events yield ratio with respect to the yield at  $\theta_{\max} = 34.00^\circ$  as tabulated in Table 7.4, but the primary vertex is set +300mm.

New Chassis Height [mm]	$\theta_{\max}$	Yield Ratio	Relative Ratio
0	31.08°	0.879	1.000
10	31.67°	0.873	0.992
20	31.55°	0.866	0.985
30	31.42°	0.859	0.977
40	31.30°	0.853	0.970
50	31.18°	0.847	0.963

Tables 7.6, 7.7 7.8 are the results for various vertex positions. In these tables, yield ratio is defined as

$$yield\ ratio = \frac{Yield_{J/\Psi}(box, vertex)}{Yield_{J/\Psi}(box = 0mm, vertex = 0mm)} \quad (7.8)$$

i.e. normalized using (box=0mm,vertex = 0mm: $\theta_{\max} = 34.00^\circ$ ) yield. And the relative ratio is defined as

$$relative\ ratio = \frac{Yield_{J/\Psi}(box, vertex)}{Yield_{J/\Psi}(box = 0mm, vertex)} \quad (7.9)$$

i.e. normalized using (box=0mm,vertex = same position) yield. For example, effects of adding 40mm height new box on J/ $\Psi$  yield is obtained as vertex = 0mm : 97.1% vertex = +300mm : 97.0% vertex = -300mm : 97.3%, which are almost independent on the vertex position. In summary, we can expect to keep at least 97% acceptance for J/ $\Psi$  events by adding 40mm height new chassis boxes.

Table 7.8:  $J/\Psi$  events yield ratio with respect to the yield at  $\theta_{\max} = 34.00^\circ$  as tabulated in Table 7.4, but the primary vertex is set -300mm.

New Chassis Height [mm]	$\theta_{\max}$	Yield Ratio	Relative Ratio
0	36.49°	1.128	1.000
10	36.34°	1.120	0.993
20	36.20°	1.113	0.986
30	36.05°	1.105	0.979
40	35.91°	1.097	0.973
50	35.77°	1.090	0.966

### 7.1.4 Chassis mounting procedure

The new electronics chassis is mounted on the existing chassis in station-2, and it is supported by the aluminum support structure on the side as illustrated in Fig. 7.14. The bottom of the support structure bends underneath the existing FEE chassis to hold tightly the new chassis preventing it falling down from the existing chassis. Especially for the ones installed on the top octants whose new chassis are mounted upside down on the existing chassis. The designed support structure is thus robust. In order to prevent the displacement to the longitudinal direction, the velcro tape between the bottom face of new and the top face of the existing chassis provide additional force to hold two chassis together.



Figure 7.14: New chassis in the mounting position on top of the existing FEE chassis held by the aluminum support structure on both sides.

## 7.2 Infrastructure

### 7.2.1 LV

#### Power Consumption

As summarized in Table 7.9, the total numbers of chassis in station-2 are 40 for the north and 32 for south arms, respectively, whereas 20 in station-1 for both arms. The combined total of station-1 and station-2 are 60 chassis for north and 52 for south arms, respectively. The low voltage input to the chassis is designed to be one and it is split into two MuTRG-ADTX boards inside the chassis. The power consumption per each MuTRG-ADTX board is estimated to be about 11.4W (22.8W per chassis if there are two MuTRG-ADTX boards installed). As summarized in Table 7.10, the total power consumptions are 1.368kW and 1.186kW in the north and south arm, respectively for the scenario of installing MuTRG-ADTX in station-1 and 2. The total power consumptions for the scenario of installation to station-3 as well are summarized in Table 7.11.

Table 7.9: The total number of MuTRG-ADTX boards and chassis per station and the arm total.

South	Station-1	Station-2	Station-3	Sta-1&Sta-2 Total	Arm Total
MuTRG-ADTX	40	64	96	104	200
Chassis	20	32	48	52	100

North	Station-1	Station-2	Station-3	Sta-1&Sta-2 Total	Arm Total
MuTRG-ADTX	40	80	112	120	232
Chassis	20	40	56	60	116

Table 7.10: The summary of the power consumption per octant, per station and per arm total for the south and north arms for station-1 and 2. Total number of boards per octant and station are found in Sections 7.1.1 and 7.1.2. The last column is the total number of the LV channels which is equivalent to the total number of chassis.

Arm	Station-1		Station-2		Arm TOTAL	
	octant	station	octant	station	power	LV Channels
South	57W	456W	91.2W	729.6W	1.186 kW	52
North	57W	456W	114W	912W	1.368 kW	60

Table 7.11: The summary of the power consumption per octant, per station-3 per arm total for the south and north arms assuming station-1, 2 and 3 installation.

Arm	Station-3		Arm TOTAL	
	per octant	per station	power	LV Channels
South	136.8W	1.094kW	2.280 kW	100
North	156.8W	1.277kW	2.645 kW	116

As a system for the low voltage power supply, the LVHP variant "M" power supply modules can be used in a PHENIX standard LVPS crate. Each LVHP variant "M" power supply module provides 2 outputs with 300W at 7.5V and each output is connected to a distributor which distributes the power into 10 channels with 30W each. 30W is high enough to provide power to the chassis with MuTRG-ADTX boards installed which consumes total of  $11.4W \times 2 = 22.8W$ . Thus minimum numbers of the power supply module are 3 in both north and south arms in order to cover 60 and 52 total number of channels (station-1 & station-2), respectively. The 3 power supply modules provide net power of 1.8kW ( $300W$  per output  $\times$  2 outputs  $\times$  3 modules) which is well above the total power consumptions of 1.368kW and 1.186kW in north and south arms. Since the maximum capacity of LVPS crates goes up to 8 power supply modules per crate, 3 modules easily fit in a single crate as illustrated in Fig. 7.15. The total number of distributors are 6 per arm and these also fit in the Los Alamos custom made distributor crate which accommodates up to 20 distribution modules. Unfortunately, there are no empty slots available in the existing crates to accommodate new modules in neither power supply and distributor cases regardless they occupy only partial fraction of the crates of the maximum capacity. Thus new crates are necessary in both north and south arms.

In case of full installation into station-3 as well, the total power consumptions are 2.280 kW and 2.645 kW in South and North arms total, respectively. They require LV channels of 100 and 116, respectively. Since each LVHP variant "M" power supply module provides 20 channels, the total number of the power supply module is 5 and 6 for south and north arms, respectively. Correspondingly, the number of distributors are required 10 and 12, respectively. These numbers are summarized in Table 7.12.

The present LVPS is designed to require a water cooled heat exchanger and a fan tray. As a consequence, the required rack size will be

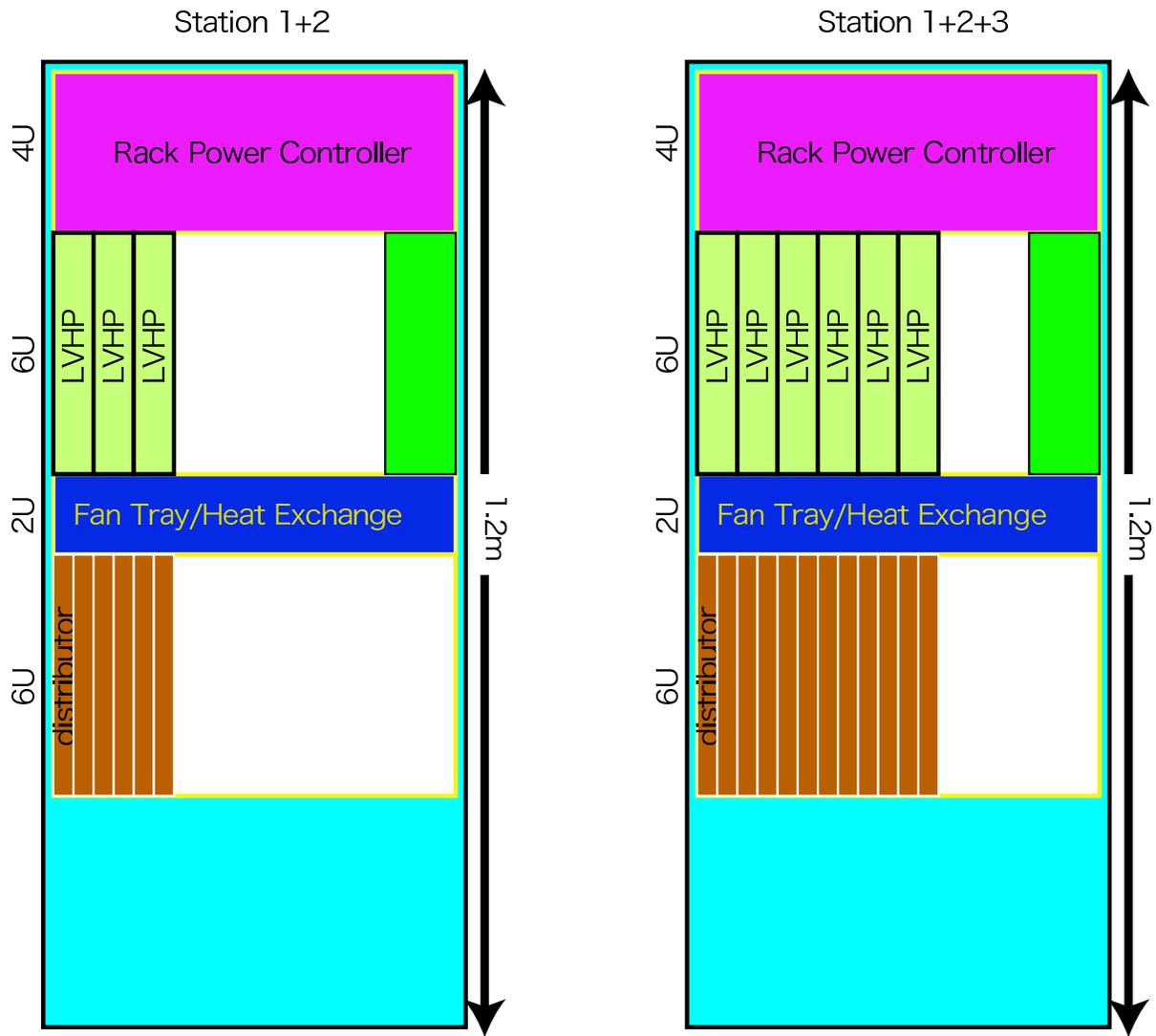


Figure 7.15: The image of the LV rack components for new electronics. The left panel shows the case of the installation to station-1 and 2, whereas the right panel shows that of station-1, 2 and 3.

Table 7.12: The number of LV power supply (LVHP variant "M") and distributor modules per arm in case of station 1+2 (top) and station 1+2+3 installs. The last two columns are number of actual use and the spare channels (total - use = spare).

Station 1+2	LVHP power supply	distributor	total channel	actual use	spare
South	3	6	60	52	8
North	3	6	60	60	0

Station 1+2+3	LVHP power supply	distributor	total channel	actual use	spare
South	5	10	100	100	0
North	6	12	120	116	4

$$\begin{array}{ccccccc}
 \text{LVPS} & & \text{fan tray/} & & \text{distributor} & & \text{rack power} \\
 \text{crate} & & \text{heat exchange} & & \text{crate} & & \text{controller} \\
 6\text{U} & + & 2\text{U} & + & 6\text{U} & + & 4\text{U} \\
 & & & & & & = 18\text{U (800mm)} \\
 & & & & & & \text{Total}
 \end{array}$$

The standard size of rack to accommodate this size will be 1200mm tall model as illustrated in Fig. 7.15. Since the number of modules are not too many and creating heat is relatively minor, we also seek for other LV supply system which do not require a water cooling system. This way, the power supply system becomes much simple, i.e. one set of a LVPS crate and a distributor crate per arm.

### 7.2.2 Rack locations

The location of racks depend on the size of the racks. It is under a search for the possible locations if the racks to be 1200mm tall. Possibilities are on the top of MuID which may require new platform to work on or in the RHIC tunnels. Descriptions in following are for the cases do not require the water cooling system, i.e. consisted of just a LVPS and distributor crates per arm. This case can be managed without making major work to the present infrastructure.

NORTH ARM: The location of racks to be installed is at the platform above the upper lampshade of the north magnet. Shown in Fig. 7.16 is the view of the platform above the upper lampshade of the north magnet looking from east side (left) and the the platform above the west upper bias lampshade. A new rack contains a LVPS crate and a distributor crate will be installed around the existing crates, which are used for the Glink modules for the north MuTr.

SOUTH ARM: There are limited space available in the platforms which move together with the south magnet. Shown in Fig. 7.17 is a view of the eyebrow platform on the south MuTr magnet upper lampshade. There are existing 3 tall racks which accommodates electronics for



Figure 7.16: The platform above the upper lampshade of the north magnet looking from east side (left) and the the platform above the west upper bias lampshade. The existing crates are used for Glink modules for the north MuTr.

the south MuTr and 3 exposed small racks for the MPC south are installed above the racks. Since new addition of two small crates are relatively minor addition, we seek for the possibility to install them in this area by re-arranging existing racks. If it turns out not feasible, then new racks will be installed on other platforms which requires disconnecting/connecting cables every time the south magnet moves.

### 7.2.3 Cooling water

The PHENIX water cooling system is now under major upgrades to have independent lines for the magnets and electronics separately. Once the upgrade is completed, the cooling system for the electronics will provide a capacity of extra 30% cooling power in addition to the required cooling power for the present electronics.

The temperature rise of the cooling water with 1 gallon/minute is known to be about  $6^{\circ}\text{F}/\text{kW}$ . For the case of station 1+2 install, even if the total power consumption of 1.186kW (south) and 1.368kW (north) are fully loaded to the cooling water, the total rises of the temperature are relatively minor, i.e.  $7.1^{\circ}\text{F}$  and  $8.2^{\circ}\text{F}$ . For the full installation including station-3, the total power consumptions are 2.280 kW (south) and 2.645 kW (north), corresponding temperature rises are  $13.7^{\circ}\text{F}$  and  $15.9^{\circ}\text{F}$ . In reality the heat will be also taken by the fan into the air, so



Figure 7.17: The eyebrow platform above the upper lampshade of the south MuTr magnet, a view from north.

the actual rise in the water temperature should be lower. Additional flow of 2 gallons/minute (1 for north and 1 for south) is minor addition to the present flow 320 gallons/minute and well below the maximum capacity of 390 gallons/minute. Thus the amount of additional cooling water flow for the new electronics does not require any major upgrade to the present system.

Since the temperature rise is such a minor, the cooling water line are connected in series for the chassis mounted in a same octant for station-2 and a same quadrant for station-1. In each cases, 5 chassis are connected in series. Plumbing works need to be done to distribute the water cooling pipes to each octant/stations. The existing cooling water line needs to be fan-ed out by 8 and the manifolds can be installed either inside or outside of the magnet.

#### **7.2.4 Dry air**

There is no major modification to the dry air system implemented for the summer test. No major upgrade to the capacity of the existing PHENIX dry air system is necessary.

### **7.3 Post-installation procedure**

After mehcanical installtion, there are two major checking points, cooling water flow, and electorical functionarity. Water flow has to be confirmed before suplying the power to MuTRG-ADTX board to prevent fly or decrease board life time. Water flow or pressure for each indiviual series of water circuit will be checked. Also water leak from each connection and along flow line should be checked. The electrical functinarity check should be done by folloing procedure.

1. Before connecting power cable to the board, terminal volatge and polarity will be checked.
2. After connectiong power cable, connect all optical cable.
3. Down load FPGA programing and threshould vale through the MuTRG-MRG board.
4. Noise scan, if the electronics has noisy channel, it could be replace whole board or masked nosiy channel for later operation.
5. Take cosmic ray event data and check chamber connection.

# Chapter 8

## Interface to LL1 and DCM

Interface to the MuTr local level 1 trigger board (LL1 board) and data collection module (DCM) is necessary to transfer the collected trigger data to LL1 and DCM in an appropriate data format and speed. The data merger board (MuTRG-MRG) and the DCM interface board (DCMI board) provides such interface in the MuTr trigger system. The MuTRG-MRG and DCMI board have interface to VME bus and optical I/O. A schematic diagram of data flow and control signal flow are shown in Fig. 8.1 and Fig. 8.2, respectively.

The MuTRG-MRG collects digitized data transmitted from MuTRG-TXs, and send strip hit information to the LL1 board and the DCMI board. Figure 8.3 illustrates the diagram of data flow in the MuTRG-MRG. The MuTRG-TX serializes strip hits with the 8b/10b encoding, and transmits them at 1.2 Gbps through optical cables. The MuTRG-MRG receives the data from 4–10 MuTRG-TXs and deserializes them by a deserializer (TI TLK1501) with a 60 MHz clock. One MuTRG-MRG covers data from one octant in station 1, 2 and a half octant in station 3. The data is then aligned and ordered in terms of strip number in the FPGA. The FPGA stores the strip hit information for two MuTr planes. The logical OR (or optionally AND) of the two planes is taken. The OR-ed signals are serialized by a serializer (TI TLK3101) with the 8b/10b encoding, and are sent to the LL1 board and the DCMI board. The data speed to the LL1 board is between 1.6 and 2.8 Gbps. One LL1 board per octant will be used to form a LL1 trigger for each octant. The LL1 board has four fiber inputs for the MuTr data. Original plan was to use two fibers for station 1 and 2, another two fibers for station 3, resulting in the maximum transfer speed at 2.8 Gbps for station 2 and minimum one at 1.6 Gbps for station 1. However, data rate may be equalized by rearranging the strip among different stations. The data format to the LL1 would be one word for carrier extend, one word for beam clock counter and module id, 6–12 words for data. A 140 MHz crystal clock will be

used to drive the serializer.

The same strip hit data is sent to the DCMI board upon a request by the global level 1 (GL1) trigger. The MuTRG-MRG accumulates the data in a buffer for 50 beam-clock tics ( $5.3\mu\text{sec}$ ). The GL1 trigger initiates the transfer of the data for the triggered beam crossing and its peripheral ones. Four DCMI boards will be used. Each DCMI board collect data from a half of MuTRG-MRGs for each arm. The maximum data size is 300 word/beamcrossing/arm. Data size may become smaller after a zero suppression if the MuTr occupancy is less than 3%. The DCMI sends data to the DCM at speed of 80 MHz/word through an optical fiber. Plan is to use one DCM per arm.

The beam clock, trigger and other control signals to the system, such as reset, initialization..., are provided from the GTM by the G-Link protocol. Other slow control signals (FPGA designs, mode selections, parameter settings, test...) are provided from an on-board computer which is installed in a VME crate. The DCMI board receives the GTM signal by HDMP-1024, and distributes control signals to MuTRG-MRGs through the serial LVDS link. The slow control signals from the on-board computer are distributed through the VME bus. The MuTRG-MRG send control signals to MuTRG-TXs by the optical link.

By considering number of I/O, the standard 6U size turns out to be too small. The size of the boards is 9U with a half depth. Four 9U VME crates are used to mount all boards, i.e. two crates for north arm, two crates for south arm. Each crate contains a set of MuTRG-MRGs for four MuTr octants and a DCMI board and an on-board computer. The base concept of the board design is to drive all components in synchronous to the beam clock as much as we can for simple and robust operation of the system.

The design of the MuTRG-MRG and DCMI board is in progress as of November, 2007. The board design has been discussed with the PHENIX experts who are developing the electronics for RPC FEE and DCM (C.Y. Chi (Columbia)), LL1 board (J. Lajoie (Iowa State)). We had opportunities to get advices from the local experts, O. Sasaki(KEK), M. Ikeno (KEK), who developed similar boards for the ATLAS and other experiments. As of now, the main functions and operation modes of the MuTRG-MRG and DCMI board have been identified. A series of tests will be performed to verify the key technologies, such as high speed link, timing alignment, data buffering, remote slow control etc... Schedule of prototyping, R&D and production is discussed in section xxx.

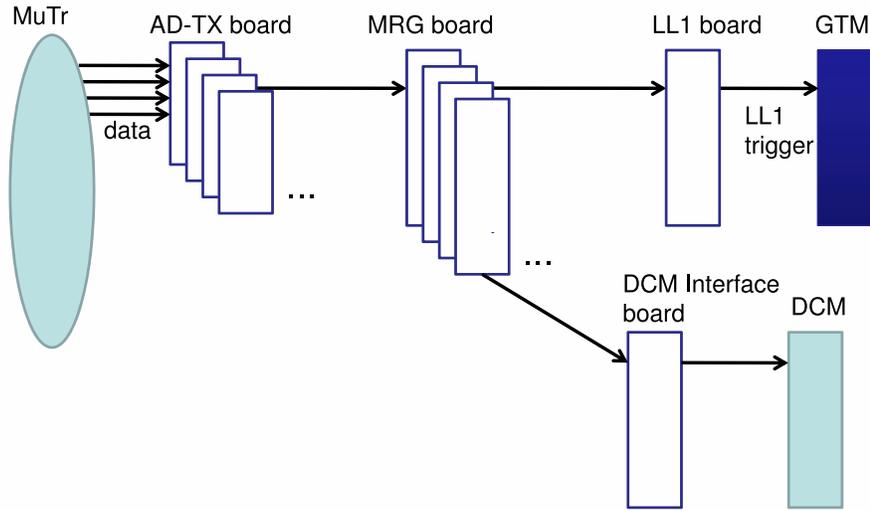


Figure 8.1: Schematic diagram of data flow.

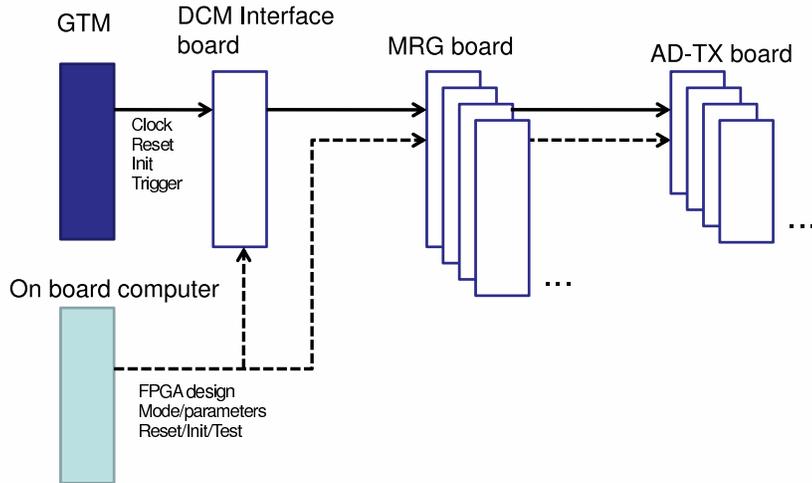


Figure 8.2: Schematic diagram of control signal flow (beam clock, trigger and slow control)

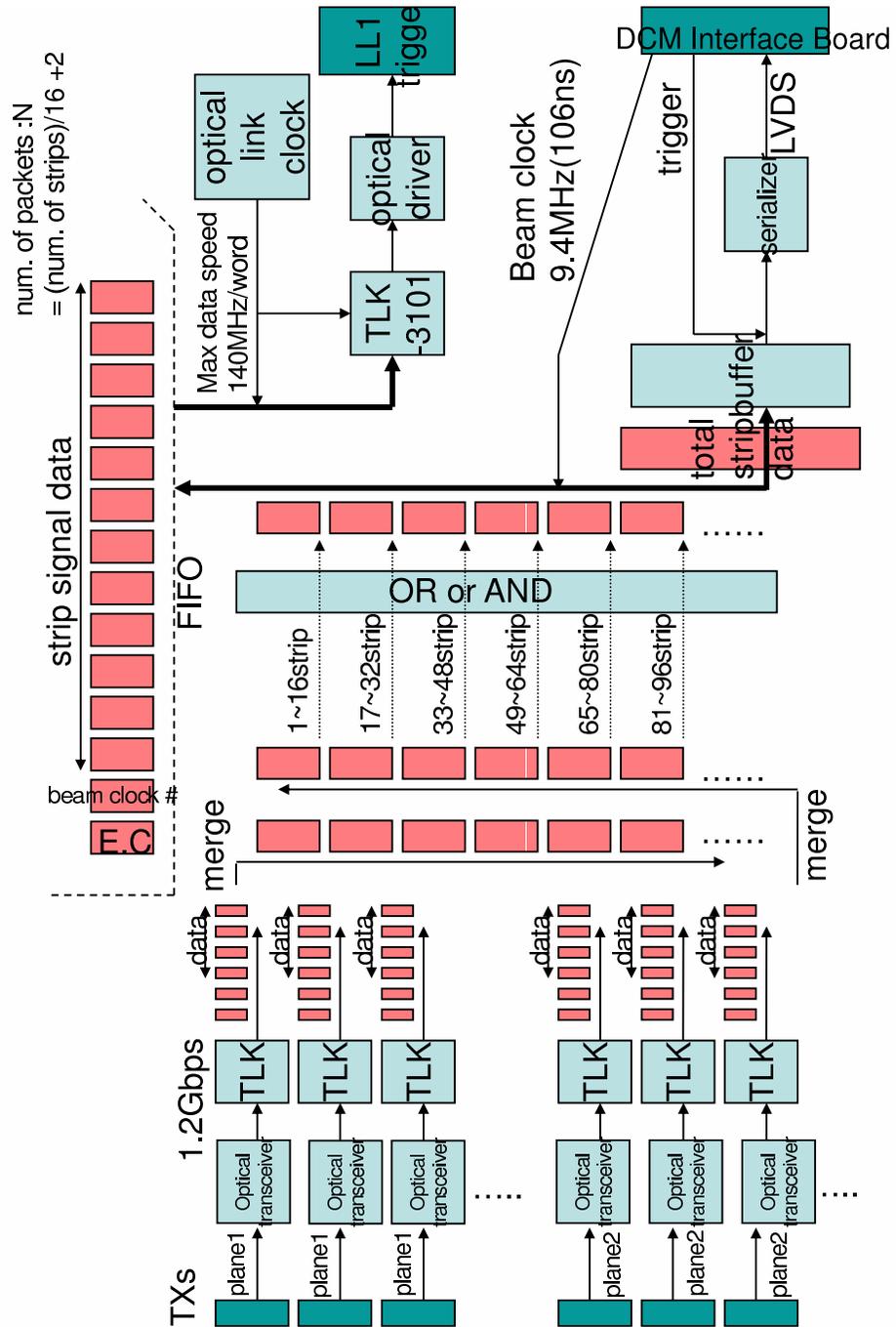


Figure 8.3: Diagram of data flow in the MuTRG-MRG

# Chapter 9

## Conclusions

In this document we have demonstrated the design of MuTr FEE upgrades are compatible with the existing read out chain.

Key performances are:

- Additional noise introduced in the existing read-out chain has been demonstrated to be less than 30%.
- The detection efficiency for the MIP is 91% at 1 kHz fake hit rate, and 93 % at 10 kHz fake hit rate. A reasonably high efficiency was obtained at significantly smaller fake hit rate than the minimum rate of 100 kHz which starts affecting the trigger rejection factor.
- The timing distribution indicated that 94% of the signal are contained within three beam-clock wide timing gate (318 nsec). Timing resolution of our electronics alone is evaluated to be 11 nsec (RMS) at around MPV for minimum ionizing particle, and most of the time jitter is accounted for the chamber signal itself.
- We have shown that an acceptance loss due to the new electronics should be less than 3% for  $J/\psi$  dimuon samples. The loss for single muon is estimated to be less than 2%.

Basing on these performances, we would like to ask for an approval of the basic design of the MuTRG-AD, and MuTRG-TX.

In addition, we will provide materials to justify the new design of the combined board MuTRG-ADTX. The results from test bench will be provided in two weeks.

# Bibliography

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