

Reply to PHENIX Review of Muon Trigger Electronics
MuTr FEE upgrade group
April 1, 2008

We would like to thank the review committee for high evaluation of our work in the design and testing of prototype electronics in PHENIX. In the following, we provide additional information regarding to remarks/suggestions raised by the review committee. Remarks/suggestions are shown in blue, while our reply is typed in black.

The separate AD and TX boards have been well and extensively tested, including tests in the north muon magnet last summer, however the plan presented to combine them into a single board has many advantages including:

- smaller footprint in the magnet and in front of station 1
- fewer cables and connections which should increase reliability
- lower cost, including fewer LV cables running into magnet and fewer types of boards to build
- likely better grounding and lower noise

It would however be prudent to verify these advantages before embarking on a rather large production run of boards. It should be noted that at the time of this review, the combined AD/TX board prototype was in the final stages of production, so test results, even from bench tests or on the test chamber, were not available. Noise from the digital and analog grounds on the board, for example, are highly sensitive to the details of the board layout, and so thorough tests on the bench and in a realistic noise environment are critical to success.

Therefore, we suggest that a full test of two of these new AD/TX boards in the north magnet during run8, with emphasis on verifying the noise performance of the new AD/TX board, be carried out, despite it possibly necessitating rearrangement of the production schedule.

We fully agree with several advantages of combined board described above. After necessary revision of design, a prototype for the AD+TX combined board (MuTRG-ADTX) has been produced (Fig. 1). New features are (1) single 6U-size board with all functions of two boards (AD and TX), (2) separate GNDs for analog part and digital part, (3) a CPLD for slow control, and (4) thinner chassis by optimizing the backplane design.

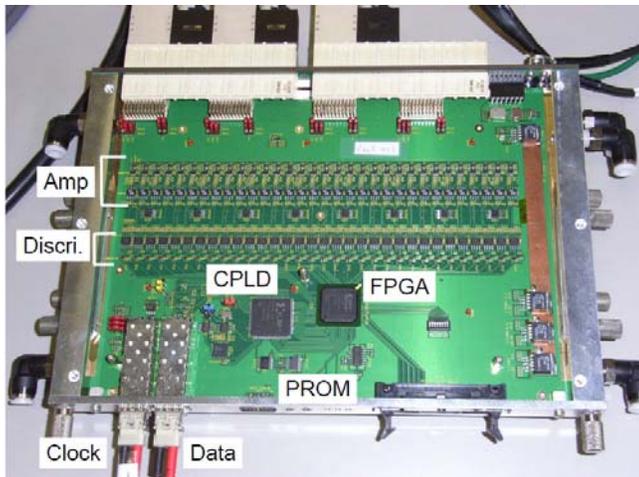


Figure 1 MuTrg-ADTX prototype board

We agree the potential risk was larger noise level. We have followed reviewers' suggestion to do a full test of noise performance of the combined board in the MuTr North during run 8. We performed a test in February 27 during a maintenance day in run 8, and following days until March 4th. We confirmed that noise level of the MuTRG-ADTX was indeed as good as the one which was obtained with separated boards (see Fig. 2 and Fig. 3 below). Results of the test are presented in https://www.phenix.bnl.gov/WWW/p/draft/mibe/muTrFEEupgrade/2008wintertest/doc/Report_of_MuTr_noise.ppt (the impact on original MuTr signal) and <http://ccjsun.riken.jp/~fukao/2008Mar22/analysis.pdf> (response of MuTRG-ADTX)

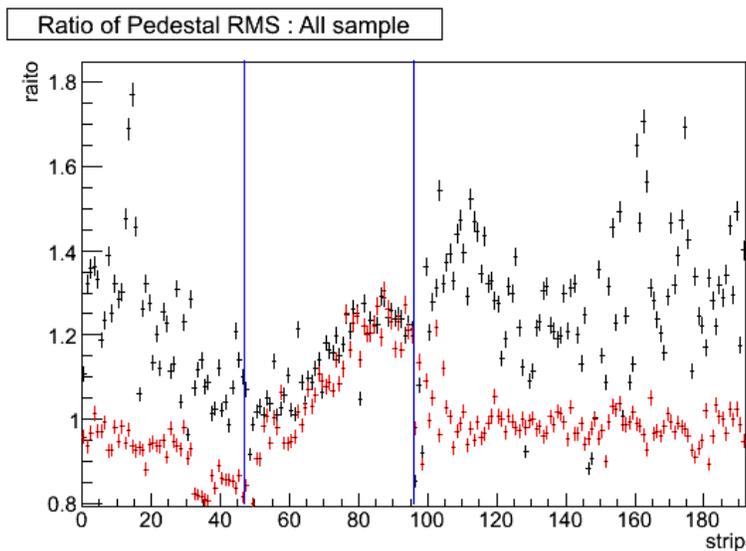


Figure 2 Ratio of the pedestal RMS with the ADTX board to that without it (Red). Similar black data are the ratio with and without AD+TX separated boards, which was measured in summer 2007 at IR. Note that the ADTX board was installed to only 48 strips (ch=46-95) , while all 192 strips were connected to the AD+TX boards in summer 2007

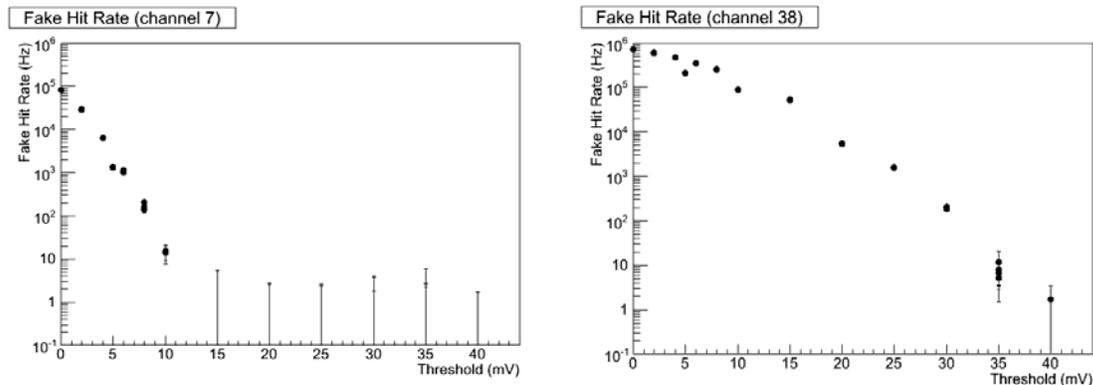


Figure 3 Samples of the fake hit rate of MuTRG-ADTX as a function of threshold. The left plot is for channel 7 (“low-gain parameter”) and the right plot is for channel 38 (“high-gain parameter”). We tested two parameters at the winter test. Compared to the parameters used for AD+TX separated board at the summer test, the gain (and noise) is decreased by a factor of ~ 0.44 for the “low-gain parameter” and is increased by a factor of ~ 1.05 for the “high-gain parameter”. Considering the difference of the gain, we confirmed that the fake hit rate is similar level to the AD+TX separated board. (1kHz or less at the threshold of 8mV for the low-gain and at 29mV for the high-gain, where the thresholds are expected to be about 0.6 MIP.)

Other remarks and suggestions:

- The intrusion of the new FEE chassis into the station 2 active region is probably overestimated since the active area of the chamber does not come all the way to the frame edge. Also Upsilon's probably have more loss due to this intrusion since they give larger dimuon opening angles and populate the larger angle region relatively more than J/ψ 's. However, given the estimated small effects on the J/ψ it is unlikely that the effect is substantial for Upsilon either.

We agree.

- The 25V increase in high voltage necessary to recover the loss of gain caused by the 95%/5% split will tax the existing high voltage performance of the muon tracking chambers. However since most of these HV problems come from leakthrough on capacitors on the unused analog outputs, "de-capacitation" should be able to make the chamber robust enough to handle the +25V. Therefore "de-capacitation" of all the muon tracking chambers is essential and will also improve the general performance of the muon tracker.

Agree. Since this is an essential step to obtain the required performance, we would like to provide necessary support to make this work successful.

- The noise levels from the AD/TX boards have a very strong dependence on threshold level. Also some parts of the muon tracker have larger noise levels than those in the region tested last summer. So a careful evaluation of the range and step size of the threshold adjustment range should be done and an optimal range

established; in the test results presented, it appears that only a very small range of DAC values can actually be usefully used.

Based on the experience in the summer test, we have decreased the range of DAC values so that the minimum adjustable step of the threshold (typically 1 % of MIP) is small enough to comfortably set the threshold at desired noise level.

- The old muon tracking FEE chassis have a dry air system, but it has not been used and is probably not necessary. Therefore it is unlikely to be needed for these new FEE chassis either and can probably be eliminated.

We agree that dry air system may not be necessary in the current system. Our primary concern is that we would like to make the system as robust as possible since access to the boards will be extremely limited once they are installed. Although it is not clear that we need to flow dry air, we would like to keep inlets for dry air supply as has been done for the existing FEE, and flow the dry air during the default operation.

- The one clock delay in the signals when the new FEE is installed on the straight planes does not seem to be a problem since the present system is only tuned to about ± 1 clock.

Agree.

- The scheme to mount the new FEE chassis on the front of the lampshade sides for station 1 may have substantial conflict with the large bundles of cables that come out at least two places around the circumference of station-1. More detailed studies should be done to determine if the proposed mounting scheme could be accomplished given this interference.

Once the central magnet is moved away from either of South or North station-1, the more concrete plan of chassis mounting design and cabling works will be made. Presently, mounting chassis on a fiberglass unistrat is considered to establish isolated grounding between the tea-cup and chassis as well as helping portable and flexible installation.

- The scheme to mount chassis at station 2 to the existing FEE chassis needs to be engineered in a more minimal way using existing holes but with strength enough to hold "upside-down" chassis on the top. Provision for several large ground connections between the two chassis should be provided.

We have developed more concrete mounting structure under a consultant of Walter and Jimmy. A new mounting structure was tested in the station 2, octant 7 as shown in Fig. 3 below. A bottom plate of the chassis was replaced with aluminum plate with extended support wings on both sides.

The wings hold the chassis by using existing six unused screw holes (three each) on both sides of FEE chassis. This mounting scheme ensures the tight mechanical and electrical connection to the existing FEE. The chassis will be elevated about 5/16 inch to allow the ADTX board in the bottom slot to be installed/uninstalled without interfering with the spider frame.

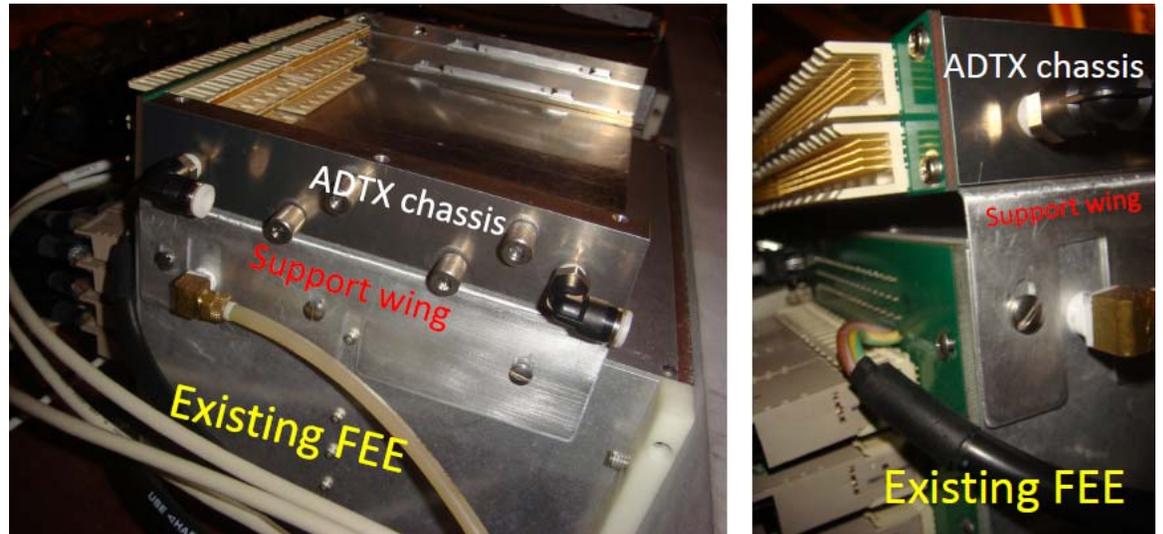


Figure 4 Existing FEE and ADTX chassis with newly developed mounting scheme

- Rack locations for the LV racks needs more study. They should be located to minimize trapping lampshade panels on magnets and so that those on the south magnet travel with the south magnet.

Present candidates of power supply platform certainly interfere with lampshade open/close work. However according to the present scaffold design, all FEE's can be accessible without opening top lampshade in North arm. South arm scaffolding work is still in progress and still remains unclear the negative impact of the rack location. On the other hand, the necessity of opening the top lampshade seems to be low in North arm, and most of MuTr.N installation/maintenance activities can be done under the minimum constraint from the new rack location. We will keep working on South arm with engineers.

- The group needs to have a comprehensive plan for quality control during installation which includes several levels of tests before installation and after. This is doubly important since much of the electronics in the upper parts of the muon tracker will be inaccessible once it is installed and the scaffolding is removed.

We start planning the QA plan for the MuTRG-ADTX board before installation. Test items have been identified based on failure mode analyses at test bench. More comprehensive list of test is being developed as the

studies with the prototype become mature. As for the quality control after installation, we'll make a plan based on previous experience with existing FEE from Mike and other MuTr experts. We will improve our plan by consulting experts in other lab as well. Prof. Osamu Sasaki at KEK kindly agreed to give a short lecture to us on quality control for ATLAS muon trigger system.

- The group has spent considerable effort on grounding with the prototype and will need to continue doing that with the final design. Given the long input signal loop, they will have to take care to make sure signal lines are well shielded. Second, in the station where they are installing the chassis on the lampshade, they will need to pay close attention to the ground between their electronics and the MuTR FEE. In addition, they will have to make sure that they are isolated from the lampshade.

Thank you for detailing out the necessary conditions of grounding and shielding. We will take above conditions into account in the final design.

- Considerable power may be dissipated in the regulators on the board if supplied with a single voltage. The board should be imaged with an IR camera to determine if the power dissipation at the regulators is prohibitive; this could suggest that bringing in multiple voltages could be desirable.

It is true that power dissipation at the regulators is not small. The heat profile of the MuTRG-ADTX board was measured with an IR camera. Figure 4 and 5 shows the heat profile without and with cooling water. The numbers in the left bottom corner is the temperature in degree Celsius.

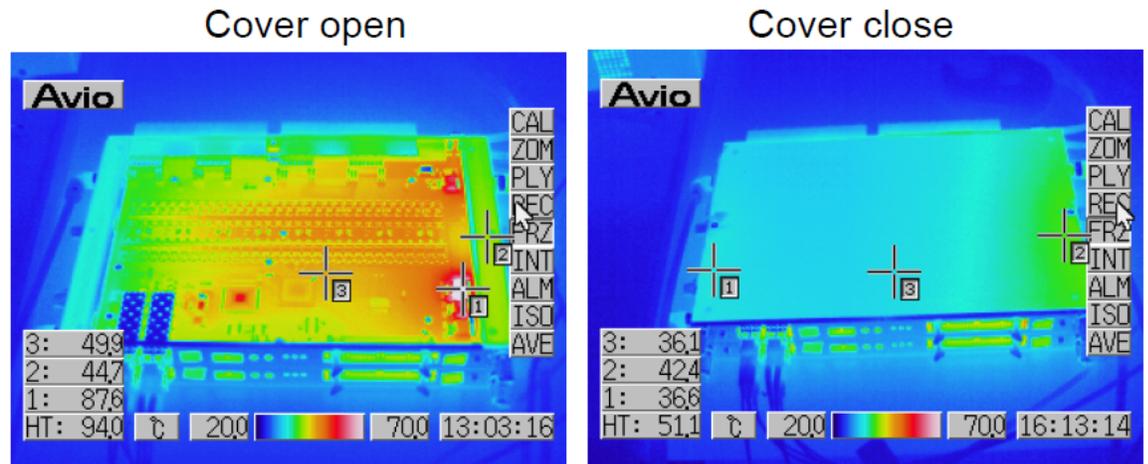


Figure 5 heat profile without cooling water

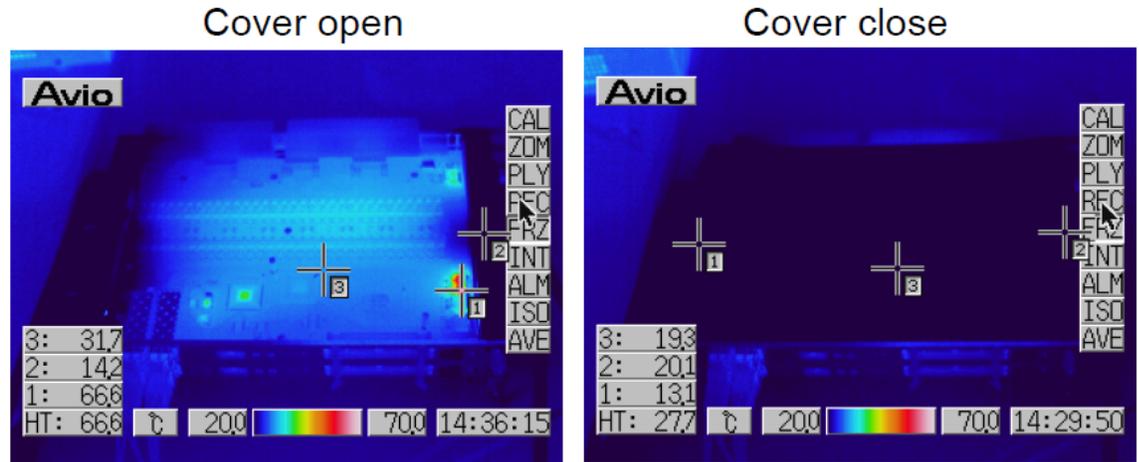


Figure 6 heat profile of the MuTRG-ADTX with cooling water

Indeed, temperature at the regulators is as high as 94 degree Celsius without cooling water. With water cooling from the chassis, the temperature goes down to about 67 degree Celsius. This concludes that the existing water cooling system has enough cooling power to keep the board temperature within normal operation temperature for the electronic parts on the board.

- The boards should be tested with incorrect power connections (power and ground reversed, for example) to determine whether the boards would be damaged by incorrect installation or power supply problems.

This test will be performed in the test bench before mass production of the board.

- The completed board should be checked for problems operating in a magnetic field and the presence of any magnetic materials.

The board and chassis were tested at station 2 octant7 under MuTr magnetic field during run 8. The board was fully functional when the magnetic field was turned on.

The chassis is made of aluminum plate. All screws are stainless steel. They are weakly sensitive to magnetic field. As for the board itself, we investigated the board by sweeping a strong permanent magnet over the board. We found following parts are WEAKLY field-sensitive:

- jumper (female) and jumper pins
- input connector pins
- optical transceiver

The optical transceiver is firmly connected to the cage on the board. The jumper pins and connector pins are soldered on the board, they will be

difficult to move by the B-field even if they are magnetic-sensitive.

A complete list of magnetic components was presented to Yousef Makdisi during the system safety review in March 14.

- The materials used on the boards and in the cabling should be documented and verified in preparation for the system safety review.

List of the material on the boards and cables were submitted for the system safety review. They are available as

https://www.phenix.bnl.gov/WWW/p/draft/mibe/muTrFEEupgrade/safety_review/MuTRG-ADTX/

They were reviewed by PHENIX safety representatives, Paul Gianotti and Yousef Makdisi et al. in March 14.

- The clock frequency should be varied around the nominal 9.4 MHz to make sure the boards operate correctly for clock frequencies at least 5% different from the nominal clock frequency.

A data transmission from MuTRG-ADTX board was tested with various beam clock frequency. Patterns of pulse were fed to the inputs for the MuTRG-ADTX, the board transmitted discriminated data to a receiver board (former TX board with minor modification). Transmission efficiency was evaluated by the ratio of number of received events divided by total number of inputs. The transmission efficiency at various beam clock frequency is shown in Fig. 6. From Fig.6, we conclude no inefficiency is introduced when the clock frequency is changed by +/-5% from the nominal frequency (106ns).

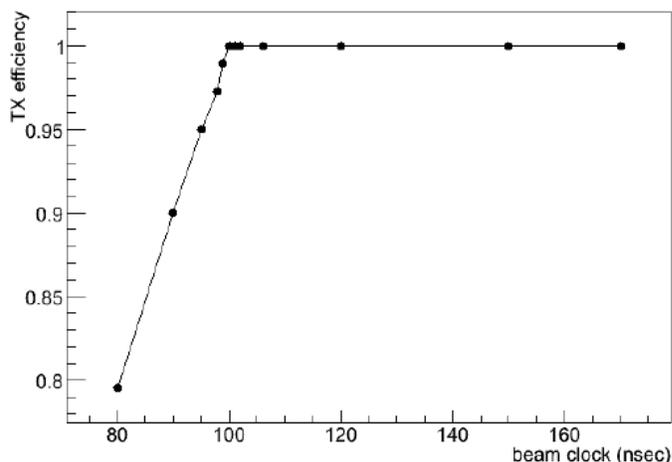


Figure 7 Transmission efficiency from MuTRG-ADTX to a receiver board as a function of clock frequency.

- The need for non-volatile memory on the board should be reexamined; it would be desirable if the boards came up into a usable state from power-up, even if not

perfectly optimal, without downloading configuration data. In particular, the Xilinx Spartan FPGA on the new AD/TX board will not be booted when powered up. It will have to be programmed from the slow control and until it is programmed, the board is left in the un-determined state. It would be better to add XILINX Flash PROM for booting FPGA at power up. If the code has to be updated, the slow control path can be used to update the XILINX Flash PROM memory.

It is true that MuTRG-AD board becomes an un-determined state (threshold value is not specified) if it is powered on without connecting to the MuTRG-TX board. This is because MuTRG-AD board doesn't have FPGA nor PROM, while the MuTRG-TX board is equipped with a FPGA and a flash PROM.

The new combined board, MuTRG-ADTX, has a flash PROM on it. Upon power on, FPGA on the board will automatically load its default configuration from the flash PROM, followed by setting threshold values for discriminator. Therefore, the board falls into a known state when it is booted.

- It is unclear whether the muon trigger will require its own GTM, or can share timing with the muon tracker; a GTM devoted to the muon trigger would allow “standalone” running without the muon tracker during installation and commissioning, but leads to greater complication later.

We consulted with Martin, Chi and Ed Desmond on this issue. In terms of availability of resource in current PHENIX online system, it is possible to provide the Muon trigger its own GTM. One needs to monitor the noise rate periodically by taking a random triggered data. Thresholds should be optimized based on such data. We could in principle share a GTM with MuTr subsystem. One driving factor to favor sharing GTM with MuTr is that one can not take meaningful data when the calibration pulse is generated on MuTr strips in the MuTr's gain calibration process. Thus, knowing the status of MuTr subsystem is a key to monitor the trigger system. The status of MuTr is best known by sharing the same GTM. The issue is that whether there is enough user bits available in G-link to get full control of the MuTRG system. We are in a process of summarizing what our needs are. We will consult MuTr experts on this business if this is realistic option or not.