Testing Plans

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Overview of Testing Procedures

- A total of 222 boards will be manufactured for ITS (+ 88 for MFT)

- Testing will be done in a 3-stage approach:
  1. Testing at the manufacturer
  2. Board bring-up and initial hardware verification at Nikhef/Utrecht
  3. Functional Testing at 3-4 collaborator sites

- We will investigate the possibility & cost of shifting some tests from Nikhef to the board manufacturer

Testing at Manufacturer

- PCB Testing:
  - Visual inspection (metallographic cuts, thickness of board, …
  - Electrical Connectivity Test (flying probes test)
  - Controlled Impedance Testing
- Assembly Testing:
  - Correct placement of parts
  - Soldering Quality
  - X-ray of BGAs
  - Automated Optical Inspection (AOI)
- Initial Powering and Testing for shorts
- All inspections will be in accordance with IPC-A-610 Class-2 specifications

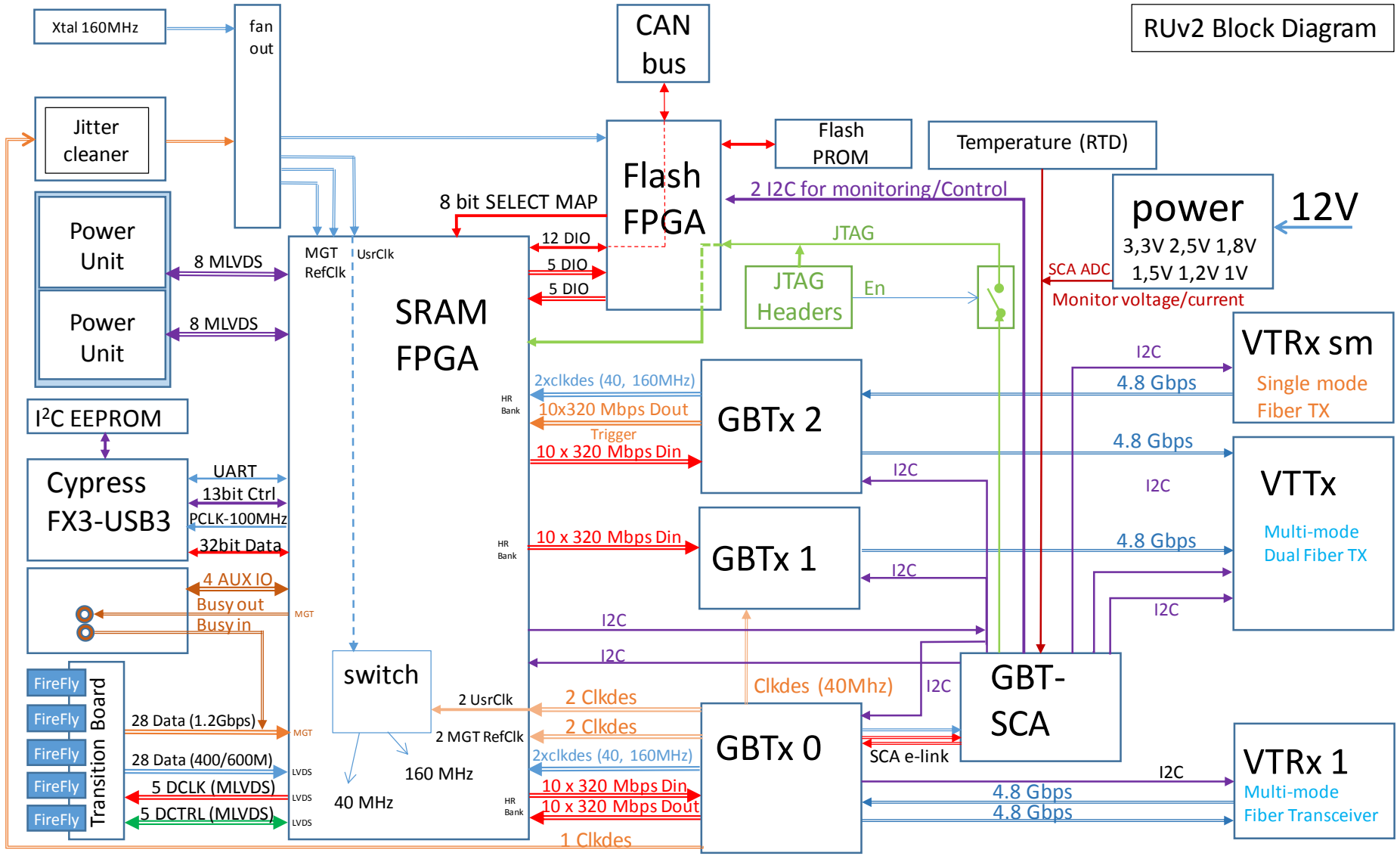
Testing at Nikhef/Utrecht

- Power on test: Voltages & Current verification
- Verify I2C bus for GBTx configuration; fuse all GBTx chips
- Read out Voltages, Currents, and temperature values via SCA
- JTAG configuration of Ultrascale & Microsemi FPGAs
- Check FX3/USB3 interface:
  - Use Cypress USB “Control Center” application to verify connection over USB
  - Use Control Center to program FX3 boot PROM

Functional Testing at Collaborator Sites

- Test the various I/Os and internal connections of the board
- Uses a custom board to interface to the various I/Os
- Testing will be scripted to provide a “yes/no” type result
- Failing boards will be returned to Nikhef/Utrecht for further trouble shooting

Readout Unit Overview



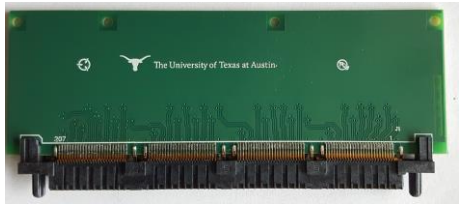
I/O lines to be tested in functional test

Purpose	Number	Electrical Standard	Direction	Receiving/sending Chip	Termination	Nominal Speed	Notes
I2C	8	MLVDS	Input	SN65MLVD080DGG	100 Ohm	200kbps	on Power Mezz
I2C	8	MLVDS	Output	SN65MLVD080DGG	100 Ohm	200kbps	on Power Mezz
HS Data	28	LVDS	Input	Ultrascale GPIO	AC-Coupled -100	600Mbps	on transition board to GPIO
HS Data	9 (28?)	LVDS	Input	Ultrascale GTH	AC-Coupled -100	1.2Gbps	on transition board to MGT
DCLK	5	MVLDS	Output	SN65MLVD080DGG		40MHz	on transition board
DCTRL	5	MVLDS	Input/Output	SN65MLVD080DGG		80MHz	on transition board
FiberOptic	3	Optical	Output	GBT VTRx/VTTx		4.8Gbps	Multimode GBT protocol
FiberOptic	1	Optical	Input	GBT VTRx		4.8Gbps	Multimode GBT protocol
FiberOptic	1	Optical	Input	GBT VTRx		4.8Gbps	SingleMode GBT protocol
Busy	1	LVDS	Input	Ultrascale GTH		1.2Gbps	Aux connector
Busy	1	LVDS	Output	Ultrascale GTH		1.2Gbps	Aux connector
AUX	4	LVDS	Input/Output	Ultrascale GPIO		?	Aux connector
USB	1	USB-3					To be tested with Host computer
CANbus	1	CAN 2 wire	Input/Output	TPS3306-15D	120 Ohm		To be tested with Host computer
JTAG							Test programming of 2 FPGAs
FX3 EEPROM							Test programming through FX3
I2C							Test programming of GBTx chips

Suggested Tests for Functional Testing

- **JTAG**: Program testing firmware to 2 FPGAs via JTAG; verify running firmware (e.g. blinking LEDs)
- **USB:** verify communication between host computer & FPGA via FX3
- **I2C**: generate PRBS pattern @200kbps on 8 outputs (SCL_w, SDA_w), receive on 8 inputs (SCL_r, SDA_r)
- **GBT**: GBT_FPGA on test board, generate PRBS on TX, receive PRBS on RX
- **Alpide Data lines**: Transceiver IP with 28 RX; generate 1.2Gbps test pattern with OSERDES @ 600MHZ DDR; receive PRBS on Transceiver RX
- **DCTRL, DCLK**: Generate 80Mbps PRBS on DCLK; receive PRBS on DCTRL
- **BUSY**: Loopback PRBS patterns from OUT to IN, using transceivers?
- **PA3-Flash I/F**: Read Flash ID; read & catalogue “bad blocks” (page 0)
- **“Serial Number”:** Read and catalogue UltraScale FPGA DNA value as unique identifier for Readout Unit
- **CANbus:** Connect USB CAN dongle to host computer, send and receive simple CAN packets @ 1Mbp
- **Ultrascale-PA3 I/F**: Send & receive test patterns
- **SelectMap I/F:** PA3 reads US SelectMap ID

Simple Test System Concept



Possibly integrate into 1 board?

e.g. KCU105 running GBT_FPGA + CRU emulator firmware

To be developed

FPGA Devkit

Fiber Mezzanine

Loopback Board

28 MGT

1.2Gbps

28 LVDS

5 MVLDS

80Mbps

5 MVLDS

Transition Bd

FPGA running custom testing firmware to generate & check PRBS patterns for loopback boards

Fiber OUT

Fiber OUT

4.8Gbps

Fiber OUT

Fiber IN

Fiber IN SM

FPGA running GBT firmware with PRBS test pattern RX and TX

RUv2

USB / Ethernet

Loopback Board

8 MVLDS

200kbps

8 MVLDS

Power Mezz

FPGA running custom testing firmware to generate PRBS patterns for loopback boards

Host Computer

USB-3

CAN Dongle

CAN

JTAG Programmer

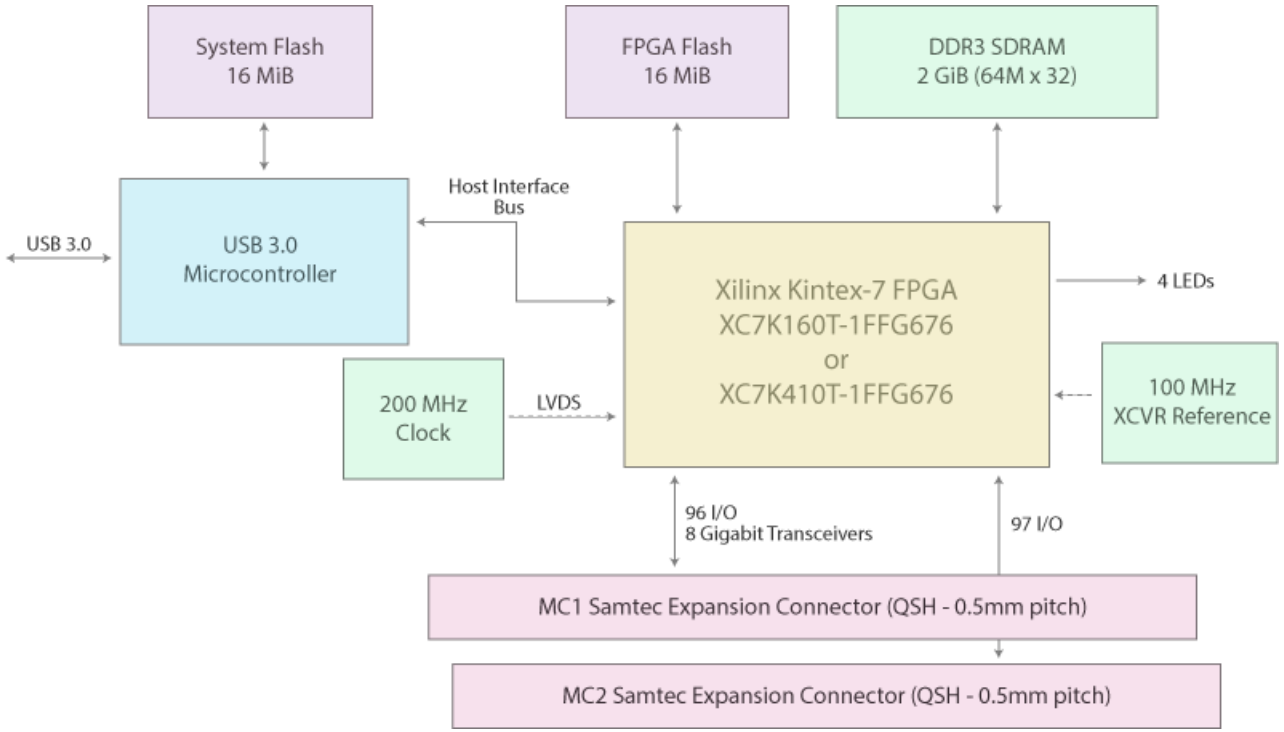
JTAG

Possible Dev-Kits

Opal Kelly XEM7360

https://www.opalkelly.com/products/xem7360/

$1,699.95 (+ $129.95 for breakout board)

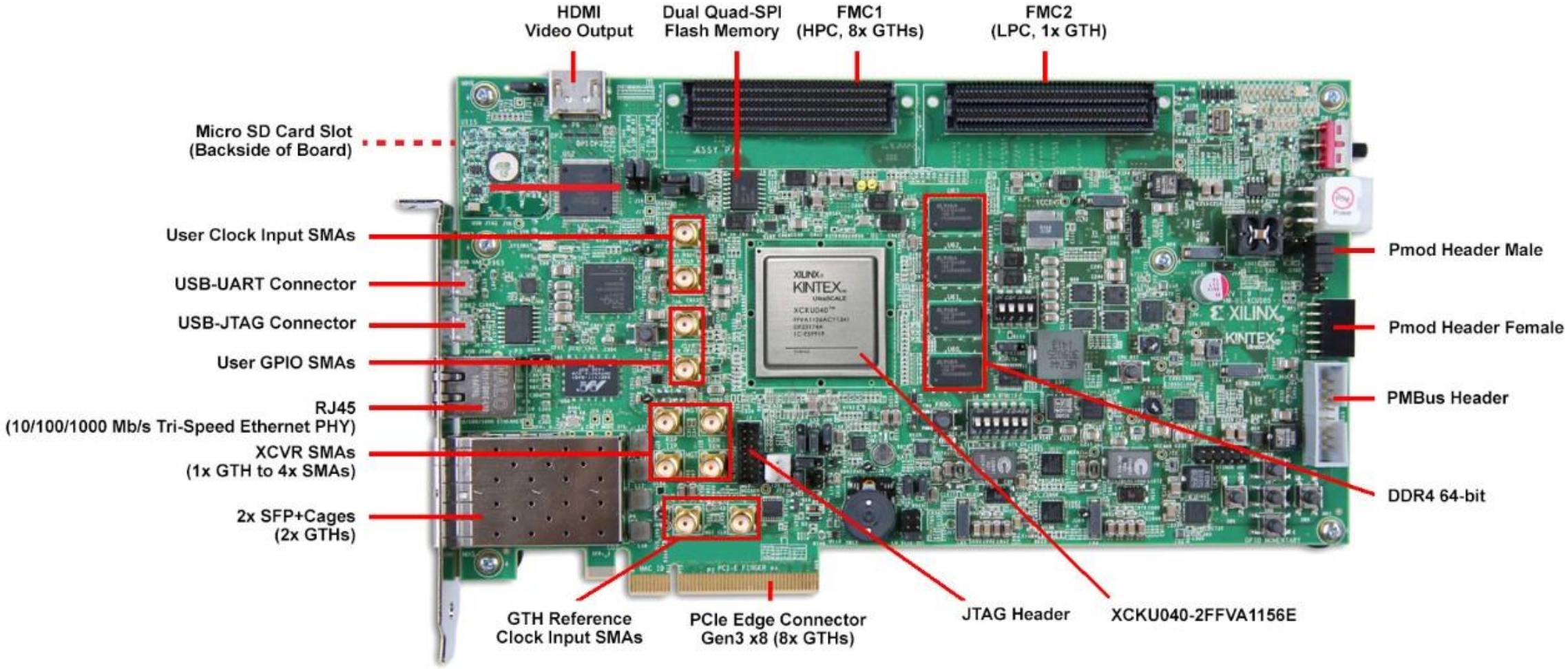


Backup Slides

Xilinx KCU105 Evaluation Kit

https://www.xilinx.com/products/boards-and-kits/kcu105.html

$2,995



Expansion Connectors

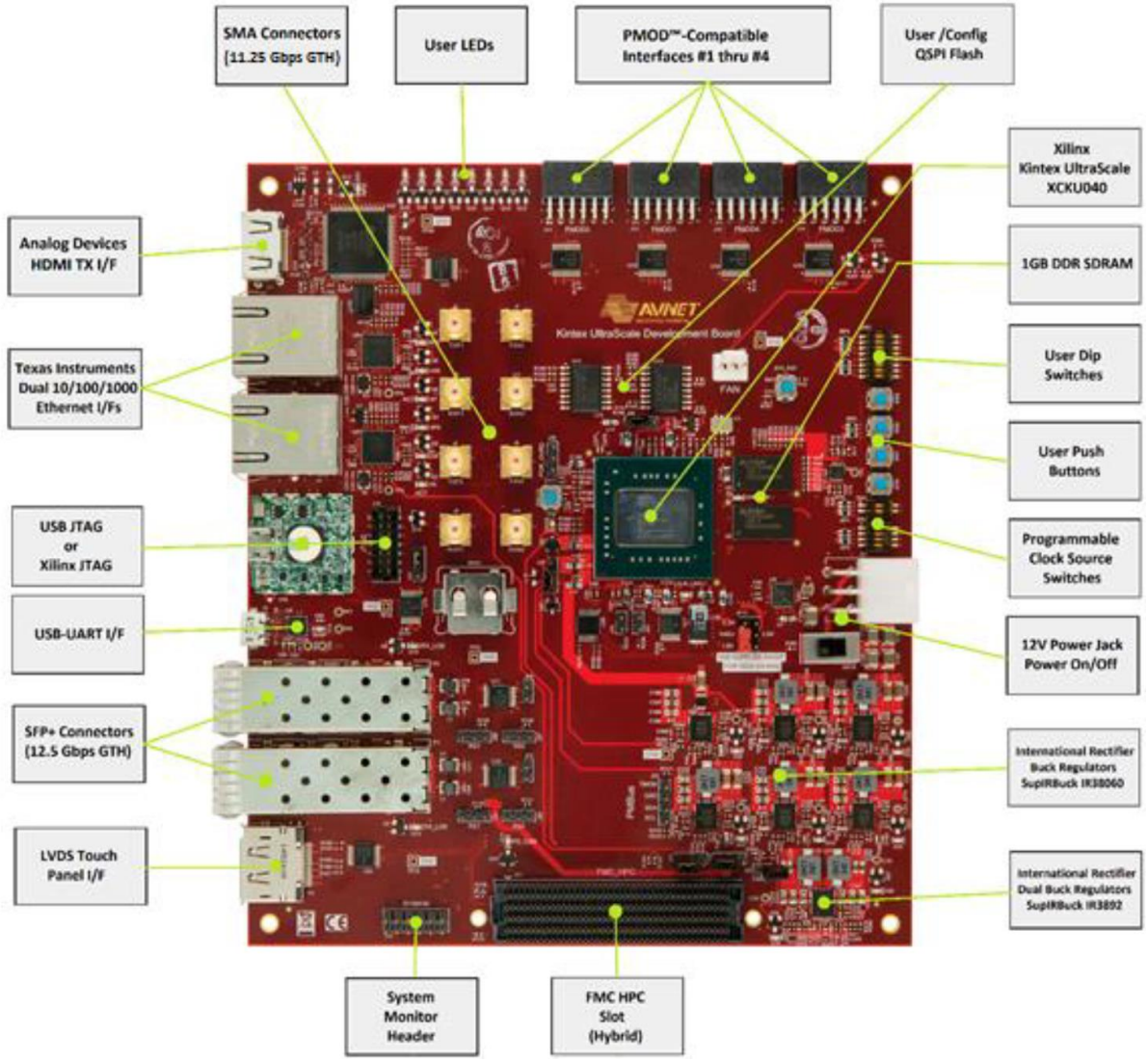
- FMC-HPC (Partial Population) connector (**8 GTX Transceiver**, 114 single-ended or 57 differential (34 LA & 24 HA) user defined signals)
- FMC-LPC connector (**1 GTX Transceiver**, 68 single-ended or 34 differential user defined signals)

Communication & Networking

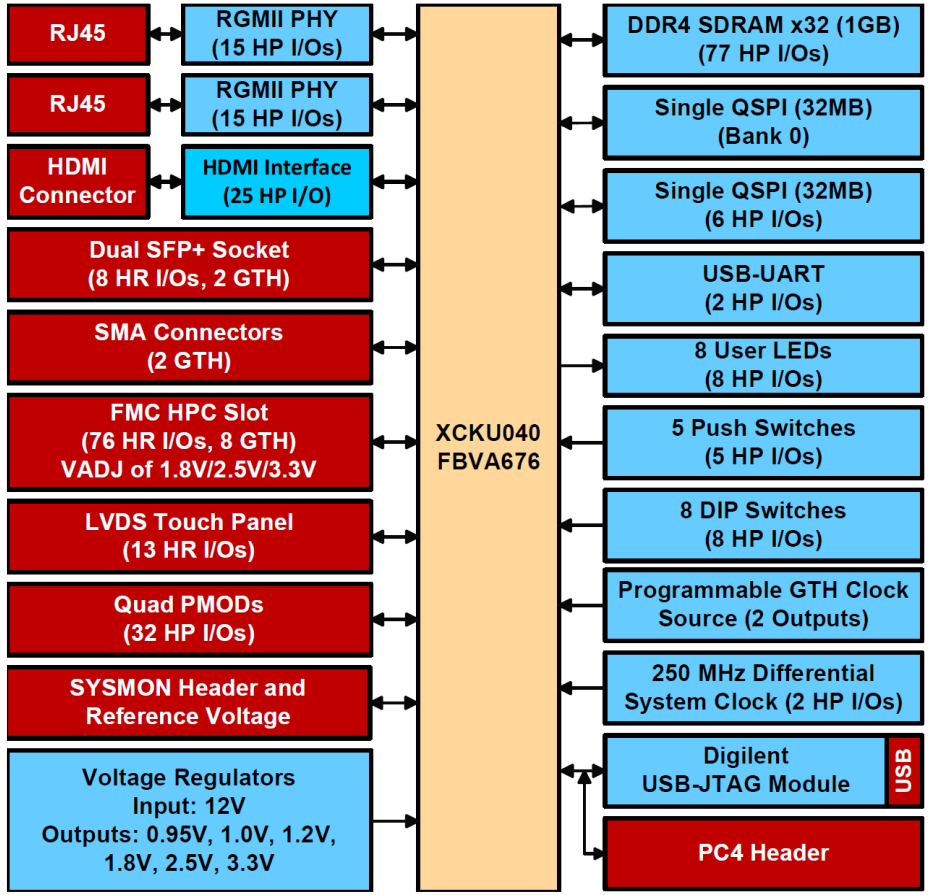
- Gigabit Ethernet GMII, RGMII and SGMII
- **2x SFP / SFP+ cage**
- GTX port (TX, RX) with four SMA connectors
- **UART To USB Bridge**
- PCI Express x8 edge connector

Avnet AES-KU040-DB-G

https://www.avnet.com/shop/us/products/avnet-engineering-services/aes-ku040-db-g-3074457345630043740/



$995



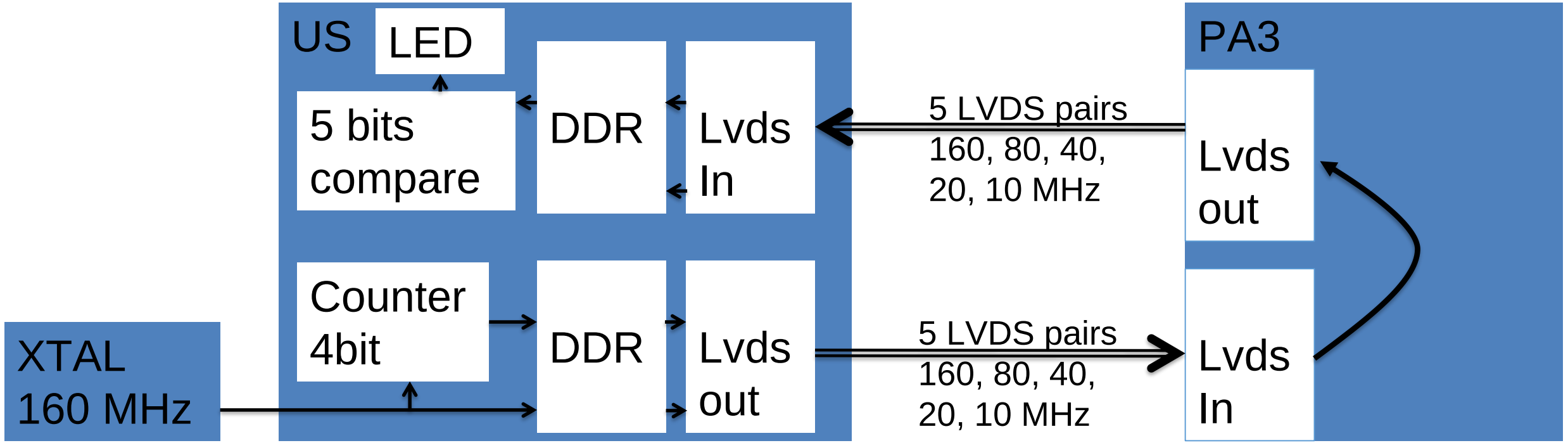
Interfaces

- **Two SFP+ Sockets** (up to 12.5Gbps)
- Two GTH SMA Interfaces (up to 11.25Gbps)
- Two 10/100/1000 Ethernet Interfaces (RGMII)
- HDMI Interface
- LVDS Touch Panel Interface
- FMC HPC Slot (VADJ of 1.8V, 2.5V, 3.3V) with **8 GTH lanes** (up to 12.5Gbps)
- Four Single Ended Pmod™-Compatible Sockets
- **USB-UART Interface**
- 8 User LEDs
- 5 User Push Button Switches
- 8 User Slide Dip Switches
- Analog SYSMON Interface

Some Example Tests already being performed

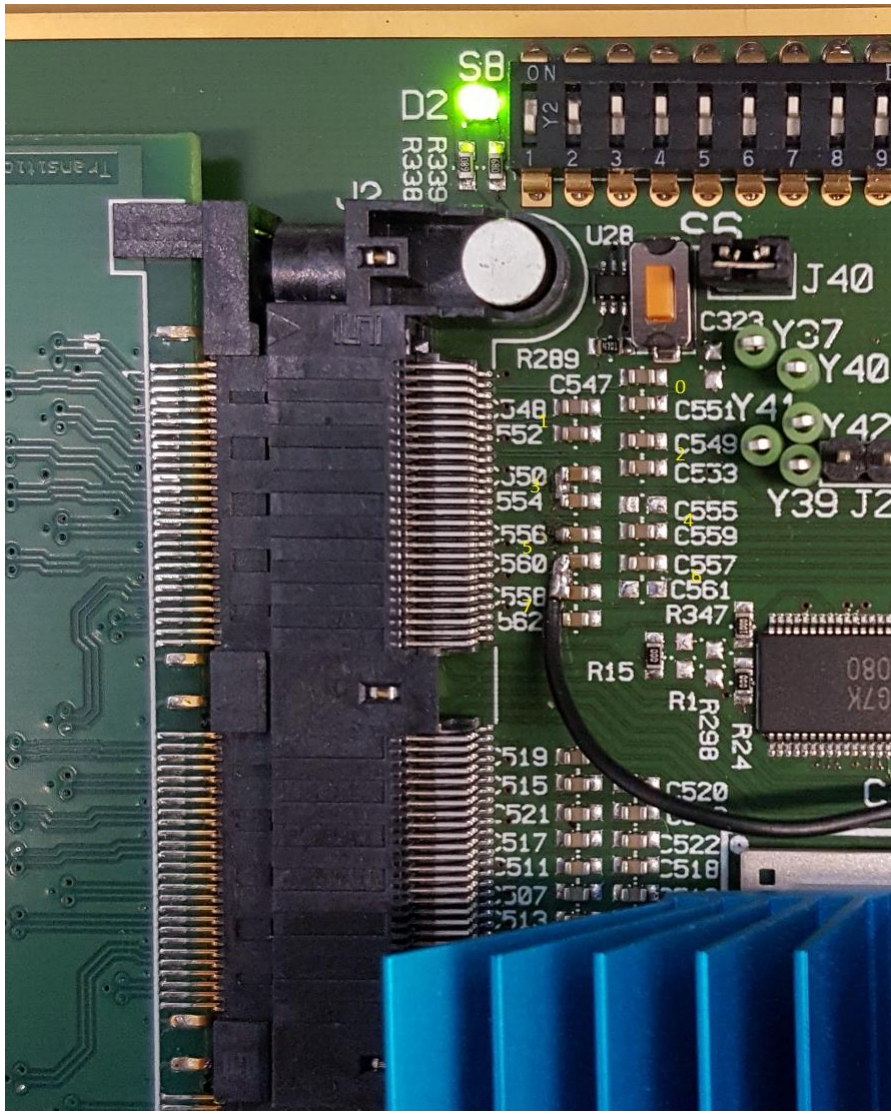
US <-> PA3 LVDS and GPIO communication

- Ultrascale-ProAsic3 Interface consists of 10 diff pairs (5xLVDS out and 5x LVDS in) and 12 SE IOs.



Transitionboard (QMS/QFS) loopback test

- For testing the connectivity (short/opens) of the RU transition-board connector, The University of Texas developed a loopback transition-board. It connects the 28 MGT inputs with 28 GPIO_LVDS outputs.
- Utrecht developed firmware for testing the connectivity. It generates 1.2Gbps PRBS7 signal on the LVDS outputs and utilizes the MGT PRBS checker to detect the errors. Tests showed the reduced driver swing and limited MGT input equalization is needed to detect all defects (open, shorts...)
- Image shows all hardware faults intentionally introduced
- The next slide shows under which conditions these faults were able to be detected.
- The BUSY out/in was tested in a similar fashion



Transistionboard loopback test

Lowering driver voltage to SUB-LVDS and changing the receiver equalization and termination makes the error conditions visible:

GPIO Diver		LVDS	SUB-LVDS						
MGT Receiver	Equalize	DFE	LPM						
	Termination	800mV		100mV	1100	GND	AVTT	Float	Float
	Coupling	AC							DC
0...2	OK	700	270						
									OK
3	Short	0	0						
									OK
4	Neg open	240	90						
									OK
5	Pos=>GND	360	135						
									OK
6	Pos open	270	110						
									OK
7	Neg=>GND	300	130						
									Ok
8	Stub								
									Ok

Example of Test Sheet used at Utrecht for RUv1

PCB	RUv1.1	Date	2010-03-2
Ser.Nr.		Tester	MJ Rossewij/Wisman

Impedance measurements (Fluke111//Fluke29):

	Location	R (ohm)	
Power in	J0	2M	
J1-5V	J1 pin 96<-33	2M	
J1-12V	J1 pin 95<-33	INF	
VCCint	Y10	10	
VMGT	Y11	100	
1V2	Y12	1k3	
1V8	Y13	540	
3V3	Y14	600	
2V5	Y15	220	
1V5	Y16	200	
FX3_1V2	J25-2	10k	
FX3_1V8	J26-2	200k	
FX3_3V3	J27-2	9M	
FX3_VIO5	J28-2	4M	

Power up:

Vin(V)	J0	4		5				12	
I(mA)	J0	0		1000				500	
VCCint	Y10/Y20	0		0,960	100			0,958	
VMGT	Y11/Y21	0		1,010	10			1,010	
1V2	Y12/Y22	0		1,220	2			1,213	
1V8	Y13/Y23	0		1,810	45			1,802	
3V3	Y14/Y24	0		3,320	63			3,310	
2V5	Y15/Y25	0		2,500	50			2,493	
1V5	Y16/Y26	0		1,525	200			1,520	

JTAG Connect to Xilinx

Jumper as "US&PA3" (J33 & J34 pin1-2, J35 pin 2-3), Connect Xilinx download cable to J8
Vivado 2016.1 (USclkForward) ->Hardware manager->OpenTarget->Cable Auto Connect: _____
Place J40, Upload_program (USclkForward) -> INIT LED:____->_____, DONE LED X->X

Function	Result "US & PA3"	Result "Only US"
Sysmonitor		
DIPswitch=>header (J13)		
Pushbutton=>LED		
Clock=>SMA (J21/J22)		
Press S6		

JTAG Connect to PA3

Jumper as "US&PA3", Connect_FlashPro cable (remove Xilinx cable!) to J11, Upload RUv1PA3test_____

Test header & dipswitch (J14)	
Config Xilinx, Clear error with S8 switch 1&2. Run error free (LED off) for	

JTAG Connect to PA3

Start_FlashPro and upload Bergen test program (FP_PA3test):

Function	Result with FP_PA3test	Result with RUv1 AUX FPGA
Test push buttons		
Test dipswitch		
Test LED		
Flash memory Read ID (A651D5EC 0068)		
Select Map read ID–press S8 (13919093)		

Upload flash page0/spare section		
RUv1_top_171202_128_7e9bbfe to flash		

Include second part to chain

Connect "whole chain" (J25/6/7/8 p2-3, J29 p1-2, J30/1/2 p2-3, J35/6 p1-2, J37 p2-3, J38). Scan Chain.

Vivado 2016.1->Hardware manager->OpenTarget->Cable Auto Connect	
Microsemi Flash Pro	

Check presence clock signal

Put LVDS 155 MHz on J15/J16

	Probe	IN_SEL	S10	S4	Amplitude	Frequency	Device
CDCLVD1212 X1 out	SMA J19/J20	0	NA	NA			Scope
					160.315/6		PM6669
CDCLVD1212 in1		1	HHMH****	OFF	154.99976		PM6996
SI5316 bypass SMA	SMA J17/J18	1					Scope
SI5316 reset			HHMH****	ON			Scope
SI5316 byp. in1			LHMH****	OFF			Scope
SI5316 clean SMA			HLMHLM**				Scope
SI5316 out off			*M******				Scope

Connect USB3

	Comment	Jumper
J25	+1V2_USB3	2-3
J26	+1V8_USB3	2-3
J27	+3V3_USB3	2-3
J28	VIO5_USB3	1-2

Connect USB3 cable, Start Cypress USB Control Center

	Comment	Jumper	Result
Upload program (*SN0*) to RAM	USB boot	XXLLL F11	
No action	I2C boot, USB on failure	XXLLL F1F	
Upload program to I2C	I2C boot, USB on failure	XXLLL F1F	
	I2C only	XXLLL 1FF	
	USB boot	XXLLL F11	
Upload WP10 image to I2C	USB3 communication?	XXLLL F1F	

Connect USB->I2C->GBTx downloadcable

Start win32 PC => cmd => java -jar programmerv2.20170503.jar
Place jumper J41, J42 & J43 on 2-3 (1V5)

Are 3 GBTx visible	

J2 loopback test

Connect FAN, connect loopback PCB
Upload: US24MGT\gtwizard_utrascale_0_example
- Hb_gtwiz_reset_all_vio_int 1->0->1

All rxprbslocked/err LEDs green?	

Connect GBTx

	CRU->RUv1	RUv1->CRU
VTRx		
VTRx2		
VTTx	NA	

Connect Sensor

400Mbps									
1.2Gbps									