Status RUv2 production unit

- Differences RUv1 -> RUv2
- Status RUv2 prototype run
- Status RUv2 series production & test-system
- Status transition-board and power mezzanine

Marcel Rossewij

Main differences RUv1 -> RUv2

Total 21 RUv1 are produced (and were all operational.)

- 8 * RUv1_0
- 13 * RUv1_1: 3 RUv1 needed replacement LMZ31710 DCDC regulator (Parts appeared broken, possibly during soldering):
  - Datasheet states improved high solder temperature immunity for date code > wk 14 2018.

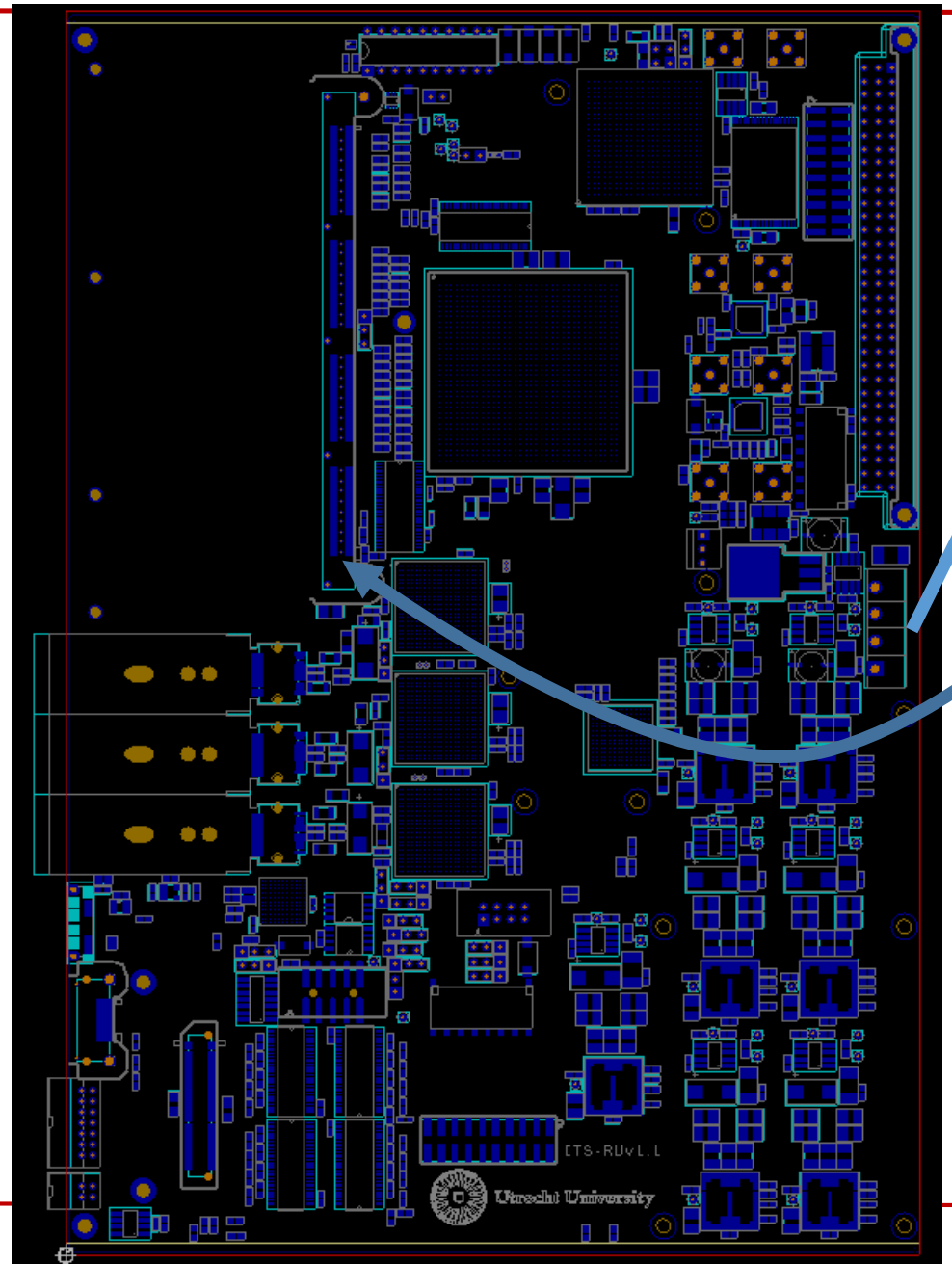
RUv1 so far succesfully passed the tests (no showstoppers found)

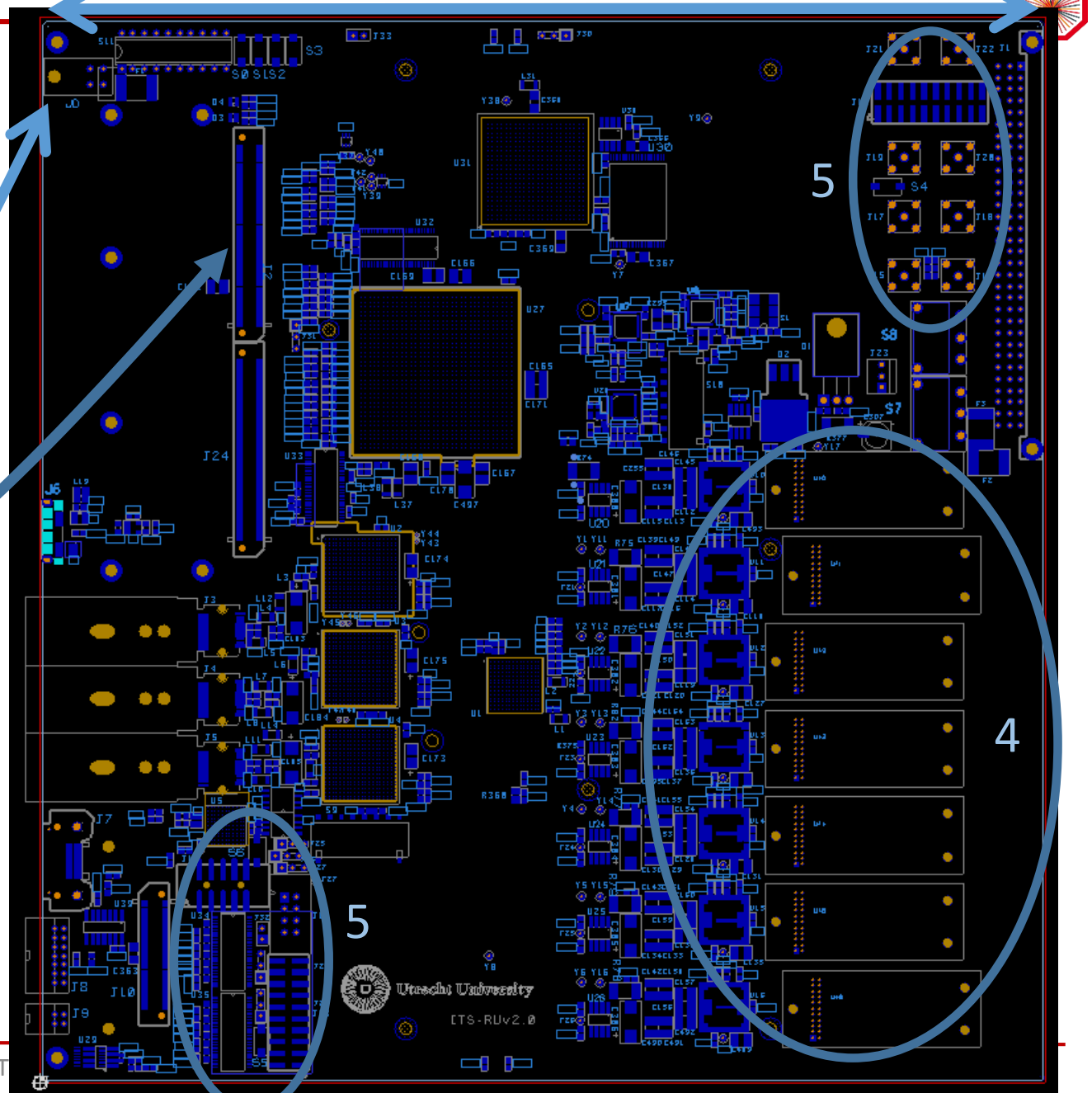
- Scrubbing jitter Issue => comes from US device itself => avoid using US PLL/MMCM for DCLK generation
- Erratic behaviour => Voltage drop before regulators => Increase PSU voltage

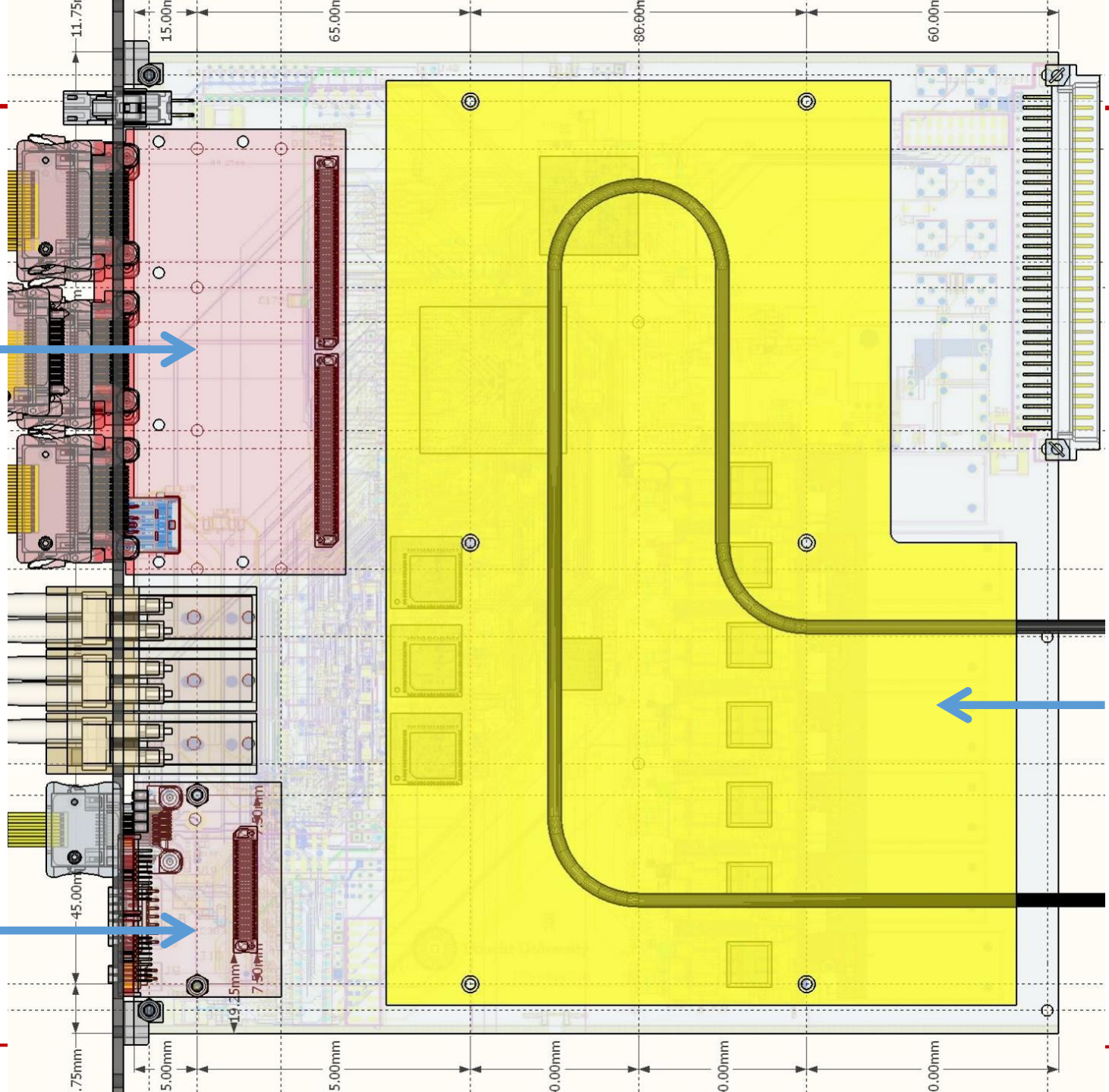
RUv2 is based on RUv1, with the following main differences:

		RUv1_x	RUv2
1	Dimensions	160x233 mm	220x233 mm
2	Power connector	J0 (Weidmuller BL/SL 5.08) on back	J0 (MOLEX 172316) to front (J1 stays as it is + switch to select between J0 & J1)
3	Transistion board connector	Samtec QFS/QMS type	2 * Samtec ERF8-50... (USB3 connector also moved)
4	Improved PI + placeholder for FEASTMP_CLP and additional capacitance	Only COTS DCDC	Placeholder FEASTMP_CLP and additional capacitance to mitigate spikes due to SEU Use of blind via's to further improve PI
5	Removal high compements from the cold plate area, aiming for same cold plate power board		

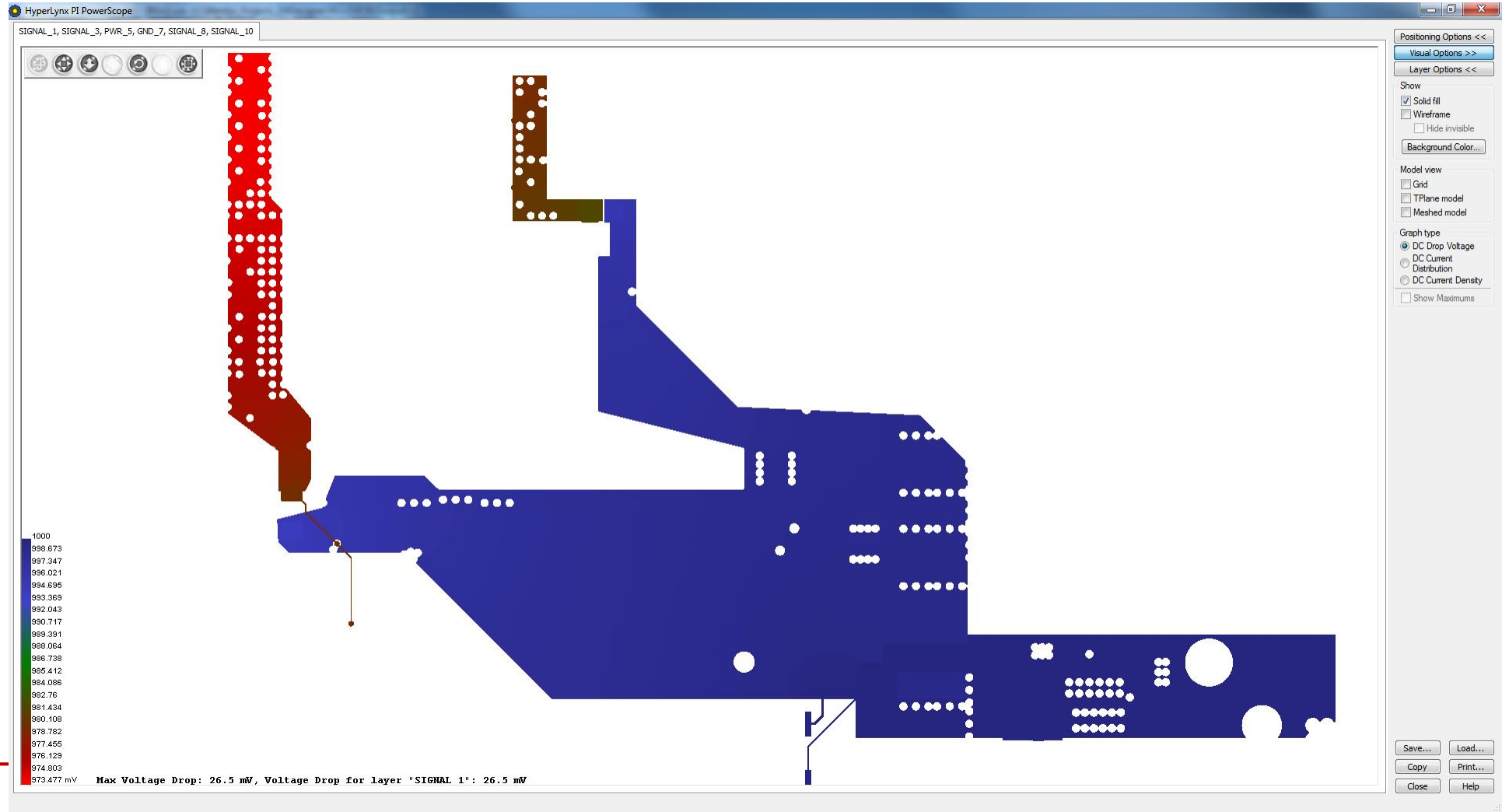
Main differences RUv1 -> RUv2






Transistion Board
Power Mezzanine
Cold plate

	V	RUv1_x (mV)	RUv2 (mV) New DCDC placement	RUv2 (mV) Adding blind via's
VCCINT	0,95	19,5	13,5	11,3
MGTAVCC	1	32,1	26,8	26,5
MGTAVTT	1,2	30,8	25,2	24,4



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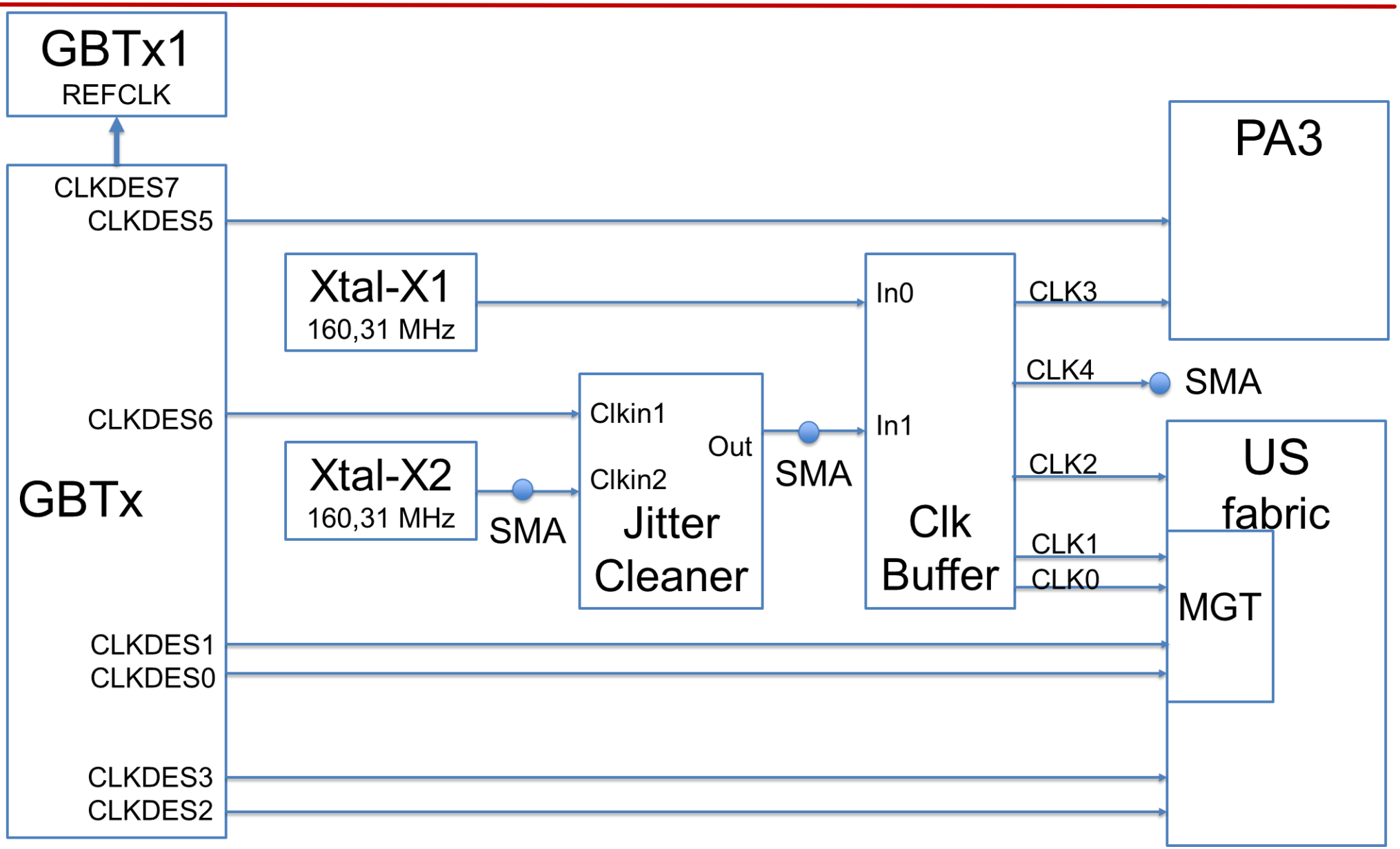
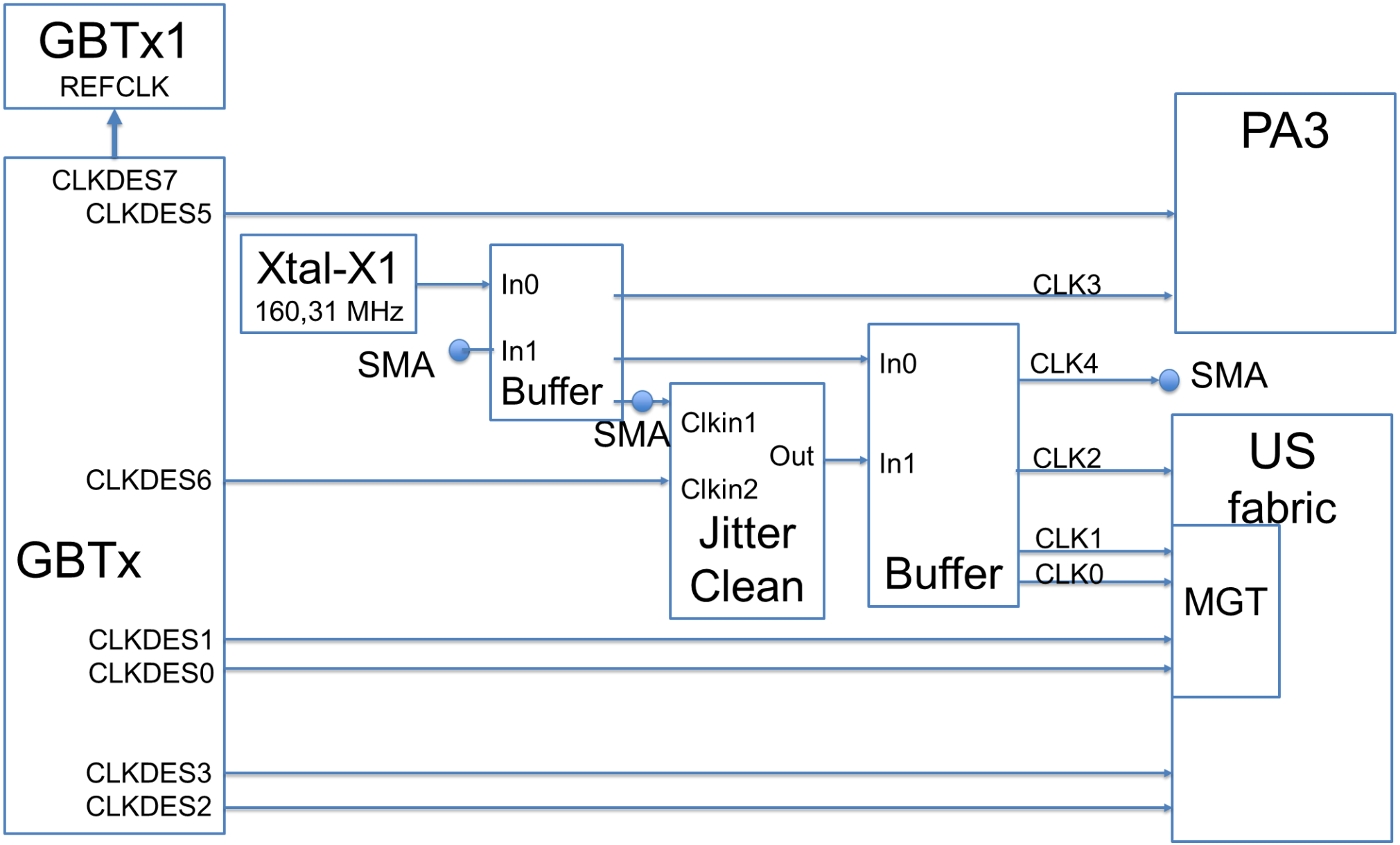
4	FEASTMP	Only COTS DCDC	Besides COTS also FEASTMP_CLP placeholder Updated DCDC placement for improved PI Use of blind via's to further improve PI
5	Removal high compements from the cold plate area, aiming for same cold plate power board		
6	Change Clock distribution with PA3 clock independent from jitter cleaner		

RUv1_1 clocking scheme



RUv2 clocking scheme



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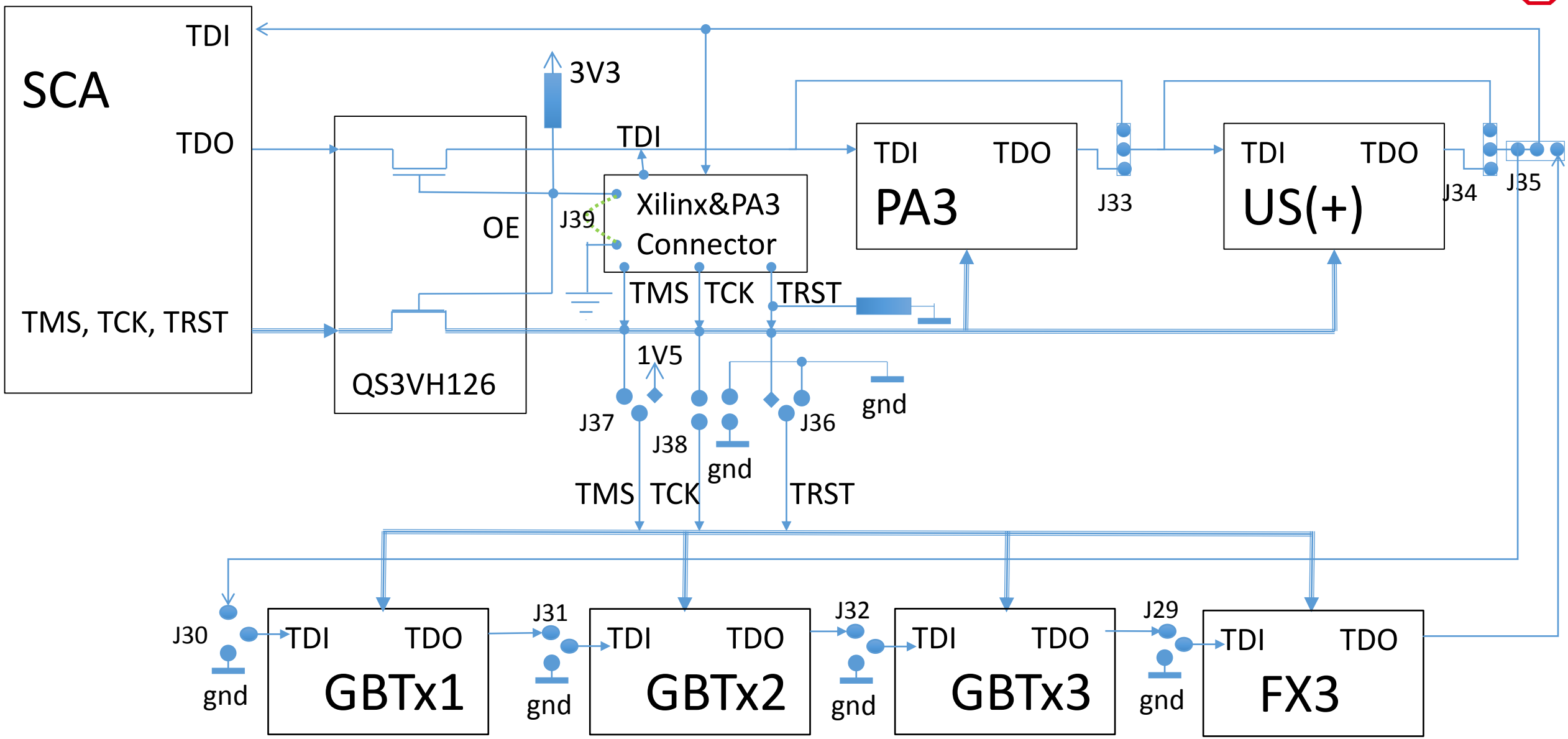
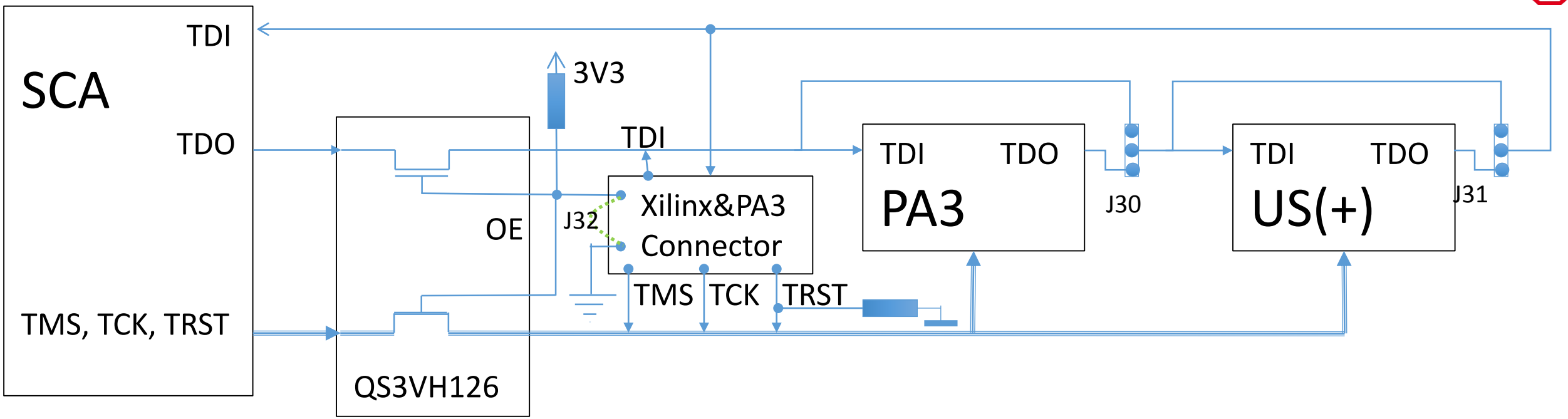
5	Removal high compements from the cold plate area, aiming for same cold plate power board		
6	Change Clock distribution with PA3 clock independent from jitter cleaner		
7	Remove secondary JTAG chain		

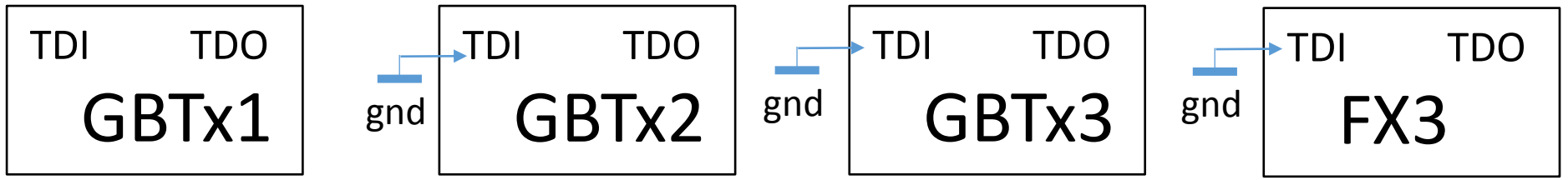
And many more smaller changes that can be found in:
Twiki WP10 -> RUv2 -> ITS_RUv2_changes

RUv1 JTAG configuration scheme



RUv2 JTAG configuration scheme





Status RUv2 prototype production

Produce 4...9 RUv2 prototypes in order to:

- To validate the design before starting series production.
- To be used in the IB readout system.

9 empty PCB have been ordered and produced.

- First assemble 4 PCBs to validate design
- If oke, produce other 5 PCBs

PRR recommends 3D x-ray capabilities at assembly house. (move to other assembly house)
4 companies (tbp, phuntronix, variass, eprpartner) were asked for producing the first 4 proto's
Only 1 company (epr-partner) indicated to have time to produce the 4 proto's
Some delay was caused by the component procurement and administrative issues.

- Production in week 25-26
- Delivery in week 26-27

Status RUv2 series production & test-system

Tender document is being written

Testing at producer:
PCB: electrical connectivity, characteristic impedance, mechanical cross sections
Assembly: AOI, SPI, 3D Xray

Test procedure in 3 phases:
1) At assembly company: test for shorts on the 7+1 power rails
2) At UU/NIKHEF: board startup (FPGAs and FX3) tests and loopback tests.
3) At Austin and other sites: endurance tests

Testsetup
Testsetup for phase 2 & 3 under development
The RUv1 transistion loopback-board (Austin) and firmware (UU) is operational
- succesfully identified problem on RUv1 SN9

Firmware is now also integrated in WP10 framework (Austin)
The RUv2 transistion loopback-board (Austin) is currently under development
The loopback cables and firmware under development (UU/NIKHEF)

Status RUv2 transition-board and power mezzanine

Austin (Jo) developped, produced and just received the power mezzanine and transition board for RUv2