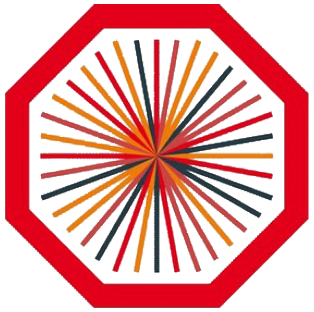
ALICE



ITS Readout Electronics

Readout Unit v1.x – Current availability and status

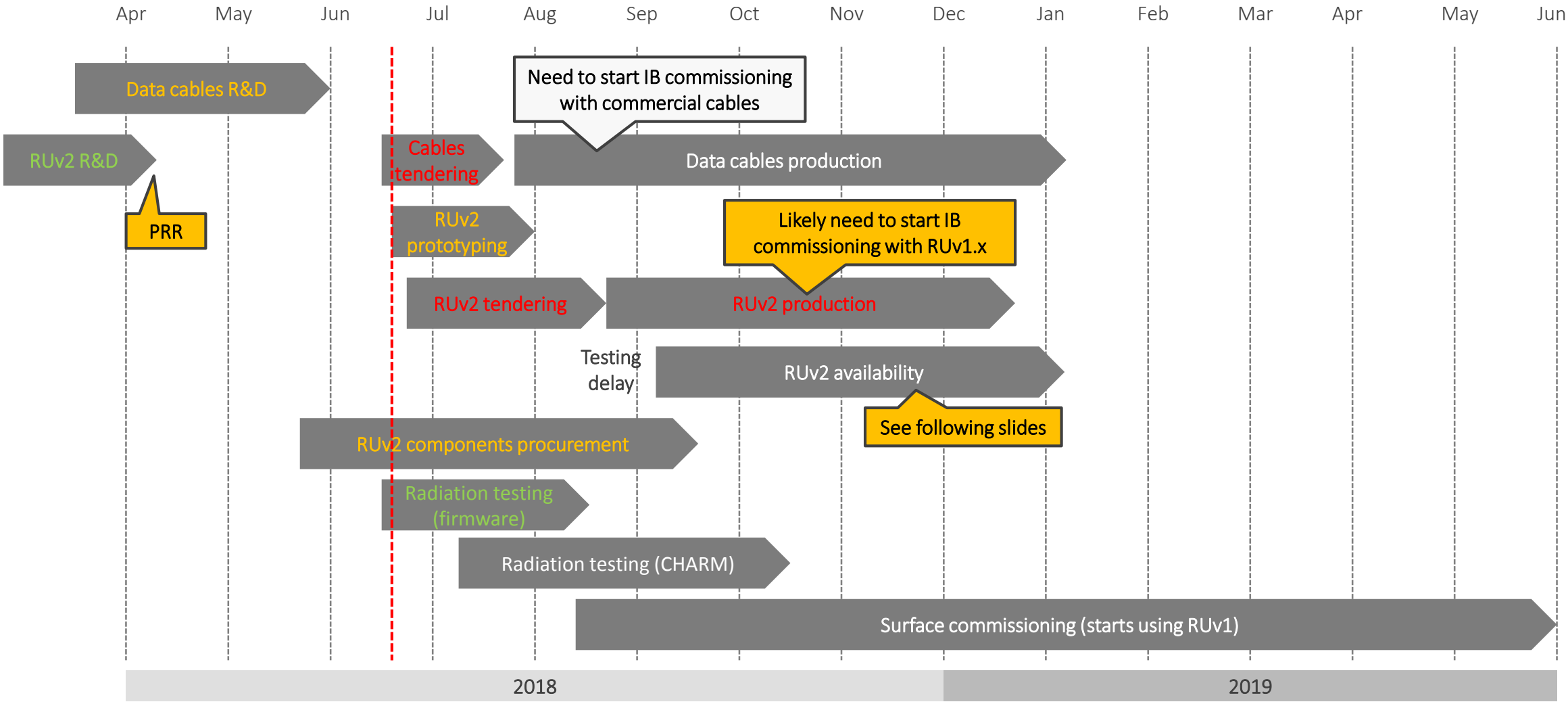
- All Readout Units v1.0 and v1.1 delivered from Utrecht/Nikhef (see more details on WP10 twiki pages)

	RU v1.0	RU v1.1	Tot	
CERN	4	5	9	Various uses, includes irradiation
Austin	1	2	3	Firmware / CRU development
Utrecht/Nikhef	1	2	3	Hardware testing
Bergen	1	1	2	PA3 system development
SPhenix	1	3	4	
Totals	**8**	**13**	**21**	

- So far found only an issue with few boards showing an "erratic" behavior
  - Found to be below-spec voltage supply due to voltage drop across the power-supply line!
  - For the production run, it has been decided to not to mount a polysilicon switch (fuse) which drops the voltage by more than 200 mV, as in the cavern the CAEN supply will have compliance protection.
  - **With correct powering all boards fully stable.**

RUv2 and Data Cables – timeline overview

Production of RUv2 (222 boards + 88 for MFT) will likely take 3-4 months (batched). Critical to the production is components availability (even passives), actually being investigated. Active components procured (see next slide)



Readout Unit v2 – Components procurement

Due to long lead times and/or pricing some key components procurement started even before completing the Readout Unit final design (RUv2).

So far found critical for RUv2 prototypes production:

7	muRata	GRM32ER60G337ME05L	SMD Multilayer Ceramic Capacitor, 330µF, 4V, ±20%, X5R	Farnell	330uF	C138-C144
2	Vishay	VJ0603Y104KXJCW1BC	Vishay 100nF ±10% 16V Ceramic Capacitor X7R 0603	Digikey	100nF	C337,C338

Alternative dealers found and components ordered -> boards in production this week

Major components procurement status

Component	Status	Lead time	Due to
GBT components (GBTx, SCA, VTxx)	Available		
Xilinx XCKU060	Close to order	10 weeks	Sep 2018
Microsemi A3PE600L	Ordered	12 weeks	Sep 2018
Memory Samsung K9WBG08U1M	Available		
Oscillator LFSPXO076300	Available		
Passives	Being investigated		

Readout Unit v2 – Tendering document ready and verified by Marcel

The RUv2 tendering document (technical specification batches, etc) is ready, including testing procedures (see following slides). Production is foreseen happening in batches and lasting 3-4 months.

Batches

- A pre-series totaling 10 boards;
- A first batch totaling 106 series production modules;
- A second batch totaling 106 series production modules;
- A third batch totaling 88 series production modules.
- Option for 40 more boards for Super Phenix

Hardware components

- 1 Xilinx XCKU060-1FFVA1156C (1156 pins BGA package)
- 1 A3PE600L-FGG484M FP (484 pins BGA package)
- 3 CERN custom made GBTx chip (434 pinst BGA package)
- 1 CERN custom made SCA chip (196 pinst LFBGA package)
- 3 SFP+ pod connectors
- 2 ERF8-050-05.0-L-DV-TR connectors (100 pins, 0.8mm pitch)
- Miniaturized passive components (0201 minimum)

Activities at the Contractor's premises

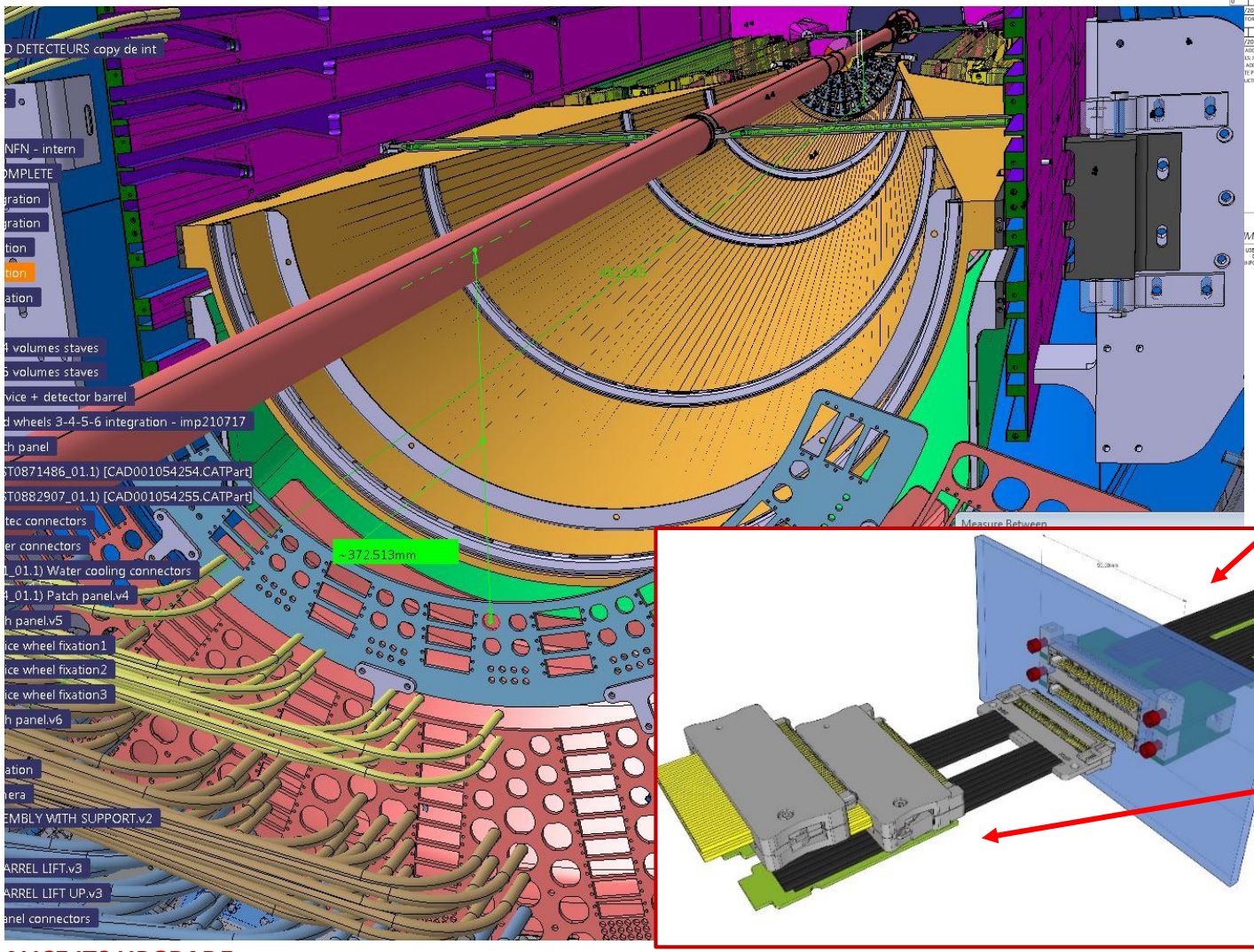
- Quality control of the PCBs.
- Ordering of passive and active components.
- Input quality control of all components.
- Assembly of the components on the PCBs and soldering.
- Quality control of the assembled boards.
- Packing, and shipping.

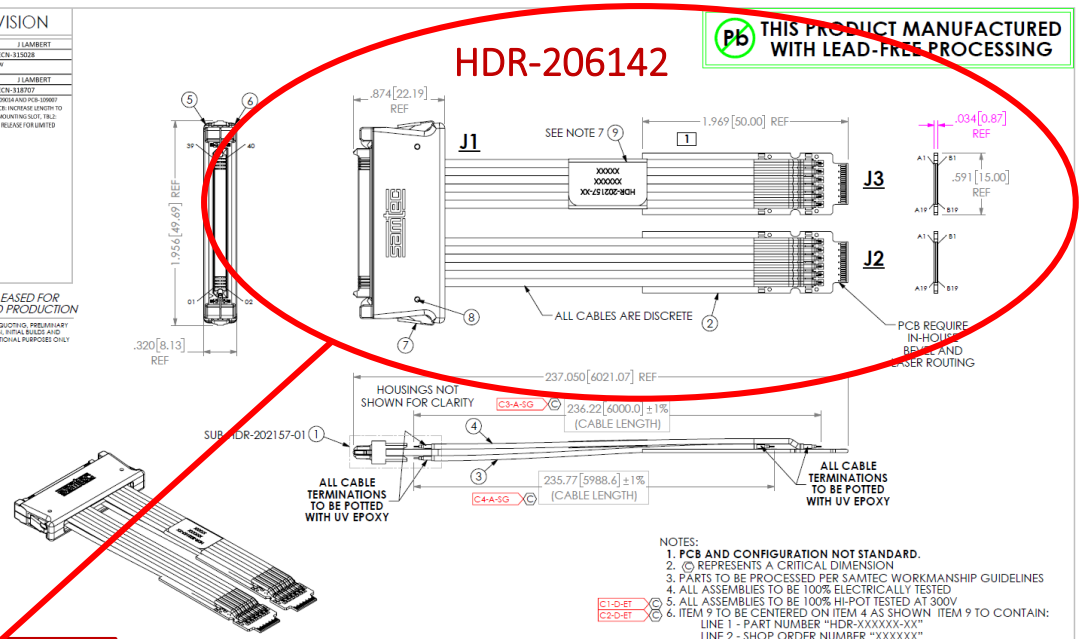
Key technical PCB parameters

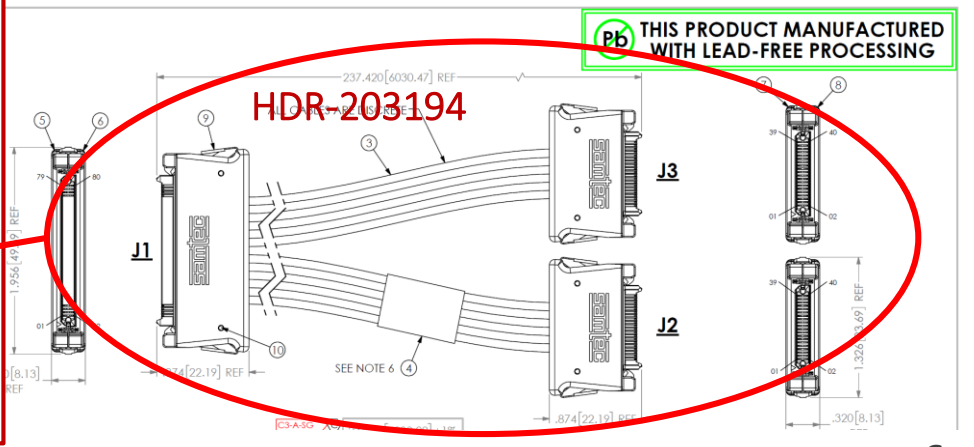
- 10 layers low loss material (Er < 3.7 at 5 GHz, Df < 0.012 at 5 GHz)
- Maximum overall thickness of (1.57±0.13) mm
- Copper Outer layer: 35 µm, Copper Inner layer: 18 µm
- Holes per PCB: 2400 (among which ##% are micro-vias)
- Minimum hole diameter: 0.3 mm
- Blind vias (layers): 1
- Minimum track width (outer layer): 90 µm, (inner layer): 90 µm
- Minimum spacing (outer layer): 90 µm, (inner layer): 90 µm

Data cables – Data connection double assembly

To simplify general layout and installation procedures a patch panel (PP2) has been inserted between the racks of the readout/power electronics (PP1) and end of the wheels (EW). Cables for power/bias/data on both side of PP2 have been **prototyped and are being tested right now**.



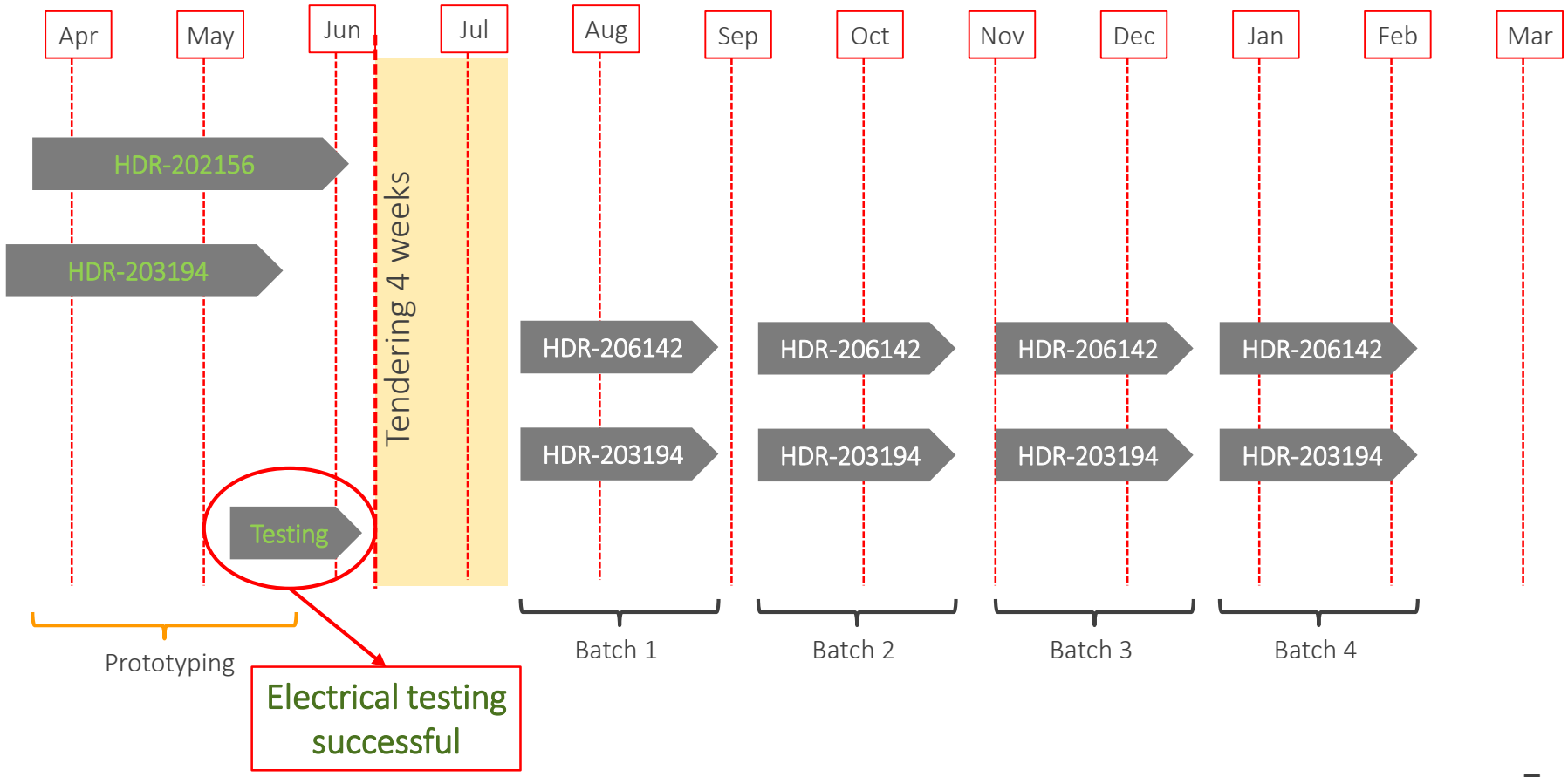




Data Cables – Prototyping and procurement

- To meet cavern installation safety rules custom-made high-speed data cables have been developed in collaboration with Samtec (now known as “CERN cables”, used by ATLAS as well).
- Each cable is split at PP2, **HDR-206142** from End Wheels to PP2, **HDR-203194** is from PP2 to RU (see slide before).
- Cables are paired into single connectors at PP2, hence for 624 cables we will order 312 assemblies (+ spares).
- Lengths and types frozen (see next slide), **ready to launch the tender** (with single participant).

Layer	Cables	Assemblies
0	12	6
1	16	8
2	20	10
3	96	48
4	120	60
5	168	84
6	192	96
Total	**624**	**312**



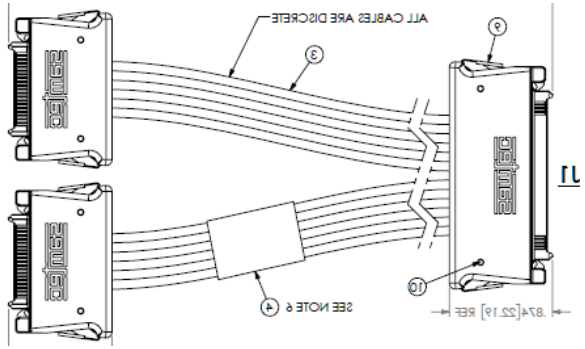
Data Cables – Lengths, types and quantities summary

PP1

PP2

PP3

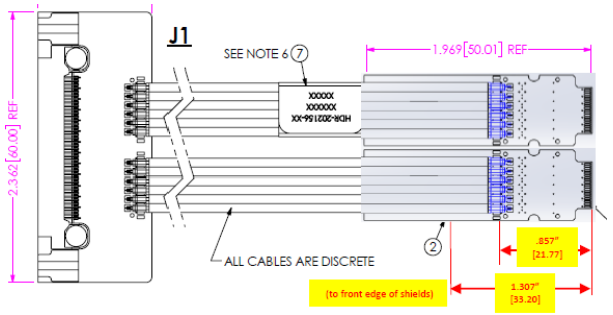
HDR-203194



Production quantities

Layer	Qty	Length
3,4,5	60 + 8	4300 mm
0,1,2,3,4,5,6	156 + 8	4800 mm
0,1,2,6	72 + 8	5300 mm
	312 + 24	

HDR-206142



Production quantities

Layer	Qty	Length
5,6	180 + 8	2150 mm
3,4	108 + 8	2450 mm
0,1,2	24 + 8	2650 mm
	312 + 24	

Data Cables – Batching

Batching has been devised to:

- Ensure inner layers can be tested with the final cables in the correct lengths as soon as possible
- Maintain a constant raw cable production rate (which is likely to be the limiting factor for production)

Type	Length	B1	B2	B3	B4	Total	Total
HDR-206142	2150			72	116	188	336
	2450	58	58			116	
	2650	32				32	
HDR-203194	4300		16	16	36	68	336
	4800	38	42	42	42	164	
	5300	32	36	36		104	
Raw cable length [m]		**1158**	**1207**	**1232**	**1212**		

CRU – RU to CRU mapping (from Paolo Martinengo) – 1

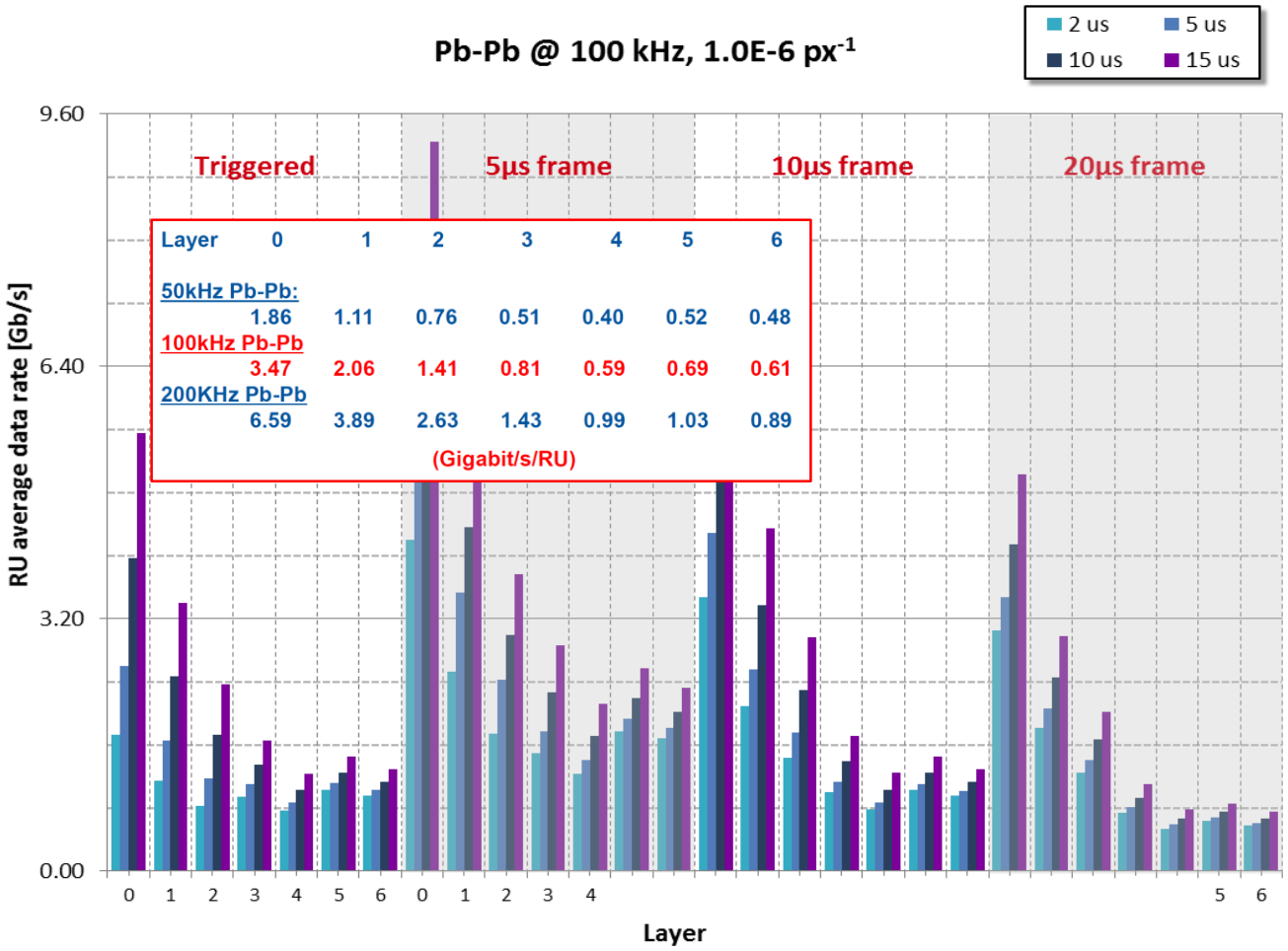
Parameters:
Bandwidth: data from RU to FLP, from FLP to EPN
Computing power available in each FLP node for cluster finding

The ALICE CRU has 24 optical inputs, 24 optical outputs
The RU has 3 optical outputs (data), 1 optical input (control)

We assume to connect 3 uplink fibers per RU, i.e. 8 RU/CRU
192 RU (48, 54, 90), 24 CRU (6, 6.75, 11.25)

1 optical link (up/down) has **3.2 Gb/s** bandwidth

	RU	CRU
IB	48	6
MB	54	6.75
OB	90	11.25
Total	192	24



Sylvain's simulation (to be updated) showed that 24 FLP, 1 CRU/FLP, load balanced can handle cluster finding, i.e. **8.26 Gigabit/s/FLP** is Ok

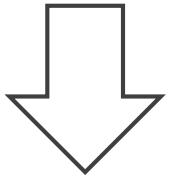
#FLP = #CRU

CRU – RU to CRU mapping (from Paolo Martinengo) – 2

Fibers come in bundles

RU are spread over a rather large distance/volume, i.e. we cannot freely mix, for instance, IB with OB in the same bundle

- Impossible to achieve load balance w/o introducing a patch panel
- It has been decided to have a patch panel in CR4 to have the possibility to connect any RU link to any CRU input



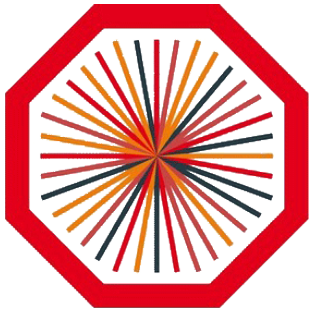
Introduction of patch panel as optical splitter provides the needed flexibility to balance the load among the FLP

MB & OB 2 fibers/RU, IB 3 fibers/RU

	RU/CRU	CRU		RU
L4, 5 ,6	12	10	2.5+3.5+4	120
L3	8	3		24
L2	6	4		20
L1	4	4		16
L0	2	6		12
Total		27		192

MB & OB 1 fibers/RU, IB 3 fibers/RU

	RU/CRU	CRU		RU
L4, 5 ,6	16	8	2+3+3	120
L3	8	3		24
L2	6	4		20
L1	4	4		16
L0	2	6		12
Total		25		192

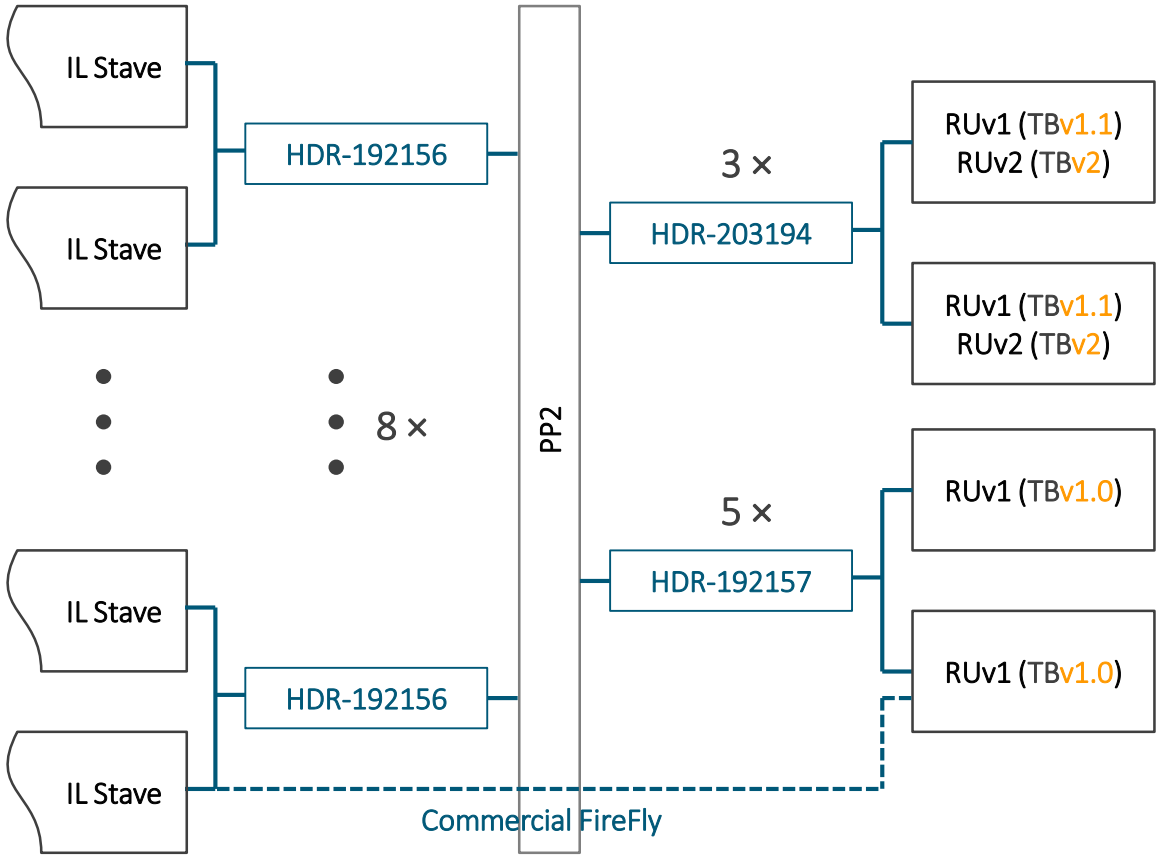


Surface commissioning

Data connection – Options for early commissioning with pre-production cables

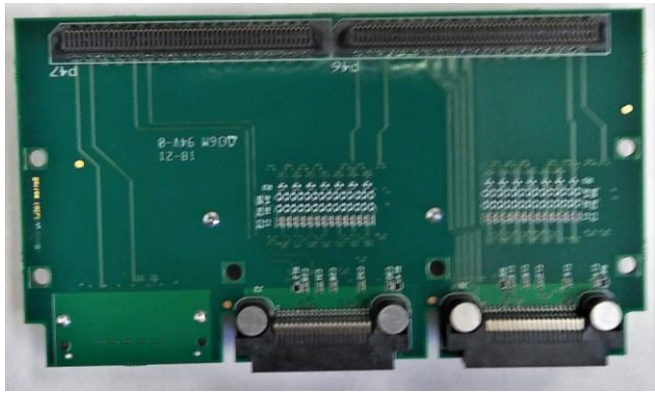
At the moment we have 8 PP2 to PP3 assemblies (HDR-192156), capable to connect 16 IB staves. From PP2 to PP3, we have prototype cables to connect:

- up to 16 RUv1 (likely 6-7 of them available for commissioning).
- Up to 6 RUv2, as they use the updated PP2 to PP1 data cable (HDR-203194)



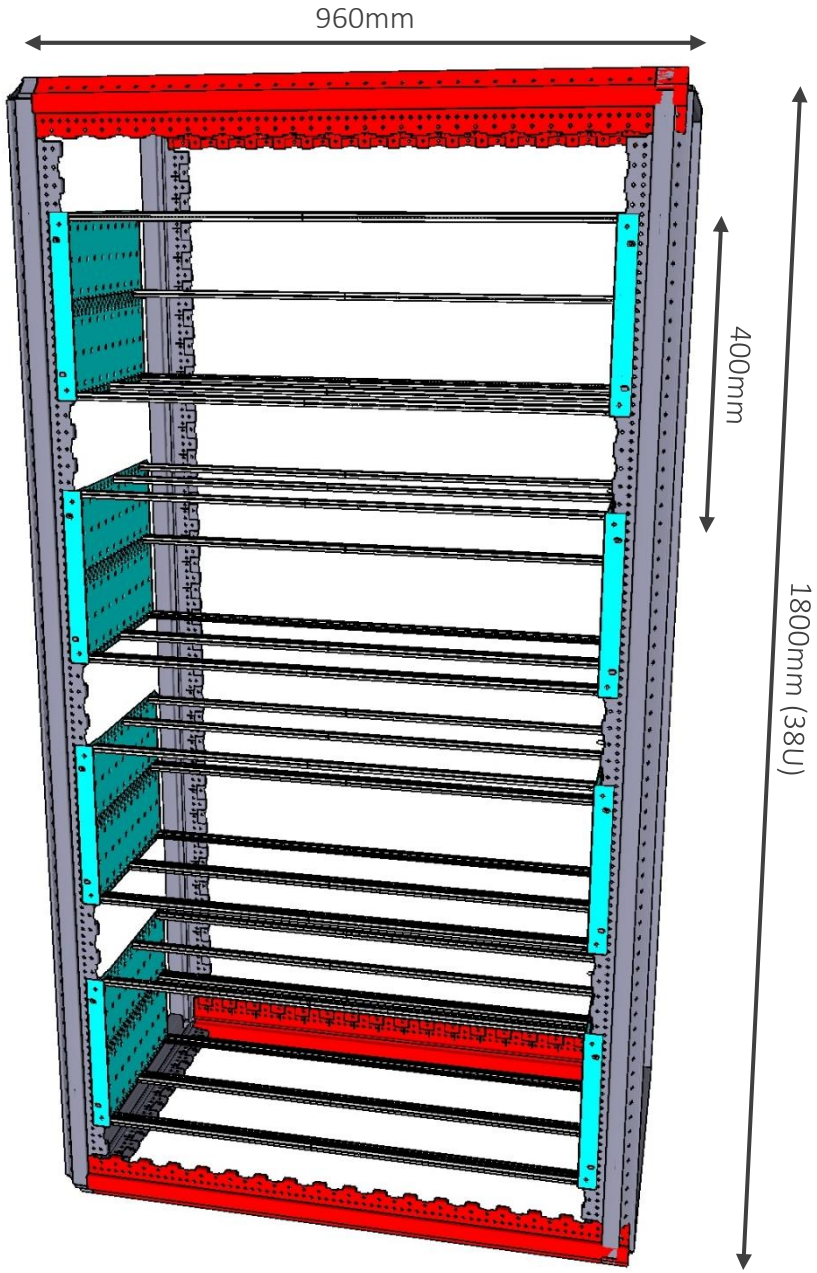
Transition Board v1.0 – compatible with RUv1.x and HDR-192157 cables (**and commercial cables**)

Transition Board v1.1 – compatible with RUv1.x and HDR-203194 cables



Transition Board v2 – compatible only with RUv2 and HDR-203194 cables

Racks – Proposed commercial solution

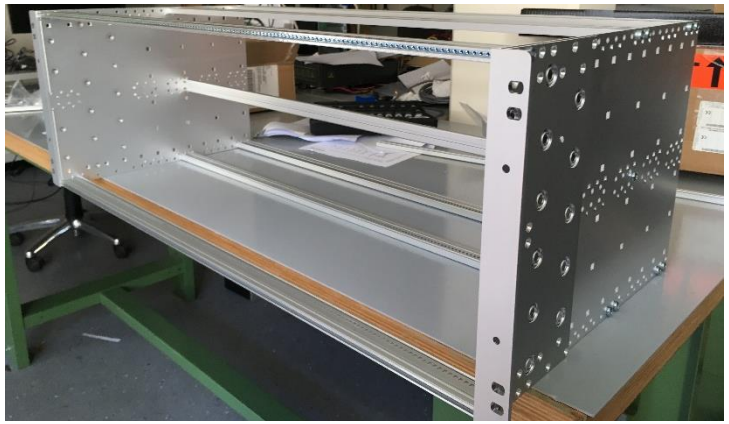


We buy catalogue available Schroff Varistar racks, 38 Units (1800mm tall), 600mm deep and 1000mm wide (actual crate clearance 817mm).

- Before assembly, we cut short by 39.6mm the 4 horizontal beams (red in picture, 896mm to 856.4mm), so to fit our 777.2 mm wide crates (H-H distance of 810.44 mm).
- We can choose between the **slim** and **heavy-duty** version.

Schroff CN 20130-048 **Schroff CN 20130-098**

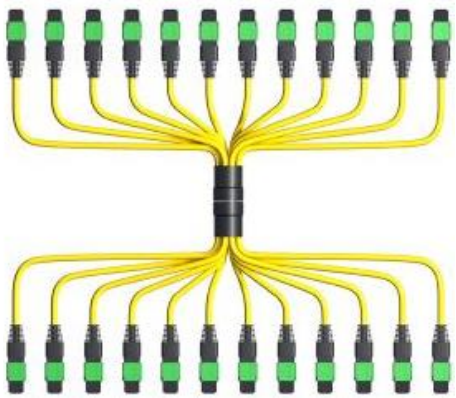
- **Waiting quotes**



Fiber optics – Trunk cables + patch cords

Main trunk cables (identical specs of cavern installation)

- **2 ×** Trunk cables (30m long), OM3, MPO-**M** (144 fibers in 12 MPO-**M** terminated bundles)



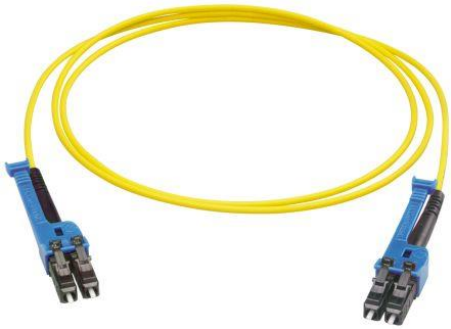
Trunk cables to CRUs connection (MPO to MPO constraint)

- **4 ×** Patch cord (5m long), OM3, MPO-**F**(12 fibers) to MPO-**F**(12 fibers)

Trunk cables to RUs connection (LC ending, single channel pluggable)

- **4 ×** Patch cord (5m long), OM3, MPO-**F**(12 fibers) to 12 × **LC**

- **4 ×** terminal panels for crates installation
- **3 ×** Single mode (trigger) LC-LC long cables



Material expected by July 2nd, testing of all components booked, components availably by July 6th (July 9th)

ITS Readout Electronic – Status summary

RUv1/v2

- RUv1 production/commissioning complete
- RUv2 prototyping ongoing: components procurement solved so far, in production this week
- RUv1.1 can substitute RUv2 in every practical detail, yet not many available: could be worth extending RUv2 prototyping to 8 units (from present 4)

Data cables

- Electrical test of final prototypes successful.
- Design finished, waiting final confirmation from Samtec.
- Final cable lengths frozen.
- Tendering document ready, batching devised.

Surface commissioning

- Trunk cables (2 × 30m O3 144 fibres) ordered.
- Patch cord (4 × 5m 12 fibers MTO-LC) ordered.
- Patch cord (4 × 5m 12 fibers MTO-MTO) ordered.
- Likely 6 RUv1.1 available for early testing.
- Racks solution devised, to be refined and approved.

Firmware / CRU connection

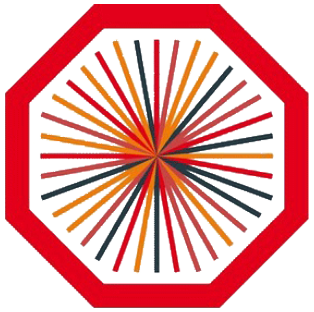
- Full readout chain completed, IB & OB
- Trigger handler with proper responses completed
- Triplication of key elements ongoing
- PA3 firmware redesigned including protection
- Initial CANbus interface (WB master) in simulation
- CRU protocol & Trigger responses under discussion

Production testing system

- Test system for RUv2 production under development
- First hardware prototypes and early firmware parts being evaluated/tested in Austin & Utrecht
- Testing plan, procedures and resources allocation in advanced state of definition.

Test beams

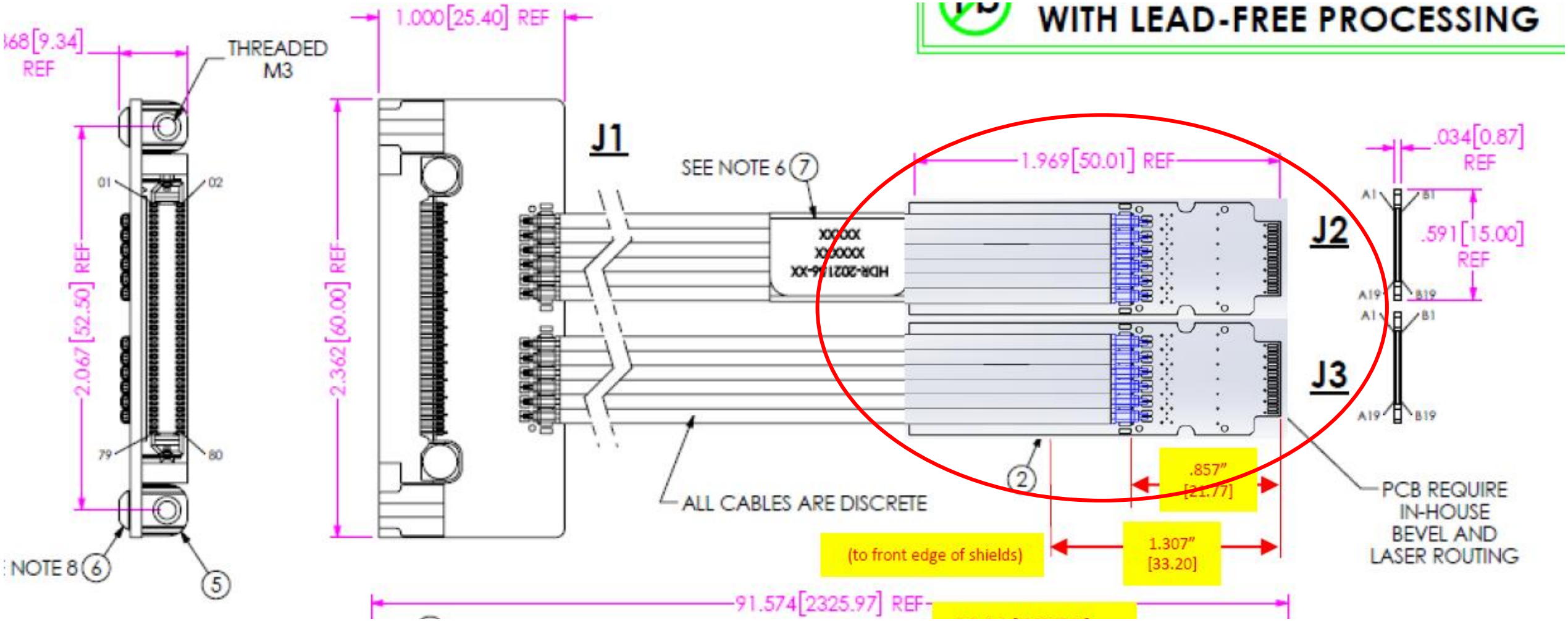
- Prague test beam changed into table-top injection, which started past week.
- CHARM test being will start in early July, with full system validation.



Backup

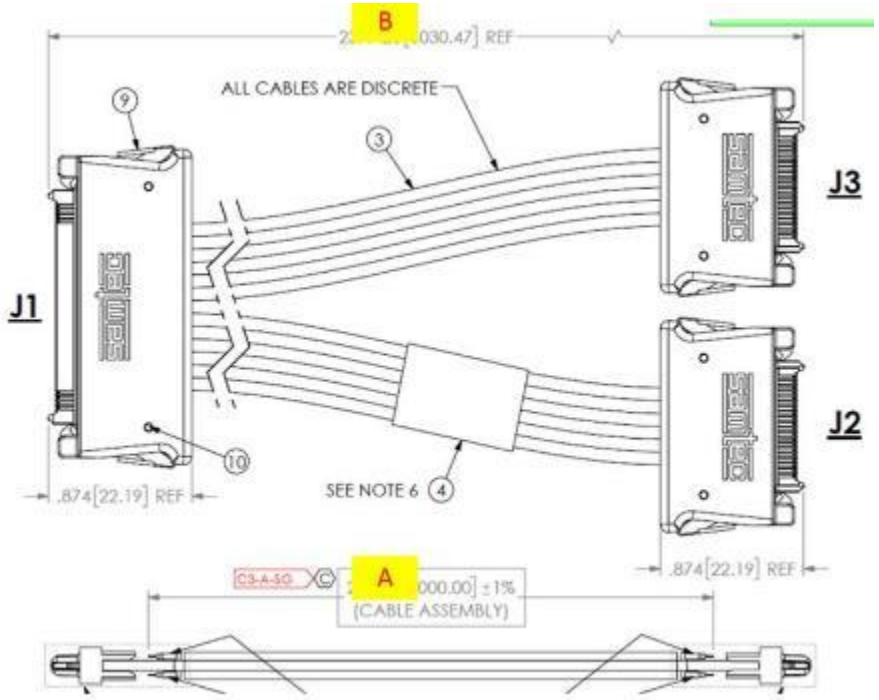
Links – Data connection End Wheel last update

Glue outflow in current prototype of the end-wheel connector PCB prevent it from correctly latching into the guide.
Latest version has the **soldering point moved 21mm from the PCB front edge** (was 7mm).

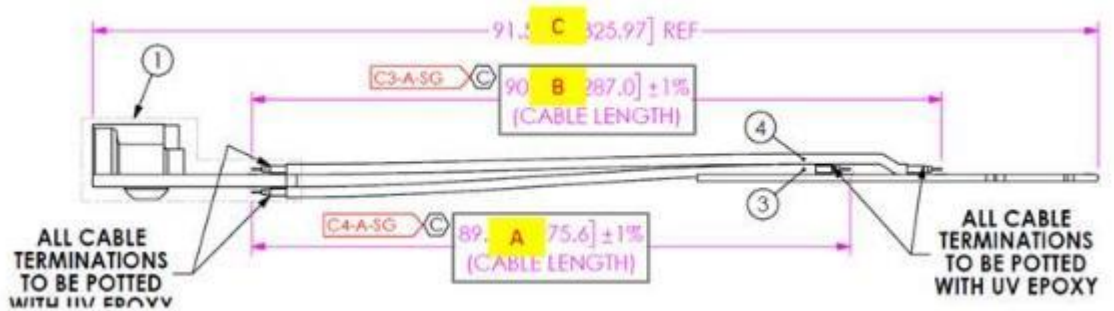


WP10 – Data cables length measurement specification

HDR-203194



HDR-206142



Testing – Overview

- A total of **222** boards will be manufactured for the ITS (88 for MFT not considered here)

- Testing will be done in a 2+ stage approach:

1) Hardware testing at the manufacturer (only functional smoke test).

2) Board bring-up, initial hardware verification and short-term functional verification at Nikhef/Utrecht.

+) Long-term functional testing at collaborator sites (sampling) & during commissioning.

Testing – Testing at the manufacturer site

Test described here will be performed by the manufacturer before shipment. The manufacture will compile a test report for each board and attach it to board itself, in addition to providing it in electronic form.

- PCB Testing:
  - Visual inspection (metallographic cuts, thickness of board, …
  - Electrical Connectivity Test (flying probes test)
  - Controlled Impedance Testing

  } See tendering document for details

- Assembly Testing:
  - Correct placement of parts
  - Soldering Quality
  - X-ray of BGAs
  - Automated Optical Inspection (AOI)
- Install all jumpers (~10 jumpers; make sure FX3 is powered as well)
- Testing for shorts (with multi-meter)
- Initial powering:
  - Specify the test points for measuring 7 on-board voltages.
  - Measure total current on power supply.
  - Measure output of sense amps (test points) to determine currents.

  }
  - Verified procedures currently on use
  - Detailed documentation available
  - Easy for the manufacturer to implement

- All inspections will be in accordance with IPC-A-610 Class-2 specifications

Testing – Acceptance testing at Nikhef/Utrecht

The second test step will happen at Utrecht/Nikhef, with the Rus undergoing extensive electrical and functional testing.

- Power on and check total current
- Verify I2C bus for GBTx configuration; fuse all GBTx chips
  - Program GBTx0
  - Verify that we see all 3 GBTx chips
  - Fuse all 3 GBTx chips with special software and special cable
- Read out Voltages, Currents, and temperature values via SCA
- JTAG configuration of Ultrascale & Microsemi FPGAs
  - Verify push buttons & LEDs & dip switches
  - Pin Headers: maybe a loopback test with a loopback cable?
- Check FX3/USB3 interface:
  - Use Cypress USB “Control Center” application to verify connection over USB
  - Use Control Center to program FX3 boot PROM
- Jitter cleaner test
- Short-term functional testing (**see next slide**)
  - Read DNA from US, store in database
  - Read flash ID, store in database

Time estimate:
≈1 hour per board × 222 boards = **45 days**

Testing – functional testing details

Most of this can be done at Nikhef during acceptance testing; only long-term BER type tests to be done separately

- **JTAG**: Program testing firmware to 2 FPGAs via JTAG; verify running firmware (e.g. blinking LEDs)
- **USB:** verify communication between host computer & FPGA via FX3
- **I2C**: generate PRBS pattern @200kbps on 8 outputs (SCL_w, SDA_w), receive on 8 inputs (SCL_r, SDA_r)
- **GBT**: GBT_FPGA on test board, generate PRBS on TX, receive PRBS on RX
- **Alpide Data lines**: Transceiver IP with 28 RX; generate 1.2Gbps test pattern with OSERDES @ 600MHZ DDR; receive PRBS on Transceiver RX
- **DCTRL, DCLK**: Generate 80Mbps PRBS on DCLK; receive PRBS on DCTRL
- **BUSY**: Loopback PRBS patterns from OUT to IN, using transceivers?
- **PA3-Flash I/F**: Read Flash ID; read & catalogue "bad blocks" (all blocks, **takes a long time**? Ask Johan how long)
- **"Serial Number":** Read and catalogue UltraScale FPGA DNA value as unique identifier for Readout Unit
- **CANbus:** Connect USB CAN dongle to host computer, send and receive simple CAN packets @ 1Mbp
- **Ultrascale-PA3 I/F**: Send & receive test patterns
- **SelectMap I/F:** PA3 reads US SelectMap ID

Testing – hardware & firmware

Testing hardware (other than external commercial instruments and supplies) will be limited to passive boards, a commercial devkit and adapters. Testing firmware will be an evolution of present test suites used for RUv1.x verification. It will be entirely based on present RU firmware (wishbone bus) to limit development effort.

Hardware elements

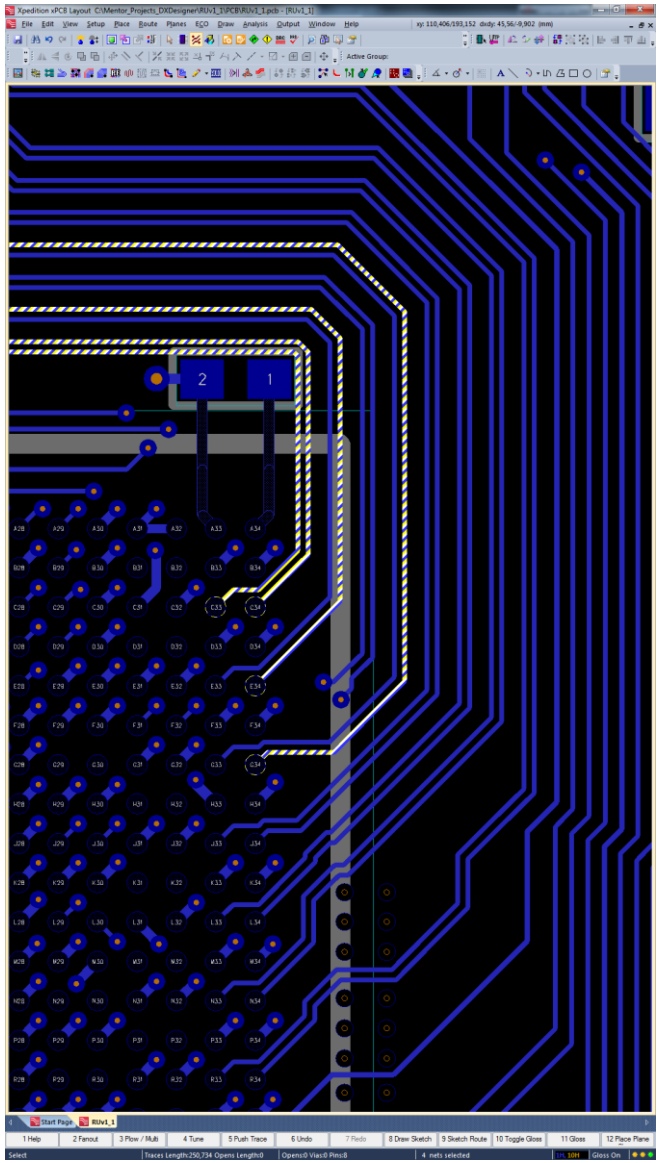
- Loopback board for transition board (to replace transition board, **Austin**)
- Loopback cable for power mezzanine: connect I2C outputs on one connector to I2C inputs on second connector
- Adapter board to connect 2 firefly cables to one 9 input cable (for Austin transition board testing?)
  - Need ERF8 type connectors on cables
  - Alternatively: use Marcel's FMC to firefly board to connect to a FPGA dev board
- Aux connector loopback cable
- Pin header loopback cable
- FPGA board with at least one SFP for GBTx testing, possibly also with FMC connector for Marcel's FMC board for transition board testing

Firmware tasks assignment

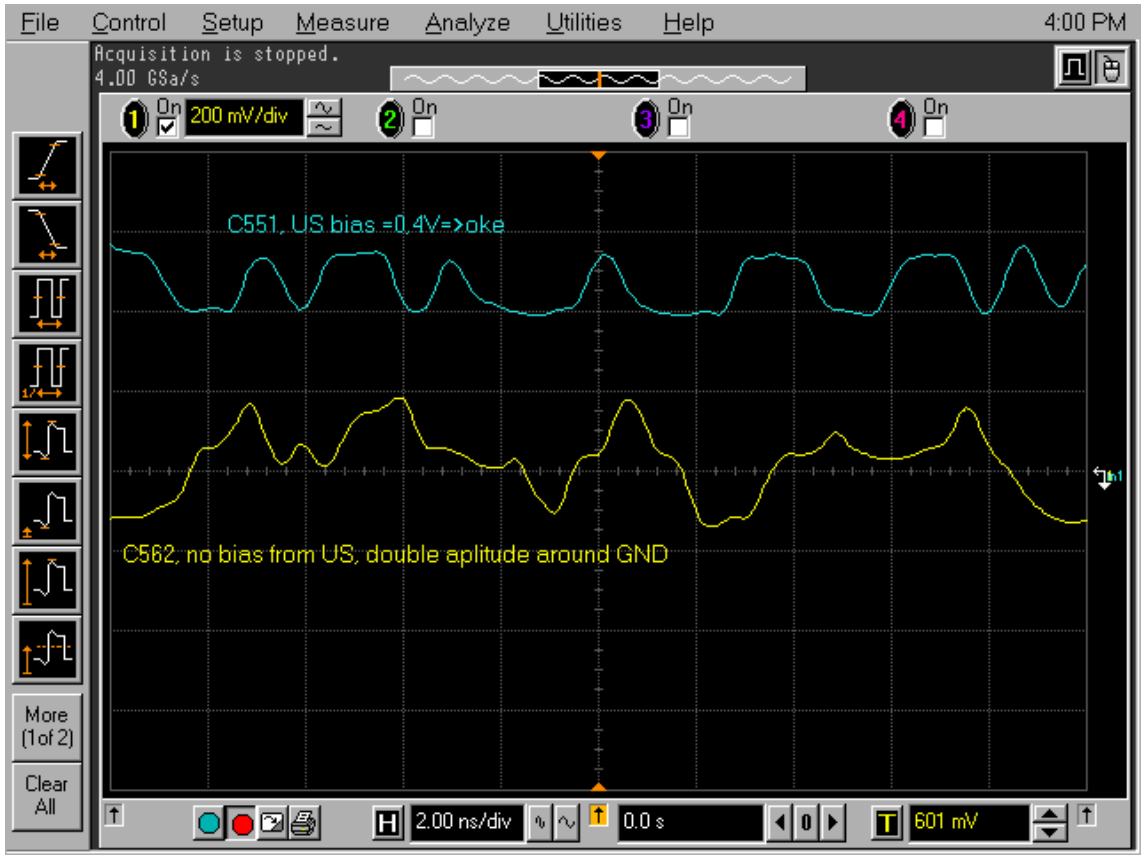
- PA3-US loopback pattern generator (Jan-David)
- Pattern generator for pin header loopback (Jan-David)
- Pattern generator for Aux connector loopback (Jan-David)
- Pattern generator for power mezzanine loopback (Jan-David)
- Test System firmware to test Alpide data on transition board (Jo)
- PA3 readout of bad blocks (Bergen)

Testing – early result of prototype loopback hardware

Early testing development in Austin/Utrecht did prove successful in spotting mounting issues in one of the **RUv1.1**:



- **Test with loopback-board showed error on one board**: RUv1_1 SN9 on channel DATA_MGT_4, 6 and 7.
- First suspect 208-pin Samtec QMS connector => scope showed that the LVDS signals were present up to the MGT AC decoupling capacitor. However, on MGT side, DC bias not present (& double amplitude) on:



Channels affected shown here. Not used for ITS-IB (**the board is good for us**).

- RUv1_1 SN9 likely badly soldered
- Board passes all other tests including PRBS tests with the (Focal) module
- RUv1_1 SN9 can be used for ITS, but not for MFT & sPhenix and

Test beams – Overview

- Decided to skip test beam in Prague: the same results can be obtained with table-top error injections, saving resources which have been allocated to RUv1.1 firmware development and to CHARM test beam preparation.
- Table-top injection starting this week, Shiming (Bergen) involved in the task. Scope of the test (will last about 1 week to get enough statistics) is to verify the hardening improvements in the firmware, implemented following the suggestions gathered at the PRR.
- For the full system hardware validation we will have a test beam at the CHARM facility at the beginning of July, with the full chain in the radiation area: Readout Unit, Staves/Modules and the Power Board. Only connection will be the optical one.