



Readout Unit Overview

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- Based on **ALICE ITS Upgrade** electronics
- **Requirement:** Less than 5% additional dead time @ 15 kHz average trigger rate and simulated occupancy
- Same Readout Units as ITS, but different **Data Aggregation Module** (ATLAS FELIX)
- Trigger Rate: 15 kHz
- **Comparison ITS – MVTX:**
 - Peak Au+Au collision rate: 200kHz (sPHENIX) : 50kHz (ALICE)
 - Peak p+p collision rate: 13 MHz (sPHENIX) : 200kHz (ALICE)
 - Event size, dN/dy : sPHENIX = 1/3 ALICE(pp), 1/5 ALICE(AA MB), 1.1 ALICE(AA central)
 - Trigger/readout rate: 15kHz (sPHENIX) : 50kHz (ALICE)
 - Expected average data rate: MVTX = 30% of ALICE (mostly central AA events, lower trigger rate)



- Hardware
 - 48 ALICE ALPIDE Staves + Interface Cables
 - 48 Front End Electronics (ALICE RUv2)
 - 6 Back End Electronics (ATLAS FELIX v2.x)
 - 6 EBDC server
 - 24 Power Boards + Supplies + Cables
 - 48 Stave to RU cables
 - 144 data fiber optic cables (3 fibers x 48 FEE)
- Electronics Spares ~20%
- Stave Spares ~75%



Readout Unit Design



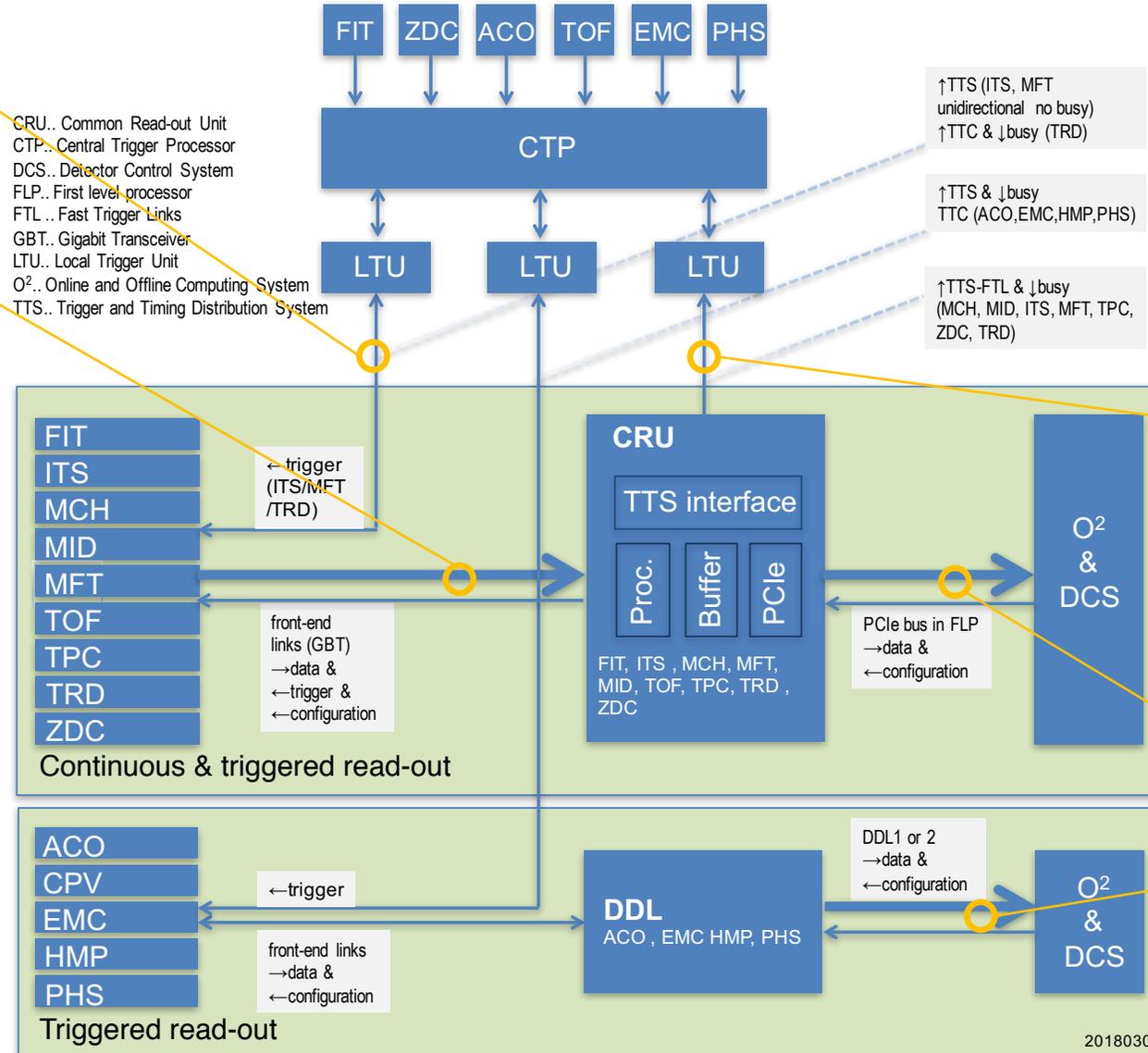
ALICE Readout and O2 System Overview



GBT & TTC
(192 + 80) & 1

GBT data links
(9215)

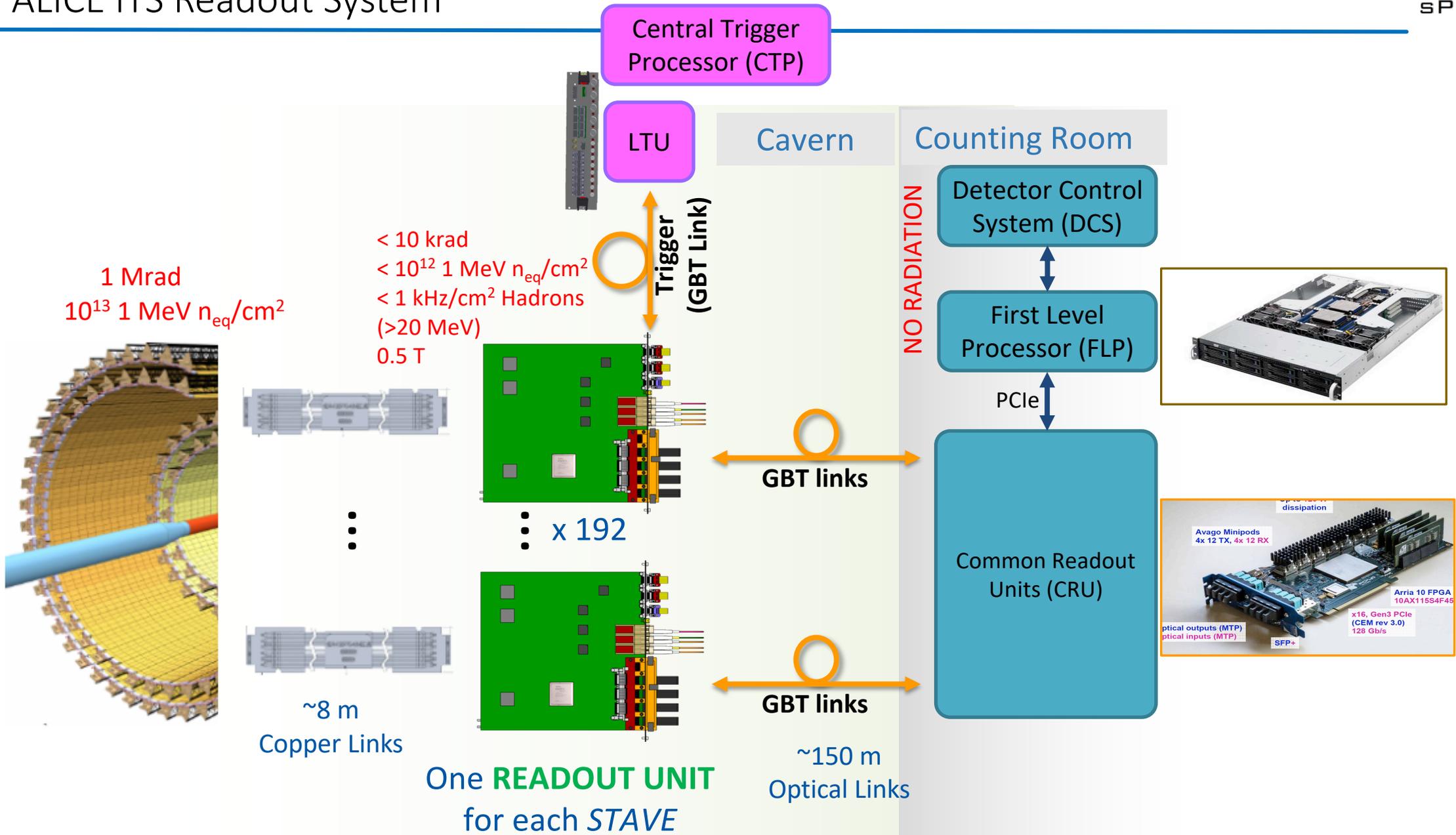
Trigger links
(4039)

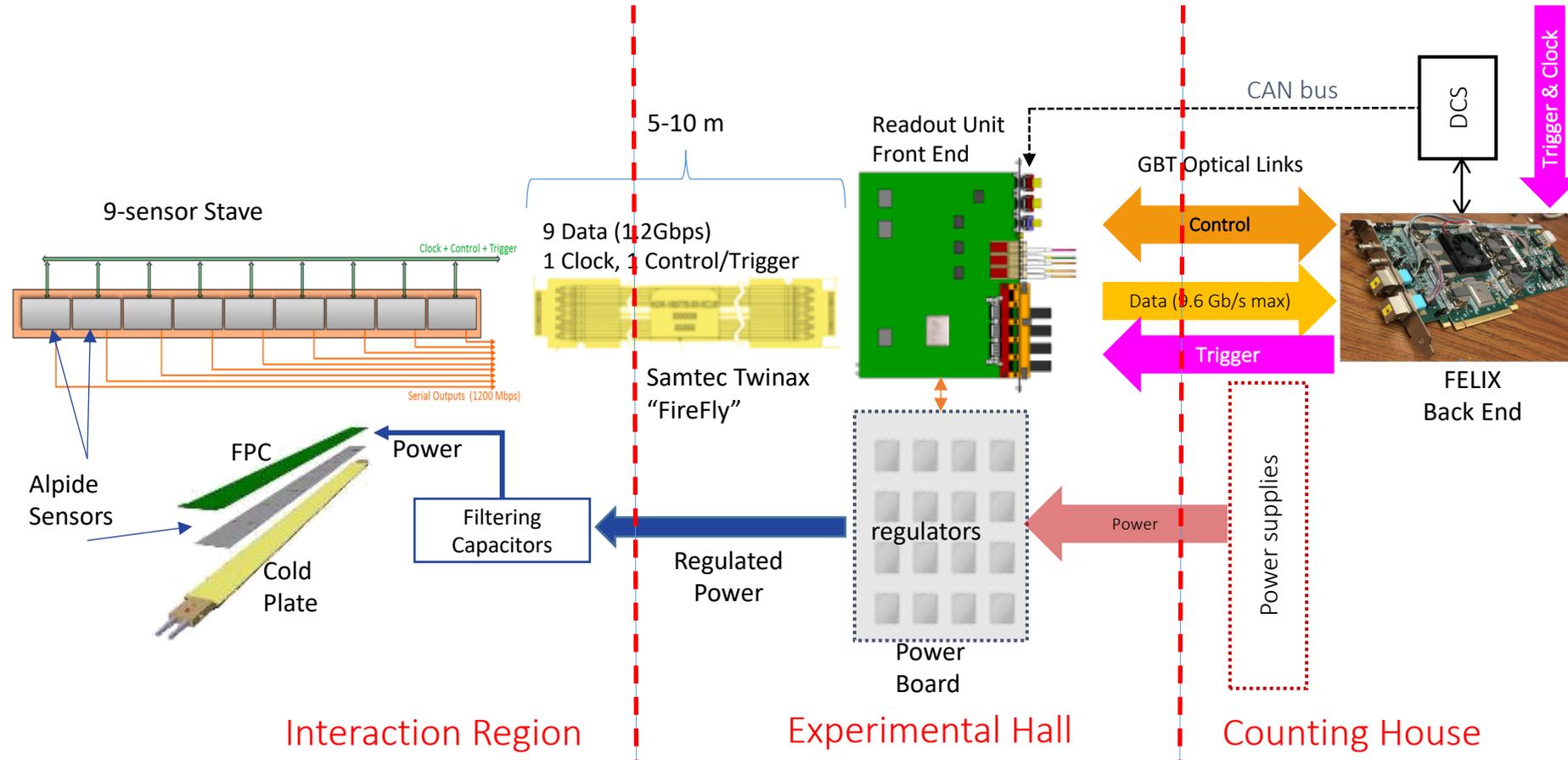


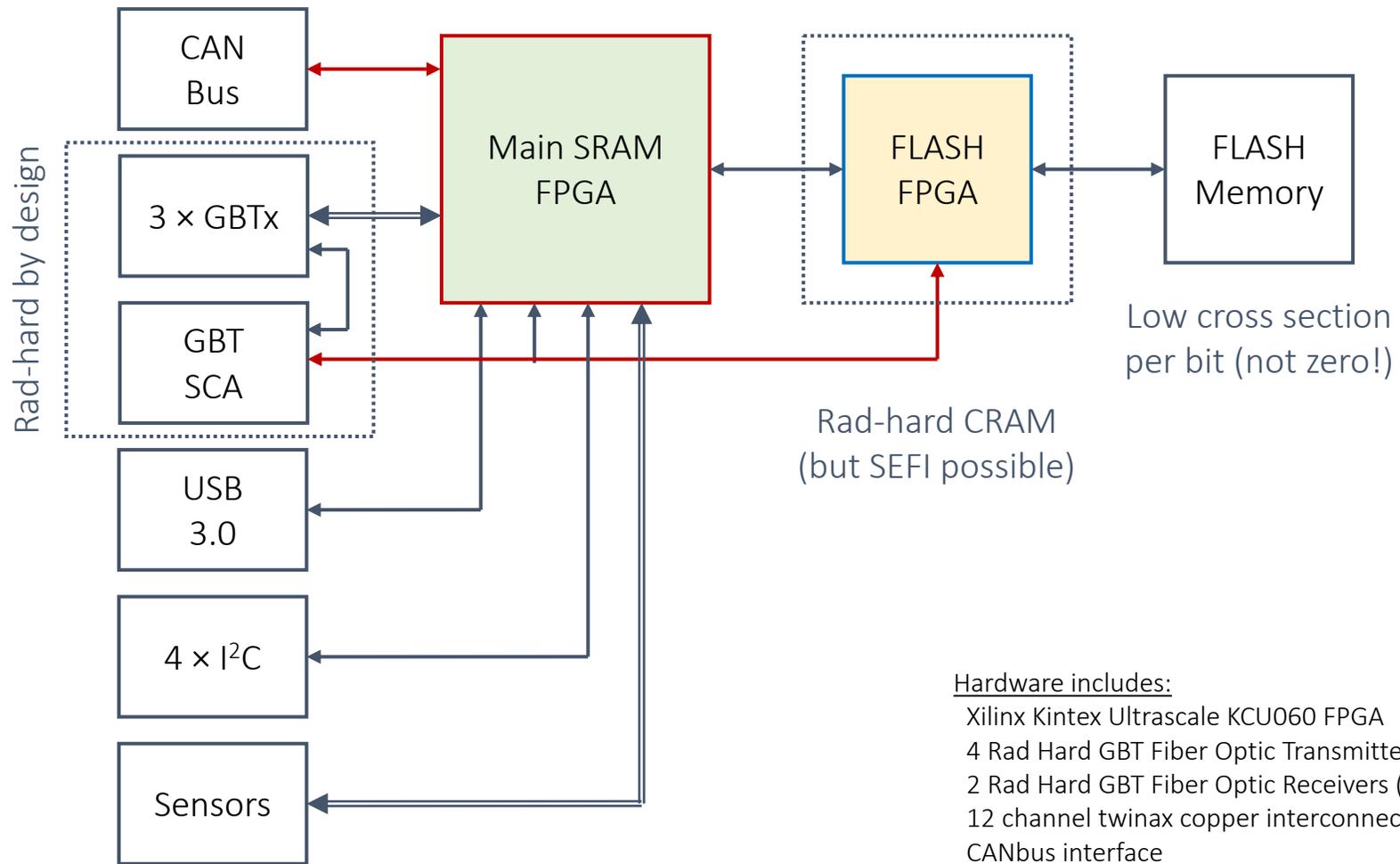
PON TTS links
(500)

PCIe

20180307



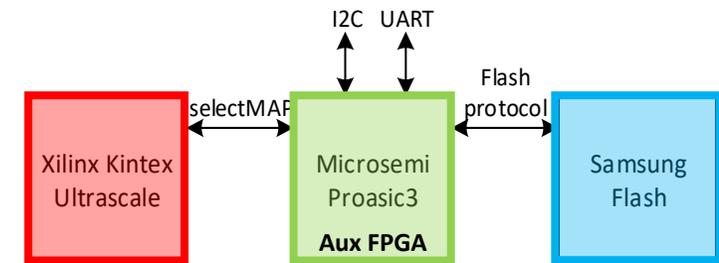
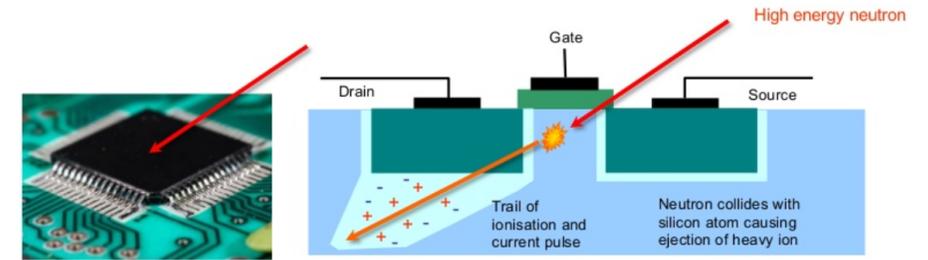




Hardware includes:

- Xilinx Kintex Ultrascale KCU060 FPGA
- 4 Rad Hard GBT Fiber Optic Transmitters (3.2 Gb/s)
- 2 Rad Hard GBT Fiber Optic Receivers (3.2 Gb/s)
- 12 channel twinax copper interconnects to stave CANbus interface
- Power board control interface

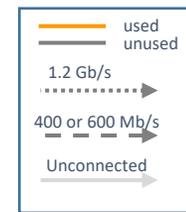
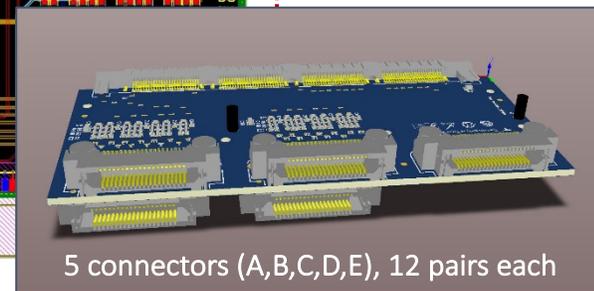
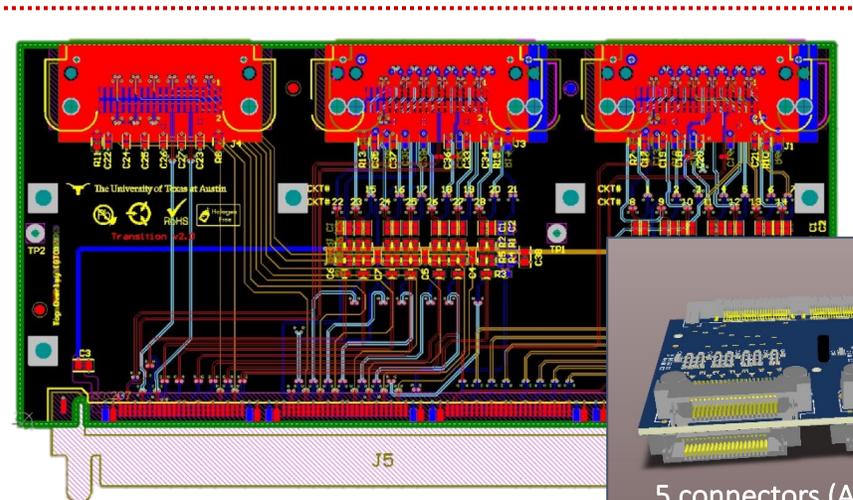
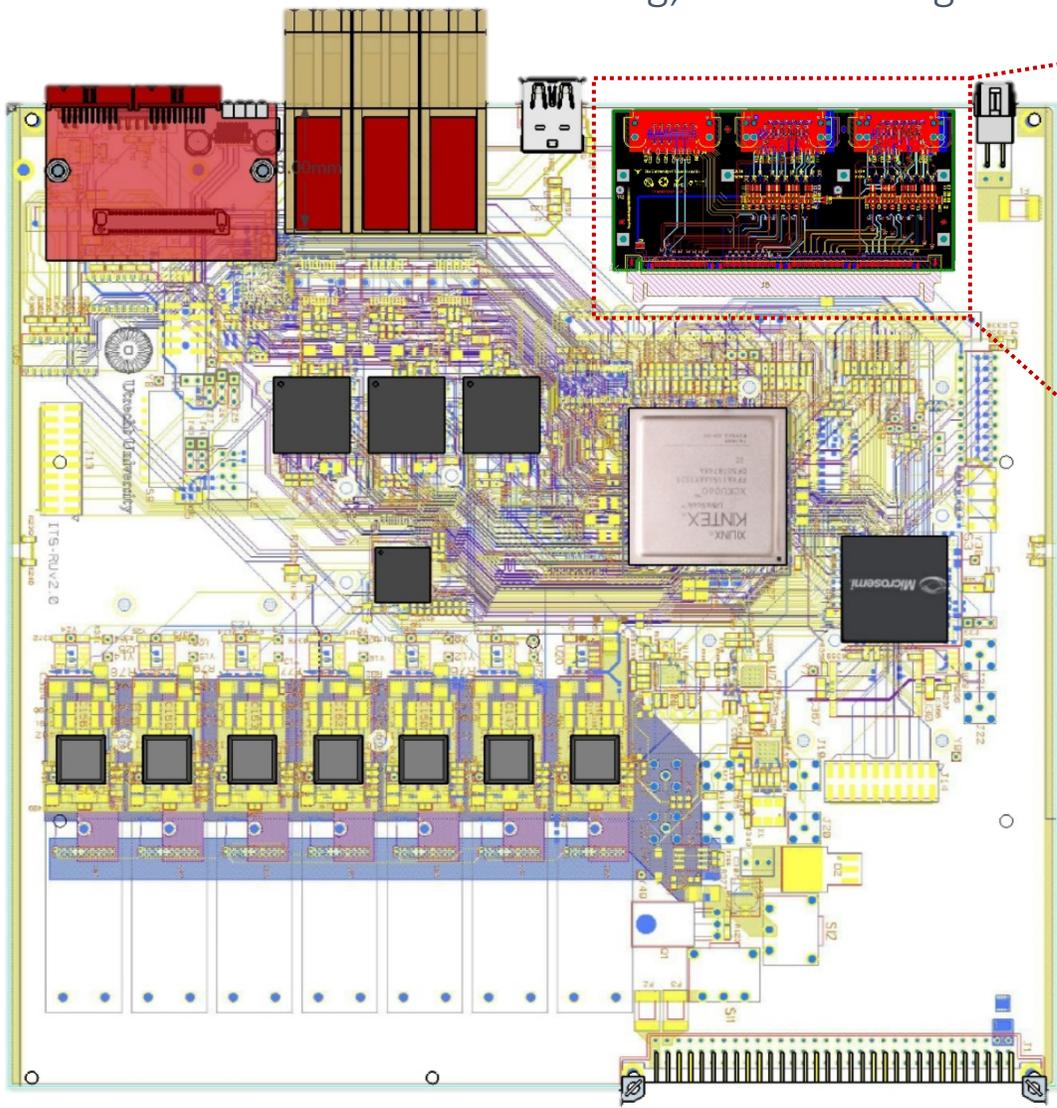
- Scrubbing is an error correction technique that uses a background task to periodically inspect/correct errors in a data memory.
 - Data memory = Config mem of Xilinx Ultrascale
 - Errors caused by single event upsets
- Relevant scrubbing techniques for the RU:
 - Xilinx Soft Error Mitigation Core (sem IP) ¹
 - Supported by Xilinx
 - Detection and correction
 - Fast
 - Black box design
 - Sem IP core only partially mitigated
 - Scan starts from zero upon an upset
 - External Scrubbing network
 - Proven solution (ALICE TPC RCU) ²
 - Full control of design
 - No support by Xilinx
 - Substantially slower than sem IP
 - Mitigation of Flash and aux FPGA is needed



¹ https://www.xilinx.com/support/documentation/ip_documentation/sem_ultra/v3_1/pg187-ultrascale-sem.pdf

² <https://cds.cern.ch/record/1141616>, chapter 4

- The RU must comply with MFT and sPhenix specifications, which require using 25 and 27 GTX lanes, respectively, for reading the sensors. To solve the routing, an interchangeable mezzanine card solution (**Transition Board**) has been adopted.

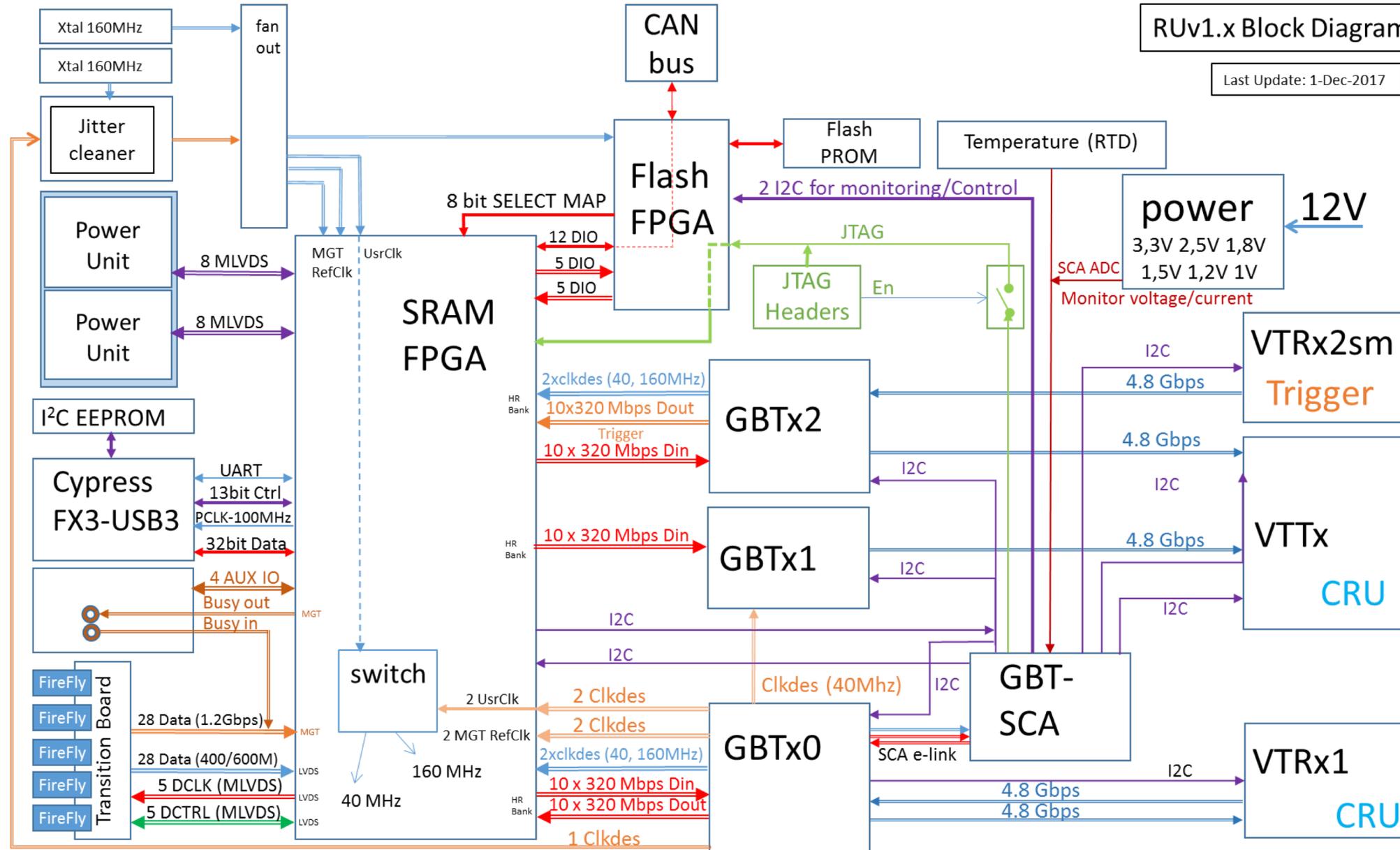




Readout Unit – Detailed Block Diagram

RUv1.x Block Diagram

Last Update: 1-Dec-2017

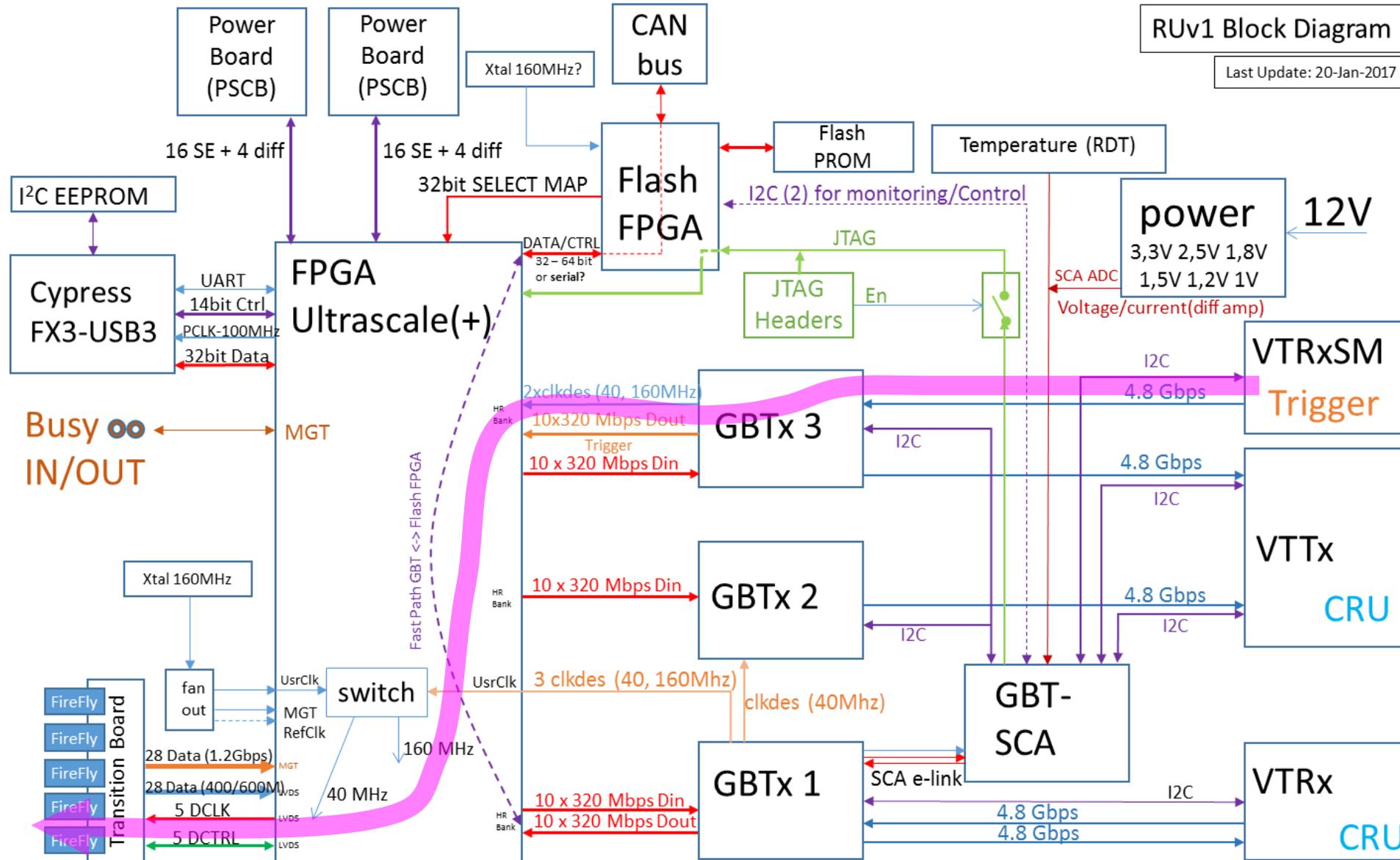




Readout Unit – Trigger Path

RUv1 Block Diagram

Last Update: 20-Jan-2017



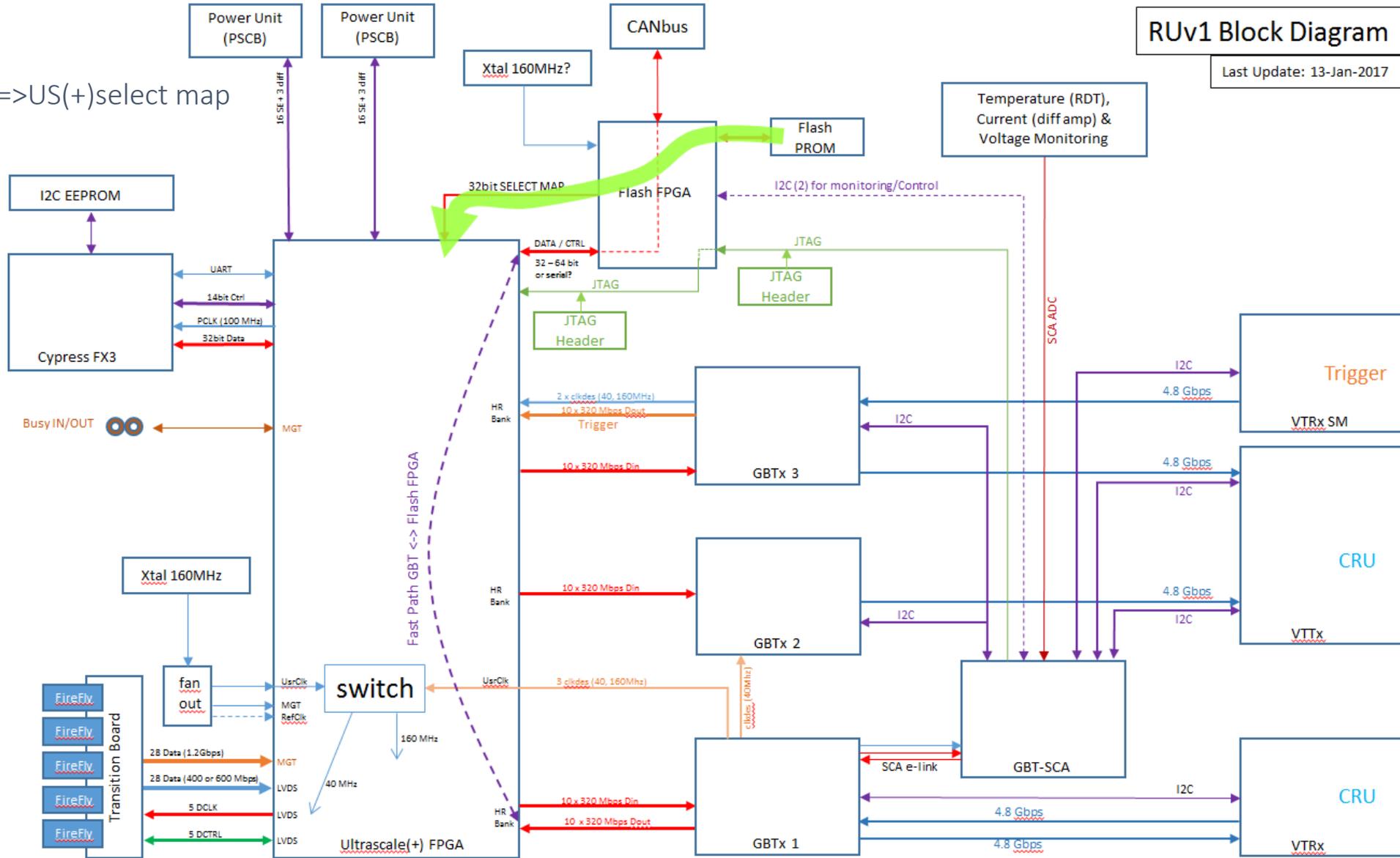


Scrubbing via Flash FPGA

RUv1 Block Diagram

Last Update: 13-Jan-2017

Flash Prom=>PA3=>US(+)select map

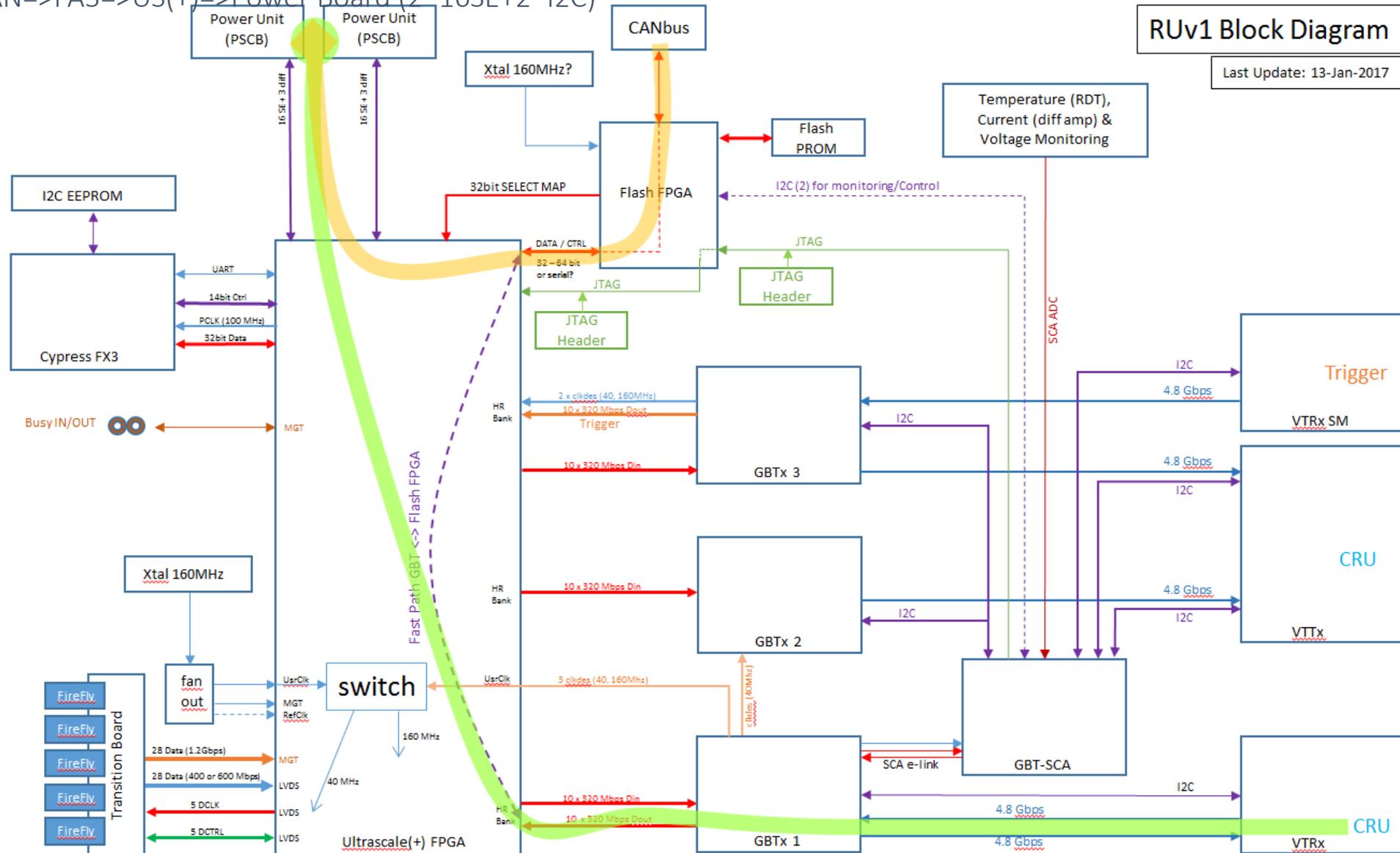




Power Unit Control via GBT or CANbus



- Main: CRU=>GBT=>US(+)=>Power Board (2*16SE+2*I2C)
- Alternative: CAN=>PA3=>US(+)=>Power Board (2*16SE+2*I2C)





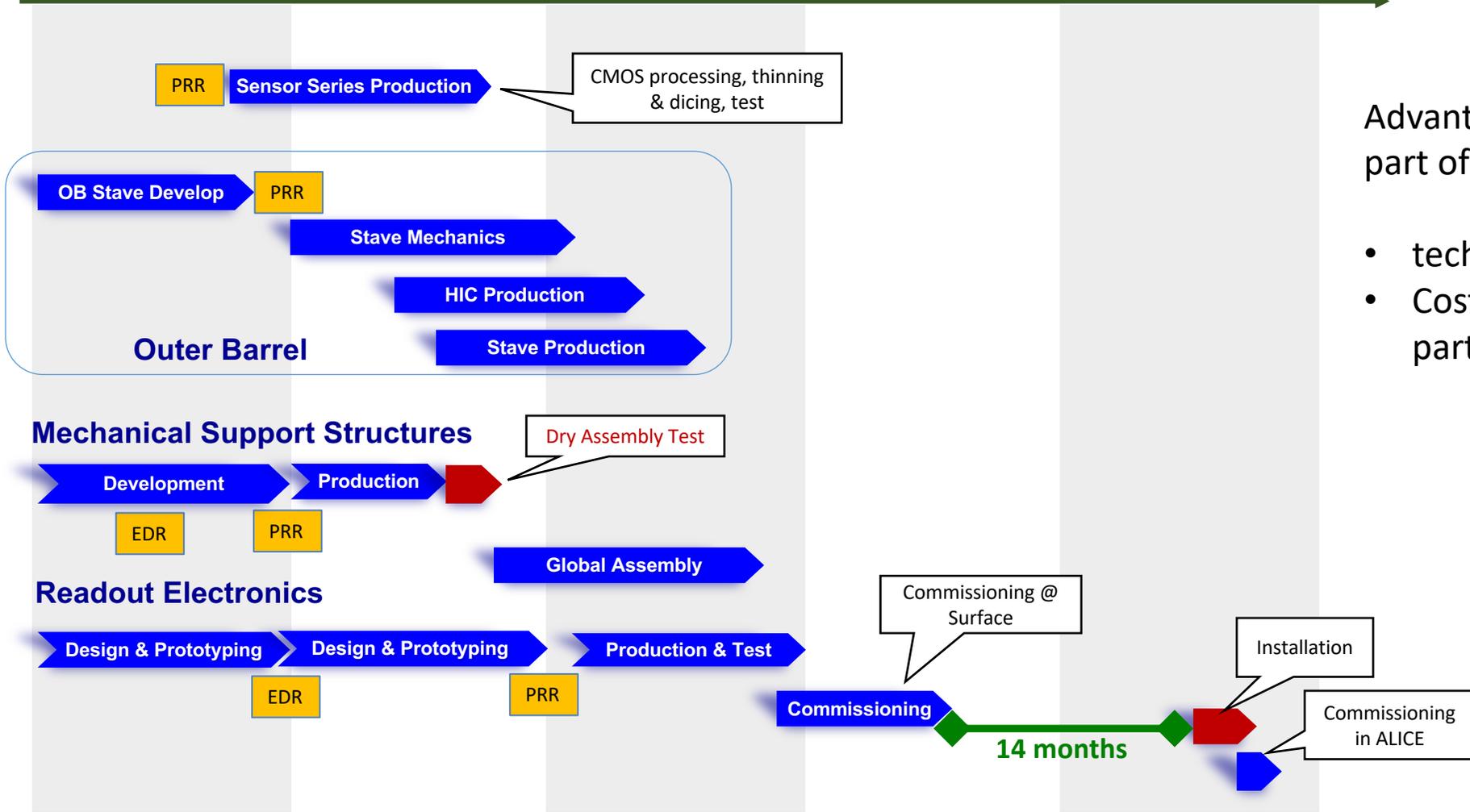
2016

2017

2018

2019

2020



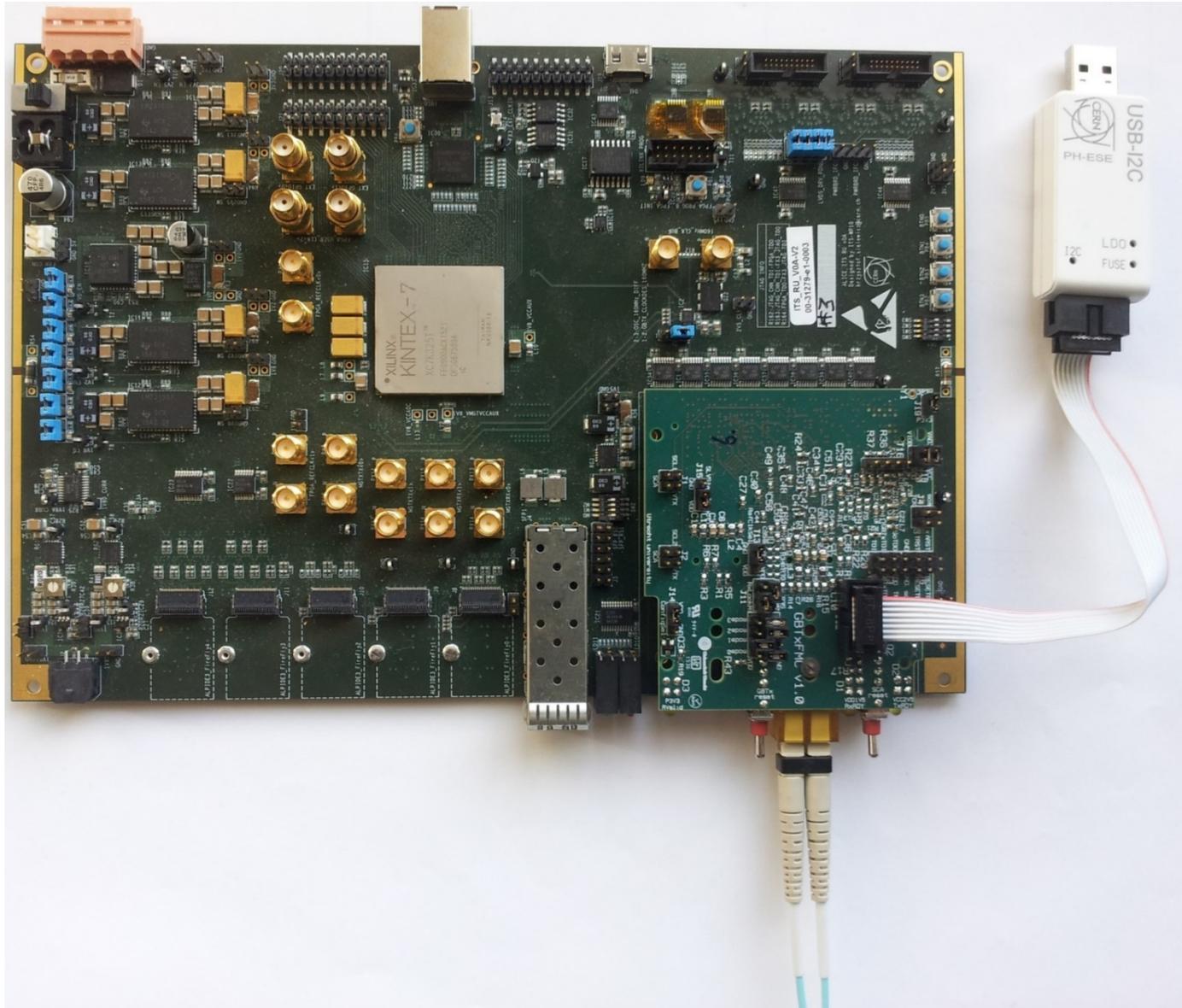
Advantage of fabricating MVTX RUs as part of the ITS RU production:

- technical risk can be reduced
- Cost savings due to the volume of parts of as much as 50%

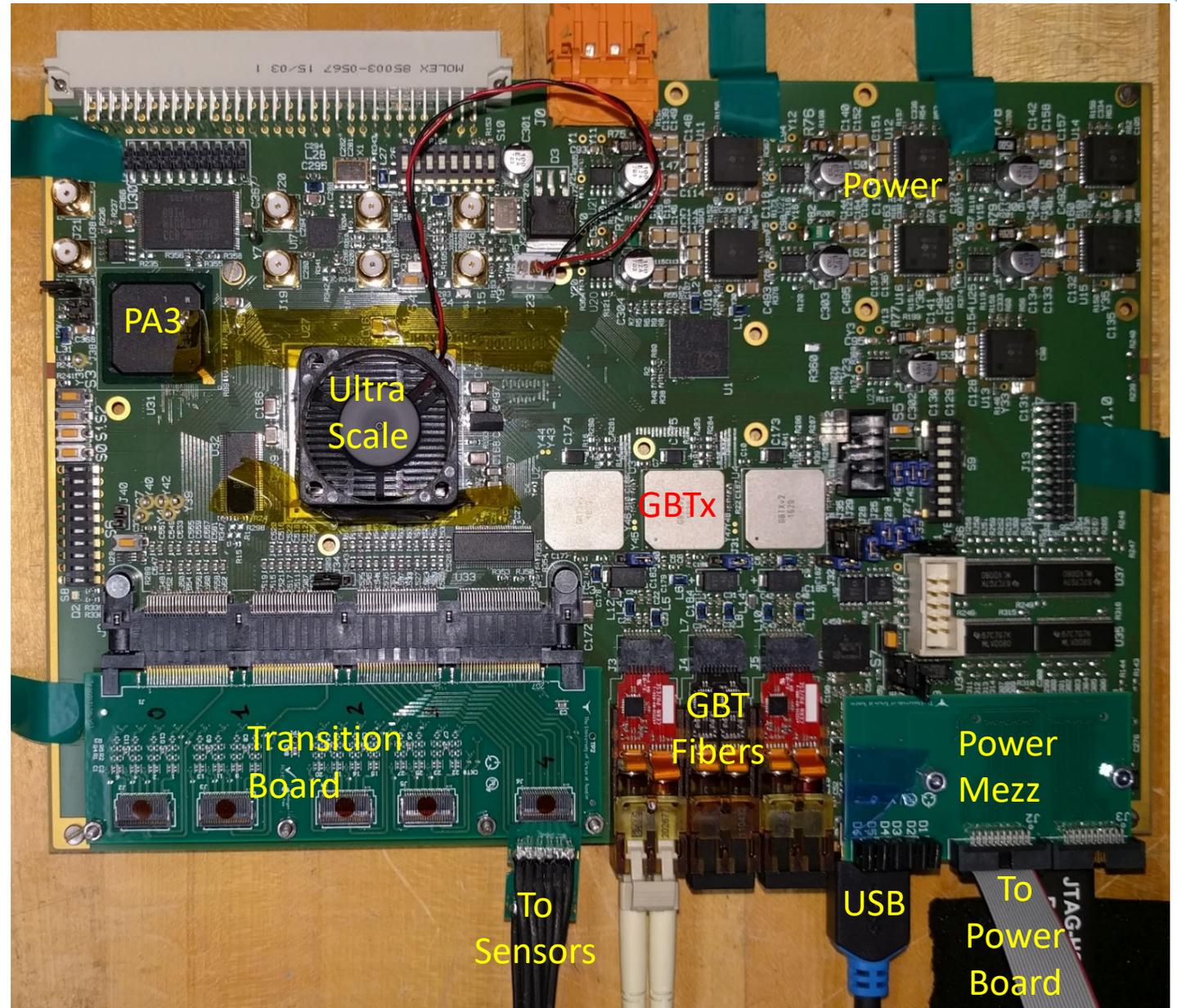


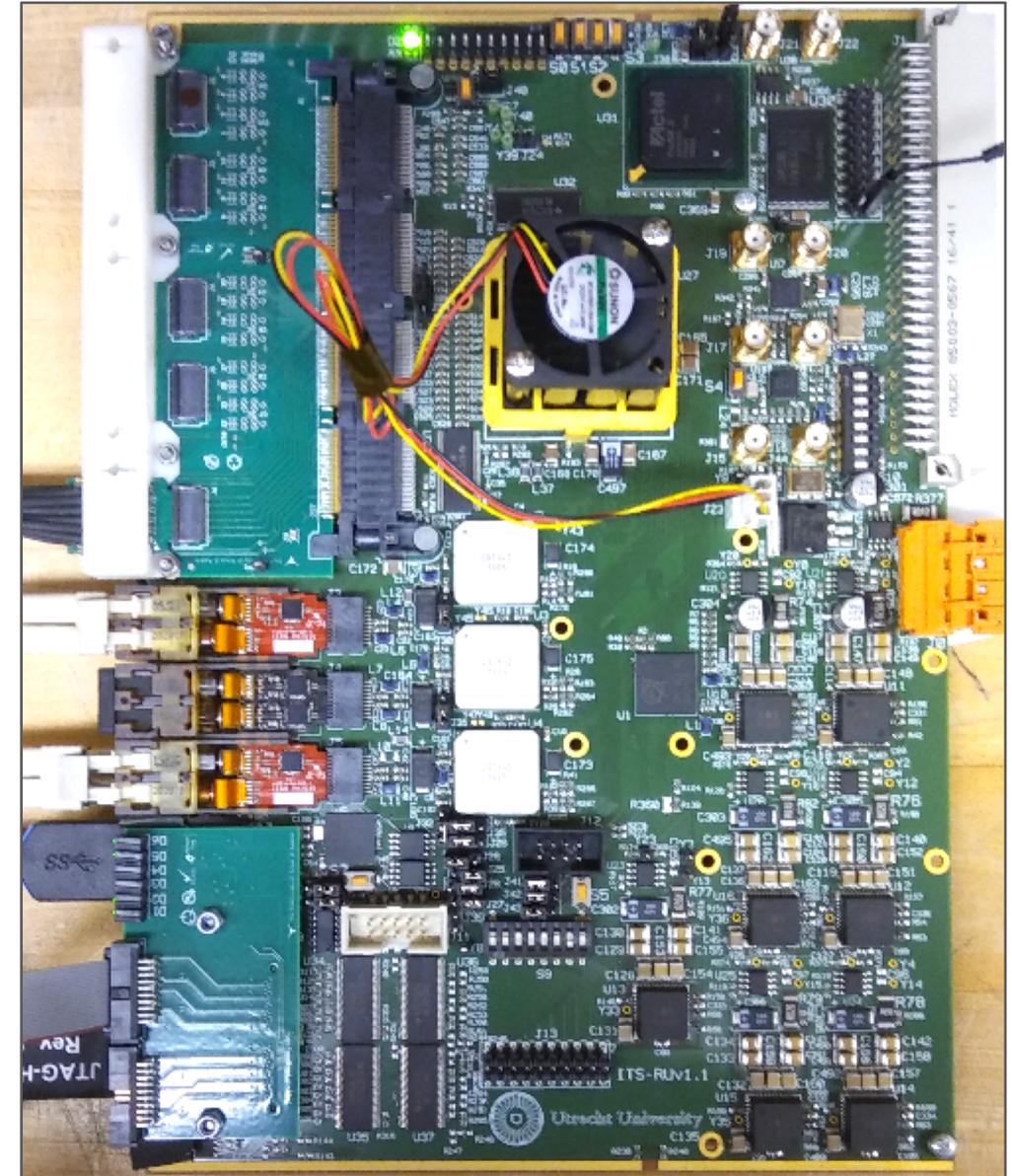
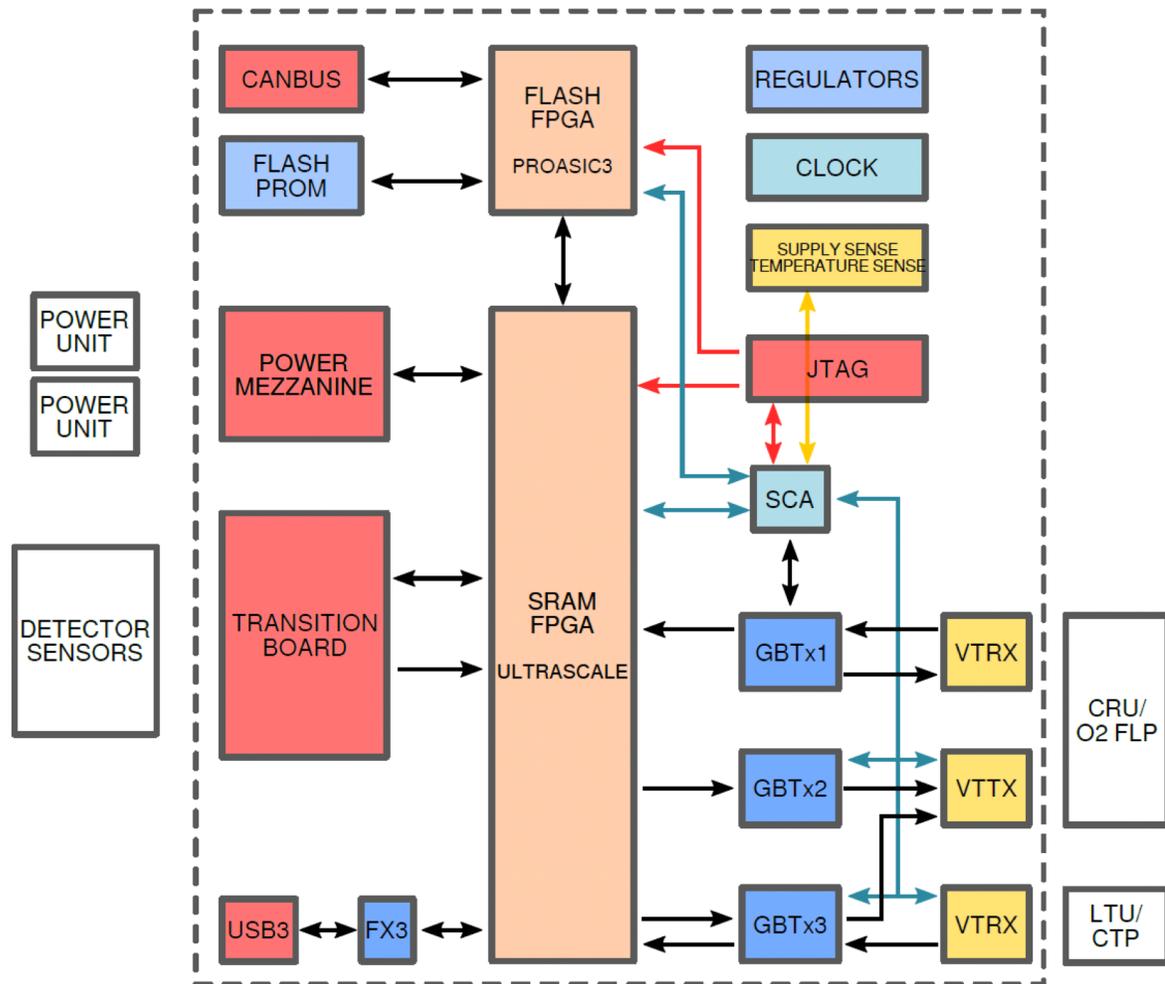
Prototypes and Tests

- Separate Boards for FPGA and GBT
- Based on Xilinx Kintex-7 FPGA
- Integrated USB Interface for debug
- Separate Fiber connection for emulation of the CRU
- Integrated Power Supply to power sensors independent of Power Unit
- GBT components on separate board connected via FMC
- Various sensor connector configuration to prototype both Inner & Outer Barrel
- VME 6U form factor
- Used for initial verification of electrical interfaces
- Initial experience with GBT parts
- Used for radiation testing of fundamental firmware components and initial testing of mitigation techniques



- 6U VME size
- Based on Xilinx Kintex Ultrascale FPGA (better radiation performance, more resources)
- Eliminate all extra components from RUv0
- Use close to final component types and numbers
- Layout close to final design
- 8* RUv1.0 boards produced
 - 2 * August 2017
 - 6 * September 2017
- 13* RUv1.1 boards produced (minor modifications and bug fixes)
 - 6 * November 2017
 - 7 * March 2018







- RU power section
 - 7 DCDC regulators (accuracy, noise, ripple, Inrush, sequencing)
 - I_{SENSE} offset problem solved by replacing amp AD626=>AD8418
- Communication with sensors/Alpide using transition board & firefly
 - CLOCK, CONRTOL, DATA @ 1.2Gbps and 400 Mbps
- Communication via 4.8 Gbps GBT links (GBTx/1/2, VTRx/VTTx)
 - Access & program GBTx using Cern USBI2C dongle (connector bug)
- Communication with the SCA-chip
 - monitor voltage/current, temperature, VTRx optical power
 - I2C, JTAG, GPIO interface
- Clock distribution: jitter/levels on crystal oscillators, jitter cleaner and clock buffer
- USB3 (using FX3 chip) communication & boot from I2C PROM
- JTAG chain (primary US & PA3 program, secondary FX3 & GBTX/1/2)
- Program Xilinx US with PA3 via select map interface
- Communication with the PU using front pannel I2C
- FLASH PROM (access, read-ID, read & write)
- CAN transceiver



Radiation Validation – Latest Beam Tests



Facility	Date	Goal	DUT	Particles	Flux ¹ [p cm ⁻² s ⁻¹]	Fluence ² [p cm ⁻²]	Duration [hours]	Notes
Prague	2015-2017	Firmware protection	RUv0	Protons 30 MeV	1×10^7	4×10^{12}	4×48	Beam limited to the FPGA only. Most effective way to check firmware design.
CHARM	Oct 2017	Cavern spectrum overall evaluation	RUv1	Mixed field	5 kRad/day ($\approx 5 \times 10^7$ n/day)	10 kRad ($\approx 1 \times 10^8$ n cm ⁻²)	48 ÷ 96	CHARM gives $\approx 2 \times 10^7$ HEH (30% to 80% being neutron) for each delivered kRad of TID. <u>Destructive test</u> due to TID.
Louvain	Nov 2017	High statistics DCDC test	DCDC boards	Neutron 23 MeV	1×10^8	$\approx 1 \times 10^{13}$	8	Extended reliability test sor SEL/SEU only (no TID effects at first order). Neutron spectrum > 10 MeV. <u>NON destructive</u> .
Prague	Dec 2017	Firmware protection	RUv1	Protons 30 MeV	1×10^7	1×10^{12}	24	Beam limited to the FPGA only. Most effective way to check firmware design.
Prague	Jan 2018	Firmware protection	RUv1	Protons 30 MeV	1×10^7	1×10^{12}	24	Beam limited to the FPGA only. Most effective way to check firmware design.
ChipIR (Oxford)	March 2018	SEE with no TID on PA3	RUv1	Neutron ≤ 500 MeV	$\approx 1 \times 10^6$	$\approx 1 \times 10^{11}$	12	Further verification of the system without destroying PA3 programmability (which dies around 10 kRad).
GIF (CERN)	2018	TID, scrubbing with realistic flux	RUv2	Mixed	1×10^4	$\approx 1 \times 10^6$	62	Easily accessible verification tool for TID and scrubbing behavior testing/verification.
Prague	2018	Further FLASH / Firmware tests	RUv2	Protons 30 MeV	1×10^7	$\approx 1 \times 10^{12}$	24	Further investigation about the FLASH (flux threshold effect?). Benchmarking of extra TMR in key firmware blocks.

Readout unit number is that one registered in the WP10 material inventory. They are rotated to account for appropriate cool-down periods and/or damage.

¹ Realistic flux obtainable at the specific facility

² Integrated flux over the irradiation time AND number of DUTs



- The system will operate in the ALICE cavern radiation environment, with a total TID of about **10 kRad** (safety factor 10) and a high energy ionizing particle flux of **1 kHz cm⁻²**. Upsets in the logic are the main concern, while TID is extensively tested.
- The Readout Electronics has been designed to incorporate hardware (hardware TMR and scrubbing subsystem) and firmware protection (TMR, ECC, etc.) against SEE effects.

So far tested in

- 6 specific test beams at the Rez facility in Prague (30 MeV proton) for firmware and scrubbing verification.
- 1 test beam at the CHARM facility (including the Power Unit) in a realistic mixed radiation field.
- 1 neutron test beam in Louvain (23 MeV Neutrons) specifically intended to further verify DCDC (**LMZ31710RVQ**)
- 1 neutron test beam at Oxford ChipIR (up to 500 MeV Neutrons) for whole system testing

- Scrubbing from auxiliary FPGA working and effective.
- **In Any Case:** even without using the scrubbing, the firmware proved resilient enough to SEE to operate on average for 1300 hours (29 h full IB or 10 h full OB) before experiencing any upset which would require recovery.
- Data interruption in case of firmware upset has been measured **and lasts on average one second** for the affected lane, or a few seconds if a reset of the FPGA is necessary.
- Errors on clock resources or other key subsystem are negligible (too rare to gather any significant statistics).
- Commercial DCDC proved compliant with the task, one power glitch every 72 hours foreseen within the whole ITS.

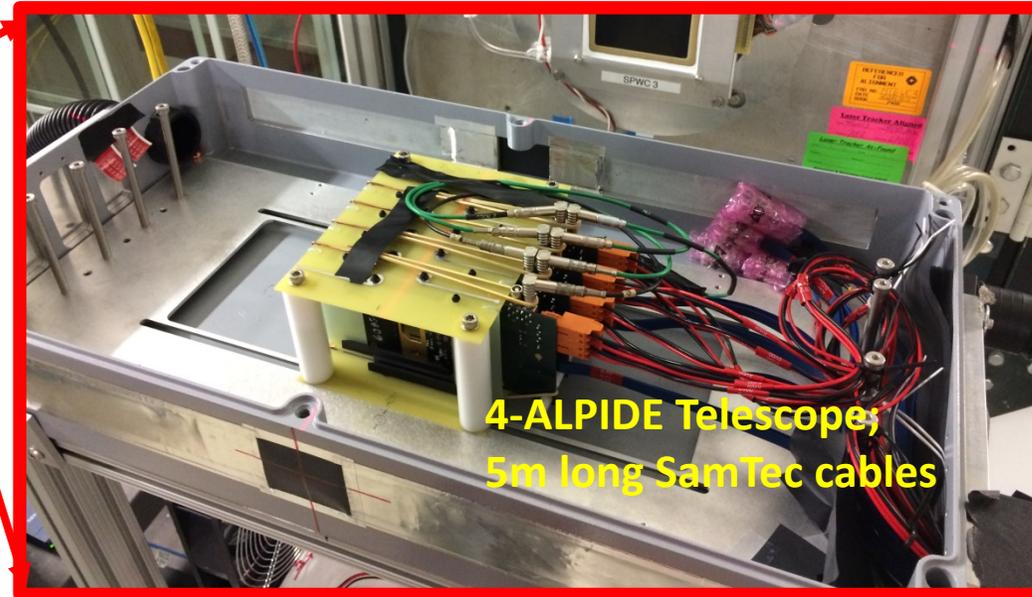
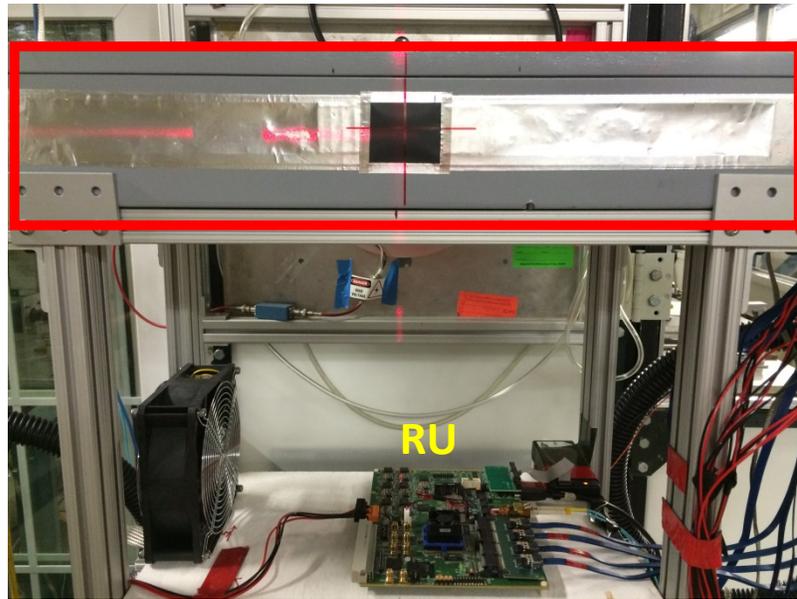


Failure mode	Affected section	Estimated occurrence in ITS operations (average MTBF)			Corrective action	Downtime per occurrence
		IB	OB	Whole ITS		
Sensor data lane	1 sensor for IB ½ module for OB	22 - 40 h	4 - 6 h	3 - 5 h	Self-repairing	< 1 s >
GBT data*	1 full stave	29 h	10 h	7 h	30% self repairing, 70% reset by slow control	< 5 s >
Clock resources	1 full stave	Negligible	Negligible	Negligible	Reset by slow control	< 5 s >
Transceiver settings	1 sensor, IB only	> 932 h	–	–	Reset by slow control	< 5 s >
Flash memory	1 full stave	Negligible	Negligible	Negligible	FLASH reprogramming (30 s beam off, 30m beam on)	30 s – 30 m
¹ PA3	1 full stave	172 h	58 h	43 h	Reset by slow control	< 0 s >
² DCDC power glitch	1 full stave	294 h	98 h	71 h	Power cycle	< 10 s >

* Data for the non-TMR block, final version will use TMR protected block. This failure mode also include sensor control and clock failures.

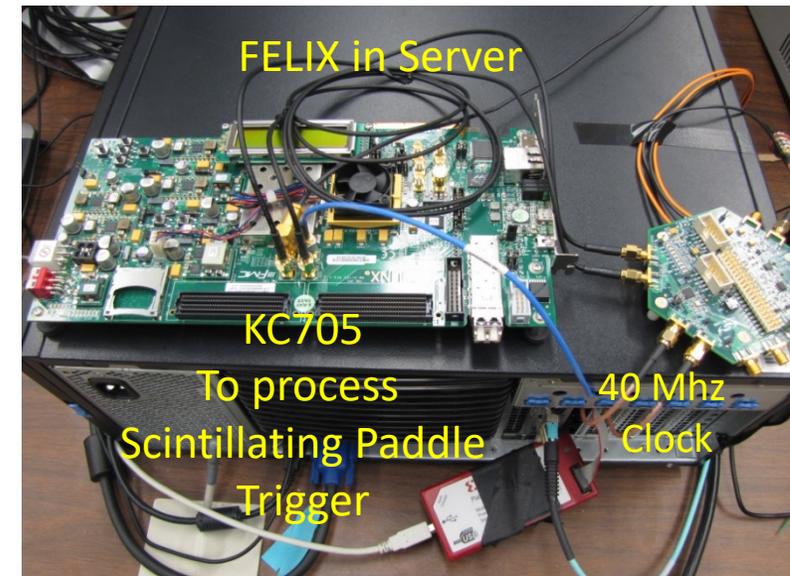
¹ When PA3 get stuck the main FPGA is not compromised, and therefore no downtime occurs. TMR of key block in PA3 firmware will further improve that.

² Considering 200 RU with 8 DCDC each (20% overestimation)



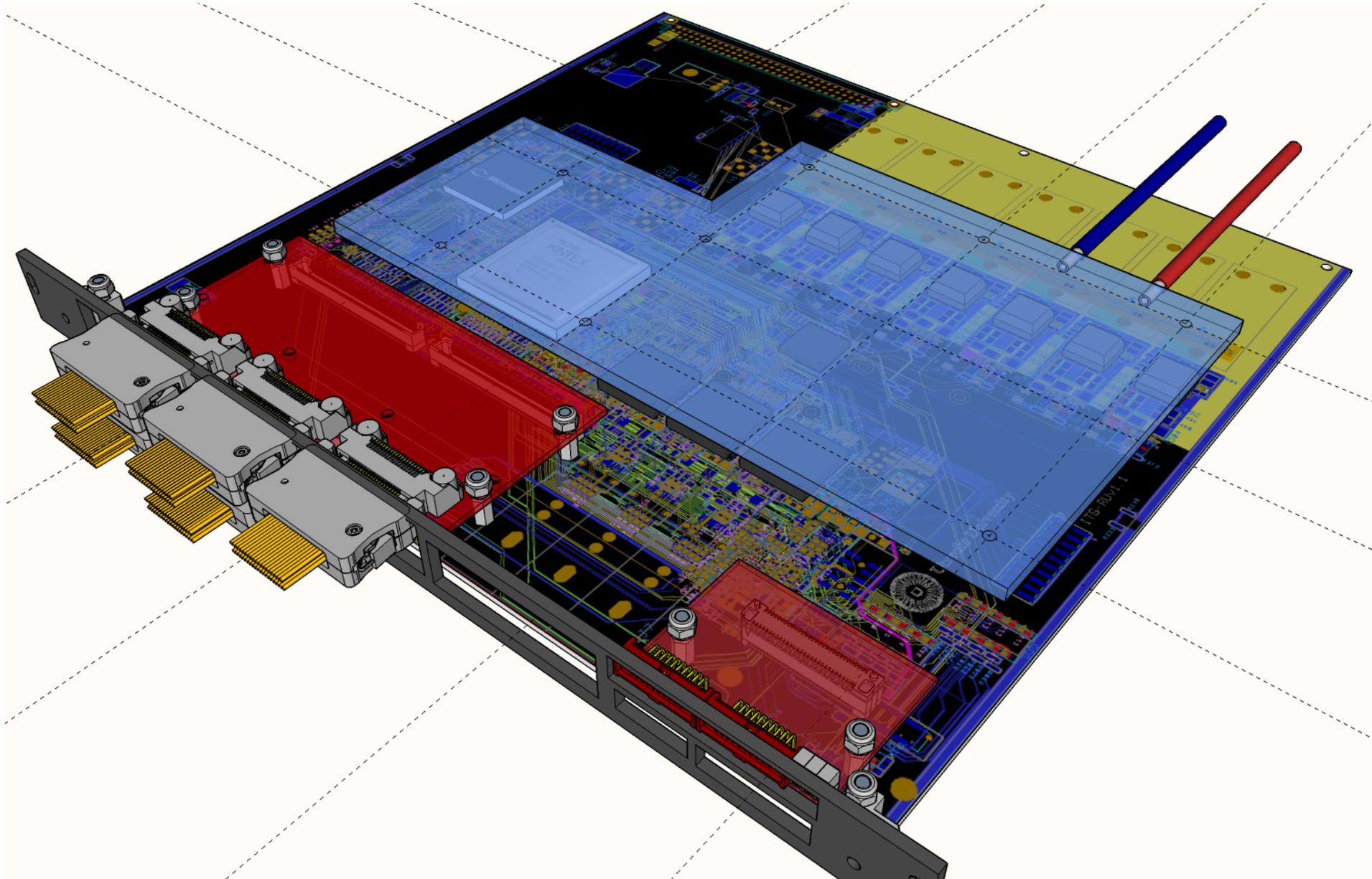
Highlights:

- Primarily 120GeV proton beam; also with low energy pion beams
- Beam trigger rate $\sim 7\text{kHz}$
- Tested High ALPIDE occupancy runs, with 10cm lead bricks in front of the sensors
- See Sho's talk for details





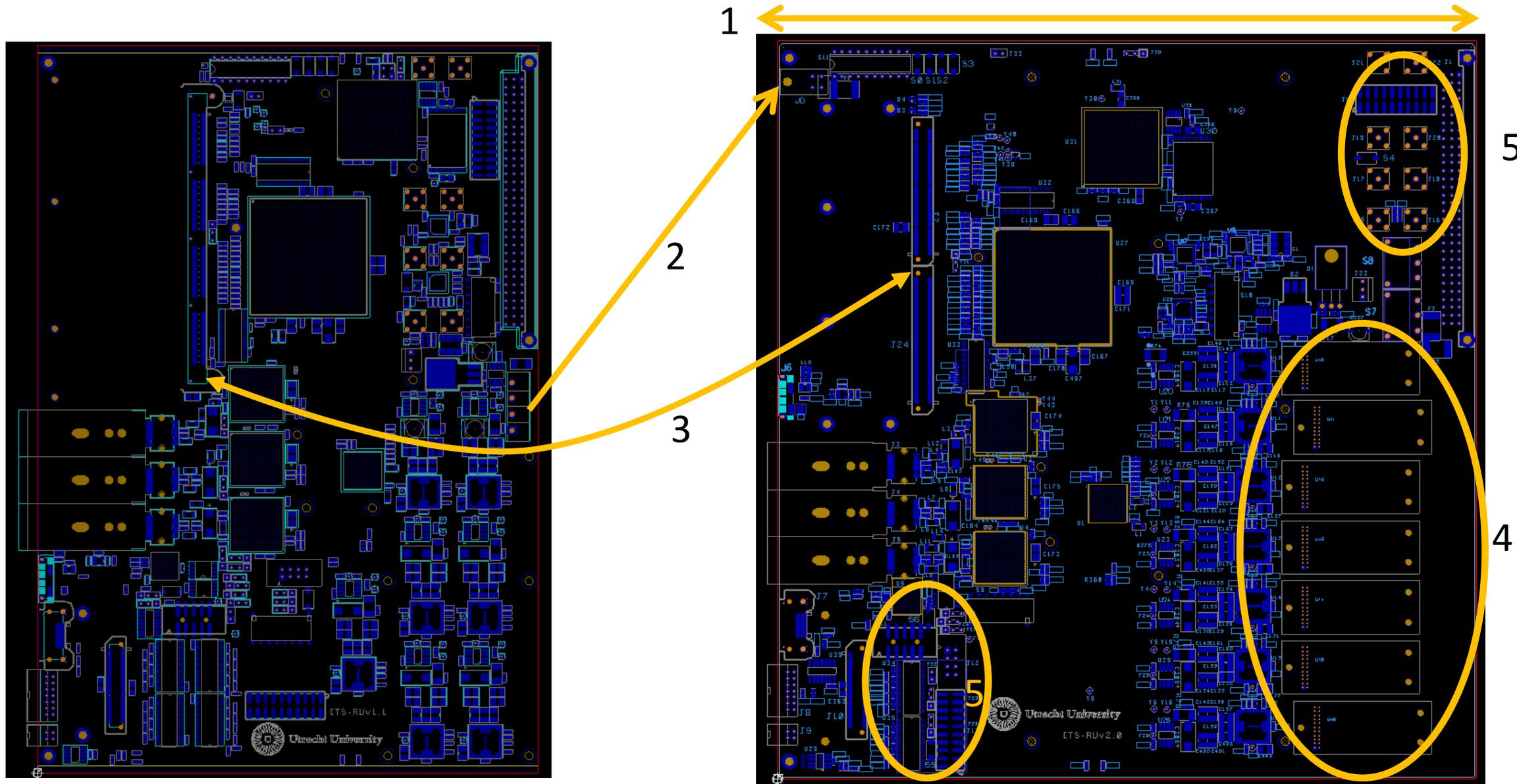
RU Production Version “RUv2”





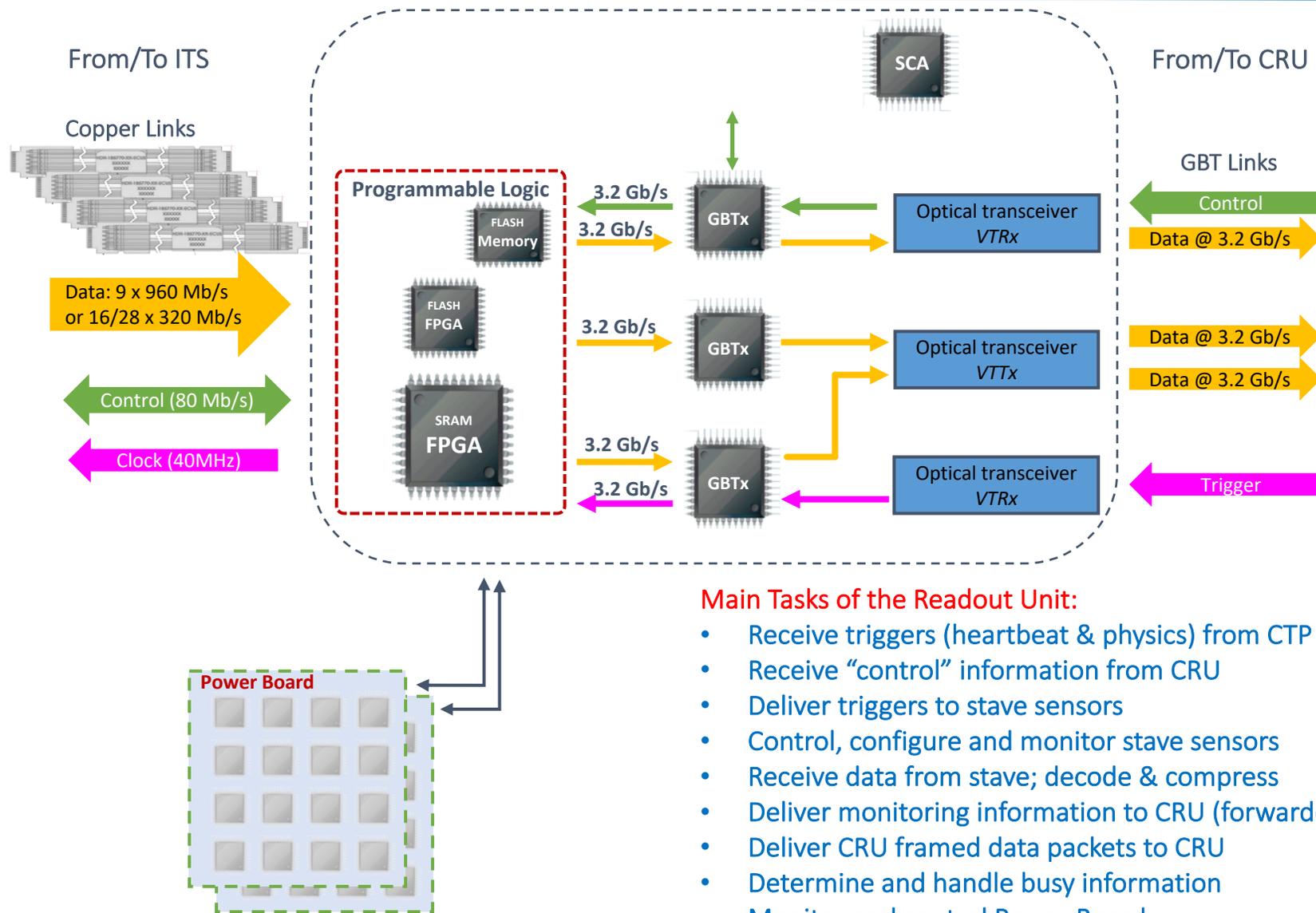
		RUv1_x	RUv2
1	Dimensions	160x233 mm	220x233 mm
2	Power connector	J0 (Weidmuller BL/SL 5.08) on back	J0 (MOLEX 172316) to front (J1 stays as it is + switch to select between J0 & J1)
3	Transistion board connector	Samtec QFS/QMS type	2 * Samtec ERF8-50... (USB3 connector also moved)
4	Power Converters	Only COTS DCDC	Besides COTS also FEASTMP_CLP placeholder Updated DCDC placement for improved PI Use of blind via's to further improve PI
5	Removal high compements from the cold plate area, aiming for same cold plate power board		
6	Change Clock distribution with PA3 clock independent from jitter cleaner		
7	Remove secondary JTAG chain		

Logic and layout of the board is mostly the same as RUv1.1





Firmware



Firmware is mostly complete (see backup slides for an overview of the various firmware components) to accomplish these tasks and to mitigate SEEs; it has been used in various radiation campaigns and readout tests

Main Tasks of the Readout Unit:

- Receive triggers (heartbeat & physics) from CTP & decode
- Receive "control" information from CRU
- Deliver triggers to stave sensors
- Control, configure and monitor stave sensors
- Receive data from stave; decode & compress
- Deliver monitoring information to CRU (forwarded to DCS)
- Deliver CRU framed data packets to CRU
- Determine and handle busy information
- Monitor and control Power Board
- Handle radiation upsets in programmable logic (& sensors)



MVTX Production & QA



The RUv2 CERN tendering document is ready, including testing procedures (see following slides). Production is foreseen in batches and will last approximately 3-4 months. 4 Initial prototypes have been produced, and are currently being verified

Batches

- A pre-series totaling 10 boards;
- A first batch totaling 106 series production modules;
- A second batch totaling 106 series production modules;
- A third batch totaling 88 series production modules.
- Option for 80 more boards for sPhenix

Hardware components

- 1 Xilinx XCKU060-1FFVA1156C (1156 pin BGA package)
- 1 A3PE600L-FGG484M FP (484 pin BGA package)
- 3 CERN custom GBTx chip (434 pin BGA package)
- 1 CERN custom made SCA chip (196 pin LFBGA package)
- 3 SFP+ pod connectors
- 2 ERF8-050-05.0-L-DV-TR connectors (100 pins, 0.8mm pitch)
- Miniaturized passive components (0201 minimum)

Activities at the Contractor's premises

- Quality control of the PCBs.
- Ordering of passive and active components.
- Input quality control of all components.
- Assembly of the components on the PCBs and soldering.
- Quality control of the assembled boards.
- Packing, and shipping.

Key technical PCB parameters

- 10 layers low-loss material ($Er < 3.7$ at 5 GHz, $Df < 0.012$ at 5 GHz)
- Maximum overall thickness of (1.57 ± 0.13) mm
- Copper Outer layer: $35 \mu\text{m}$, Copper Inner layer: $17.5 \mu\text{m}$
- Holes per PCB: 5000
- Minimum hole diameter: 0.63 mm
- Blind vias (layers): 32 (1)
- Minimum track width (outer layer): $110 \mu\text{m}$, (inner layer): $100 \mu\text{m}$
- Minimum spacing (outer layer): $110 \mu\text{m}$, (inner layer): $100 \mu\text{m}$



- A total of **222** boards will be manufactured for ITS, 88 for MFT, option of 80 boards for MVTX
- Testing will be done in a 2+ stage approach:
 - 1) Hardware testing at the manufacturer (only functional smoke test).
 - 2) Board bring-up, initial hardware verification and short-term functional verification at Nikhef/Utrecht.
 - +) Long-term functional testing at collaborator sites (sampling) & during commissioning.

For MVTX, the second stage of testing will be performed by UT Austin in combination with LANL





- The contractor shall inspect all parts individually according to the applicable standards (see backup slides). All component defects and assembly errors shall be eliminated.
- The contractor shall test 10% of the boards manufactured for ionic residues
- The dimensions of the mechanical parts shall be checked to ensure conformity. Items which are outside tolerance for straightness, flatness, position of holes or other reasons shall be rejected.
- The contractor shall have an approved and formal process designed to monitor and record each phase of the manufacturing of the supply, such that complete conformity with the requirements of this specification is achieved.
- All specified tests and measurements carried out during all stages of production, from material procurement up to delivery shall be recorded. The contractor shall provide these records in electronic form (Microsoft Word, Excel, Project or OpenDocument and in PDF).



- ITS Readout Unit satisfies the requirements of the MVTX Readout
- ITS Readout Unit prototyping is successfully completed for electrical, functional and radiation performance
- A Manufacturing Plan that includes RU production and assembly for MVTX is completed
- Tender document will be posted after initial RUv2 prototype testing
- A testing plan is in place and test components are being designed and fabricated
- UT Austin will take responsibility for organization with ITS of the board manufacture and testing
- Board testing after delivery will be performed by UT Austin in combination with LANL