sPHENIX Director's Review
MVTX Electronics

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April 9-11, 2019

BNL

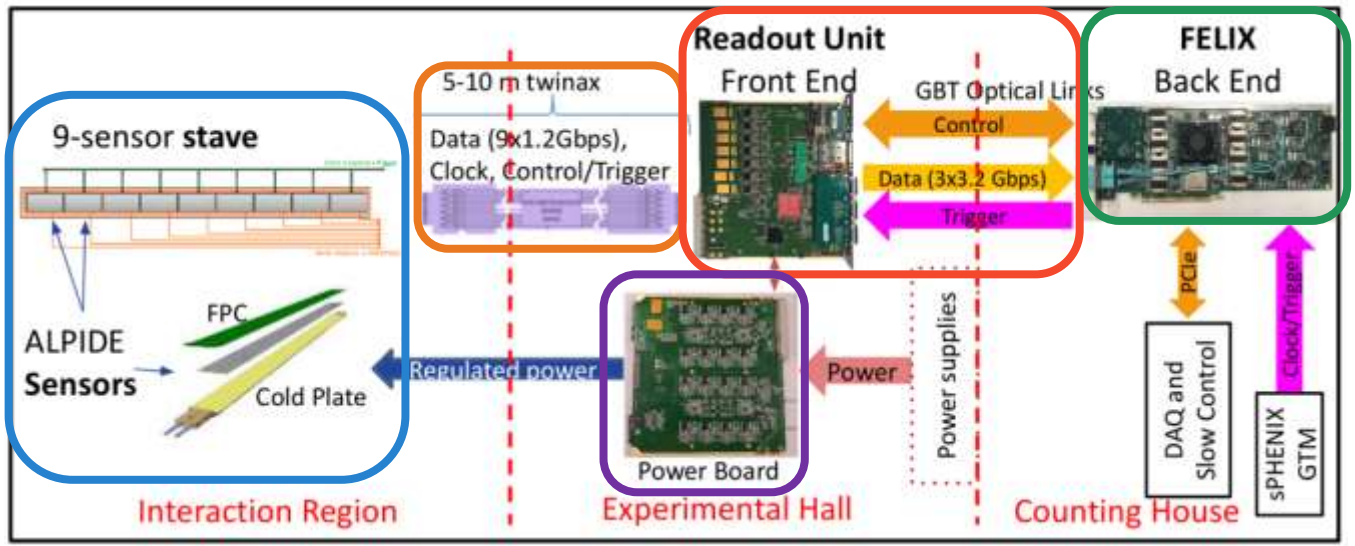
WBS 3.2.2: Electronics

- Stave Extension Cable (3.2.2.1)
- Readout Unit (3.2.2.2)
- FELIX backend card (3.2.2.3)
- MAPS Power System (3.2.2.4)

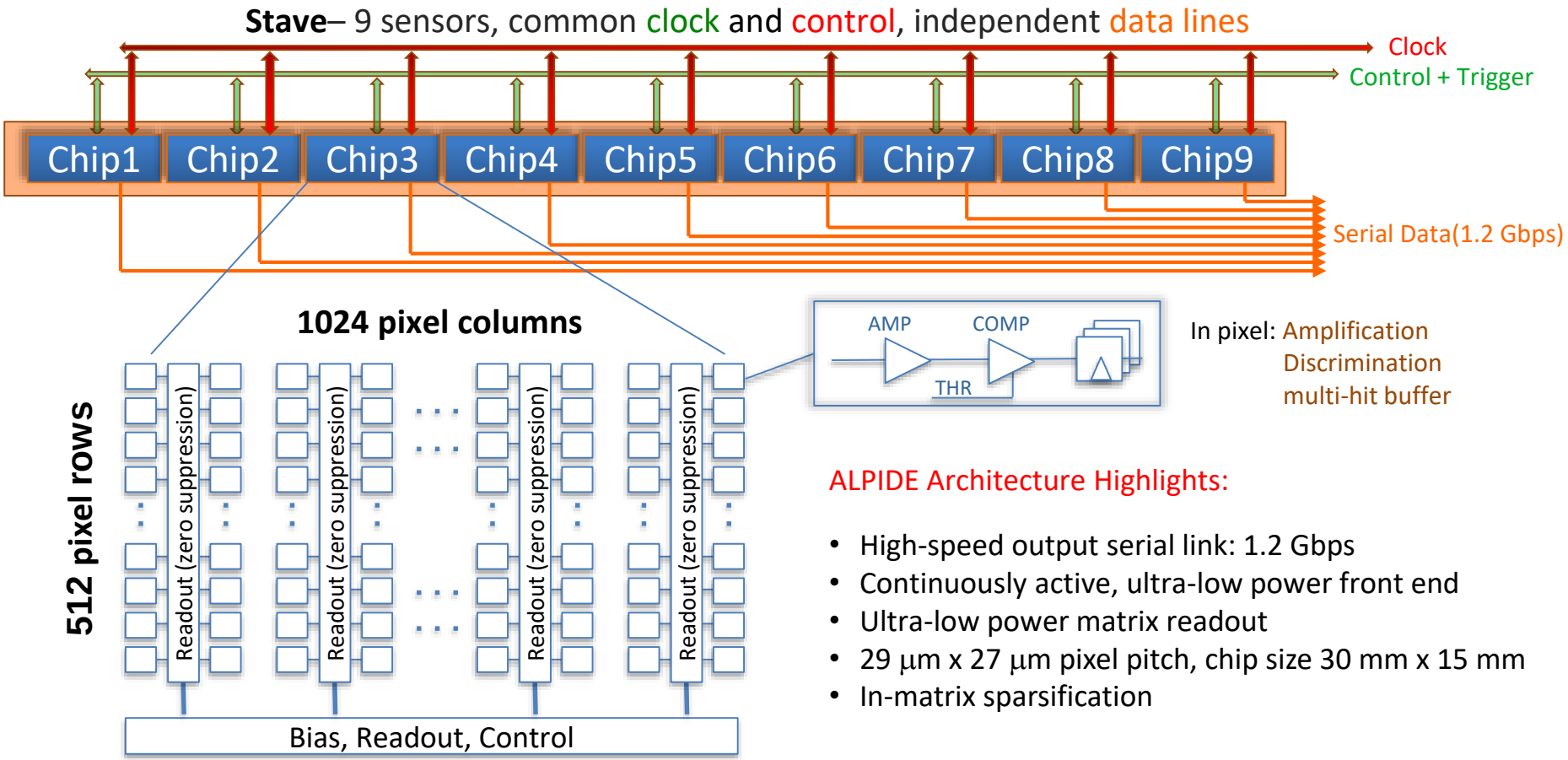
L3 Technical Overview

- Staves
- Signal cables

- Readout electronics
- FELIX Back End
- Power System



Staves

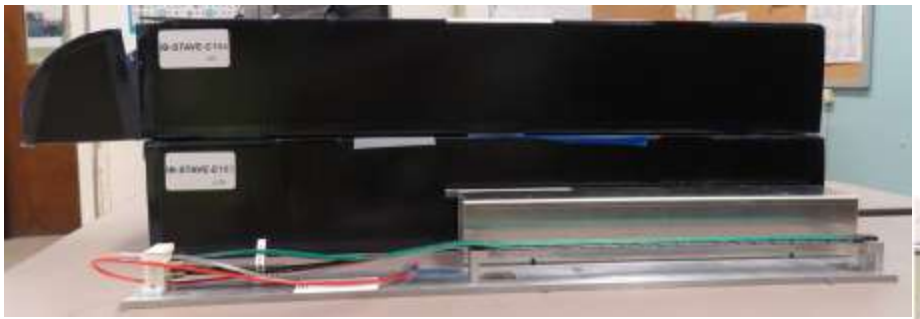


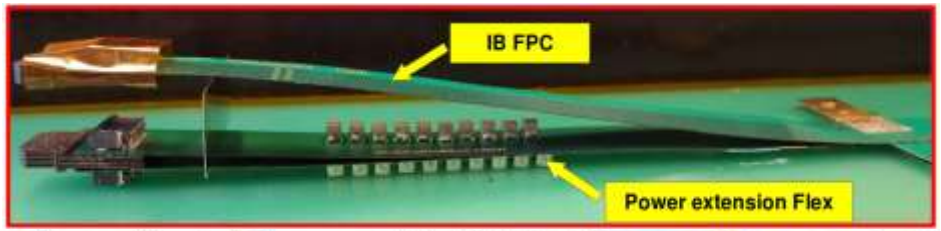
ALPIDE Architecture Highlights:

- High-speed output serial link: 1.2 Gbps
- Continuously active, ultra-low power front end
- Ultra-low power matrix readout
- 29 μm x 27 μm pixel pitch, chip size 30 mm x 15 mm
- In-matrix sparsification

Stave Extension Cable

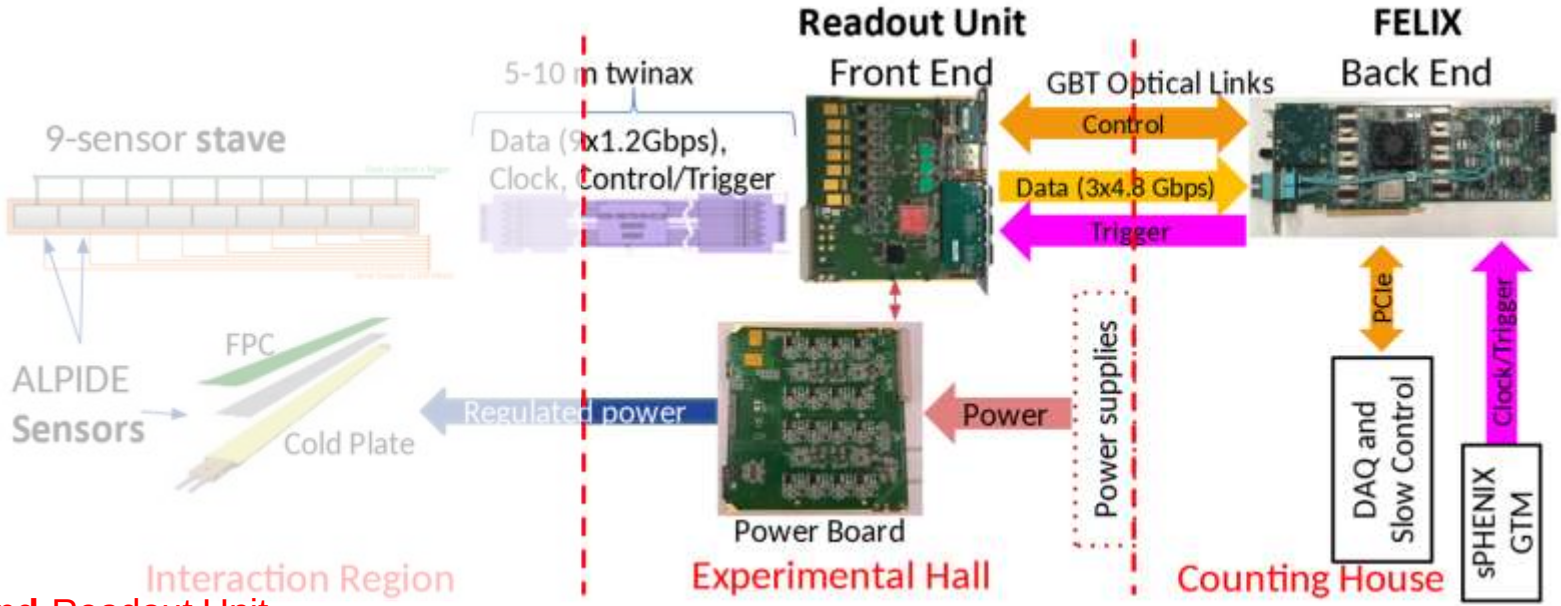
- Stave consists of three “flex printed circuits”: one signal FPC, two power FPCs
- For MVTX mechanical integration (thickness of patch panel), the power FPCs had to be extended to 40 cm (from 15 cm)
  - We qualified 40 cm and 60 cm FPCs at CERN: identical performance
- 4 staves at LANL





MVTX stave modifications have been qualified, and we have our first staves

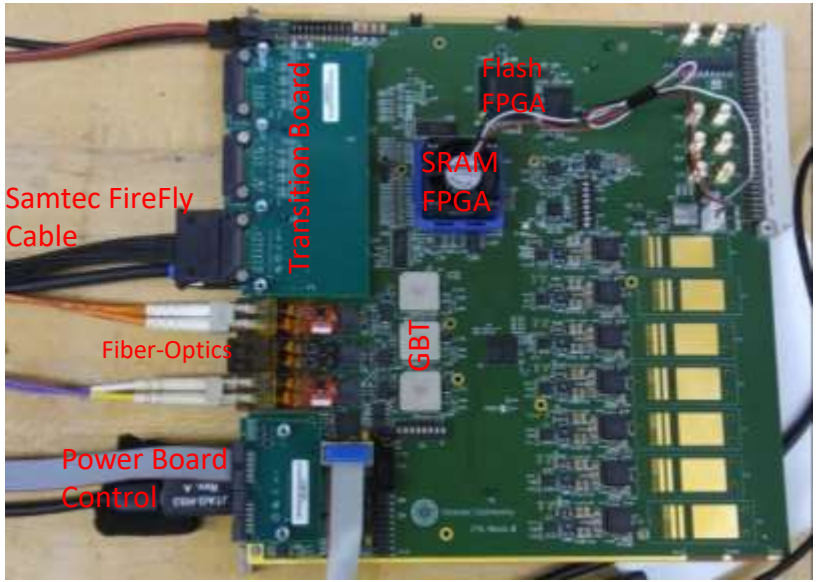
Readout Electronics Highlights



Front End-Readout Unit

- Stave **data readout, control** and **monitoring**
- **Trigger** & **busy** management
- **Power control** and **monitoring**
- **Event** building and **transmission** to back end (DAQ) through rad-hard Fiber-Optics (**GBT**)

Readout Unit

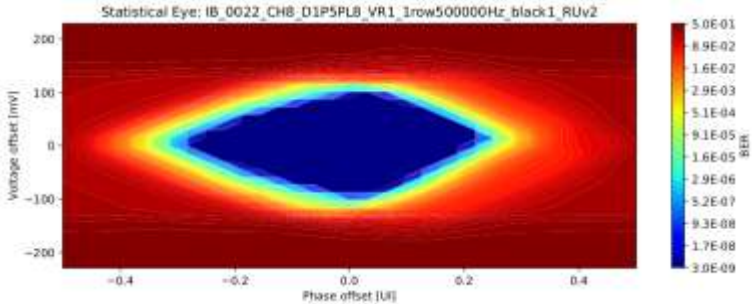


Architecture Highlights:

- SRAM based FPGA (Xilinx Kintex Ultrascale)
- Flash-based FPGA (Microsemi PA3) for configuration & radiation mitigation (“scrubbing”)
- GBTx ASICs (Radiation hard Giga Bit Transceiver) to FELIX
  - **3 total up-links (9.6 Gbps total), 2 data, 1 data & control**
  - **1 trigger down-link**
  - **1 control down-link**
- GBT-SCA: Rad. hard Slow Controls Adapter for monitoring and control
- Samtec “FireFly” copper twinax cable connection with stave

Signal Cable Design

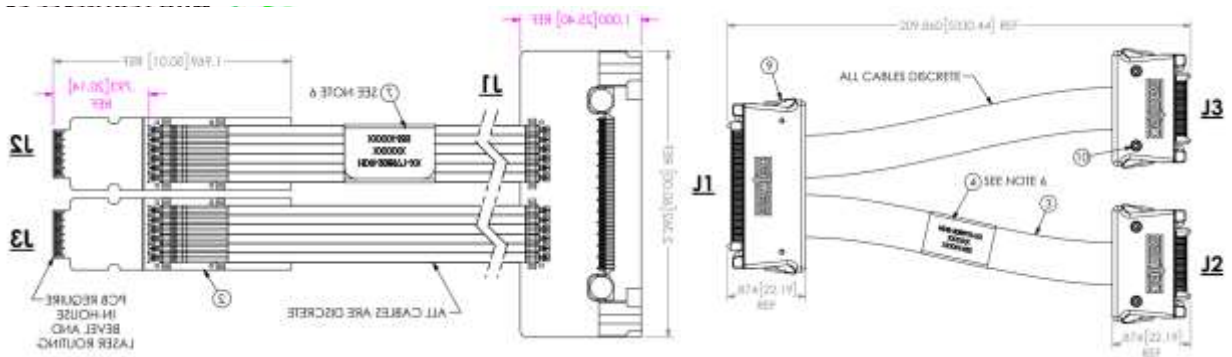
- Samtec twinax cables carry clock (40 MHz), control (40 Mbps bidirectional), data (9 x 1.2 Gbps)
- ALICE is using halogen-free cables (32 AWG, LDPE dielectric) due to CERN LSZH requirement; 2.65m + 5.3m cables have been tested and are now in production
  - No PRBS errors over 48 h-equivalent of a single chip; BER < 2.22 * 10^{-14}
  - Transmission is reliable (eye diagram is open) down to minimum ALPIDE driver strength



CCS-183564-XX-03-TB	
Parameter	**Reference value**
Impedance tolerance [%]	100Ω ±5%
Maximum insertion loss [db @ 1GHz for 1m]	-1.72 dB
Maximum return loss [dB @ 1GHz for 1m]	-18.40dB
Maximum within pair skew [ps/m]	10ps/m
Maximum pair to pair skew [ps/m]	50ps/m

Stave

Stave

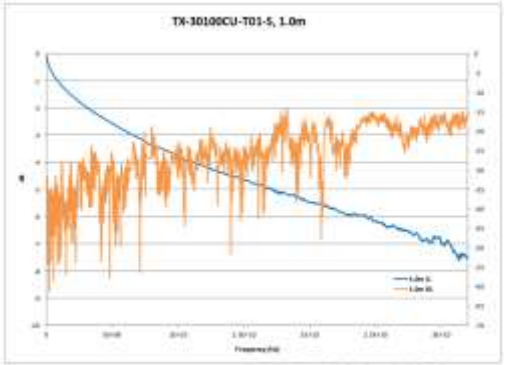


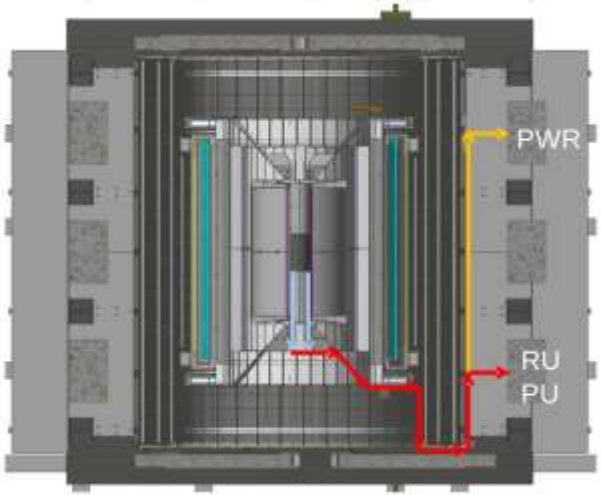
RU

RU

Cable Testing

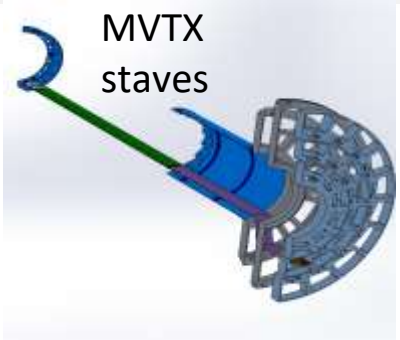
- BNL has approved non-halogen-free cables (30 AWG, FEP dielectric); improved signal integrity over the ALICE cables
- sPHENIX cable run estimates are converging: 1.4 + 6.5 m
- We have test cables in lengths 1.2/2.65 + 5.3/8.8 m (mix-and-match for total length 6.5 - 11.45 m)
- We will qualify these cables using stave and RU (bit error rates, statistical eye), and scope/network analyzer





We will test full-length MVTX cables in the next months

Power System Overview



RU configures and monitors stave current and voltage through I2C interface of power board

Power Board

Readout Unit

Bulk Power

Positive voltage domains

x3

PT100 Interface

RDO Interface (I^2C)

V adjust (DP)

V, I monitor

Overcurrent detection

Overcurrent reset

Overcurrent threshold

x16

LDO

LDO

LDO

LDO

Bias section

x4

FET Switch

Negative LDO

V control / V, I monitor

Power in (3.3V)

Power in (-5V)

I^2C isolator

Detector

Bulk Power: CAEN Supplies

A3009B
8V/9A/45W 12-ch
floating

3.3V output
that powers 1.8V
digital and analog
rails

EASY3000
Crate for hostile
area

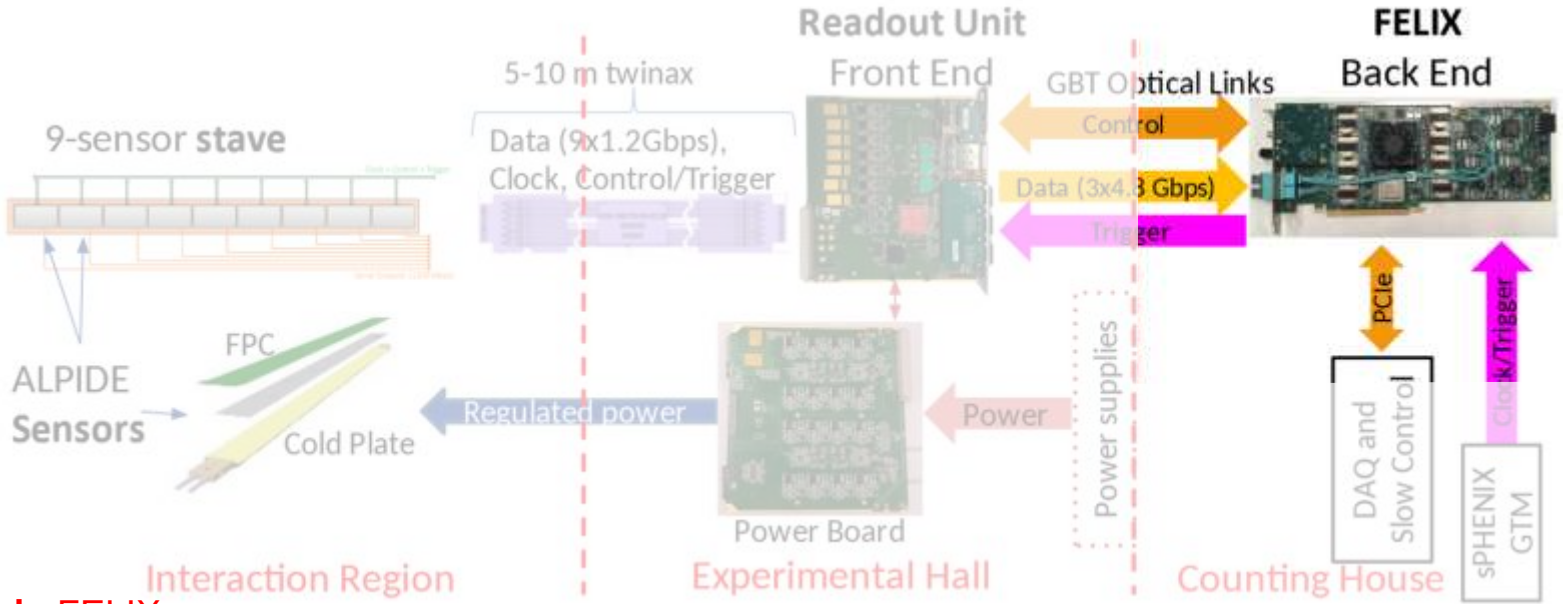
A1676A
Branch controller
Up to 6 crates

A3486
220/400Vac->48Vdc
2ch/2kW / 1ch/4kW

A2518
8V/10A 8-ch
individual floating

SY4527
Basic 600W model

FELIX Highlights

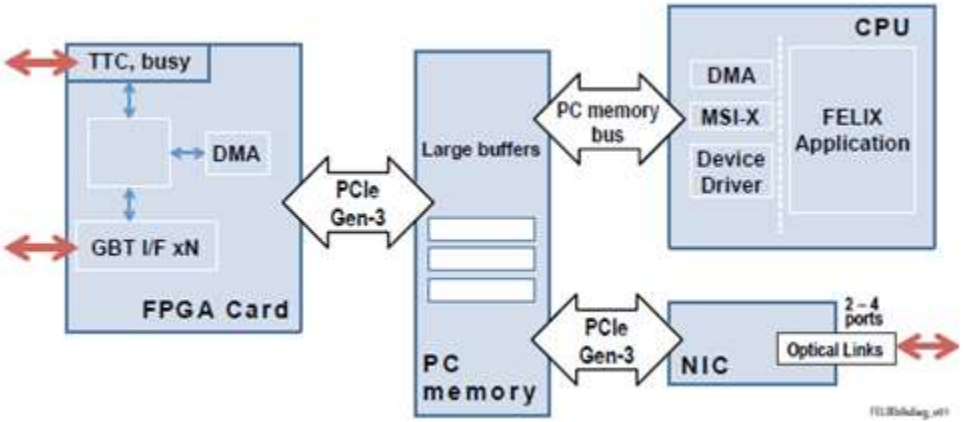


Back End - FELIX:

- Data **readout** from up to 8 Readout Units
- **Slow Control** and **Monitoring** of Stave and RU
- **Trigger** and **Timing** systems interface
- **Data aggregation** and sub-event packaging
- Data **transmission** through PCIe to Server CPU

Felix Architecture

FELIX v1.5



FELIX Block Diagram

Architecture Highlights:

- Xilinx Kintex Ultrascale KU115 FPGA
- 48 **bi-directional** GBT links
- 16-lane Gen-3 PCIe
- Mezzanine site for sPHENIX timing system card

Performance:

- PCIe Tx > 100Gb/s

FELIX v2.0

sPHENIX Timing Mezzanine

L3 Collaborators

- LANL
  - **Samtec Cables acquisition and testing**
  - **Firmware RU & FELIX**
  - **FELIX acquisition**
  - **Stave Extension FPC**
- UT Austin
  - **Readout reception and testing**
  - **RU Firmware integration**
- LBNL
  - **Power Board Production**
  - **CAEN power supplies acquisition and integration**

Schedule Drivers

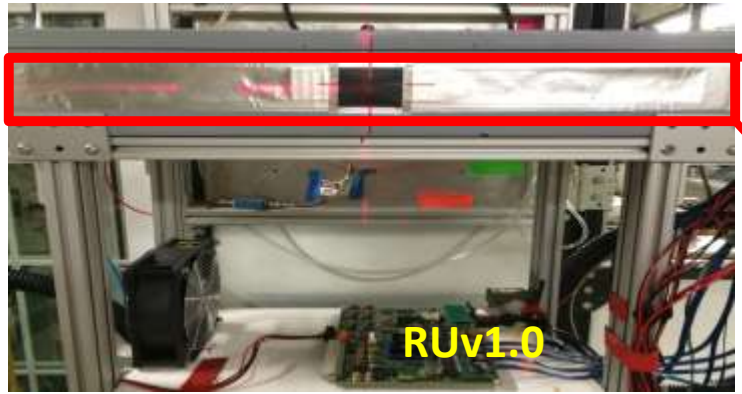
- Budget availability
- Readout Unit Reception & Testing
  - Expected availability for the RUs: mid May 2019
  - Testing ~2 months (plus ~2wk initial setup, as budget becomes available)
- RU Transition Board Production
  - Design ~ 1 week
  - Production and assembly ~ 4 weeks
- Cable Testing
- FELIX Acquisition
  - 8 boards included in the TPC FELIX production mid 2020
- Firmware Adaptation for RU and FELIX
- CAEN System acquisition
- Power Boards: manufacture, assembly, and testing

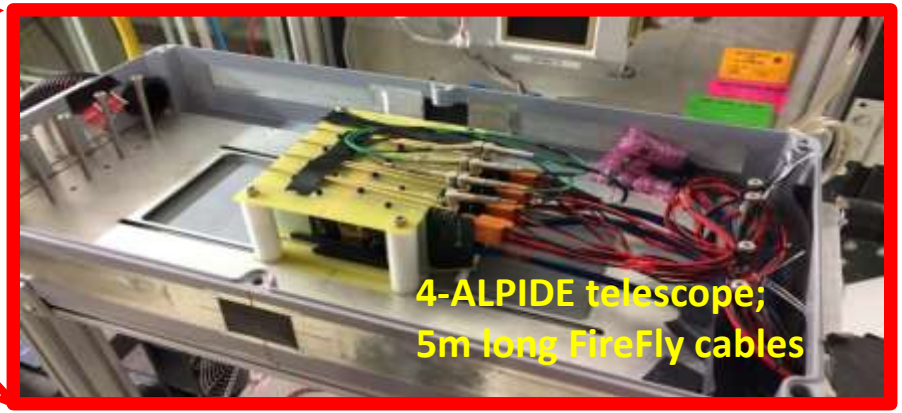
Cost Drivers

- Stave Extension: $0 (completed!)
- RU test, mechanical & Cables: $186k
- FELIX: $122k
- Power System: $357k

TOTAL: $665k

Status: 2018 Fermilab Test Beam





Feb-Mar, 2018 Setup

Status: Production

- RUv2.1 & Power Board in production by ALICE
- FELIX v2.0 in production by ATLAS
- MVTX firmware and software in sync with current ALICE and ATLAS work, with MVTX-specific data path logic in FELIX

same functionality production-qualified

RUv2.1 @UT June

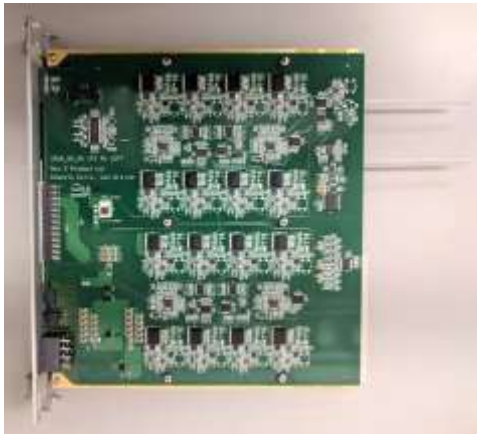
Production PB in discussion with LBNL

FELIX v2.0 in hand

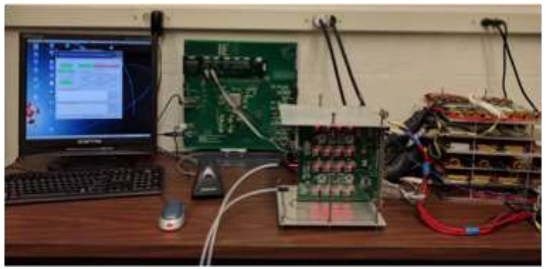
Key readout boards qualified and in production

Status: Power System (ALICE ITS)

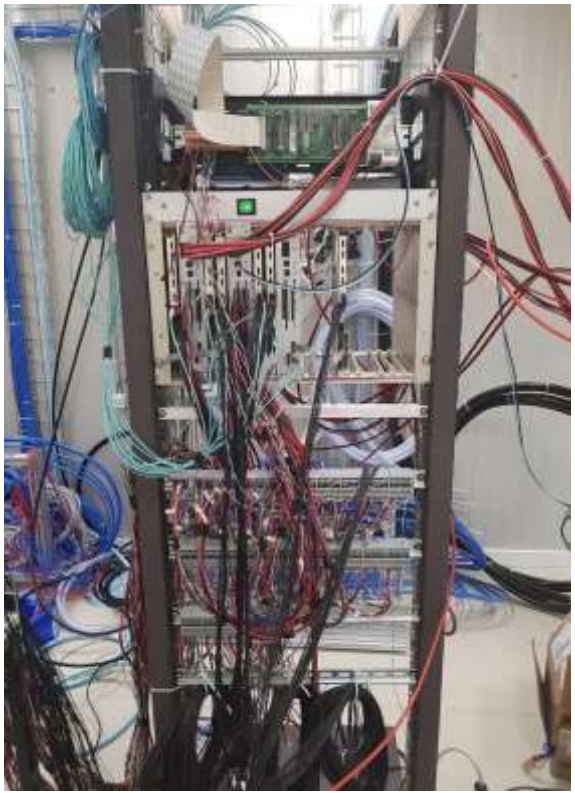
Power board



Test system at LBNL



Power boards & RU in rack



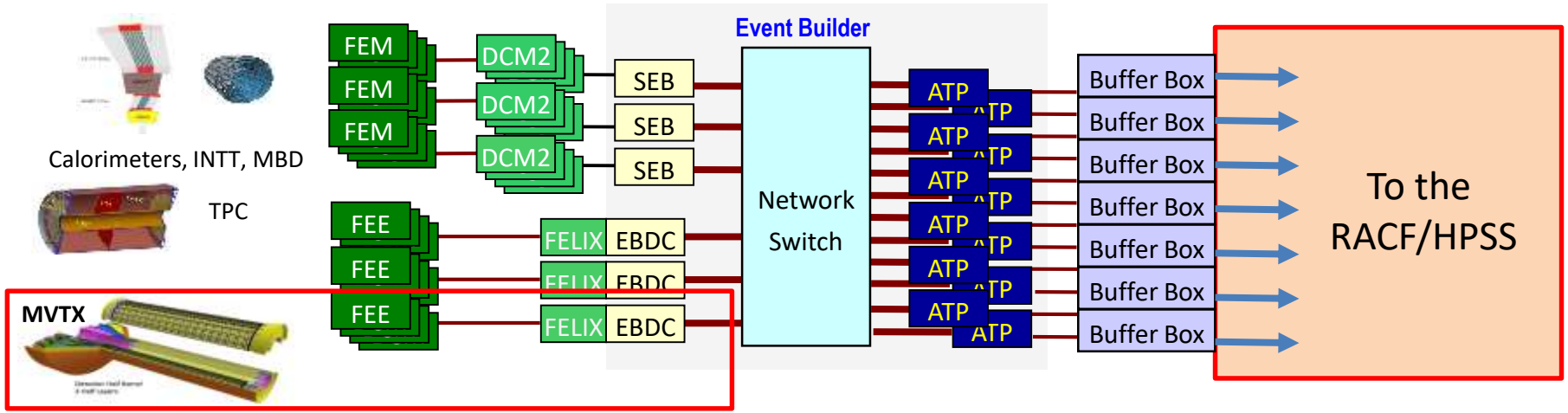
CAEN Power supplies

Summary

1) Does the current design demonstrate that the MVTX Staves and Readout Units will be compliant with its specifications? **Yes.**
   - **Triggered system at 15kHz using pulser at expected MVTX data rate, and approximately 7Khz at random during beam test.**
2) Can the data from MVTX staves be extracted, readout and integrated into sPHENIX Data Acquisition System? **Yes.**
   - **Test beam data from ALPIDE sensors was taken using full MVTX readout chain:**
     - **ALPIDE Sensor->Readout Unit->FELIX->rcdaq (sPHENIX daq).**
   - **Data was recorded in PRDF (sPHENIX data format) and is being analyzed in Fun4All (sPHENIX analysis framework).**
3) Are the electrical interfaces of the Staves and Readout Units to the other sPHENIX components at a proper level of understanding? **Yes.**
   - **The optical interface from the Readout Unit to the other sPHENIX components has been validated with FELIX.**
     - **Demonstrated clock and trigger and gigabit data transmission.**
   - **Power System is well understood.**

Back Up

sPHENIX DAQ Architecture



MVTX Hardware:

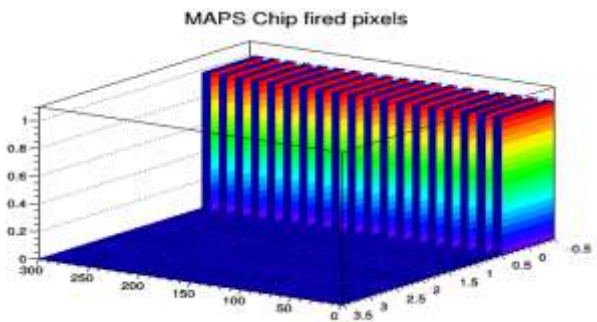
- 48 Staves
- 48 FEE (Readout Units v2.1)
- 6 FELIX v2.0
- 6 EBDC servers
- 24 Power Boards

Acronyms:

FEE	Front End Electronics
FELIX	FrontEnd LInk eXchange
EBDC	Event Buffer and Data Compressor
ATP	Assembly and Trigger Processors
Buffer Box	Interim storage
FEM	Front End Module
DCM2	Data Collection Module
SEB	Sub-Event Buffer

RCDAQ

- RCDAQ = sPHENIX Data Acquisition framework
  - **rcdaq plugin developed which will serve as a conduit between the FPGA DMA PCIe endpoint and software used to transfer data to sPHENIX Data Acquisition framework**
  - **Plots generated by RCDAQ in the initial stage of integration using pulsed mode of the ALPIDE pixels readout by Readout Unit and FELIX in the lab.**



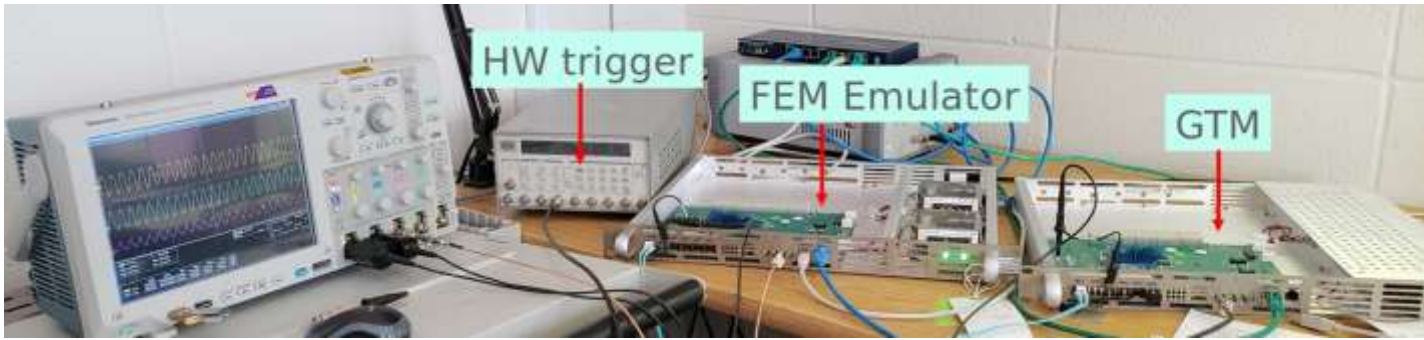
RCDAQ developed by Martin Purschke, BNL

Full MVTX integrated with sPHENIX DAQ (charge 2)

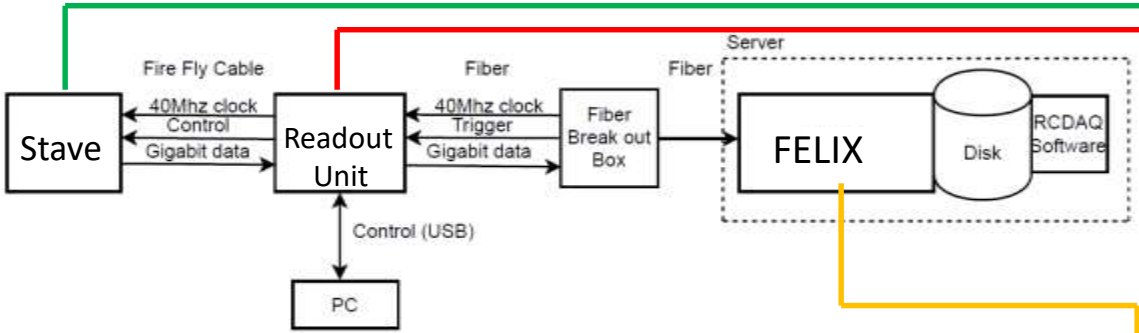
sPHENIX DAQ Integration

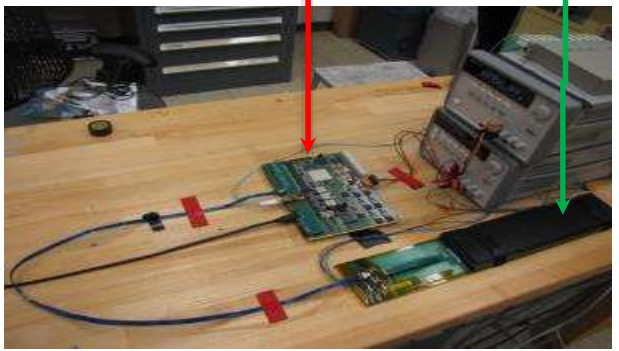
- sPHENIX detectors implement “plugins” to tie in to the central DAQ; the MVTX plugin was demonstrated at the 2018 test beam
- sPHENIX clock and trigger is distributed by Granule Timing Module (GTM): the FELIX firmware for MVTX includes the “receiver” that handles a trigger from sPHENIX through the timing mezzanine, and the GTM will be used at the 2019 test beam
- MVTX is participating in discussions for the sPHENIX DAQ design

MVTX is fully integrated with sPHENIX



MVTX Full Chain



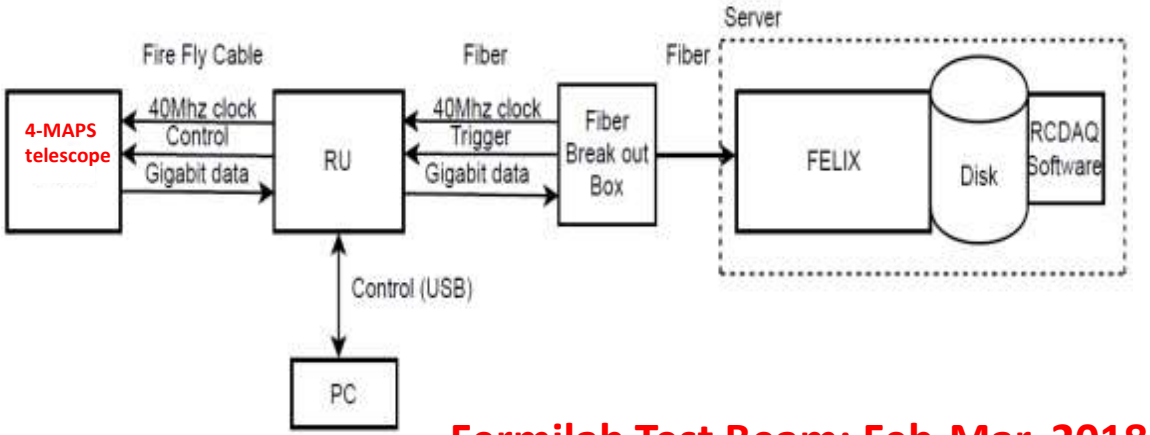


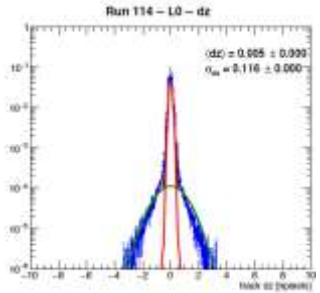
Readout Unit + Stave

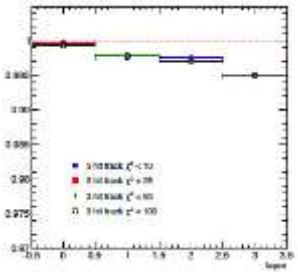
- Successfully configured, triggered and readout Stave:
  - **Readout Unit configures Stave**
  - **FELIX distributes clock to Readout Unit**
  - **Readout Unit distributes clock to the Stave**
  - **Stave is triggered, sends data at 1.2Gb/s**
  - **Configured GBT link to recover clock from FELIX**
  - **RU receives data and sends it to FELIX over GBT optical link**
  - **FELIX packs data, stores it on disk using RCDAQ**
  - **ALPIDE triggered and read out at 15kHz, 448 hits**
  - **Emulated 8 RU's using 1 fiber link per RU on FELIX, 15kHz**

Server + FELIX

MVTX Full Readout Chain Demonstrated (3/2018)

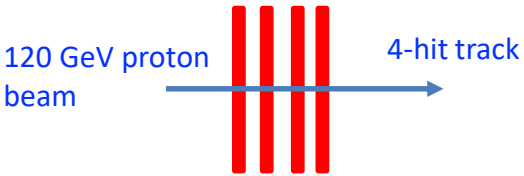






- Tracking spatial resolution: <5 um
- Hit efficiency: > 99.5%

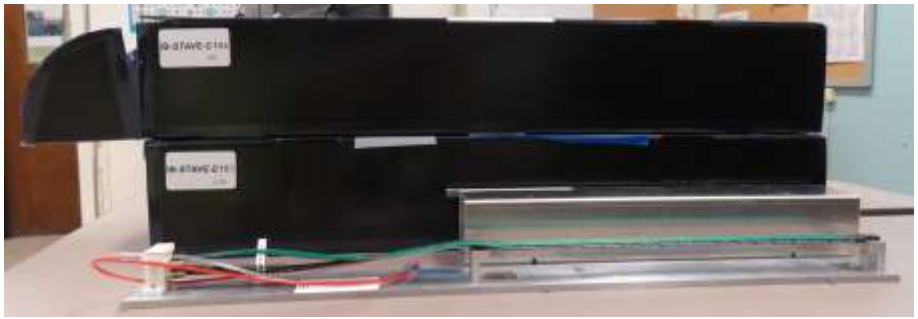
Fermilab Test Beam: Feb-Mar, 2018



4-MAPS telescope

2019 test beam: 4-stave telescope

- Scheduled for end of May, again at Fermilab
- Additions compared to the 2018 test beam:
  - **Staves (from single chips)**
  - **Full-length MVTX signal cables (from 5 m off-the-shelf cables)**
  - **FELIX v2.0 (from v1.5)**
  - **Cooling system**
  - **Power board**
  - **sPHENIX GTM**



Full test of all components of the MVTX detector

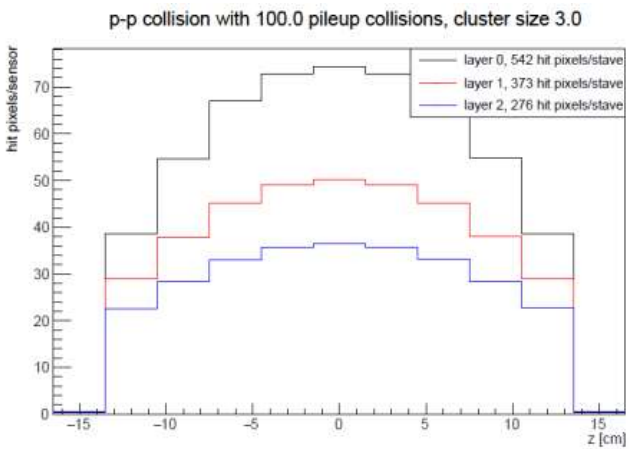
Estimated Data Rate

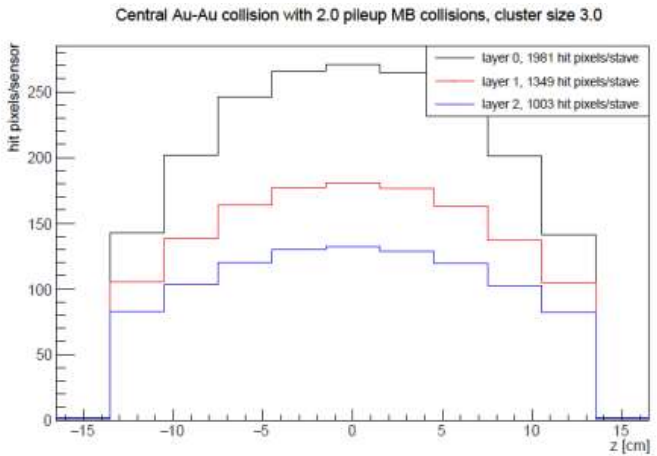
	10^{-4} noise occupancy	Hit occupancy only $p+p$ [MB/s]	Hit occupancy only Au+Au [MB/s]	Hit + noise occupancy $p+p$ [MB/s]	Hit + noise occupancy Au+Au [MB/s]
RU	26	29	107	55	133
FELIX	219	173	630	392	848
MVTX	1305	1041	3781	2346	5089

Readout Units 3 GBTX @ 400 MB/s = 1200 MB/s >133MB/s

FELIX (48 input on FELIX, twice the number needed to support 8 RUs (3 links each))

- 2x 8-lane PCIe Gen3 @ 7880 MB/s = 15760 MB/s > 848 MB/s

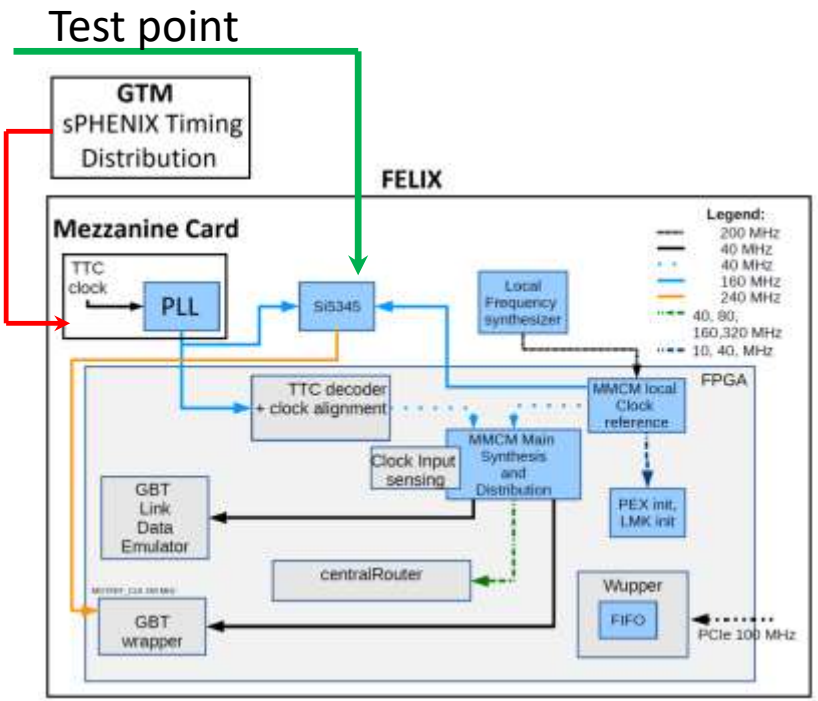




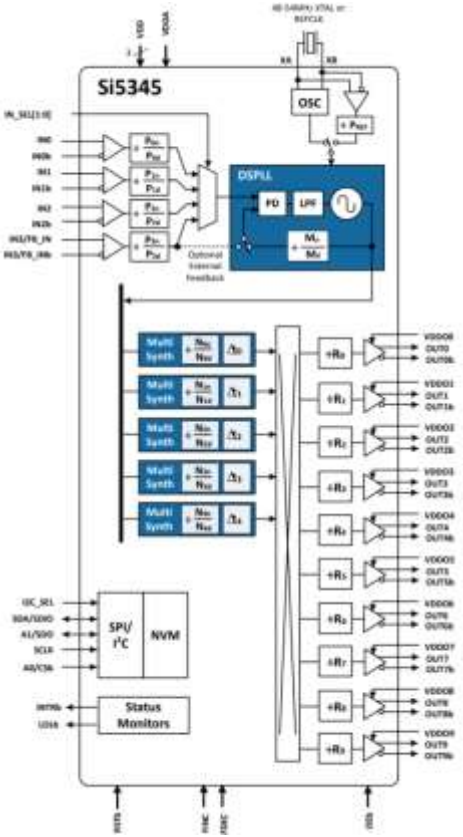
Meets specification (charge 1)

Worst Case Conservative Estimates

FELIX Clock Distribution



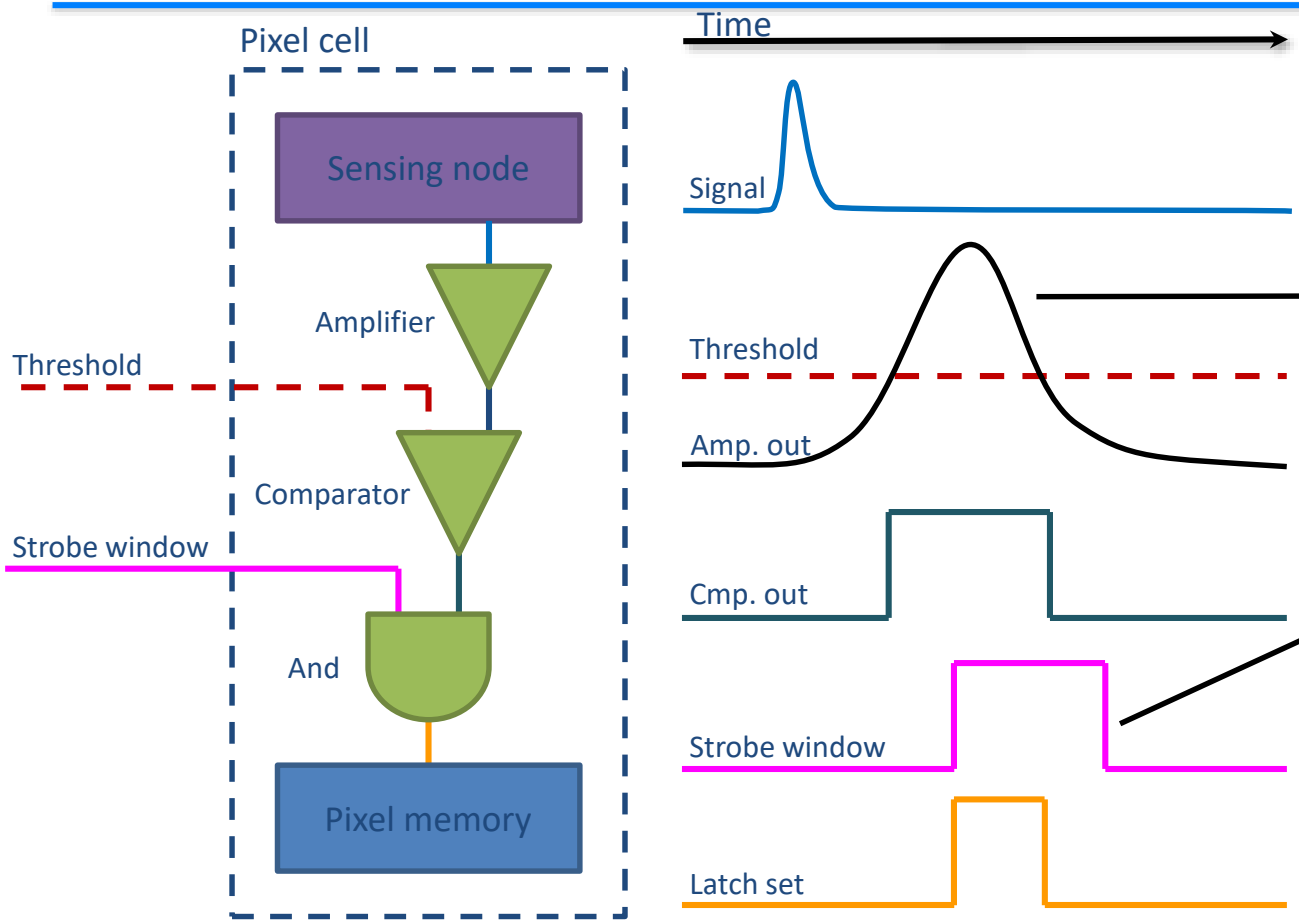
FELIX Clock Block Diagram



Si5345 Block Diagram

- Current lab setup: External clock taken as input on test points, and sent to an on-board si5345 (configurable PLL) to generate the 40Mhz clock required by FELIX.
- sPHENIX: FELIX will take the RHIC 9.362 MHz clock from the sPHENIX Timing System. Mezzanine Card will convert the 40Mhz clock required by FELIX.

ALPIDE Timing



Analog "slow" shaping time acts as a memory (µs order) to buffer the signal until the trigger arrives.
Called "pulse length"

Only pixel with signal higher than threshold DURING the strobe window will get latched in memory

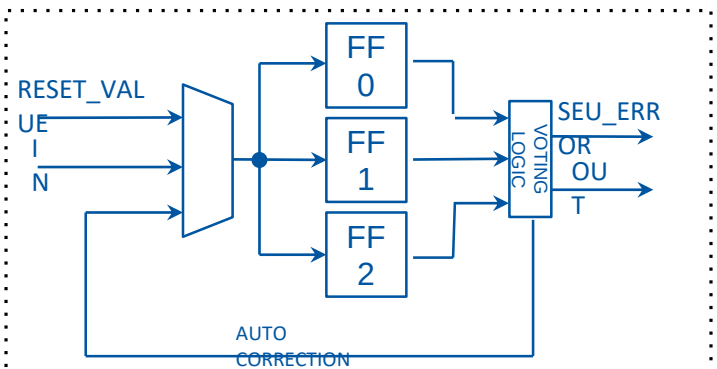
Confirmed at LANL: pulse length can be extended to meet sPHENIX trigger latency requirement (Charge 1)

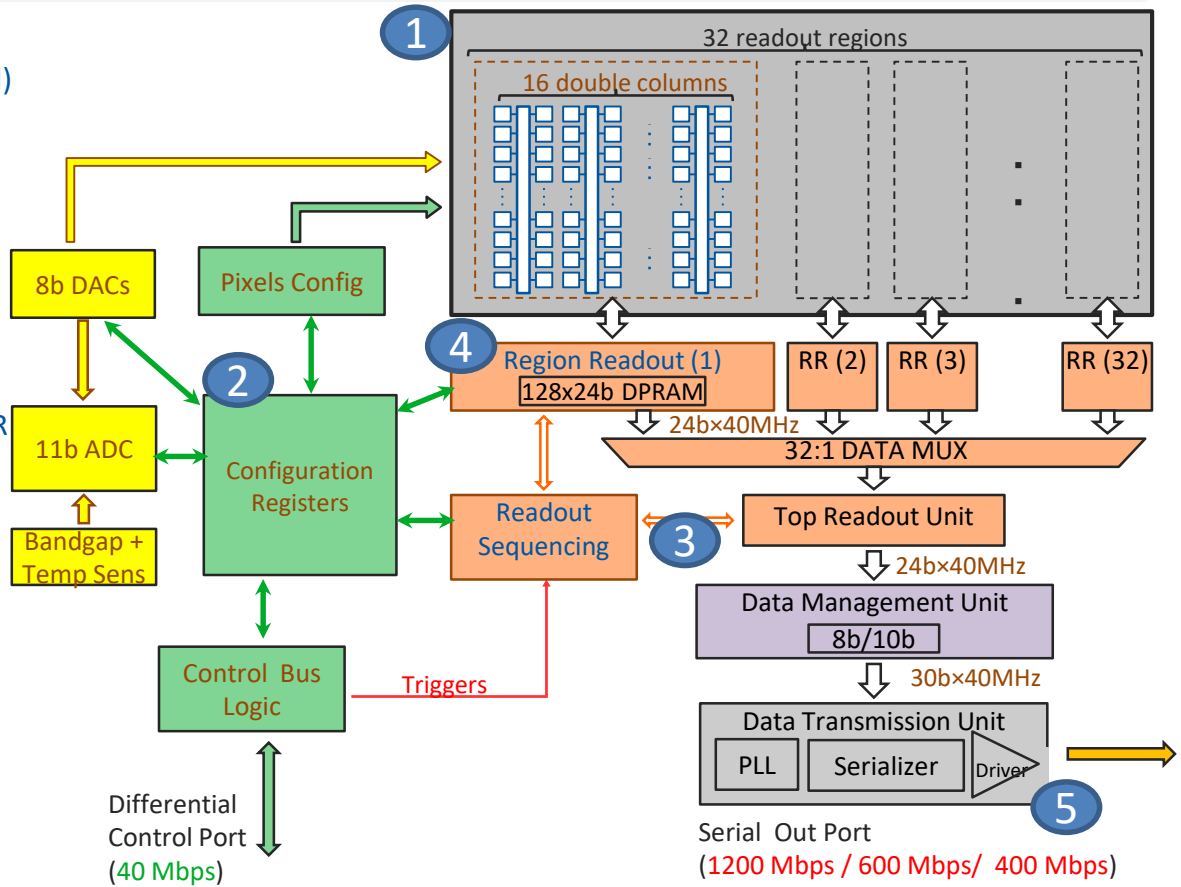
TMR protection on ALPIDE

ALPIDE elements potentially SEU sensitive

1. Pixel Logic: mask and pulse registers (not protected)
Mitigation : Refresh pixel mask bits in background
2. Periphery logic: state machine, FIFO pointers, counters and configuration registers with TMR
3. Top readout unit and data management unit FIFO with Hamming protection
4. Region Readout DPRAM partially protected
   format protected
   hit data not protected
5. Data Transmission Unit: PLL and Serializer with TMR

Basic **T**riple **M**odular **R**edundancy register cell





ALPIDE Radiation Upsets

- SEU impact estimates for elements in chip matrix and periphery (based on cross section values measured using CERN beam tests):
  - **Operation-critical registers protected using TMR**
  - **Probability of corrupted single hit clusters below 1×10^{-10} s^{-1}**
  - **<0.1% of pixel mask bits toggled each hour**
- Pixel mask bits will be refreshed periodically in the background (10 ms deadtime to refresh all pixels in MVTX)
- SEL cross section measured per ALPIDE
  - **About 1 SEL per day in MVTX, automatically recovered**
- The measured SEU and SEL cross sections are not a risk for the operational stability of MVTX

Power Board Radiation

- Power Boards located alongside RUs, same environment
- Power channels tested to 17 krad, bias channels to 20 krad
  - **Good stability (no self oscillations)**
  - **No degradation of noise**
  - **Negligible shifts of voltages and currents**
- Full production Power Board tested at CERN to 14.8 krad TID, no significant effect
- Single Event Upsets observed on current DAC and negative voltage regulator;
  - **expect weeks of operation between power system interrupts**

Radiation studies by LBNL

Power System: CAEN Acquisitions

- CAEN Modules already acquired through LANL LDRD:
  - A3486S, one unit, w/ remote control, $17,5K
  - A3009, Two units, $20,196
  - A2518, Two units, $5343
  - A1676A controller, one unit. $1,919
  - SY4527F mainframe, one unit, $11,136
  - EASY3000, one unit, $3,659
- These can be used as either the primary system, or as backup