sPHENIX MVTX Readout and Controls

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The proposed sPHENIX MVTX system (Monolithic-Active-Pixel-Sensor-based Vertec Detector) consists of ALICE ALPIDE chips, ALICE Readout Units (RU) and ATLAS FELIX PCIe boards, and the Power Supply distribution boards developed by LBNL for the ALICE ITS upgrade.

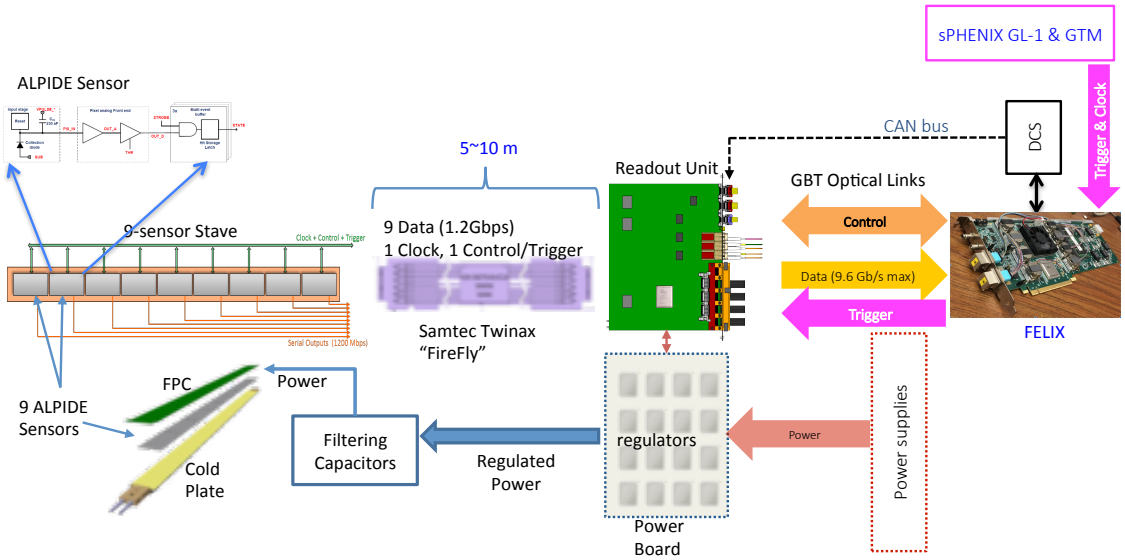
All hardware specs are already determined or to be fixed soon either by ALICE (ALPIDE and RU) and ATLAS (FELIX).

Here we summary the latest high level technical specifications of ALICE ALPIDE chip controls and operations, ALICE RU and ATLAS FELIX boards I/Os, controls and also the PS distribution and monitoring system.

REF:

pALPIDEfs datasheet, v1.0b, Mar 24, 2014
ALPIDE-3 Operation Manual – Draft (Feb. 2, 2016)
ALICE ITS Upgrade, Readout Electronics – WP10 (Jan. 06, 2016)
ALICE ITS Upgrade Report, WP10 Data Rate (May 1, 2015)
ALICE ITS Upgrade TDR (2014)
ATLAS FELIX v1.5 (2016)
sPHENIX CDR (2017, updated)

MVTX Readout and Control System



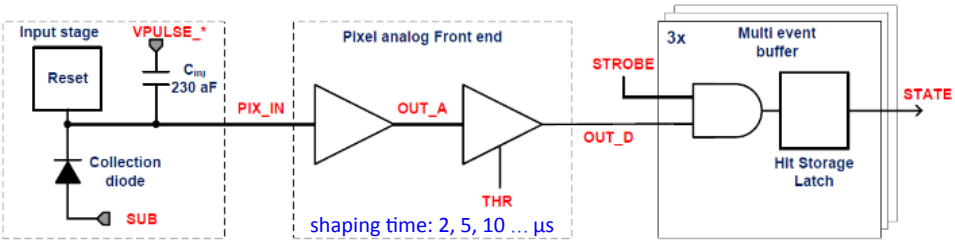
LANL, UT-Austin, LBNL, BNL, ALICE/ITS …

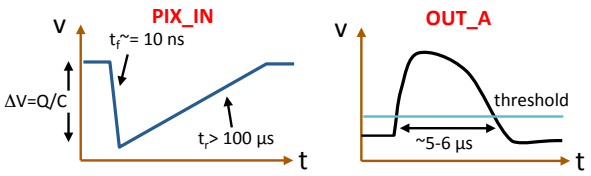
Figure 1 Over view of MVTX readout system.

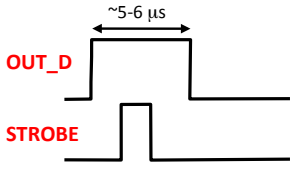
MAPS operation on nutshell:

ALPIDE/MAPS Timing & Operation

Well fit sPHENIX/RHIC environment, 10MHz Clock (LHC 40MHz)



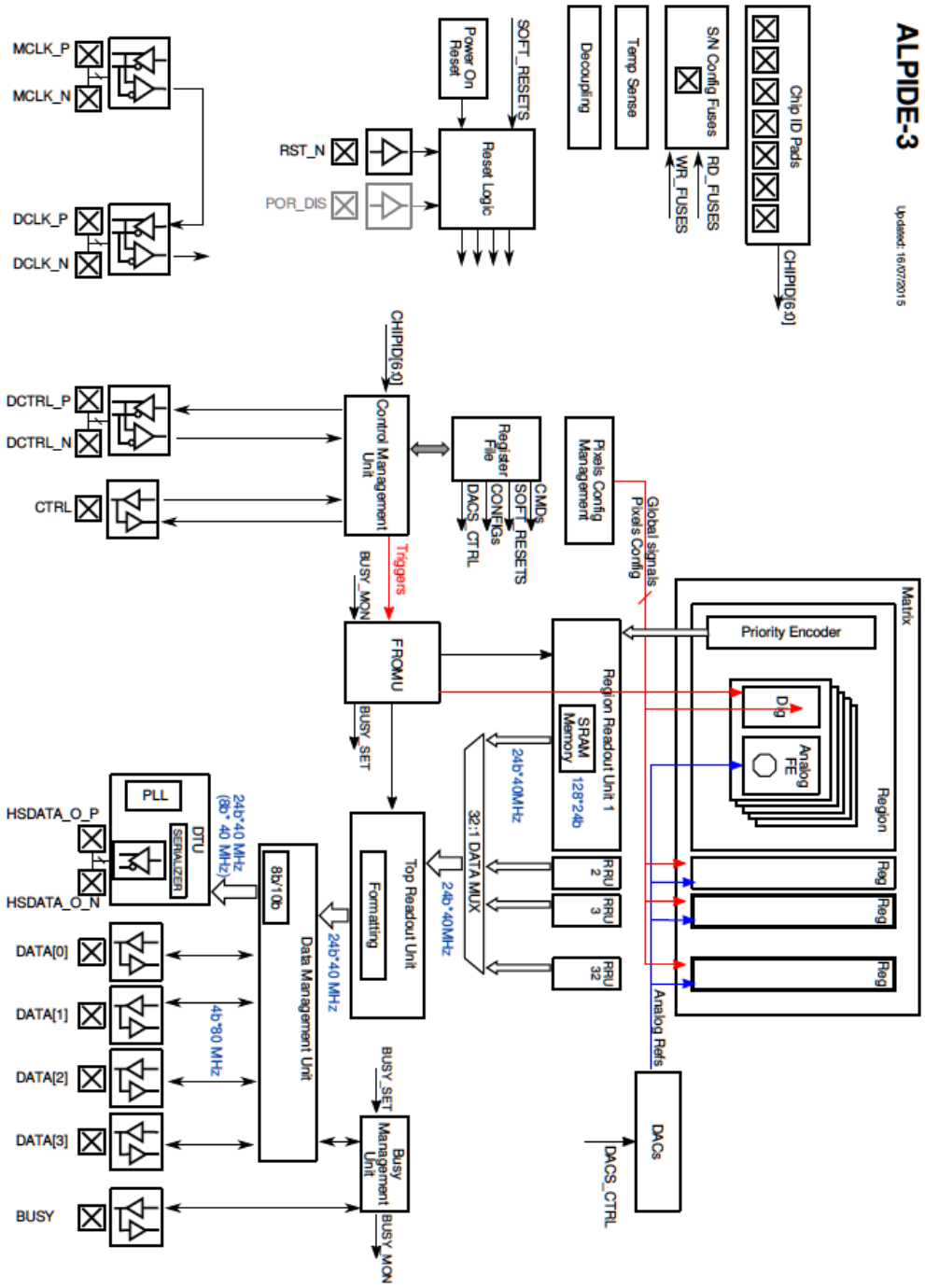




sPHENIX trigger latency: ~4 µs

ALPIDE-3 design on nutshell

Block diagram and pinout. The serial data stream is 8b/20b encoded.



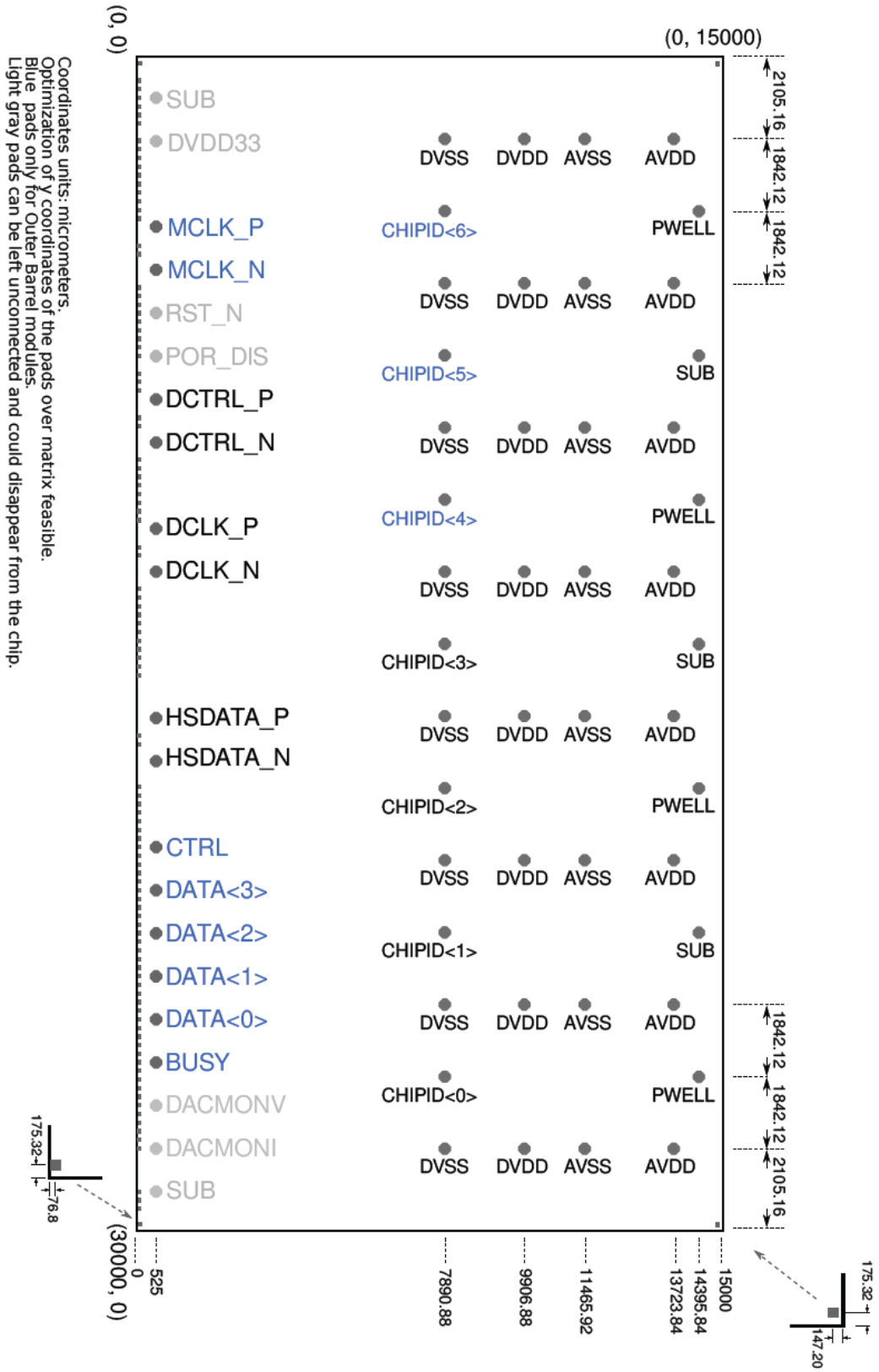


Figure 2 ALPIDE-3 Pad layout

Interface signals:

The main functional I/Os of ALPIDE-3 chip are listed here. The COMS I/Os are 1.8V compatible. The high-speed data line transmits serial data at the maximum rate of 24b x 40MHz = 960Mbps.

Signal	Type	Direction	Purpose
MCLK_P	Differential (MLVDS)	INPUT	Forwarded clock input
MCLK_N	Differential (MLVDS)	INPUT	Forwarded clock input
RST_N	CMOS, internal pull-up	INPUT	Global chip reset
POR_DIS_N	CMOS, internal pull-up	INPUT	Power On Reset Disable
DCTRL_P	Differential (MLVDS)	BIDIR	Differential Control port
DCTRL_N	Differential (MLVDS)	BIDIR	Differential Control port
DCLK_P	Differential (MLVDS)	BIDIR	Main clock input and clock forwarding output
DCLK_N	Differential (MLVDS)	BIDIR	Main clock input and clock forwarding output
HSDATA_P	Differential (LVDS)	OUTPUT	Serial Data Output
HSDATA_N	Differential (LVDS)	OUTPUT	Serial Data Output
CTRL	CMOS, internal pull-up	BIDIR	Control port (OB local bus)
DATA[7]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
DATA[6]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
DATA[5]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
DATA[4]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
DATA[3]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
DATA[2]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
DATA[1]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
DATA[0]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
BUSY	CMOS, internal pull-up	BIDIR	Busy flag
DACMONV	ANALOG	OUTPUT	Current Monitoring Output
DACMONI	ANALOG	OUTPUT	Voltage Monitoring Output
CHIPID[6]	CMOS, internal pull-down	INPUT	Topological chip address
CHIPID[5]	CMOS, internal pull-down	INPUT	Topological chip address
CHIPID[4]	CMOS, internal pull-down	INPUT	Topological chip address
CHIPID[3]	CMOS, internal pull-down	INPUT	Topological chip address
CHIPID[2]	CMOS, internal pull-down	INPUT	Topological chip address
CHIPID[1]	CMOS, internal pull-down	INPUT	Topological chip address
CHIPID[0]	CMOS, internal pull-down	INPUT	Topological chip address

Typos: V and I

The MCLK, DCTRL and DCLK differenctial ports are implemented with a custom designed differential transceiver cell. This has been desgined with reference to the standard TIA/EIA-899 Electrical Characteristics of Multipoint-Low-Voltage-Differential-Signaling (M-LVDS).

MCLK_P, MCLK_N: Clock forwarding input port, used to implement the clock distribution in the Outer Barrel Module application scenario. This is a receiving only port, the driver behind it being disabled in all scenarios. The receiver is enabled when the chip is configured as Outer Barrel Module Master and the signal applied to this port is then forwarded to the DCLK_P, DCLK_N port. A chip configured as Inner Chip or Outer Barrel slave chip keeps the receiver on this port disabled.

RST_N: Global active-low reset signal. The ALPIDE-3 chip includes a power-on-reset circuit. The chip can also be reset by commands issued by the control interface. This port can be left unconnected in applications not needing a dedicated reset pin.

POR_DIS_N: Disabling of the power-on-reset circuit, active low. Driving low this input masks the output of the internal power-on reset circuitry. If the internal power-on-reset is used this pin can be left unconnected since it is internally pulled-up.

DCTRL_P, DCTRL_N: Differential bidirectional control port. Intended to implement the half-duplex control bus segments between the Inner Barrel chips or the Outer Barrel Module Master chips and the off detector electronics. The DCTRL port is unused by a chip configured as Outer Barrel Module Slave Chip.

DCLK_P, DCLK_N: Main clock input and forwarded clock output. Nominal clock frequency is 40 MHz. This is the chip clock source regardless of the operating mode and configuration scenario. In all configurations the receiver circuit at this port provides the clock to the chip core. A chip configured as Outer Barrel Module Master has an active driver on this port and forwards on it the signal received on the MCLK_P, MCLK_N port.

HSDATA_P, HSDATA_N: Differential data output port. This port is used for the high speed serial transmission of data between chips and the off-detector electronics. It is used by chips configured as Inner Barrel Chip or Outer Barrel Module Master. Signaling rate on this port is 1.2 Gb/s in the Inner Barrel Chip configuration and 400 Mb/s in the Outer Barrel Module Master configuration. The serial stream is (by default) 8b/10b encoded.

CTRL: Single ended, bidirectional control port. Intended to implement the half-duplex local control bus segments between the Outer Barrel Module Master chip and the associated slaves. These chips shall have their CTRL ports directly connected by a single shared wire. The CTRL port is unused by a chip configured as Inner Chip.

DATA[7:0]: CMOS bidirectional data port. Intended to implement a shared parallel data bus between the Outer Barrel Module Slave chips and the associated Master. By default, the 4 lowermost lines of this port operate in Double Data Rate mode, with bits launched or sampled at both clock edges and one complete byte transfer completed at every clock cycle. Thus the uppermost 4 bits can be left unconnected and the bus can be implemented using 4 parallel wires shared by the chips. Optionally, the chips can be configured to revert to Single Data Rate signaling also on the lowermost 4 bits. In this case one byte is launched or sampled at every rising edge of the clock. This operating mode can be used for readout of chips through a 8 bit Single Data Rate parallel bus.

BUSY: Single ended port. It is intended to implement the communication of the BUSY state between the Outer Barrel Module Slaves and the associated Master chip by wiring in parallel all

their BUSY ports. This port is not used when the chip operates as an ITS Inner Barrel chip. This port can be in one of two states: actively driven low or high impedance, thus emulating an open-drain topology. The signaling is active low. The pad provides weak internal pull-up. An external strong pull-up resistor might be required to speed-up the rise-time of the de-assertion (rising) edge depending on the total capacitance of the line and the number of chips connected to it. The sampling of the input on this port is equipped with a sychronizer to guarantee reliable operation.

DACMONV: Analog pin with dual purpose. It can be used to monitor each of the voltages generated by the on-chip voltage DACs. It can also be used to override the internal voltage DACs. The overriding is possible for one user-selectable DAC at a given time.

DACMONI: Analog pin with triple purpose. It can be used to monitor each of the currents generated by the on-chip current DACs. It can also be used to override the internal current DACs. The overriding is possible for one user-selectable DAC at a given time. It can also be used to override the internal current reference, thus changing the range of all current DACs simultaneously.

CHIPID[6:0]: Chip topological address and mode selection. This port is intended to assign a binary coded address to each chip depending on its position on the ALICE ITS Modules. The address is used in the transactions via the control interface. The address value also selects if the chip behaves as a Inner Barrel Chip, an Outer Barrel Module Master chip or an Outer Barrel Module Slave chip. This pads have been designed to be directly wired to digital supply in order to set a binary '1' on a given line. Leaving one unconnected effectively sets to '0' the corresponding bit line due to the internal pull-down.

Supply, ground and bias nets:

Net	Type	Purpose
AVDD	SUPPLY	Analog domain supply
AVSS	GROUND	Analog domain ground
DVDD	SUPPLY	Digital domain supply
DVSS	GROUND	Digital domain ground
DVDD33	SUPPLY	Fuses programming supply
PWELL	SUBSTRATE	Substrate bias
SUB	SUBSTRATE	Substrate bias

Recommended operating conditions:

		MIN	TYP	MAX	Unit	Condition
AVSS	Analog ground		0		V	
AVDD	Analog supply	1.62	1.8	1.98	V	
DVSS	Digital core ground		0		V	
DVDD	Digital core supply	1.62	1.8	1.98	V	
PWELL	Substrate bias		0	0	V	Shorted to AVSS
SUB	Substrate bias		0	0	V	Shorted to AVSS
V_I	Voltage at any CMOS input	0		DVDD	V	
V_{IL}	Low level digital input voltage			0.33*DVDD	V	
V_{IH}	High level digital input voltage	0.66*DVDD			V	
I_{OL}	Low level digital output current			13.7	mA	Vo <0.45
$\|I_{OH}\|$	High level digital output current			13.6	mA	Vo >DVDD-0.45
V_P or V_N	Voltage at any differential bus terminal	0		DVDD	V	
$\|V_{ID}\|$	Magnitude of differential input voltage	50		DVDD	mV	
R_L	Differential load resistance	40	50	60	Ω	
T	Operating temperature	-25	25	85	℃	

Control interface and protocol

Chip identification: CHIPID[6:0]

HSB: CHIPID[6:4] are used to identify the chip operation mode – 1) Inner Barrel; 2) Master 3) Slave. For MVTX application, all bits are set to 0, b000xxxx .

CHIPID[3:0] are used to identify the location of a chip in a stave.

Control interfaces:

The slow control interfaces sere two purposes:

1) provide read/write access to internal registers, commands, configuration and memories;
2) distribute trigger commands and broadcast synchronous signals

For the MVTX application (ALICE ITS/IB mode), only the differential DCNTRL port is used.

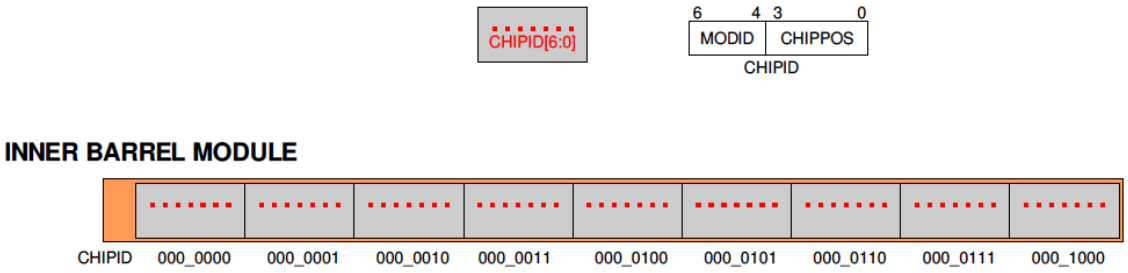


Figure 3 Illustration of chip identification and geographic address allocation.

The nie(9) chips on the IB module are directly connected to a shared control differential line using the DCNTRL port. The control bus is entirely based on differential singaling and has multipoint topology.

Control transactions format:

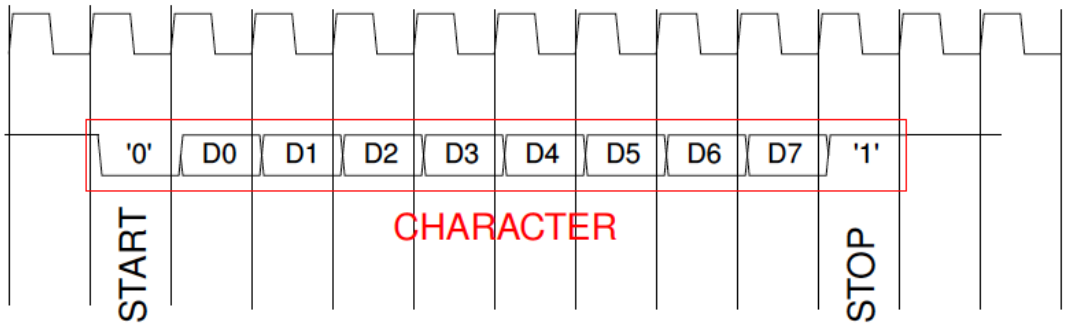


Figure 4 Format of a single charachter ecchanged on the control bus.

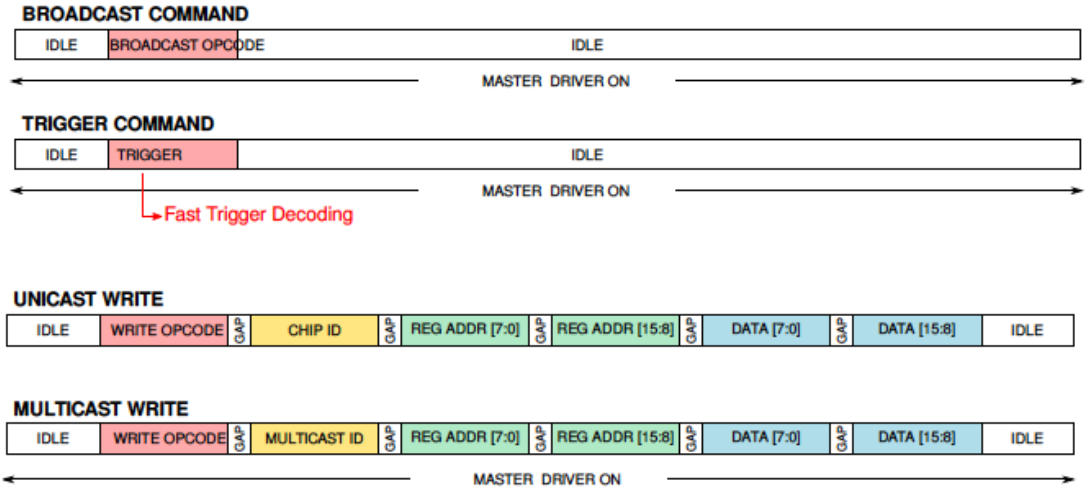


Figure 5 Format of valid transactions on the control bus. Note for MVTX, all chips are operating in the Master Mode.

The ALPIDE-3 control interface provideds access to the chip internal registers and data path memories, with 16-bit wide address field and 16-bit wide data payload.

Opcode	Hex value	Purpose
TRIGGER	8'hB1	Trigger command
TRIGGER	8'h55	Trigger command
TRIGGER	8'hC9	Trigger command
TRIGGER	8'h2D	Trigger command
GRST	8'hD2	Chip global reset
PRST	8'hE4	Pixel matrix reset
PULSE	8'h78	Pixel matrix pulse
BCRST	8'h36	Bunch Counter reset
RORST	8'h63	Readout (RRU/TRU/DMU) reset
WROP	8'h9C	Start Unicast or Multicast Write
RDOP	8'h4E	Start Unicast Read

Figure 6 Valid opcodes of control transactions.

Here are a few important registers:

Periphery Control Registers:

Bits	Purpose
1:0	Chip Mode selector
2	Clustering enable
3	Start Memory Self Test
4	Unused
5	Matrix Readout Speed
6	Force Busy
7	Force Busy Value
15:8	Not used

- **Chip Mode Selector** – 0: Configuration Mode (default), 1: Readout Triggered Mode, 2: Readout Continuous Mode.
- **Clustering Enable** – 0: Clustering disabled, 1: Clustering enabled (default)
- **Start Memory Self Test** – Bit will auto reset, memory status is written on bit 1 of Region Readout Status Register.
- **Matrix Readout Speed** – 0: 10MHz, 1: 20MHz (default).
- **Force Busy** – 0: disabled (default), 1: BUSY line is forced to the value specified in Force Busy Value bit.
- **Force Busy Value** – Logical value forced in the BUSY line when Force Busy is asserted.

Pixel CFG Registers:

In each pixel there are two wriable registers: 1) te Mask register and 2) the Pulse Enable register.

Pixel CFG Register 1:

Bits	Purpose
8:0	Pixel row selector
9	Sets all rows
10	PIXCNFG_REGSEL
11	PIXCNFG_DATA
15:12	Not used

- **Pixel Row Selector** – Value of a single row to be selected
- **Set All Rows** – Set to 1 to select all rows
- **PIXCNFG_REGSEL** – Selection of the in-pixel register to be addressed: 0: for the Pulse Enable register, 1: for the Mask register
- **PIXCNFG_DATA** – Bit to be written in the target register

Pixel CFG Register 2:

Bits	Purpose
9:0	Pixel column selector
10	Sets all columns
15:11	Not used

- **Pixel Column Selector** – Value of a single column to be selected
- **Set All Columns** – Set to 1 to select all column

DACs setting registers:

For each of DACs, there are 8-bit setting field. The default values are show below.

Summary of ALPIDE-3 registers and memory addressing.

Address[15 : 0]			Mode	Reset	Register or memory
RGN_ADDR [4 : 0]	BASE_ADDR [2 : 0]	SUB_ADDR [7 : 0]			

NC	0	0	R/W	h0000	Command Register.
NC	0	1	R/W	h0020	Periphery Control register
NC	0	2	R/W	h0000	Region Disable Register 1
NC	0	3	R/W	h0000	Region Disable Register 2
NC	0	4	R/W	h0010	FROMU Configuration Register 1
NC	0	5	R/W	h0000	FROMU Configuration Register 2
NC	0	6	R/W	h0000	FROMU Pulsing Register1
NC	0	7	R/W	h0000	FROMU Pulsing Register 2
NC	0	8	R	-	FROMU Status Register 1
NC	0	9	R	-	FROMU Status register 2
NC	0	10	R/W	h0AAA	DAC settings for DCLK/MCLK I/O buffers
NC	0	11	R/W	h00AA	DAC settings for CMU I/O buffers
NC	0	12	R/W	h008F	CMU and DMU Configuration Register
NC	0	13	R	-	CMU Errors Counter
NC	0	14	R/W	h008D	DTU Configuration Register
NC	0	15	R/W	h0088	DTU DACs Register
NC	0	16	R	-	DTU PLL Lock Register 1
NC	0	17	R/W	h0000	DTU PLL Lock Register 2
NC	0	18	R/W	h0000	DTU Test Register 1
NC	0	19	R/W	h0000	DTU Test Register 2
NC	0	20	R/W	h0000	DTU Test Register 3
NC	0	21	R/W	h0008	BUSY min width
NC	0	22	R/W	h0000	Fuses Write LSBs
NC	0	23	R/W	h0000	Fuses Write MSBs
NC	0	24	R	-	Fuses Read LSBs
NC	0	25	R	-	Fuses Read MSBs
NC	0	26	R	-	Temperature Sensor
0-31	1	0-127	R/W	-	RRU MEB LSBs.
0-31	2	0-127	R/W	-	RRU MEB MSBs
0-31	3	0	R/W	h0000	Double Column Disable Register
NC	4	0	R	-	DMU and TRU State
NC	5	0	R/W	h0000	Pixel CFG Register 1
NC	5	1	R/W	h0000	Pixel CFG Register 2
NC	5	2	R/W	h0000	Pixel CFG Register 3 (Special Behaviour)
NC	6	0	R/W	h0400	Analog Monitor and Override Register
NC	6	1	R/W	h0075	VRESETP
NC	6	2	R/W	h0000	VRESETD
NC	6	3	R/W	h0056	VCASP
NC	6	4	R/W	h0039	VCASN
NC	6	5	R/W	h00FF	VPULSEH
NC	6	6	R/W	h0000	VPULSEL
NC	6	7	R/W	h0040	VCASN2
NC	6	8	R/W	h0000	VCLIP
NC	6	9	R/W	h0000	VTEMP
NC	6	10	R/W	h0000	IAUX2
NC	6	11	R/W	h0032	IRESET
NC	6	12	R/W	h0040	IDB

NC	6	13	R/W	h0040	IBIAS
NC	6	14	R/W	h0033	ITHR
NC	6	15	R/W	h0000	Buffer Bypass Register
0-31	7	0	R	-	Region Readout Status Register

Triggering and Timing

There are two readout modes for ALIPIDE chips – 1) triggered and 2) Continuous.

For sPHENIX we foresee to use the trigger mode as sPHENIX data taking will be mainly based triggers (maximum rate = 15kHz).

A readout STROBE signal will be generated after receiving an external trigger. The STROBE length is programmable, the default value is 50ns (less than one RHIC clock).

The expected sPHENIX LVL-1 trigger latency is about 4 us, based on our experience from PHENIX operation at RHIC.

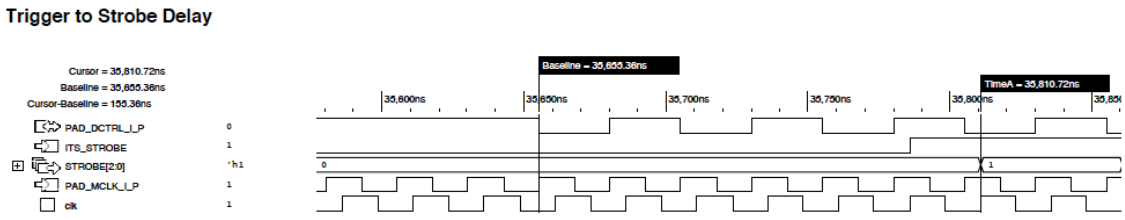


Figure 7 Trigger and Strobe decay

RHIC clock is 9.4MHz, much slower than the LHC clock of 40MHz. All sPHNIX and MVTX trigger and timing is synchronized to the 9.4MHz RHIC clock.

We plan to operate ALIPDE chips at the same 40MHz LHC clock. This new 40MHz clock will be generated and phase locked to the RHIC 9.4MHz clock, mostly likely at FELIX end.

A dedicated daughter card will be developed by the BNL ATLAS group for the next version FELIX board v.20, to allow 9.4MHz RHIC clock as input.

Data Readout

We will use the high-speed data transmission line to send data from ALPIDE chip to the RU through FireFly cables. The serial port implements a clock synchronous transmission based on the 600MHz clock produced by the internal PLL. Data are 8b/10b encoded with the LSB launched first. Further more, a bit is sent on every

clock edge. It is important to note that data area loaded for transmission 30-bit at a time – 3 characters of 10-bit encoded bytes. For MVTX, the 600MHz clock signal is directly used to produce DDR stream at 1.2Gbps.

Data Format:

We will use the same data format defined by the ALICE ITS upgrade. The valid data words are identified by predefined prefix bit strings.

Data Word	Lenght (Bits)	Value (binary)
IDLE	8	1111_1111
COMMA	8	1011_1100
CHIP HEADER	16	1010<chip_id[3:0]><frame_start_data[7:0]>
CHIP TRAILER	16	1011<readout_flags[3:0]><reserved[7:0]>
CHIP EMPTY FRAME	24	1110<chip_id[3:0]><frame_start_data[7:0] ><reserved[7:0]>
REGION HEADER	8	110<region_id[4:0]>
DATA SHORT	16	01<data_field[13:0]>
DATA LONG	24	00<data_field[13:0]>_0_ <hit_map[6:0]>
BUSY ON	8	1111_0001
BUSY OFF	8	1111_0000

COMMA Control symbol for the 8b/10b encoding to be transmitted only on the serial port. Standard K28.5 words with running disparity are utilised. Thus, the encoded COMMA value of 8'hBC is either 10'b001111_1010 or 10'b110000_0101 depending on the running disparity. The COMMA transmission can be used for clock recovery and synchronisation to the data stream. The COMMA word can be observed in the following scenarios:

- When there is no readout in progress and the chip is completely idle.
- When there is a readout in progress but the chip hasn't had enough time to process data and/or pack it. This would typically happen:
  1. following a CHIP HEADER on an IB before the readout and processing has been completed.
  2. in the first frame payload on an OB before the chip has had a chance to pack data for maximum transmission efficiency.

IDLE Also referred to as NOP for historical reasons, the IDLE codeword can be observed in two different scenarios :

- In an OB, on the local bus when it is compeletly undriven i.e. there is no readout in progress
- In an OB, IDLEs are stripped from the data stream except for turnover byte when the virtual token is passed over (see Section 3.4.3)
- In an IB, when a word as defined in Table 3.28 is less than 3 bytes, that word is padded with IDLE words to bring the total to 3. For example, that means 2 × IDLE word padding for a REGION HEADER and a single IDLE for a DATA SHORT.

CHIP HEADER Symbol transmitted at the beginning of each data frame. Bits CHIPID[3:0], which are sent as the least significant nibble of the first CHIP HEADER byte, identify the geographical location of a given chip on a ITS module. Additionally, the second byte of the CHIP HEADER word contains bits [7:0] of the 9 bit Frame Start Data information. That data field has the following composition :

frame_start_data[7:0] = <BUNCH_COUNTER_FOR_FRAME[8:3]><STROBE_COUNTER[1:0]>

where BUNCH_COUNTER_FOR_FRAME is an internal 40 MHz running counter meant to be synchronised to the LHC Bunch Crossing Counter via the BCRST instruction (Table 3.1.3) and STROBE_COUNTER is an internal counter incremented every time the internal a STROBE pulse is propagated to the Matrix.

CHIP TRAILER Byte transmitted at the end of each data frame.

Data composition of the variable field <readout_flags[3:0]> can be structered in one of two ways:

- In the case of a busy signal violation (TRIGGER sent while BUSY is still asserted and we are operating in TRIGGERED mode):

$$< readout\_flags[3:0] >= \{< is\_busy\_violation >< 3'b000 >\}$$

- When there is no busy violation or we are operating in CONTINUOUS mode :

$$< readout\_flags[3:0] >= \{< 1'b0 >< FLUSHED\_INCOMPLETE > < FATAL >< BUSY\_TRANSITION >\}$$

The flags outlined above are generated as follows:

- IS_BUSY_VIOLATION – when the BUSY has been asserted and a new TRIGGER is received whilst in TRIGGERED mode.
- FATAL – when the Frame Start Fifo is full (depth 16) and another a new TRIGGER is sent. Only observed in CONTINUOUS Mode.
- FLUSHED_INCOMPLETE – in Continuous Readout Mode only, when a MEB slice was flushed in order to ensure that the MATRIX always has a free memory bank for storing new events. Only observed in CONTINUOUS Mode.
- BUSY_TRANSITION – when the BUSY has been set during the readout of the frame in question. Only observed in CONTINUOUS Mode.

Finally, the reserved[7:0] field was incorporated in the data format in order to simplify the token exchange logic on the OB. This field is set to be an IDLE byte.

CHIP EMPTY FRAME Word transmitted at the beginning of an empty data frame. This conserves a byte of bandwidth as opposed to sending a CHIP HEADER followed by a CHIP TRAILER. Bits CHIPID[3:0], which are sent as the least significant nibble of the first CHIP EMPTY FRAME byte, identify the geographical location of a given chip on a ITS module. Additionally, the second byte of the CHIP HEADER word contains bits [7:0] of the 9 bit Frame Start Data information (see CHIP HEADER for a detailed description of data encapsulation). Finally, the reserved[7:0] field was incorporated in the data format in order to simplify the token exchange logic on the OB. This field is set to be an IDLE byte.

REGION HEADER Chip data frames are made of 32 region data frames. Each region data frame is initiated with this word. The variable part *region_id[4:0]* is the index of the region. Region data frames are sent sequentially in ascending order. The region header is only sent for regions with data content.

DATA SHORT Pixel hit data information container. This word is used to transmit pixel hit position information. Is is used for single pixel hits when clustering is enabled or for all pixel hits when clustering is disabled. The variable field in the DATA SHORT word has the following structure:

data_field[13:0] = <encoder_id[3:0]><addr[9:0]>

where *encoder_id* is the index of the priority encoder inside a region and *addr* is the pixel hit index generated by the priority encoder.

DATA LONG Pixel hit data information container. This word is used to transmit cluster information. It is generated only when clustering is enabled. The variable field in the DATA LONG word has the following structure:

¡ data_field[13:0]><hit_map[7:0]]>= <encoder_id[3:0]><addr[9:0]><hit_map[6:0]>

where *encoder_id* is the index of the priority encoder inside a region, *addr* is the pixel hit index generated by the priority encoder for the first hit in a cluster and *hit_map[6:0]* contains the cluster shape information in the form of a bit map. A bit in the hit_map is set for any active pixel among the 7 immediately after (based on PE pixel addreses) the one indicated by the addr[9:0] field. The LSB of hit map corresponds to first subsequent pixel and bit 6 to the 7th. Therefore, a DATA LONG can transmit a maximum of 8 pixels at once.

BUSY ON Code word transmitted on assertion of the BUSY status. Transmitted on both the serial link and on the parallel bus. See Section 3.4.3 for further notes on the BUSY signaling mechanism.

BUSY OFF Code word transmitted on the serial port on de-assertion of the BUSY status. Transmitted on both the serial link and on the parallel bus.

Data format rules:

- Data words are transmitted byte by byte, most significant byte first.
- IDLE, BUSY_ON and BUSY_OFF words can be arbitrarily inserted betweeen other code words.
- Words that are 16 or 24 bits (DATA SHORT, DATA LONG, CHIP HEADER, CHIP EMPTY FRAME) cannot be split by a IDLE or a BUSY.
- The BUSY words are transmitted as soon as possible without violating data integrity.

The Front-End Electronics - Readout Unit (RU)

RU is developed by the ALICE experiment to readout out ALICE/ITS detectors. We will use RU with minimal modification for the sPHENIX MVTX system, one RU per stave of 9 ALIPIDE chips. The RU interfaces the sensors on the stave, control and trigger systems of the sPHENIX experiment. RU collects the high-speed data stream from the sensors and convert them into optical signal through the GBT optic links to the beck-end electronics (currently envisioned to use FELIX boards developed by ATLAS) in the Counting House. It manages control lines which distribute RHIC clock, sPHENIX trigger and other slow control commands. RU also implements ancillary functions such as power supply control and monitoring.

The main functionalities of the Readout Unit are summarized here:

- Receive and distribute clock and trigger to the sensors
- Collect high-speed data stream from sensors and send repackaged data to the Beck-End (FELIX) via TGB links,
- Handle busy signal from the sensors
- Monitoring the sensor status
- Perform power monitoring and safety control & interlock

A single RU serves one full stave composite of 9 ALPIDE sensors, hosting 3 GBT links paired with 2 FPGA, each FPGA can read up to 16 links from the stave. For MVTX application, only one FPGA is used for readout, leaving the 2nd one as a spare for backup. There are a total of 48 RUs in the MVTX readout system.

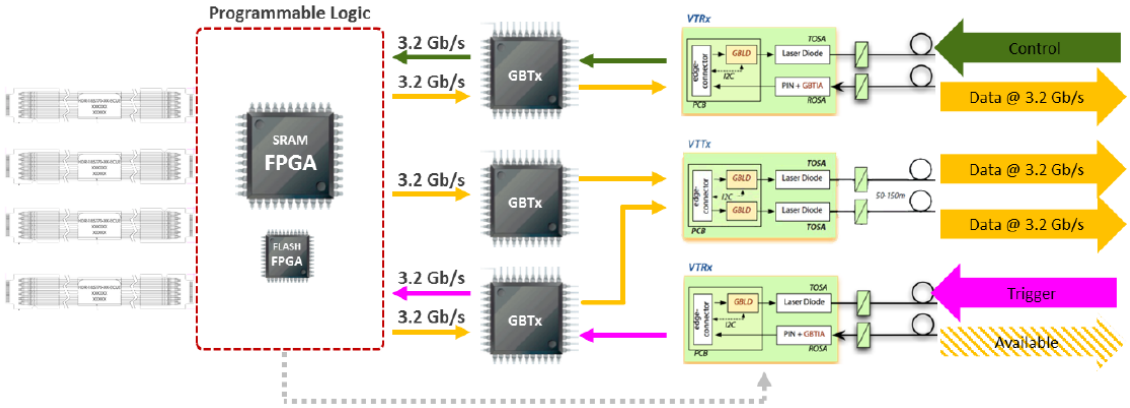


Figure 8 Diagram of MVTX Readout Unit. One RU serves one 9-chip stave. The Beck-End are served by FELIX boards hosted on sPHENIX DAQ Servers in the counting house.

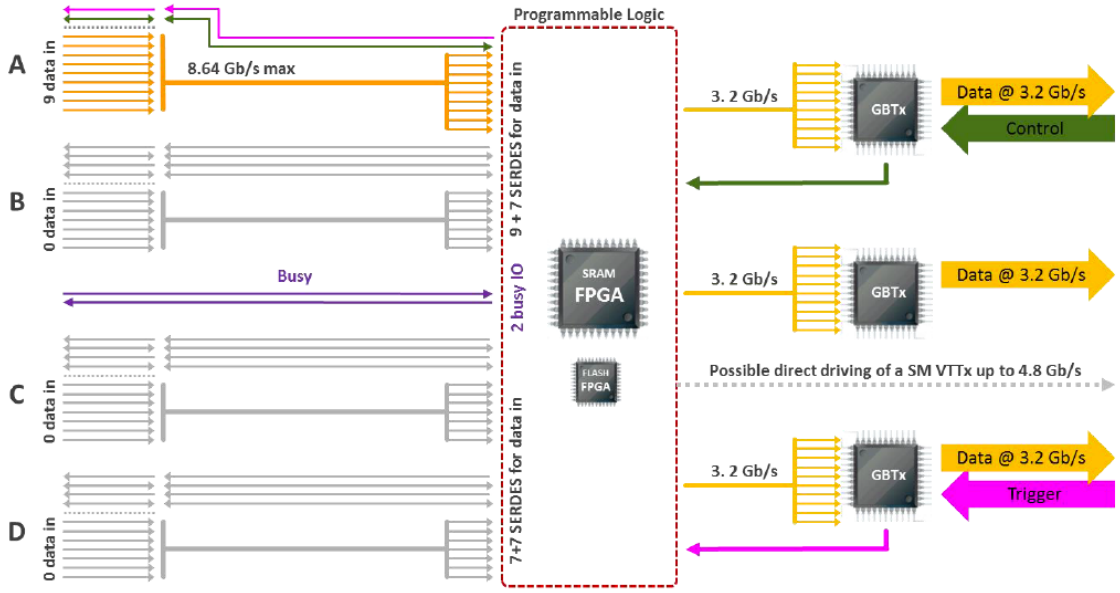
The GBT Versatile Link payload bandwidth is 3.2Gb/s. Here we summarize the RUs and GBTx chipsets needed to readout the entire 48 MVTX detector staves for the maximum design rates.

Readout Units and GBT links for maximum design rates

Layer	Staves	Copper assemblies	Copper capacity	RUs per stave	RUs per layer	VTRx count	VTTx count	Data fibers	Control fibers	Data fibers capacity	Data fibers usage
			[Gb/s]							[Gb/s]	[%]
0	12	12	103.7	1	12	24	12	36	12	115.2	90.0
1	16	16	138.2	1	16	32	16	48	16	153.6	90.0
2	20	20	172.8	1	20	40	20	60	20	192	90.0

Figure 9 Maximum data rate for each MVTX layer

Here we show the MVTX data and control routing schematic layout. It is worth to mention that for the sPHENIX baseline program (200kHz Au+Au), a single GBTx chip will provide enough bandwidth and the others could be used to hot-swap fiber links in case of connection problems. A MVTX stave is connected to the first connector A, with clock and control (2 lines) and 9 data lines running over the 12 available FireFly copper links.



sPHENIX MVTX actual bandwidth requirements:

The projected maximum collision rates for sPHENIX are summarized below:

System	Energy	$dN_{ch}/d\eta$	Highest Rate
p+p	200 GeV	2.29	12.9 MHz
p+Au	200 GeV	9.16	2.8 MHz
Au+Au	200 GeV	190	219 kHz

ALICE has simulated data rate based on Pb+Pb collisions at the top collision rate of 200kHz (ALICE projected rate for Run-3 is 50kHz). With 2us shaping time of ALPIDE chip (the fastest shaping mode, also planned for sPHENIX MVTX operation), the estimated RU average data rate at 200kHz triggered readout is [Gb/s]:

- Layer-0: 4.8 Gb/s, or 1/2 of the hardware bandwidth limit (9.6Gb/s)
- Layer-1: 3.2 Gb/s, or 1/3 of the hardware bandwidth
- Layer-2: 2.4 Gb/s, or ¼ of the hardware bandwidth

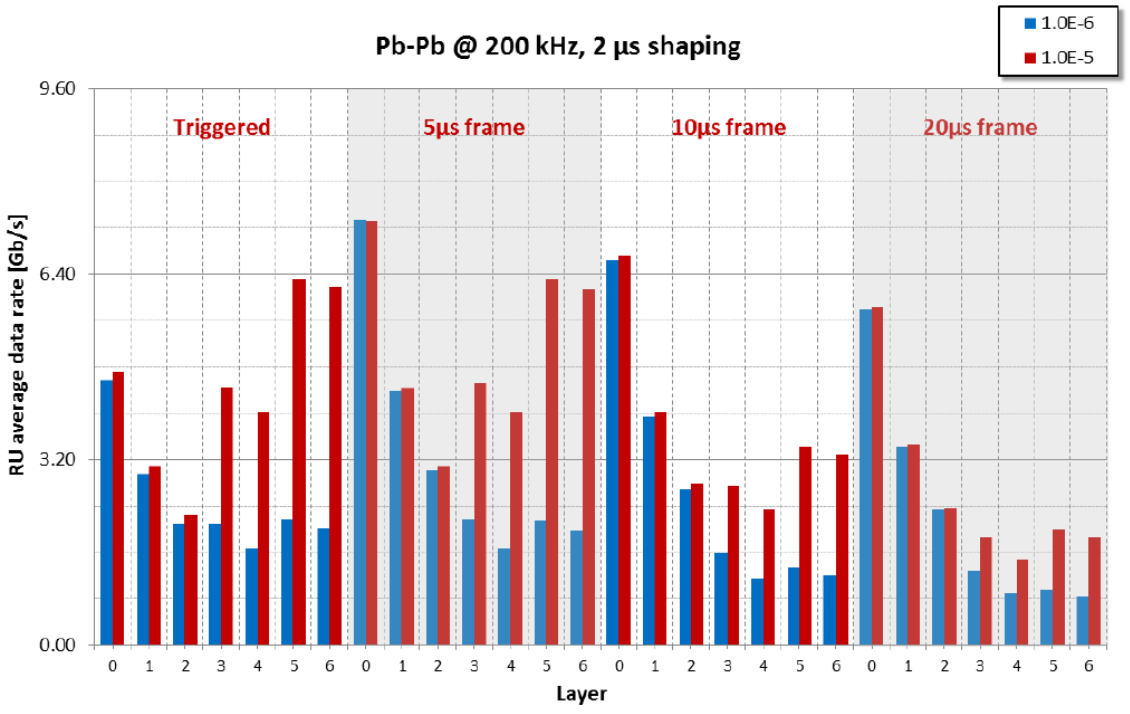


Figure 10 ALICE RU average data rates for Pb-Pb collisions at 200kHz, with 2us ALPIDE shaping time. Both triggered and continuous readout modes are simulated. The MVTX/sPHENIX is designed to operate in the triggered mode with maximum rate of 15kHz.

The average event multiplicity of Au+Au collisions in sPHENIX is estimated about 1/5 – 1/4 of the multiplicity of Pb+Pb collisions at ALICE/LHC.

sPHENIX MVTX vs ALICE ITS/IB

	ALICE (Run3)	sPHENIX (Max)
Pb+Pb / Au+Au	100 kHz (50kHz)	200 kHz
p+p	400 kHz (200kHz)	13 MHz
Trigger/Readout	>50 kHz	15 kHz

Event track multiplicity dN/dη: sPHENIX = 1/3 ALICE (pp), 1/5 ALICE(AA)

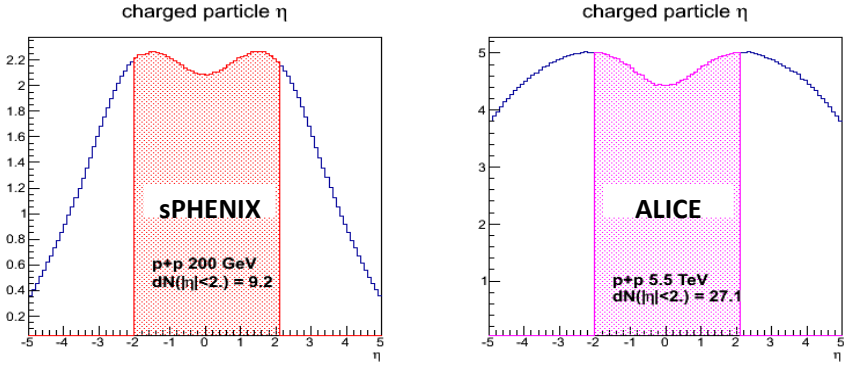


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Figure 11 Event track multiplicities of p+p collisions from sPHENIX and ALICE.

Furthermore, sPHENIX is designed to take data at 15kHz trigger rate. So the expected data rate from sPHENIX is about ¼ x 15/200 of ALICE/ITS IB (~1.9%).

The expected MVTX average RU data rates for Au+Au collisions at RHIC are:

- Layer 0: 0.1 Gb/s
- Layer 1: 0.07 Gb/s
- Layer 2: 0.05 Gb/s

They are well below the hardware limit of 9.6Gb/s per RU with 3 GBT links. MVTX has the capacity to take all 200kHz Au+Au collisions at RHIC! For the p+p collisions at RHIC, since the event multiplicity is very low compared to Au+Au collisions, the

expected data rate is order of magnitude below the Au+Au rate. Later, one can consider to develop MVTX-based trigger for sPHENIX.

The overall data rate from MVTX is:

0.1 x 12 + 0.07 x 16 + 0.05 x 20 = 3.3Gb/s

The sPHENIX DAQ bandwidth is designed to handle 80Gb/s data to HPSS.

The Back-End Electronics – FELIX

FELIX board developed by BNL for the ATLAS upgrade project is chosen as the default path for MVTX/sPHENIX beck-end option.

FELIX has 48 bi-directional optical links that can be coupled to RU GBT links. One FELIX board will readout 8 RUs, using 24 fiber links. A total of 6 FELIX boards are required to readout all 48 RUs, with one FELIX board per Server that does event building and data compression.

Basic functions of FELIX:

- PCIe Gen3 x 16 lane
- 48 bi-directional optical links upto 14 Gb/s
- With circuit to interface Timing & Trigger Control system (TTC) for both LHC and RHIC experiments
- Micro-controler to support FPGA reprogramming and firmware update

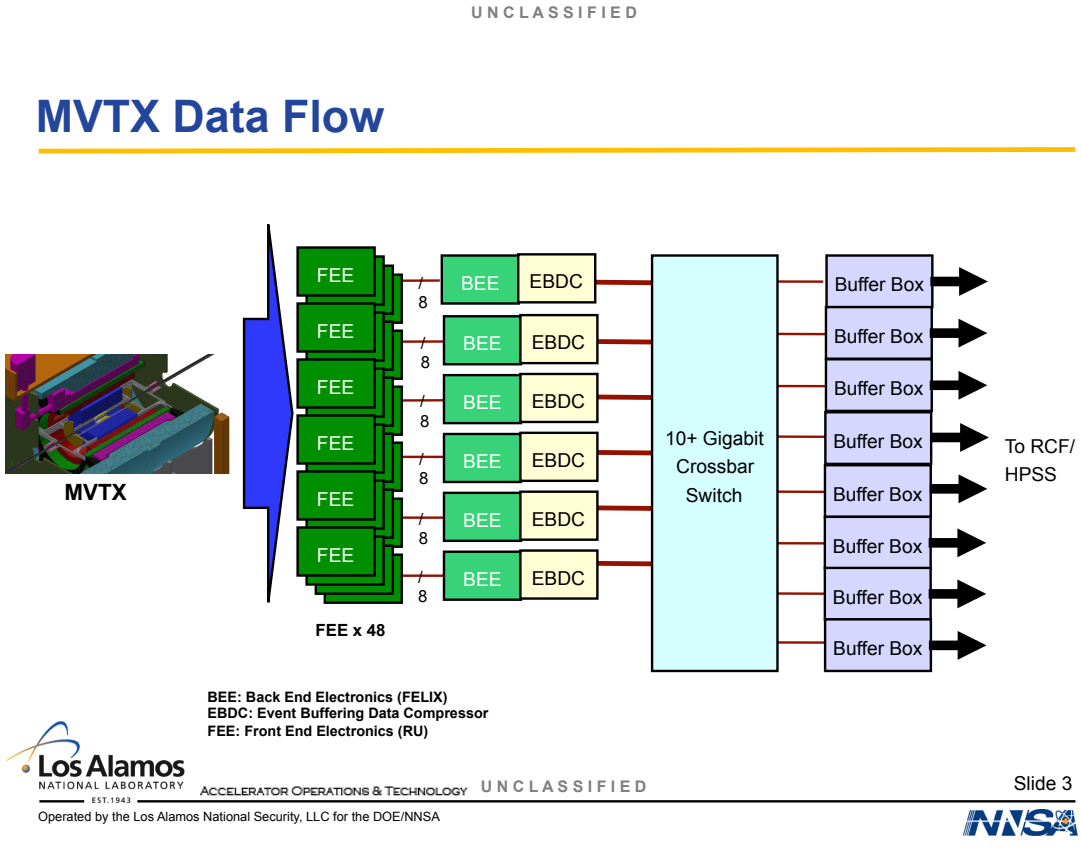

Figure 12 Layout of the MVTX readout and sPHENIX DAQ system.

The current FELIX version 1.5 can only operate with LHC clock of 40MHz. A new version 2.0 is designed to be able to handle 10MHz RHIC clock through an on board Timing & Trigger Mezzanine card. We foresee this new FELIX boards will be used for both MVTX and TPC detectors in the PHENIX experiment.

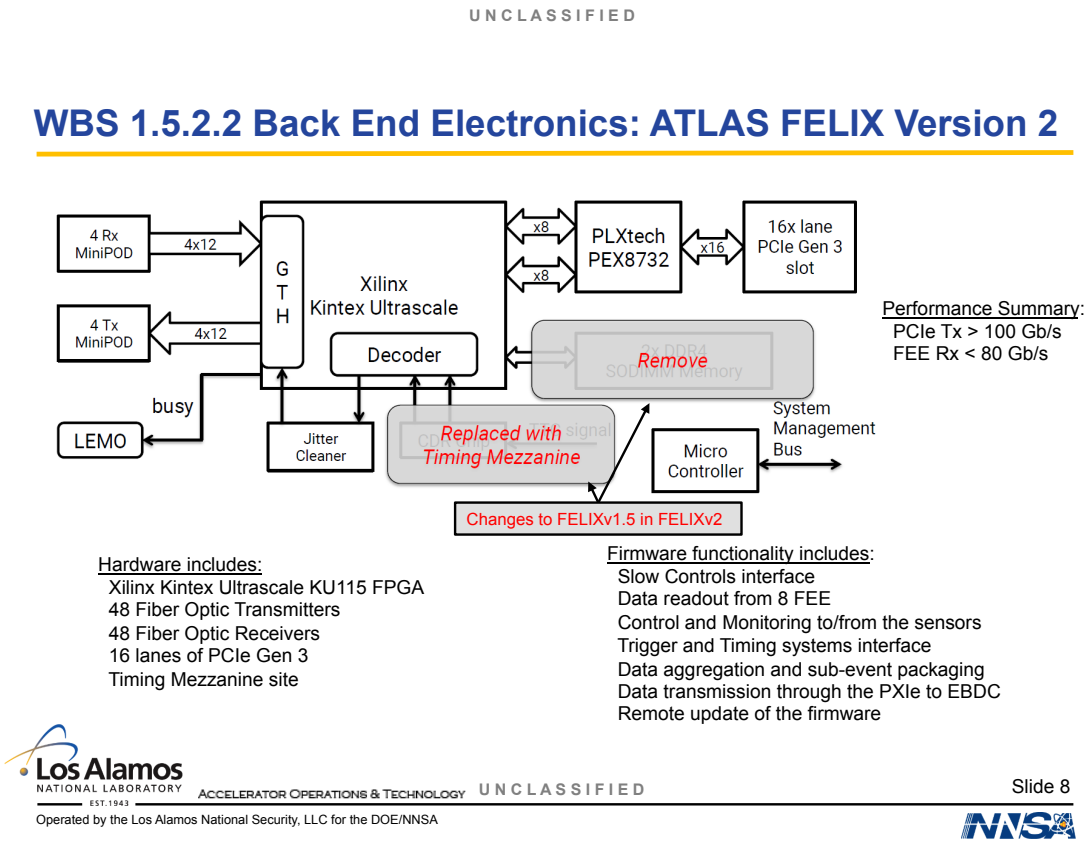

Figure 13 ATLAS FELIX board will be used for the sPHENIX MVTX readout.

Power System

The MVTX power system is based on ALICE/ITS-IB system developed by LBNL. The system distribute clean analogy, digital and bias posers to the sensors, and also provide detector health status through remote readout. A near final prototype will be available for R&D at LANL by the end of this summer, 2017.

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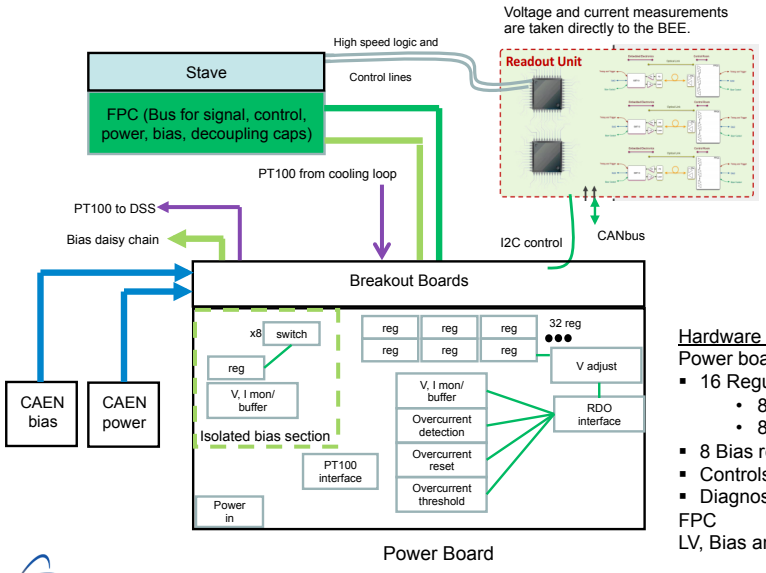
WBS 1..5.2.3 Power System



Based on ALICE/ITS-IB system

Power Board Requirements:
- Module Efficiency > 99%
- Noise rate < 10^{-6}
- Radiation Tolerant
- Control Interface to FEE
- Overcurrent protection
- Remote current readout
- Remote voltage readout
- Remote voltage setting

Hardware Features:
Power board includes 2 sections consisting of:
- 16 Regulators:
  - 8 Analog power regulators
  - 8 Digital power regulators
- 8 Bias regulation switches
- Controls
- Diagnostics

FPC
LV, Bias and Control Cables

Courtesy of G. Contin, LBNL

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