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RUv1 status

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FX3 decisions

FX3 will be placed on the RU

- Piggyback has no space&price advantages

Power can be removed with jumpers

CAN interface decisions

Employ electrically isolated transceivers?
⇒ No need as RU are localized (no CM problems expected)
What Can speed? => Up to 1Mbps

CAN controler	Type	Voltage	TID (krad)	Price
Atmel	AT7908E (CPU interface)	5	300k	
ESA greece	ETM ASIC (only inputs)	3,3	1M	
COTS				
TI	TMS570 Hercules		Under NDA	
Microsemi/	PA3 + IP in fabric			IP
Xilinx	SF2 + internal ECC CAN periperal			

Can contoller implemented with FPGA IP
=> Opencores CAN slave with whishbone interface

CAN interface open ends

Which FPGA

- US(+)/SF2
- PA3

transceiver	type	Voltage	TID(krad)	Price
Intersil	ISL72026/7/8SEH	3,3	75	$836
Cobham/ aeroflex	UT64CAN333x	3,3	100	
TI	SN55HVD233-SP	3,3	50	Prelim
COTS				
TI	SN65HVD233M-EP		??	5,1

Connector via front pannel? What connector? DSUB9/RJ45?

Transceiver: SN65HVD233M-EP

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Preliminary component list

			#	TID (krad)	B(T)
Xilinx	XCKU060-1FFVA1156C	FPGA	1		NA
Microsemi	A3Px	FPGA	1		NA
TI	LMZ31503RUQ	DC/DC	5/4	30 [1]	1T
	LMZ31506RUQ		2		?
	MIC29501	Lin. reg.	0/1	20 [1]	NA
	SN65HVD233MDREP	Can-trans	1		NA
	SN74CB3T16210DGG	Fet switch	2		NA
	DS90LV047ATM	LVDS driver	1	70 [3]	NA
	DS90LV048ATM	LVDS receiver	1	70 [3]	NA
Analog dev.	AD626AR	Diffamp	7	45 [1]	NA
Samsung	SN74CB3T16210DGG	Flash	2	70 [2]	NA
GBT	GBTx	SERDES	3	Oke	NA
	SCA	IO	1	Oke	NA
	VTRx	E/O convers.	2	Oke	NA
	VTTx	E/O convers.	1	Oke	NA
TI **On-semi**	CDCLVD1212 NB7L14	2:12 LVDS buf 1:4 LVPECL buf	1	1130 [4] >20 [5]	NA
IQD	CFPS-73 (tr/tf=6ns)	Crystal	1	50 [6]	NA
		Jitter cleaner			

RUv1 baseline

1. Report Leo
2. IDA airbus 10 March 2015
3. TulliosPreferredPartList
4. http://indico.cern.ch/event/299180/contributions/1659565/
5. https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20140017803.pdf
6. https://edms.cern.ch/document/1327311/1

RUv1 Block Diagram

Power Unit (PSCB)

Power Unit (PSCB)

16SE + 3diff

16SE + 3diff

CANbus

Temperature (RDT), Current (diff amp) & Voltage Monitoring

Flash PROM

32bit SELECT MAP

I2C (2) for monitoring/Control

Flash FPGA

I2C EEPROM

MGT

DATA / CTRL

32 – 64 bit or serial?

JTAG

JTAG Header

JTAG

JTAG Header

UART

14bit Ctrl

PCLK (100 MHz)

32bit Data

Cypress FX3

SCA ADC

I2C

4.8 Gbps

VTRx SM

Trigger

2 x clkdes (40, 160MHz)

10 x 320 Mbps Dout

Trigger

I2C

Busy IN/OUT

HR Bank

10 x 320 Mbps Din

GBTx

4.8 Gbps

I2C

Fast Path GBT <-> Flash FPGA

Xtal 160MHz

HR Bank

10 x 320 Mbps Din

4.8 Gbps

I2C

I2C

GBTx

VTTx

CRU

fan out

UsrClk

MGT RefClk

switch

UsrClk

3 clkdes (40, 160Mhz)

clkdes (40Mhz)

160 MHz

FireFly

FireFly

FireFly

FireFly

FireFly

Transition Board

11/20/28? Data (1.2Gbps)

MGT

28 Data (400 or 600 Mbps)

LVDS

40 MHz

5 DCLK

LVDS

5 DCTRL

LVDS

SCA e-link

GBT-SCA

I2C

4.8 Gbps

4.8 Gbps

10 x 320 Mbps Din

10 x 320 Mbps Dout

HR Bank

GBTx

VTRx

CRU

Ultrascale(+) FPGA

Old slides

RUv1 baseline

- Main FPGA:
  - XCKU60FFVA1156 (maintain US+ compatibility)
  - Interfacing Alpides & GBTx
- Reliable FPGA
  - Microsemi PA3 or SF2
  - Scrubbing Xilinx
    - ⇒ interfaces Flash device
- Height follows VME standard: 6U high

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CAN interface

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Employ electrically isolated transceivers?

=> No need as RU are localized (no CM problems expected)

=> Connector via front pannel? What connector? DSUB9?

⇒ What Can speed? 1Mbps?

CAN controler	Type	Voltage	TID (krad)	Price
Atmel	AT7908E (CPU interface)	5	300k	
ESA greece	ETM ASIC (only inputs)	3,3	1M	
COTS				
TI	TMS570 Hercules		Under NDA	
Microsemi/ Actel	PA3 + IP in fabric			IP
	SF2 + internal ECC CAN periperal			

All CAN controller need external transceiver

transceiver	type	Voltage	TID(krad)	Price
Intersil	ISL72026/7/8SEH	3,3	75	$836
Cobham/ aeroflex	UT64CAN333x	3,3	100	
TI	SN55HVD233-SP	3,3	50	Prelim
COTS				
TI	SN65HVD233M-EP		??	5,1

Scrubbing

What scrubbing method is used/supported

- Blind
- Readback

What interface is used/supported for scrubbing

- Select map
- JTAG

What bandwidth is needed to keep up with scrubbing?
Is it for select map 100MHz * 32 bit?

What is the minumum Prom size?

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EEProm/FLASH

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General remarks on Flash memories

- Charge pump sensitive part, fail from 10krad.
  - Erase/write only in absense beam/radiation.
- Smaller Feature sizes & thinner oxide layers improves radiation sensitivity.
  - Although optimum around 51n (25 nm worse again)
- SLC preferred above MLC above TLC
- Cross section COTS NAND flash order couple orders smaller than SRAM
  - likely still ECC needed!
- Other technologies (not Flash) seem promising: e.g. phase change proms

https://escies.org/download/webDocumentFile?id=63654
https://escies.org/download/webDocumentFile?id=49254
Samsung (σ_norm = 9.15E-13, K9WBG08U1M, datecode: 3708) order better than micron (σ_norm = 8.64E-12, MT29F8G08AAA-WP, datecode: 4208)
https://escies.org/download/webDocumentFile?id=63077
sheet 30: 51 nm Samsung better than 25nm Micron
http://radecs.ies.univ-montp2.fr/fichiers/abstract_13_Irom_2010-07-06_07_32_45_RADECSLATENEWS1.pdf
51 nm performs better than 72, 90 & 120 nm
https://nepp.nasa.gov/workshops/etw2012/talks/Tuesday/T13_Irom_NVM_Radiation.pdf
51 nm performs better than 25, 72, 90 & 120 nm

Brand	type	Voltage	Feature (nm)	Size Mbit	TID krad	o/ bit	Clock MHz	Width	Bandwidth Mbit/s	Price
Atmel	AT69170F	3,3		4	20		15	1	15	
	AT28C010	5		1	10		8	8	66	
	AT17LV010	3,3		1	20		10	1	10	
Xilinx	XQR17V16			16	50		33	8	264	
3Dplus	3DP032	3,3		32	50		33	8	264	
	3DP064			64						
	3DP128			128						
Northrop	W28C0108	3,3		1	300		4	8	32	
Aeroflex	UT8MR2M8	3,3		16	1000		22	8	177	
Cobham	UT8MR8M8			64			20	8		
	UT8QNF8M8	3,3		64	10		16	16	266	
DDC	Rad-package									
COTS										
Atmel	AT45DB161B	2.5-3.6		16	14 [1]		20	1	20	
MICRON	MT29F4G08AAC	1,8-3,3	72	4000	250 [2]	E-9,5	80	8	640	
MICRON	MT29F8G08AAA		51	8000		E-10				
Samsung	K9WBG08U1M		51		70	E-11				

Alpide/firefly interfacing

Use of transistion board? => Yes

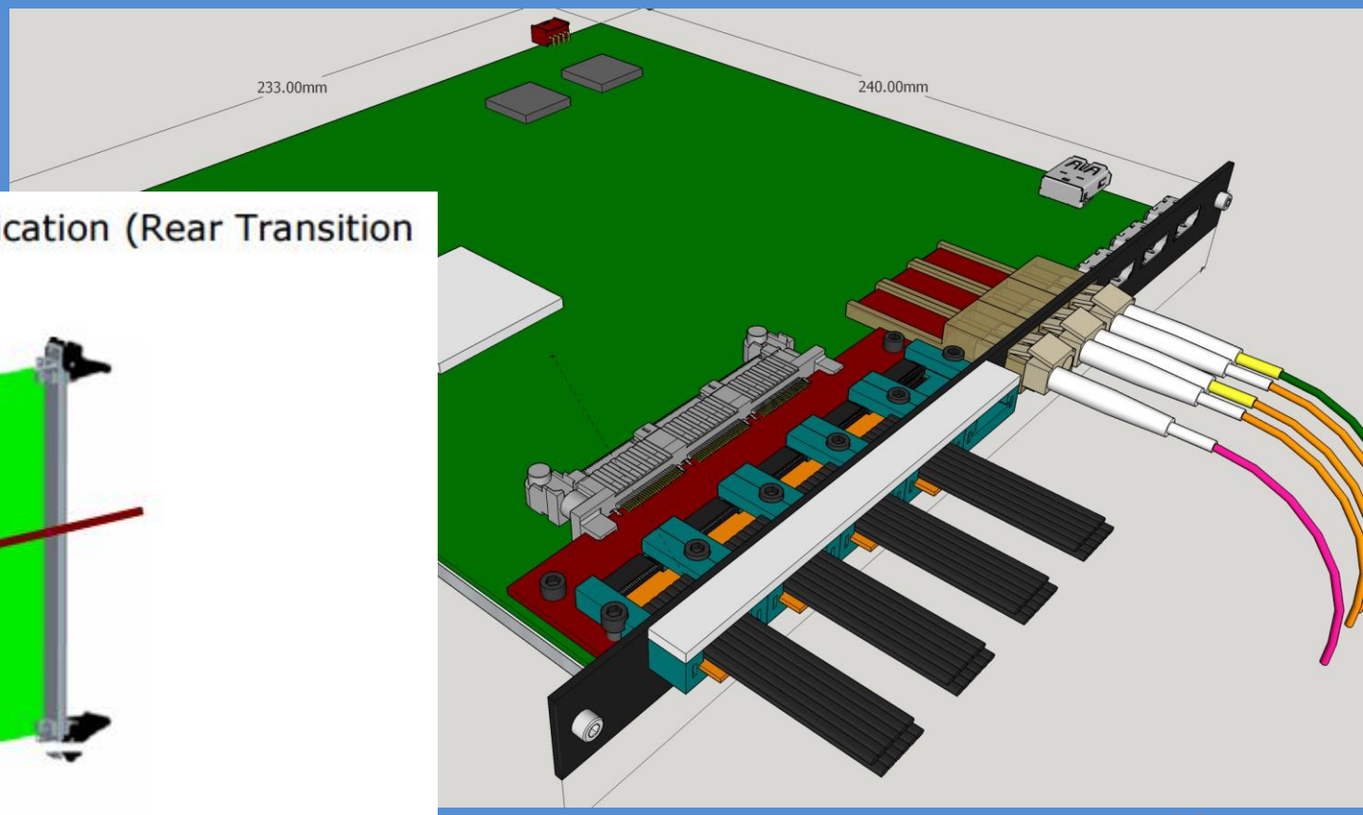
If so, via front panel or rear transition module? => front

e.g. VPX VITA 46.10m => No

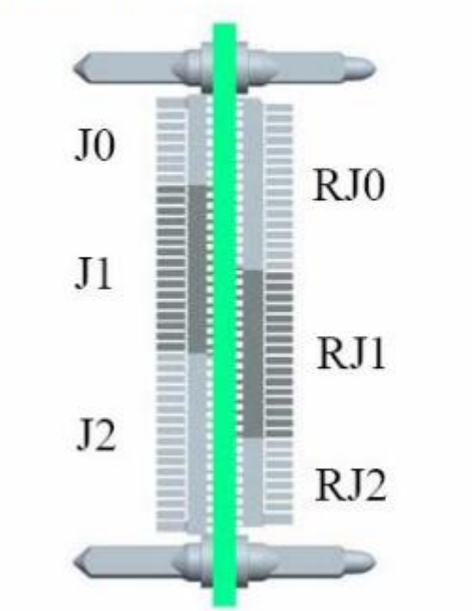
How many (4, 5 or 6) Firefly connectors and how to route? 5

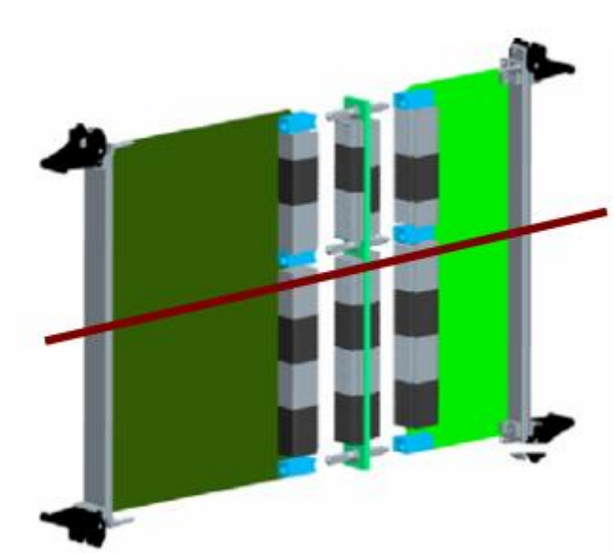
400MHz via GPIO or SERDES? => TBD

600MHz via GPIO or SERDES? => TBD



Rear Transition Module support according to the VITA 46.10 specification (Rear Transition Module on VPX)





PU interface

Do we interface with PU in the first place? => Yes
If so, is differential I2C and 17*SE oke? => Yes *2
Also CAN interface required? => Yes

CAN controler	type	Voltage	TID (krad)	Price
Atmel	AT7908E	5	300k	
ESA greece	ETM ASIC	3,3	1M	
COTS				
TI	C2000		No data	

Unlike presented before TI C2000 not rad tolerant

CAN transceiver	type	Voltage V	TID krad	Price
Intersil	7202xSEH	3,3	75	
Cobham/ aeroflex	UT64CAN333x	3,3	100	
TI	SN55HVD233-SP	3,3	50	Prelim
COTS				
TI	SN65HVD233M-EP		??	5,1

RU crate & coldplate

RU crates
- Does RU share coldplate? =>No
- If so with PU
  - Other RU module
    - If so, is rotation symmetry required?
  - combination

Do we use a backplane for
- Power distribution => Maybe
- PU status/control => Maybe
- Support for rear transistion modules => No

Powering and regulators

How are RU powered?

- Which voltage (12V)? => Likely
- Power comes from the back? => Maybe
- What connector? => TBD
- Backplane or induvidial cables? => TBD
- How it is grouped/segmented? => TBD

Do TI DC/DC regulators from RUv0 operate in 0,5T?

=> Initial tests seems promising!!

USB interface

Place FX3 on RUv1 board or on a daughterboard? => TBD

JTAG on front panel

Do we want a JTAG connector on the front pannel?

=>if possible, otherwise elso on the board

US(+) power on current

US: XCKU85/115 have

- very high power on current
- not in 1156 pin package

UCKU095 relative expensive =>

Use XCKU60FFVA1156 (smallest divice with 28 SERDES)

Device	$I_{CCINTMIN}$ + I_{CCINT_IOMIN}	I_{CCO}	$I_{CCAUXMIN}$ + I_{CCAUX_IOMIN}	$I_{CCBRAMMIN}$	Units
XCKU025	I_{CCINTQ} + I_{CCINT_IOQ} + 2400	I_{CCO_0Q} + 100	I_{CCAUXQ} + I_{CCAUX_IOQ} + 380	$I_{CCBRAMQ}$ + 50	mA
XCKU035	I_{CCINTQ} + I_{CCINT_IOQ} + 2400	I_{CCO_0Q} + 100	I_{CCAUXQ} + I_{CCAUX_IOQ} + 380	$I_{CCBRAMQ}$ + 50	mA
XCKU040	I_{CCINTQ} + I_{CCINT_IOQ} + 2400	I_{CCO_0Q} + 100	I_{CCAUXQ} + I_{CCAUX_IOQ} + 380	$I_{CCBRAMQ}$ + 50	mA
XCKU060	I_{CCINTQ} + I_{CCINT_IOQ} + 3284	I_{CCO_0Q} + 137	I_{CCAUXQ} + I_{CCAUX_IOQ} + 520	$I_{CCBRAMQ}$ + 100	mA
XCKU085	I_{CCINTQ} + I_{CCINT_IOQ} + 6568	I_{CCO_0Q} + 274	I_{CCAUXQ} + I_{CCAUX_IOQ} + 1040	$I_{CCBRAMQ}$ + 137	mA
XCKU095	I_{CCINTQ} + I_{CCINT_IOQ} + 3300	I_{CCO_0Q} + 40	I_{CCAUXQ} + I_{CCAUX_IOQ} + 400	$I_{CCBRAMQ}$ + 150	mA
XCKU115	I_{CCINTQ} + I_{CCINT_IOQ} + 6568	I_{CCO_0Q} + 274	I_{CCAUXQ} + I_{CCAUX_IOQ} + 1040	$I_{CCBRAMQ}$ + 137	mA

Kintex UltraScale Device-Package Combinations and Maximum I/Os

Table 4: **Kintex UltraScale Device-Package Combinations and Maximum I/Os**

Package (1)(2)(3)	Package Dimensions (mm)	KU025	KU035	KU040	KU060	KU085	KU095	KU115
		HR, HP GTH	HR, HP GTH	HR, HP GTH	HR, HP GTH	HR, HP GTH	HR, HP GTH, GTY(4)	HR, HP GTH
FFVA1156	35x35	104, 208 12	104, 416 16	104, 416 20	104, 416 28		52, 468 20, 8	
FFVA1517	40x40				104, 520 32			
FLVA1517	40x40					104, 520 48		104, 520 48
FFVC1517	40x40						52, 468 20, 20	
FLVD1517	40x40							104, 234 64

ProAsic3 options

Estimated minimum number of IOs for FLASH device

price	price
A3P250	20
A3P400	30
A3P600	40
A3P1000	50

I/Os Per Package [1]

ProASIC3 Devices	A3P015[2]	A3P030	A3P060	A3P125	A3P250 [3]		A3P400 [3]		A3P600		A3P1000	
Cortex-M1 Devices					M1A3P250 [3,5]		M1A3P400 [3]		M1A3P600		M1A3P1000	
	I/O Type											
Package	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O[4]	Differential I/O Pairs	Single-Ended I/O[4]	Differential I/O Pairs	Single-Ended I/O[4]	Differential I/O Pairs	Single-Ended I/O[4]	Differential I/O Pairs
QN48	–	34	–	–	–	–		–	–	–	–	–
QN68	49	49	–	–	–	–	–	–		–	–	–
QN132[7]	–	81	80	84	87	19	–	–		–	–	–
CS121	–	–	96	–	–	–	–	–	–	–	–	–
VQ100	–	77	71	71	68	13	–	–		–	–	–
TQ144	–	–	91	100	–	–	–	–	–	–	–	–
PQ208	–	–	–	133	151	34	151	34	154	35	154	35
FG144	–	–	96	97	97	24	97	25	97	25	97	25
FG256[5,6]	–	–	–	–	157	38	178	38	177	43	177	44
FG484[6]	–	–	–	–	–	–	194	38	235	60	300	74

Notes:

1. *When considering migrating your design to a lower- or higher-density device, refer to the ProASIC3 FPGA Fabric User Guide to ensure complying with design and board migration requirements.*
2. *A3P015 is not recommended for new designs.*
3. *For A3P250 and A3P400 devices, the maximum number of LVPECL pairs in east and west banks cannot exceed 15. Refer to the ProASIC3 FPGA Fabric Users Guide for position assignments of the 15 LVPECL pairs.*
4. *Each used differential I/O pair reduces the number of single-ended I/Os available by two.*
5. *The M1A3P250 device does not support FG256 package.*
6. *FG256 and FG484 are footprint-compatible packages.*
7. *Package not available.*

New developments

RU must accomodate DCS CAN slave to control PowerBoard:

- ~~TI controler~~
- FPGA CAN controler with external transceiver chip
  - Commercial CAN (fabric) IP available for e.g. PA3.
  - SF2 has integrated CAN pheripheral (SECDED in buffers)

Preliminary: Latest radiation test indicate PA3 as sensitive as SF2

Replacing PA3 with SF2 provides following advantages:

- More modern device, better support and availability
- Lower power consumption
- True native LVDS support (no external resistors needed)
- Integrated CAN pheripheral

US(+) IO sufficient?

bank			device	Voltage	BLVDS	comment
HP	High Performance	Fast	US/US+	…1,8V	No	
HR	High Range	Voltage range	US	…3,3V	Yes	
HD	High Density		US+	…3,3V	No	No diff out, max 250 MHz

Kintex UltraScale Device-Package Combinations and Maximum I/Os

Table 4: **Kintex UltraScale Device-Package Combinations and Maximum I/Os**

Package (1)(2)(3)	Package Dimensions (mm)	KU025	KU035	KU040	KU060	KU085	KU095	KU115
		HR, HP GTH	HR, HP GTH	HR, HP GTH	HR, HP GTH	HR, HP GTH	HR, HP GTH, GTY(4)	HR, HP GTH
FFVA1156	35x35	104, 208 12	104, 416 16	104, 416 20	104, 416 28		52, 468 20, 8	
FFVA1517	40x40				104, 520 32			
FLVA1517	40x40					104, 520 48		104, 520 48
FFVC1517	40x40						52, 468 20, 20	
FLVD1517	40x40							104, 234 64

Kintex UltraScale+ Device-Package Combinations and Maximum I/Os

Table 6: **Kintex UltraScale+ Device-Package Combinations and Maximum I/Os**

Package (1)(2)(4)	Package Dimensions (mm)	KU3P	KU5P	KU9P	KU11P	KU13P	KU15P
		HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY
FFVA1156(3)	35x35				48, 416 20, 8		48, 468 20, 8
FFVE1517	40x40				96, 416 32, 20		96, 416 32, 24

Signal	Speed	Dir		#	US IO standard	HP/ HR	V_{cco}	Speed Mbps	US+ IO Standard	HP/ HD	V_{cco}	Speed Mbps
e-links	320	Inputs	SLVS diff	28	SLVS_400_18 SLVS_400_25	HP HR	1,8 2,5		SLVS_400_18 SLVS_400_25	HP HD	1,8 2,5	- 250
		Outputs	LVDS	30	LVDS LVDS_25	HP HR	1,8 2,5	625 500	LVDS LVDS_25	HP HD	1,8 2,5	625 250
alpide DCLK	40	Output	LVDS	5	LVDS LVDS_25	HP HR	1,8 2,5	625 500	LVDS	HP	1,8	625
			BLVDS		BLVDS_25	HR	2,5		No BLVDS	-	-	-
CTRL	40	Bidir	BLVDS	5								
Data	400/ 600	Input	LVDS	28 4*7	LVDS LVDS_25	HP HR	1,8 2,5	625 500	LVDS LVDS_25	HP HD	1,8 2,5	625 250
JTAG	100	IO	lvcmos	5	Bank 0 1,5-3,3V				Bank0 1,5-1,8V			
Select Map	100	IO	lvcmos	40	Bank 0 & 65 1,5-3,3V	HR			Bank 0 & 65 1,5-1,8V	HP		
Data PA3	100	IO	Lvcmos 1,5-3,3	40	Lvcmos	HP HR	…1,8 …3,3		lvcmos	HP HD	…1,8 …3,3	
GPIF II UART	100	IO	lvcmos 1,7-3,6	48 2	LVCMOS 1,8-3,3	HP HR	1,8 …3,3		lvcmos	HP HD	…1,8 …3,3	
JTAG I2C	100	IO	Lvcmos 1,2-3,6	5	LVCMOS 1,5/1,8	HP HR	…1,8		LVCMOS 1,5/1,8	HP HD	…1,8	
GPIO	100	IO										
GBT SCA	320	IO	Lvcmos 1,5	20	LVCMOS 1,5	HP HR	1,5		LVCMOS 1,5	HP HD	1,5	

US(+) IO for RUv1

- Speed (Mbps) values are for SDR. Some double when used in DDR
- BLVDS_25 requires 3 termination resistors
- HP for High speed signals
- No diff out on HD (=> HR)

Signal	Speed	Dir	#	#pins	Standard	HP/HR	V_{CCO}
e-link	320	In	28	56	SLVS_400_18	HP	1,8
e-link	320	Out	30	60	LVDS		
Alpide data	400/600	In	28	56	LVDS		
Alpide CLK	40	Out	5	10	LVDS		
Total HP				182			
Alpide CTRL	40	Bidir	5	15	Lvcmos=>BLVDS	*	1,5-3,3
SelectMap	100	IO	40	40	LVCMOS	Bank65	1,5 or 1.8
PA3_data	100	IO	40	40	LVCMOS	*	1,8-3,3
GPIF/UART	100	IO	50	50	LVCMOS	*	1,8-3,3
GBT/SCA	100	IO	20	20	LVCMOS15	HP	1,5
GPIO	100						
Total LVCMOS				165			
Grand Total				347			

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US(+) IO sufficient? => oke

ALICE

at least 350 IO with 200 HP IOs => Oke US (>KU035) & US+

Kintex UltraScale Device-Package Combinations and Maximum I/Os

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Package (1)(2)(3)	Package Dimensions (mm)	KU025	KU035	KU040	KU060	KU085	KU095	KU115
		HR, HP GTH	HR, HP GTH	HR, HP GTH	HR, HP GTH	HR, HP GTH	HR, HP GTH, GTY(4)	HR, HP GTH
FFVA1156	35x35	104, 208 12	104, 416 16	104, 416 20	104, 416 28		52, 468 20, 8	
FFVA1517	40x40				104, 520 32			
FLVA1517	40x40					104, 520 48		104, 520 48
FFVC1517	40x40						52, 468 20, 20	
FLVD1517	40x40							104, 234 64

Kintex UltraScale+ Device-Package Combinations and Maximum I/Os

Table 6: **Kintex UltraScale+ Device-Package Combinations and Maximum I/Os**

Package (1)(2)(4)	Package Dimensions (mm)	KU3P	KU5P	KU9P	KU11P	KU13P	KU15P
		HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY	HD, HP GTH, GTY
FFVA1156(3)	35x35				48, 416 20, 8		48, 468 20, 8
FFVE1517	40x40				96, 416 32, 20		96, 416 32, 24

JTAG configuration levels

- With V_{JTAG}=1,5V, problem arises with FX3 I2C
- With V_{JTAG}=1,8V, GBTx cannot be included in the JTAG chain
- Making V_{JTAG}>1,8V also excludes the US+ connected directly

Master devices	Voltage	Comment
SCA-JTAG	1,2-3,3	
Xilinx cable USB II	1,5-5	
FlashPro cable	1,2-3,3	
Slave devices		
GBTx	1,5	
US	1,5-3,3	
US+	1,5-1,8	
FX3	1,2-3,6	JTAG bank shared with I2C prom. Min. EEPROM voltage is 1,7V !! On FireFlyFMCv3 JTAG bank is 3,3V
PA3	1,4-3,6	

Device	Rail	V_{Min}	V_{Typ}	V_{Max}	I_{Typ}	I_{Max}	P_{Typ}	P_{Max}	comment
GBTx Tx320	VDD		1,5		667	795	1000	1193	
GBTx Xx320					1000	1125	1500	1688	
GB Tx+2*Xx					2500	3046	4000	4569	
SCA	VDD (core)	1,2	1,5	1,65	36	63	54	95	
	AVDD		1,5		1	1	1	1	
	DVDD	1,2	2,5	3,3	7	8	18	21	Likely on 1,5...1,8V to support US+ selectmap
VTRx	VCC	2,25	2,5	2,75	200	250	500	625	
VTTx					300	400	750	1000	
VTTx+2*VTRx					700	900	1750	2250	
ProAsic3 IGLOO2	VCC (core)	1,425	1,5	1,575	3	30	5	45	static
	VCCPLL	1,4	1,5	1,6	333	404	500	607	SelectMap 100 MHz, 40in+40out @ 1,8V
	VJTAG	1,4		3,6					
	Vpump	3	3,3	3,6					Little
	LVDS diff	2,375	2,5	2,625		14		35	4*out, 2*In
Utrascale	V_{CCCINT} ultrascale+	0,922 0,825	0,95 0,85	0,979 0,875		10000 20000			
	V_{CCO_HR}	1,14		3,4	1				
	V_{CCO_HP}	0,95		1,8	1				
	V_{CCAUX}	1,75	1,8	1,85		1581			
	V_{CCADC}	1,75	1,8	1,85		19			Optional, needed when ADC in use
	V_{REFP}	1,2	1,25	1,3					Use internal Reference
	$V_{MGTAVCC}$ Utrascale+	0,970 0,873	1 0,9	1,030 0,927		2300			Estimate for 32 SERDES Rx
	$V_{MGTAVTT}$	1,17	1,2	1,23		2400			Estimate for 32 SERDES Rx
	$V_{MGTVCCAUX}$	1,75	1,8	1,85		0			
	$V_{MGTAVTTRCA}$	1,17	1,2	1,23					
	$V_{CFG\ (JTAG/SPI)}$	1,5		3,3 1,8?					
	$V_{SelectMap\ US+}$	1,5		3,3 1,8					
FX3	(A)V_{DD} (core)	1,15	1,2	1,25		200		240	
	DIO/UART	1,7		3,6					
	JTAG/I2C	1,15		3,6					
	Bus/bat	3,2	3,3	6		60		200	
24LC1025	V	2,5		5,5		5		13	
24FC1025		1,8						9	

PS rail and currents

3V3	PA3_Vpump	FX3_Vbat		Total
3,3	1	60		61

2V5	PA3_LVDS	VTT+2*VTRx		Total
2,5	14	900		914

1V8	US_V_{CCaux}	US_V_{CCADC}	US_$V_{MGTVCCAUX}$	
1,8	1581	19		1600

1V5	GB Tx+2*Xx	SCA	PA3	
1,5	3046	64	336	3446

1V2	US_V_{MGTx32}	FX3		
1,2	2400	200		2600

V_{MGT}	V_{MGT}			
$1_{/0,9}$	2300			2300

V_{CCINT}	V_{CCINT}			
$0,95_{/0,85}$	10000			10000

Optional Regulators

		Test	TID (krad)	Mag.	I (A)	Vi min	Vi max	Vo min	Vo max	Accuracy	$	Comment
MIC29501	Linear	Leo	20	Oke	5			1,25	25		6	
MIC29710			15		7,5						10	Obsolete?
TPS5430	Switched		20	?	3	5,5	36	1,22			2	
LMZ31503			30	?	3	4,5	14,5	0,8	5,5	1% Ref	8	
LMZ31710			?	?	10	2,95	17	0,6	5,5	1% Ref	12	
FEASTMP	Switched	Cern	200k	40.000 Gaus	4			0,9	5		35	Height =15mm
FEAST2.1								0,6			15	QFN
LHC4913	Linear		300k	Oke		3	12	1,22	9		14	
MCP1824ST	Linear	Tullio	100k	Oke	0,3			0,8	5		1	

- How large is magnetic field at RU? => 0,5 Tesla
- Is/will LMZ31710 tested for radiation? => not yet

RUv1 PS regulators

3V3	PA3_Vpump	FX3_Vbat		Total	
3,3	1	60		61	LMZ31503

2V5	PA3_LVDS	VTT+2*VTRx		Total	
2,5	14	900		914	LMZ31503

1V8	US_V_{CCaux}	US_V_{CCADC}	US_$V_{MGTVCCAUX}$		
1,8	1581	19		1600	LMZ31503

1V5	GB Tx+2*Xx	SCA	PA3		
1,5	3046	64	336	3446	FEASTMP or LMZ31710

1V2	US_V_{MGTx32}	FX3			
1,2	2400	200		2600	LMZ31503

V_{MGT}	V_{MGT}				
$1_{/0,9}$	2300			2300	LMZ31503

V_{CCINT}	V_{CCINT}				
$0,95_{/0,85}$	10000			10000	LMZ31710