LVDS high-speed tests

- Motivation: Use LVDS fabric I/O's instead of transceivers to receive 1.2Gb/s Alpide data.
- Assembled RUv0a with speed grade -2 FPGA
- Data-sheet (see next slide) claims >1200MHz for LVDS high-performance
- Modified LVDS receiver lines that match on Firefly cables to allow TX ("HR" bank)
- Implemented OSerdes (data) and DDR (clock) in firmware on TX side
- Implemented ISerdes & IDelay on Rx side, including bitslip
- (slow) Clock in TX line serves as data aligner.
- Use PRBS-7 test pattern with 8-bit parallelism as input to OSerdes
- Compare ISERDES output to appropriately delayed PRBS pattern and count differing bits
- Used 400MHz IDELAYCTRL which results in 39ps delay taps
- Used 2 clocks in Firmware:
  - Board clock for wishbone interface and IDELAYCTRL source (200 or 400 MHz)
  - SMA input of Silicon Labs eval board as source for F_{div}
- FPGA PLL was used to clean SMA input and generate bit clock (4x SMA input)

Kintex Data Sheet

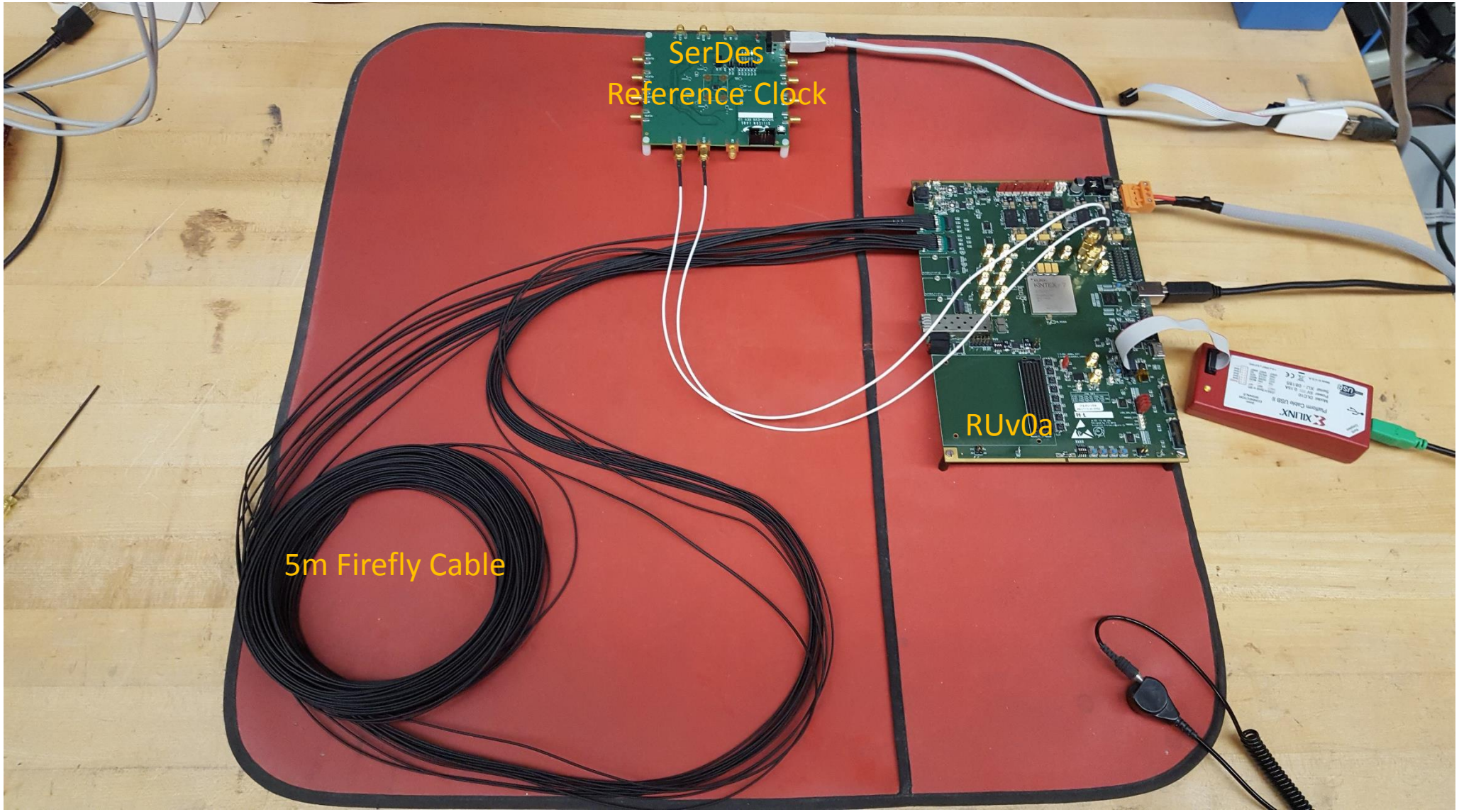
Table 17: **Networking Applications Interface Performances**

Description	I/O Bank Type	Speed Grade					Units
		1.0V			0.95V	0.9V	
		-3	-2/-2LE	-1/-1M/-1LM	-2LI	-2LE	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	HR	710	710	625	710	625	Mb/s
	HP	710	710	625	710	625	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	HR	1250	1250	950	1250	950	Mb/s
	HP	1600	1400	1250	1400	1250	Mb/s
SDR LVDS receiver (SFI-4.1)(1)	HR	710	710	625	710	625	Mb/s
	HP	710	710	625	710	625	Mb/s
DDR LVDS receiver (SPI-4.2)(1)	HR	1250	1250	950	1250	950	Mb/s
	HP	1600	1400	1250	1400	1250	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate

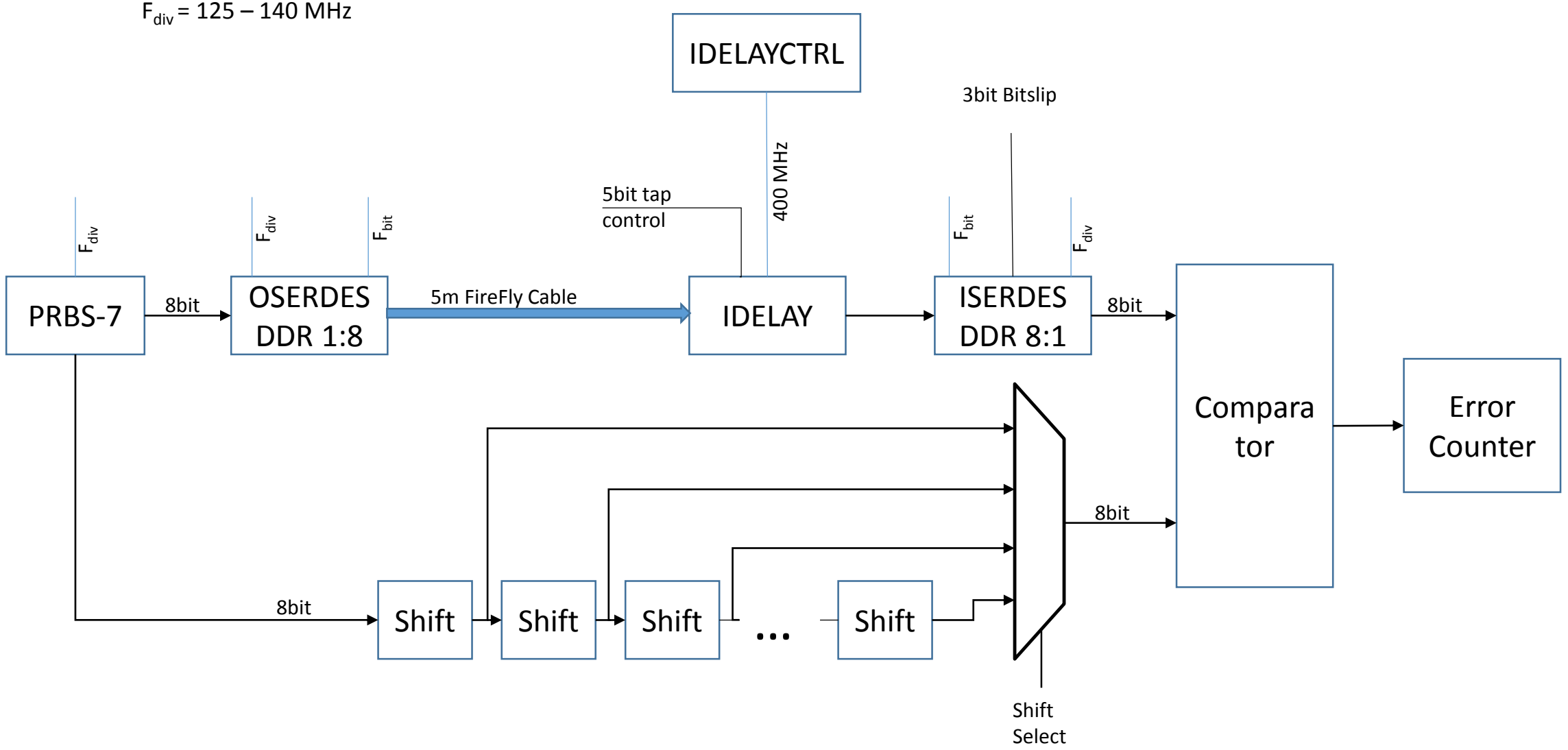
Setup



Schematic Modifications

RUv0a Schematic Page 7

LVDS Testing Firmware



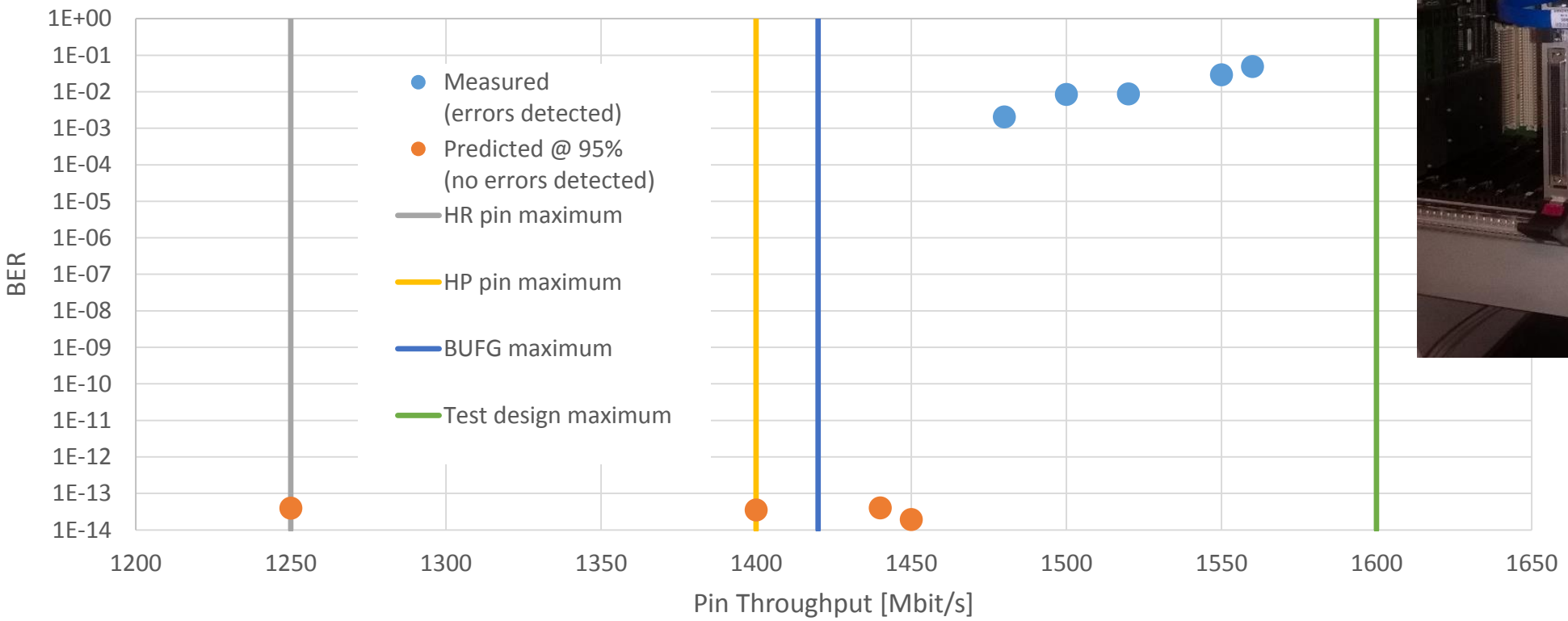
Results

- F_{div} frequency was varied between 125 and 140 MHz
- Corresponding bit rate is 1000 MHz – 1120 MHz
- Number of bits was counted with a prescale of 100 million times 8 bits (counted parallel words)

F_{div}	Bitrate	Prescaled BitCtr	Bit Errors	Error Rate
125	1000		0	
130	1040	1,169	0	
135	1080	1,046	0	
137	1096	9,059	0	1.38E-13
137.5	1100	10,003	0	1.25E-13
138	1104	10,786	1	1.16E-13
138.5	1108	101	570	7.05E-09
139	1112	50	11,855,199	2.96E-04
140	1120	51	62,179,260	1.52E-03

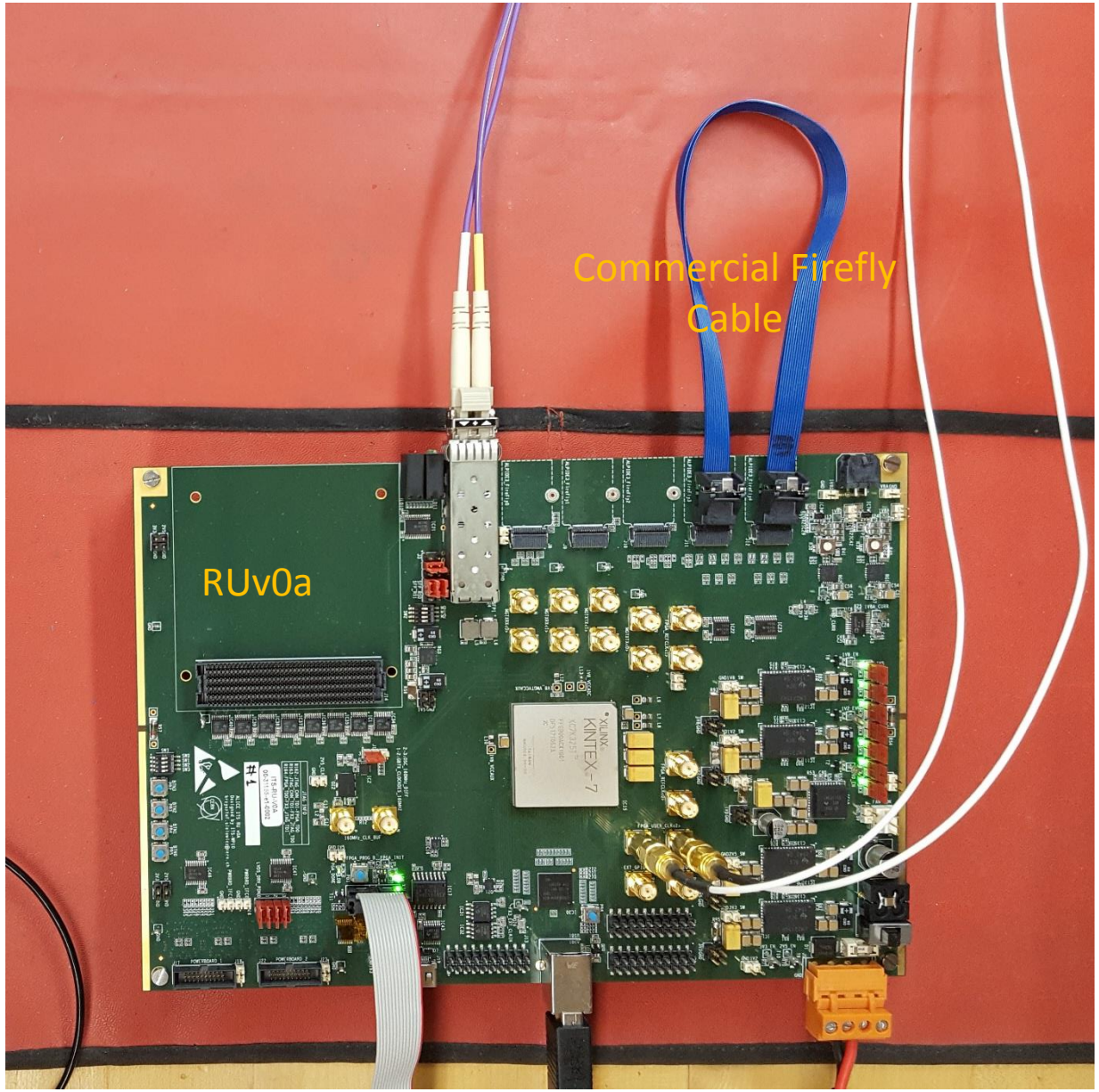
Comparison: J. Pospisil (ALICE Trigger) Results

ALICE Trigger group performed similar tests with their LM0 board and a short (15cm) FireFly cable. The setup is shown on the right, and the results are shown below (reported at TWEPP 2015):



Test with “standard” short Samtec cable

After receiving a commercial FireFly cable sample from Samtec, I repeated the trigger group’s tests with our setup as shown here (same firmware as earlier tests shown)



Results with short cable

- Samtec Cable part number: ECUE-12-030-C1-FF-01
- F_{div} frequency was varied between 137 and 190 MHz
- Corresponding bit rate is 1096 MHz – 1520 MHz
- Number of bits was counted with a prescale of 100 million times 8 bits (counted parallel words)
- TX and RX are still connected DC, AC coupled testing still outstanding

F_{div}	Bitrate	Prescaled BitCtr	Bit Errors	Error Rate
137	1096	125	0	
140	1120	151	0	
145	1160	151	0	
150	1200	10,169	0	1.23E-13
165	1320	8,021	0	1.56E-13
180	1440	7,701	0	1.62E-13
187.5	1500	9032	0	1.38E-13
188	1504	3,002	809	3.37E-10
190	1520	52	54,101,431	1.30E-03