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**Scientific Instrumentation**

**ITS upgrade**

**Review ITS RUv1**

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| **Project** | ITS upgrade (W0001192) | **Author(s)** | M.J. Rossewij |
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**Document History**

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| --- | --- | --- | --- | --- |
| **Version** | **Date** | **Author** | **Section** | **Description** |
|  |  |  |  |  |
| 0.1 | 31-march-2017 | M.J. Rossewij | - | First concept. |
| 0.2 | 5-april-2017 |  |  | Include feedback Krzysztof  Include comments Johan Alme  Include discussion WP10 (4-4-2017)  Include comments Raphael Tieulent |
| 0.3 | 6-april-2017 |  |  | Include feedback Johan Alme  Include suggestion Leo/Alberto |
|  |  |  |  |  |

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| --- | --- |
| AJ | Attiq/ Johan Alme |
| JA | Johan Alme |
| JS | Joachim Schambach |
| KS | Krzysztof Marek Sielewicz |
| MB | Matthias Bonora |
| ML | Matteo Lupi |
| MR | Marcel Rossewij |
| PG | Piero Giubilato |
| RT | Raphael Tieulent, Gaetan, Cyrille |
| SV | Simon Voigt Nesbo |
|  | Johan |

Priority: Low, Medium, High, Critical

Action: None, Fix, Discus, Open

Status: ok, done

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Page | Person |  | Priority | Action | Status |
| Gen | MB.008 | Is there any plan to add probing points for some of the connectors? At least Points for DCLK, DCTRL and one HSDATA link (Inner Barrel, one for Outer Barrel) would be quite useful for debugging.  No plan yet. It can be on RU or transition-board. IB HSDATA could be probed on the RU AC-coupling capacitors. I think the OB HSDATA can best be probed on the transition-board. For DCLK and DCTRL, do we want the SE or diff signals and do we want one or all signals? What probe point: pin, pad?   * Add scope probe GND pins * Power rails/Supply levels * Clock lines (without affecting the signal) * Analyse top level for critical signals. | High | Fix |  |
|  | ML | - There are no test pads |  |  |  |
|  | PG | I2C\_POWER\_BUS: wen connected to U11, U12 (front panel side) and U47, U48 (back-plane side) the used pinout is different: while not a functional issue, having identical pinout usage of the transceivers would simplify verification and debugging.  Connectivity was chosen for optimal routing | Med | None |  |
|  | PG | no connection to the front-panel AUX connector (ERF8-010-01-L-D-RA-L-TR, 20 pins available, to be connected to US pins, one bidirectional 1 GTX) | Critical | Fix |  |
|  | PG | still missing power-mezzanine schematic (front panel connectors for the power board + LEDs) | Med | None |  |
|  | KS | \*) Could you please standardize all schematic sheets to A3?  This can be done for the smaller sheets. This might be difficult for the 2 larger sheets (TOP and FPGA power). I will try to shrink them.  OK, thank you. | Med | Fix |  |
|  | ML | - Different pages have different size. I would stick to A3 format. |  |  |  |
|  | ML | - Resistor symbol could be replaced with the typical resistor symbol. I spoke to Krzysztof and he said that it is common to use this symbol (IEC) in Europe, this however does not help the readability of the schematics. | Med | None |  |
|  | ML | - In a symbol (e.g. the U7, etc) it is advised to have the +3V3 on top (on the side of the block), and the GND on bottom (still on the side). https://wikis.cern.ch/display/MPEEP/Schematics\_Rules\_Guidelines | Med | Fix |  |
|  | KS | \*) I think it’s worth refreshing the knowledge about high-speed PCB designing by reading the following document provided by Xilinx:  https://www.xilinx.com/support/documentation/user\_guides/ug583-ultrascale-pcb-design.pdf  Ok | Med | Read |  |
|  | KS | \*) Can you please provide us with the document for estimating the power consumption of the Ultrascale: <https://www.xilinx.com/products/technology/power/xpe.html>  I will try to complete the sheet. | Med | Fix |  |
|  | KS | \*) I'd propose to add a cover page that would present RUv1 + all mezzanine cards around so that a reader has an overview of the system (transition board + small LED board + RUv1)  Ok, I will add this | Low | Fix |  |
|  | JA.5 | 5. is a full 32 bit SM if neded? I have not checked yet ( I will!) but isn't the flash quite much slower than the SM? |  |  |  |
|  | KS | \*) Do we really need 32-bit data bus for scrubbing as the data interface between PA3 and Flash is only 8-bit?  Moving to 8 bit is fine to me. I thought the 32 bit could make sense when doing readback when no PROM-data is needed. However, if we agree on 8 bit, It can be reduced of course.  We have to discuss this point again. If we don’t need 32-bit data bus then the layout will be easier and we’ll free some I/Os.  Reduce to 8 bit | High | Fix |  |
|  | MR | Fix Page numbering | High | Fix |  |
| 1 | ML | Overlap between bus/nets with nets name make is difficult to read and identify | Med | Fix |  |
|  | ML | When coming out of a block some signals change name using different conventions (i.e. SCINP -> SCINP2 on the GBTx2 and CLK[0:3]P -> CLK3P on the clock block) | Med | None |  |
|  | ML | - High congestion in net connections: e.g. USB3 block has nets going all around it coming from the US FPGA block. The congestion could be reduced by moving all the connections to the right of the USB3 block and having hence the length of nets.  It was chosen to keep the inputs on the left side. However, in the attempt to shrink the sheet size, the might be beneficial to follow the suggested approach. | Low | Fix |  |
|  | ML | - Some ports of the block are written in vertical. This makes the reading hard. One of those overlaps with another net name. | Med | Fix |  |
|  | ML | - Some signals are ending with a #. It is not clear to me the meaning of this symbol.  The # comes from the FX3 DS indicating active low. We can change this with the more common bar above. | Med | Fix |  |
|  | ML | - The jumpers J25, J26 and J27 are quite confusing: the relative position of the name of the component with respect to the symbol is not the same. It is not immediately clear what is what. Moreover, the +1V2 net name is close to the GND net. | Med | Fix |  |
|  | ML | - LED net.  - I see LED[0:3] coming out of the FPGA. LED[0:6] is coming out of of the POWER\_BOARD block. The two nets are somehow connected together. The bus reaches the top left of the schematics where another ambiguous (but different) connection to the bus LED [4:6], coming from the PA3 is present.  LED[0:3] is driven by the FPGA  LED[4:6] by the PA3  LED[0:6] are inputs for the POWER\_BOARD. If you think it is more clear, It can be split in 2 inputs: LED[0:3], LED[4:6]  Split with different busnames or keep as it is now with identical ripper orientation | Low | Fix |  |
|  | ML | - The nets going to the FPGA are confusing, they overlap with the next. The nets change name after the split.  Also here the bus can be split on the block symbol |  |  |  |
|  | ML | - The /RST net has the negated which is too close to the net right over it. The distance from the other net could be increased, or a different naming for negated signals could be used (e.g. \*\_n, \*\_N). | Low | Fix |  |
|  | ML | DIPswitch - The name of the component overlaps with the port name.  Enlarge block and change component name to Switch | Med | Fix |  |
|  | ML | There are 3 GBTx, one without index, and two with an index starting from 1. I would suggest renaming it to GBTx0, GBTx1, GBTx2. | Med | Fix |  |
|  | ML | On top of GBTx2 there are 2 ports (CLOCKDES0N, CLOCKDES0P) which are unconnected. If they are unconnected, I suggest to replace them with an unconnected symbol.  The same comment for LDSCL, LDSCA, CLKCKDESP[1:6], CLKDESN[2:6], SCCLKP, SCCLKN, SCOUTP, SCOUTN ports on GBTx2 | Med | Fix |  |
|  | ML | The ports REFCLKN, REFCLKP are not aligned with the nets connected to them. | Low | Fix |  |
|  | ML | Connection of SCINP2, SCINN2 is not clear. | Med | Fix |  |
| 2 | MB.007 | GPIO/Fabric transceivers are named DATA\_LVDS. Before the EDR we had a discussion that naming those ports \_LVDS is misleading. I think the latest consensus was to name them \_GPIO.  Also change this in VHDL top (its called \_SIO, S from select)? | Med | Fix |  |
|  | ML | - The naming of the signals on the RUv1 does not correspond to the one on the transition board schematics on pag 34. One solution we came up with Piero, would be to rename the signals going to the transition board by adding an \_J (as for connector) in the name. This would make clear that they are going to a connector.  I should be discussed/decided what are the proper names |  |  |  |
|  | ML | - I can’t find the part number on the SAMTEC website using the the given known parameters. After checking with Piero, we found out that the correct part number is the QFS-104-01-SL-D-RA (with -01-SL missing on the schematics). | Med | Fix |  |
|  | RT.1 | we do have enough MGT and LVDS I/O for the MFT | Med | None |  |
|  | RT.2 | Page 2 : "ALPIDE\_TRANSISTIONBOARD\_INTERFACE", You do foresee a 1.8V on the transition board. Do you except active element on this transition board ? No. Do you foresee SLVS - LVDS conversion here? No.  The 1V8 is intended to provide power to the optional external termination networks (on the transition-boards) providing the common mode bias to the AC-coupled LVDS signals. (UG571 page 129/130) | Med | None |  |
|  | KS | \*) Please add bulk ceramic 47u caps close to QFS-104-XX-XX-D-RA on 3V3 pins  Why do you think this is necessary?  It’s a normal practice to add bulk caps close to connectors to minimize the voltage ripple and improve EMI performance.  Then it should be connected to 1V8 I suppose? | Med | Fix |  |
| 3 | PG | To be updated to J##, part: Molex 087833-0420 (Digi-key WM18858-ND) | Med | Fix |  |
|  | SV | Does the CAN bus need termination resistors on the board, or is this placed off the board?  As more RUv1 will be connected to a signle CAN/bus I assumed the termination will not be on the board (at the end of the lines) | Med | None |  |
|  | PG | Pin 4 connected to CAN\_PA3:LBK\_PA3 net, should be connected to CAN\_PA3:R\_PA3 | Critical | Fix |  |
|  | KS | \*) Depending on the layout we can think about adding 1u ceramic to U53 and U54  The decoupling is now implemented as in figure 25 of: <http://www.ti.com/lit/ds/symlink/sn65hvd233-ep.pdf>  If considered needed, we can add more decoupling capacitors  OK | Med | Fix |  |
| 4 | KS | \*) I'd propose to add a bicolor LED to show the state of US INIT\_B signal please refer to the RUv0a schematic)  Include LED with jumper to disable in cavern. Must it really be bi-collor? This requires introduction of buffer. Disabling and disconnecting requires 2 jumpers. Singe color LED can be done with simple FET and with single jumper. | Med | Open |  |
|  | KS | \*) PAGE 4/65 no decoupling on lines VCCO\_0 (AB9, Y9)  It shares the decoupling capacitor with bank 47 | Med | None |  |
|  | KS | \*) US MSEL pins -> is 100R a recommended value by Xilinx? I remember that in Kintex-7 it is 1k  UG570 recommends ≤1 kΩ. However, I see no problem making it 1 kΩ.  1k seems better. | Low | Fix |  |
|  | KS | \*) Please add 100n in parallel with S9 for PROGRAM\_B to de-bounce switch  Ok, will do this | Med | Fix |  |
|  | KS | \*) all signals from block RUV1\_XCKU 4/65 have to be very carefully checked with Xilinx Review Document (propagated by GAR some time ago)  - External temperature diode will not be used. Leave Temperature diode disconnected or to GND.  - Use internal temperature sensor. Check system monitor documentation UG580 what is needed for that.  Proposal: use internal reference (Temp. accuracy is then 4K) | High | Open |  |
|  | ML |  | Med | Fix |  |
|  | ML | - Assign a component designator to each of the FPGA blocks. This allows easy reference to the pin banks.  Can you explain in more detail what you mean exactly | Med | Open |  |
|  | ML | - Resistors do not have a component designator | High | Fix |  |
| 5 | MB.001 | labels reach into block (AC coupling,  R291) | Low | Fix  Fix |  |
|  | MB.002 | Naming of pins after AC coupling is not consistent. E.g DATA\_MGTN4 -> MGTN4, but CLOCKDESN2 -> CLOCKDES\_N2. The Ruv0 schematic used a convention where the signal was renamed in the form of <signal> -> <signal>\_C. |  |  |  |
|  | ML | - Name is changed from the FPGA pin name to the net. This should not be done as it could cause headaches when assigning the pins and in the firmware. Please use the same names for the pin and the net connected to it. => Use pin-names on nets | Med | Fix |  |
|  | ML | - It could be a good idea to have a schematic page with only the data decoupling capacitances. |  |  |  |
|  | MB.004 | Is it possible to remove the AC\_COUPLING blocks from this page and have the couplings directly, in a separate page (like in the RUv0 schematic, page 5) | Med | None |  |
|  | MB.005 | ERROR Page5: Quad 128; it looks like CLOCKDES\_N2, CLOCKDES\_P2, CLK\_N2, CLK\_P2 are connected to MGTHTXN0-MGTHTXN3 | High | Fix |  |
|  | ML | - Is not possible, due to net overlap, to understand which clock is connected to which pin of the FPGA. See CLKDES\_N1 |  |  |  |
|  | MR | Use filtered version for the 1V2 | Med | Fix |  |
|  | KS | \*) 5/65 please add a remark close to the MGTREF\_R/L signals that special routing consideration must be taken into account while layouting.  Ok | Med | Fix |  |
| 4-25 | ML | - There is no component designator for the blocks in this page. => Will Add this to all FPGA blocks  - The type of the component is out of the box relative to the component. => Will Fix this  - Xilinx FPGA model is not reported in the schematics. This is useful for the pin check. At least the package used should be stated in each of the pin banks => Will change name to: XCKUxxx-xFFxA1156 (in FPGA IO optimizer->properties->PCB Flow-> FPGA Part Number) | High | Fix |  |
|  | ML | - Less than 25% of the page is used, the capacitors are cluttered in the centre of the page. | Med | Fix |  |
|  | ML | - Using the hierarchical component for this nets makes impossible to understand which signals are using each capacitance. Using this for hw debugging a signal is a nightmare. |  |  |  |
|  | ML | - The decoupling scheme for the MGT data is not clear: e.g. it is not clear what page is relative to the AC\_COUPLING\_8\_3. | Med | Fix |  |
|  | MB.003 | The AC\_COUPLING blocks are refered to as AC\_COUPLING\_N\_M. In the following sheets, there is AC\_COUPLING\_4 and AC\_DECOUPLING. Which one does apply? |  |  |  |
|  | ML | Some decoupling are 100 nF, some other 10 nF |  |  |  |
| 5-14 | KS | \*) AC coupling capacitors on HSDATA lines, are you sure about 10n -> on ITS\_RUv0a I installed 100n. Also all the testing was done with 100n.  UG576 recommends 10nF for refclk (which is in AC\_COUPLING4) and 100nF (which is in AC\_COUPLING\_8) for the signals.  Thanks for the explanation | High | None |  |
| 15 | ML | - Block unused. Remove?  UG583: Unconnected VCCO Pins  In some cases, one or more I/O banks in an FPGA are not used (for example, when an FPGA has far more I/O pins than the design requires). In these cases, it might be desirable to leave the bank’s associated VCCO pins unconnected, as it can free up some PCB layout constraints (less voiding of power and ground planes from via antipads, less obstacles to signals entering and exiting the pinout array, more copper area available for other planelets in the otherwise used plane layer).  Leaving the VCCO pins of unused I/O banks floating reduces the level of ESD protection on these pins and the I/O pins in the bank. For maximum ESD protection in an unused bank, all VCCO and I/O pins in that bank should be connected together to the same potential, whether that be ground, a valid VCCO voltage, or a floating plane.  AR11906:  In the case of a completely unused I/O bank, leaving the VCCO pins of unused I/O banks floating reduces the level of ESD protection on these pins and the I/O pins in the bank and is generally not recommended. However, ESD events at the unconnected solder balls in the inner rows of the pin array are unlikely and not considered a high risk.  Depending on routing difficulties, we will keep it unconnected or connected |  |  |  |
| 16 | ML | - reduce net length. | Low | Fix |  |
| 16-  19 | ML | - Net name different than pin name.  - DCLK{P|N}{0|1} goes to GBTX1\_DCLK\_d{p|n}[{0|1}]. This is an unwanted behaviour. DCLK is used later on also for the ALPIDE. I suggest to rename the nets so that they contain also the GBTx name on it. | Med | Fix |  |
| 17 | JS | GBTx1 doesn't need elink clocks, delete them | Med | Fix |  |
|  | ML | DIPSWITCH5 is not connected to the relative pin of the FPGA. It is connected to another (or more) pin of the FPGA. Check this page. |  |  |  |
|  | SV | On the US FPGA some of the DIPSWITCH signals don't appear to be connected to the DIPSWITCH inputs, same for GBTX1\_DCLK\_dn[0] and [1]. Is it supposed to be like this?  => This error was accidently introduced and will be fixed. | High | Fix |  |
|  | KS | \*) 17/65 it looks like there are shorts on 1V8 power net  This will be fixed | High | Fix |  |
|  | ML | - There is a +1v8 net wandering around the page. It is not clear what it is connected to. |  |  |  |
| 18 | JS | TXDATAVALID should be output | Med | Fix |  |
|  |  | - Well done with the assignment of the Multiple TxDATAVALID{ |1|2}. This should be repeated for all the triplicated pins (SCA\_GPIO\_{A|B|C}). The nets are way more readable in this way!  Will do this at the end as it requires manual symbol customization after automatic generation | Low | Fix |  |
|  | ML | - Decoupling are better not to be directly connected to the component. This enhances readability.  Will move bank decoupling to FPGA power sheet | Med | Fix |  |
|  | ML | - Better to keep nets short as they are easy to follow. | Med | Fix |  |
| 20 | ML | - No return signal is present from the R pins of the SN65MLVD080 to the FPGA for what concerns the DCTRL. |  |  |  |
|  | JS | I just noticed that the ALPIDE\_DCTRL lines seem to be connected only in one direction to the MVLDS buffer, they need to be bi-directional, so the R RE pins need to be connected to the FPGA  We indeed need to connect the R pins. Unfortunately, we need 5 pins for that and we have only have 2 pins left on the 3V3 bank. I see a few ways around:  1) Give up the direct CAN interface (and go via the PA3 as initially proposed), which will free up the desired pins  2) Use for each control signal a SN65MLVD080DGG buffer (or maybe a smaller version) with DE and RE\_n connected  3) Use level converters  I think the first option is most attractive. What do you think?  Or do you see other options?  Go for option 1) Give up CAN interface | Critical | Fix |  |
|  | ML | - RE pin of the SN65MLVDS080DGG is not connected. This should be connected so that the transmission to the FPGA is always allowed.  Connect RE to GND  Moreover, we should decide what to do with the unused channels.  Good question. Do you have a suggestion? (use the 82 device or connect one driver to the open receiver)  Suggestion Alberto/Leo: Enable drivers and set D to GND. No termination needed for those signals. | High | Fix |  |
|  | KS | \*) 20/65 add series 22R on ALPIDE\_DCLK lines  Are you sure this is necessary. This was not mentioned in the document below:  https://indico.cern.ch/event/623552/contributions/2515597/attachments/1427463/2190905/201703\_wp10\_meeting\_TMR.pdf | Med | None |  |
|  | ML | Nets and nets name overlap | Med | Fix |  |
|  | ML | - The signal {DCTRL|DCLK}\_{P|N} could be renamed to ALPIDE\_{DCLK|DCTRL}\_{P|N} to enhance readability (take into account also the suggestion of pag 2 about the connector). | Med | Fix |  |
|  | ML | - No 100 Ohm termination is present between DCTRL\_{P|N} pins. =>Also for DCLK | High | Fix |  |
|  | ML | - For clarity group the triplicated signals on the RUv1\_XCKU so that the 3 signals are adjacent and they can be shorted immediately. This improves by far the readability of the schematics by reducing the congestion.  - Group the signals by channel, not by function. The nets relative to the DCTRL 0 could be close one to another instead of having them interleaved with the other channels. This reduces the congestion and increase the readability.  - CAN nets are going all around the RUV1\_XCKU block, couldn’t they be connected all on one side so that they are grouped together reducing the congestion?  Agree. Unfortunate, the symbol generator does not do it this way. It can be changed manually. Will do this at the end. | Low | Fix |  |
|  | ML | - There is an ALPIDE\_DCLK\_EN0 which is not related to one of the nets it is overlapping with. | Med | Fix |  |
|  | ML | - There is a GND (label? net? comment?) over to pin 61 of the SN65MLVD080 | Med | Fix |  |
|  | ML | - Component type SN65MLVD080DGG is present 2 times on the schematics. | Med | Fix |  |
|  | RT | we do not understand the interconnection of 3 CLK outputs to generate the clock. If this is to be able to select among 3 different inputs for the clock it will be safer to do it inside the FPGA and have only one output. That is for the TMR, see:  <https://indico.cern.ch/event/623552/contributions/2515597/attachments/1427463/2190905/201703_wp10_meeting_TMR.pdf> | Med | None |  |
| 22,  23 | ML | - Net name different than pin name.  Change SIO => GPIO first | Med | Fix |  |
| 23 |  | - There is a square point on pin F13. | Critical | Fix |  |
|  | MB.009 | Some net signals have the same name as ports from different parts. For example, the PA3 to FPGA connection is named DION[x], When searching for this, most of the results are related to some GBTx pins. Just a small thing, but this could ease the search for signal traces when reading the schematic. | Med | None |  |
|  | ML | - DIOP[8:9] are not connected to the pin they are aligned with. The seem to be connected to the Vref and another pin. | Critical | Fix |  |
|  | ML | - There is a +1v8 annotation over the +1v8 nets. | Low | Fix |  |
| 24 | KS | \*) 24/65 there is no series termination on the data lines between Ultrascale and FX3  There are 2 options: either we put 22R (or similar, to be calculated using the simulation) in series on the data/clock/control lines or we turn on the internal series termination (special design must be prepared and compiled to see whether it's possible to enable the termination on all the required lines).  I prefer the second option.  OK, but then one has to do a very careful SI analysis. | Med | Fix |  |
| 24 | ML | - Net name different than pin name. | Med | Fix |  |
| 25 | MB.006 | MGTAVCC uses 1V2, which is shared with USB3\_1V2. The GTH TRansceiver guide states that this supply should not be shared with non-mgt loads (UG576, page 327). Same goes for MGTVCCAUX (1.8V), which is connected with VCCO and USB3\_1V8. Is this intentional?  Like RUv0, the MGTAVCC and MGTVCCAUX are decoupled by an inductor. | High | None |  |
|  | KS | \*) I'd suggest that all the capacitors for decoupling of the Ultrascale are put on a single schematic sheet, so that it's easier to review that (please refer to RUv0a schematic). | Med | Fix |  |
|  | MR | 2 \* 47uF on VCCAUX | Med | Fix |  |
|  | MR | Replace all to 3,5A Ferrite Bead.(1206)  BLM31PG121SN1  Farnell: 2672838 | High | Fix |  |
|  | MR | Add netnames: MGTAVCC, MGTAVTT, MGTVCCAUX, VCCAUX | Med | Fix |  |
|  | ML | - Assign a component designator to each of the FPGA blocks. This allows easy reference to the pin banks.  - In a symbol (e.g. the U7, etc) it is advised to have the signals going to the supply voltages on top (on the side of the block), and the GND on bottom (still on the side).  - Overlapping the GND with the VCC\*. Difficult to read the schematics.  - Consider disentangling nets  - Consider separating decoupling capacitors from nets to increase readability. | Low | None |  |
| 26 | KS | 1) 26/65 add 10u ceramic to the decoupling of each 3V3 pin of the memory  Ok | Med | Fix |  |
|  | ML | - Component designator overlaps with (double) component type. | Med | Fix |  |
|  | KS | 2) What is the scenario for termination between PA3 and Flash Memory?  So far, there was no termination foreseen. Although might be a good idea to introduce some series termination on WE and RE.  Again, I’d say that detailed SI analysis must be performed. I’d also add a serial resistor on the clock line.  I think this is asynchronous interface  Add series termination at WE and RE  Do SI simulations | Med | Fix |  |
| 27 | ML | - Use a signal name for DCLK, DOUT which clarifies that those are GBTx signals. | Med | None |  |
| 28 | ML | - Group the signals to avoid nets crossing when possible. | Low | None |  |
| 29 | MR | Replace 0,12u coilcraft with BLM31PG121SN1 (also used on sheet 25) | Med | Fix |  |
| 34 | JS | GBTx2 should be in transceiver mode, so MODE[3:0] = 0010 | Med | Fix |  |
| 36 | KS | \*) 36/65 - why not all of "NotBonded" pins are connected to GND?  In fact, those are the pins to be connected to the proper bank powersupply for A3PE3000 compatibility. This needs to be done still!  OK | High | Fix |  |
|  | AJ | will it be compatible for 3000L device?  => will connect the 4 GND and 4 VMVx pins in the proper way |  |  |  |
|  | JA.1 | I would prefer that the SCA chip uses SPI to communicate With the APA (I don't really see what the GPIOs are meant for?)  There are already two I2C from SCA to PA3. Should we also add SPI (and/or give up a I2C)?  I2C is fine - I didn't see that (and I might be blind - but I still don't - I only see the GPIOs. I am using the schematic on the twiki - is that the worng one?)  Oke, we stick with I2C | High | None |  |
|  | JA.2 | On the APA I would want a mem mapped design that takes care of scrubbing/initial configuration, flash update etc (also the clock Control and the canbus IF). This has two masters (1) SCA SPI Interface and (2) debug UART Interface. No (2) will only be used during Development and test.  What is needed to make the UART?  Essentially UART is just an idea. I would prefer to have a pinheader With RxD and TxD lines. Preferably we could also include one mre line that is pulled low when the Connector is Connected - this we can use for arbitration between the I2C Master and the UART debug Master  What is a MRE line?  One question: I don't know to well the FX3 chip - could we use this also for a debug interface on the PA3?  You only want to use the FX3-UART or another interface? | High | Discus |  |
|  | JA.3 | Why do the SCA chip Control the selectmap IF directly? Why isn't this fully controlled by the APA? That would be easier?  The SCA chip does not control to selectmap IF. The PA3 does.  Maybe I look at the wrong schematics - but it seems that the SCRUB\_CONTROL is also going to the SCA chip. Is this only for monitoring?  Indeed 3 scrub control lines (INIT, DONE, PROGRAM) go to the SCA only for monitoring | High | None |  |
|  | JA.4 | I miss a debug Interface on the APA. During lab testing this is crucial. It won't be possible to design and test this functionality if the full GBT Chain is needed... I would suggest a pinheader With the possibility to attach an UART IF.  OK, how many pins and what IO voltage?  See JA.2 comments. I just checked the RCU2. Then it was Connected to 3.3V, but I must check if this is mandatory or not. | High | Discus |  |
|  | JA.6 | I am guessing the DIO pins are general purpuse communication pins between the Xilinx and the APA?  That is correct | Low | None |  |
|  | JA.7 | An external Power on Reset chip would be good. In this we we can use this to do the initial configuration of the Xilinx as soon as the board is properly powered. (I missed that when we did the design on the TPC RCU1) | High | Discus |  |
|  | JA | And one final question regarding the reconfiguration: Is it possible to use the ICAP in the XIlinx to Count SEUs at the same time as we are contiously scrubbing over the selectMap Interface? In that case I would og for such a solution as it is much simpler.  Discuss with scrubbing experts | High | Discus |  |
| 37 | ML | - Resistors identifier/value is ambiguous due to congestion.  Will fix this later | Low | Fix |  |
| 38 | ML | - Net name different than pin name | High | Fix |  |
| 37-43 | ML | Add refdes | High | Fix |  |
| 39 | ML | - There is VDD pin shorted to GND. Is it intended to work like this? |  |  |  |
|  | AJ | VMV for "Bank 2 & Bank3 " are grounded , I think related pins it will be internally treated as unused pin?  DS page 3-1 states that VCCIBx and VMVx from unused banks must be connected to GND | High | None |  |
|  | AJ | What is difference if a pin is "Not Bonded (NC)" w.r.t. if one is left floating ?  Both are unconnected pads on the PCB | Low | None |  |
| 43 | KS | \*) 43/65 - VCCIB connected to CLOCK\_CONTROL? It looks like schematic entry error.  This allows the bank to operate on the same supply as the jitter cleaner  Can you please add a remark on the schematic to explain this? | Med | Fix |  |
| 44 | KS | \*) I'd suggest that the power filter as on RUv0a is implemented  I suppose you refer to LC1. This contains inductors. Do you think this will still be effected in the magnetic field?  OK, this is a good point. Anyway, there must be some input filtering, at least some bulk caps.   * + Add electrolitic capacitors   + Add resetable fuse   + Add polarity diode   + KS: investigate what filtering is used on other Cavern boards | Med | Fix  Open |  |
|  | KS | \*) 44/65 all PWRGOOD should be connected to testpoints for easy probing. Also I’d add extra 0R resistor on those lines so that we can play with it if there is something wrong with the power-up sequence.  I can add testpoints.  Where exactly do you want the 0 ohm?  I’d propose to add then just after output from the DC-DC converter. If the power-up-sequence network doesn’t work then we can unsolder 0Rs and we have the nice access to the signals. | Med | Fix |  |
| 45 | ML | In a symbol (e.g. the U11, etc) it is advised to have the signals going to the supply voltages on top (on the side of the block), and the GND on bottom (still on the side). | Med | Fix |  |
|  | KS | \*) 45/65 – please add 10u ceramic close to the 3V3 of ERF8-030-XX.X-X-DV  Ok | Med | Fix |  |
|  | PG | The complete complete part number is ERF8-030-05.0-L-DV-TR | Med | Fix |  |
|  | PG | * 22 is SCL1\_WRITE\_P, should be \*SDA1\_WRITE\_P\* * 24 is SCL1\_WRITE\_N, should be \*SDA1\_WRITE\_N\* | Critical | Fix |  |
|  | SV | Maybe you could move some of the bus wires connected to J63 so that all signal names are fully readable  We will fix the label crossing | Med | Fix |  |
|  | SV | On U11 there is 2x SDA2\_AUX\_READ\_P. I would assume one should be SDA2\_AUX\_READ\_N? |  |  |  |
|  | PG | * 56 is SCL2\_WRITE\_P, should be \*SDA2\_WRITE\_P\* * 58 is SCL2\_WRITE\_N, should be \*SDA2\_WRITE\_N\* | Critical | Fix |  |
|  | PG | Pins 1, 3, 30, 32 on both symbols (DE on SCL#/SDA# READ lines) are floating, should not to be tied to ground?  According to DS page 13, the outputs are ‘Z’ when DE floating | Critical | None |  |
|  | KS | \*) Please add bulk ceramic 47u caps close to on 3V3 pins | Med | Fix |  |
|  | RT | It turns out that the "Power" part using an I2C bus does not fulfill the MFT needs to connect the GBT-SCA which are on the detector to control the DC/DC converters.  After long discussion we think that we will use the FireFly inputs and the built the SCA e-link (3 diff-pairs) using the LVDS I/O. We see that 28 LVDS are foreseen and only 10 are needed for CLK/CTRL for MFT. OK. | High | None |  |
| 46 | ML | - U6 and U55 are without component type. |  |  |  |
|  | KS | \*) 46/65 What is U6 and U55?  They are PT1000. I will include the text PT1000. Shall I change refdes to R?  I’d call them R?  How R277/278 were calculated?  They must be 0 ohm. | Med | Fix |  |
| 47 | ML | - Net name overlapping with nets and components. | Med | Fix |  |
|  | MR | Remove R123/R124 | Med | Fix |  |
| 48 | KS | \*) 48/65 - Input power range of 24FC1025 is 2.5-5.5V. It looks like the memory on the schematic operates out of specification.  According to the datasheet, it can work on 1V8.  <http://www.microchip.com/wwwproducts/en/24FC1025>  The preliminary version of that datasheet states that it can’t operate at 1V8. It was corrected in the new version. | Critical | None |  |
|  | ML | - No component identifier for component with ‘A’ in the middle of the page. |  |  |  |
|  | KS | What is the device that controls PMODEx and FSCLx?  Dipswitch with tristate. I will make the partnumber/farnellcode visible  OK | Med | Fix |  |
| 49 | KS | No termination on the interface between Ultrascale and FX3.  Is that really needed?  This is an interface running at 100MHz. If there is something wrong with the signal integrity we’ll have some serious troubles.  Add series termination on clock line, perform SI analysis on the other lines | Med | Open |  |
|  | KS | \*) 49/65 - no decoupling for VIO5 I will add | Med | Fix |  |
|  | PG | Part should be updated to Micro-B 3.X part: Hirose ZX360D-B-10P (Digi-Key H125269CT-ND) | High | Fix |  |
| 53-  59 | ML | - U15 component symbol has artefacts  - U15 pins on bottom left are unreadable | High | Fix |  |
| 53-  59 | KS | \*) 53-59/65 - In my opinion there is no enough input and ouput capacitance.  On example of 59/65 - for sure there should be no tantal capacitor e.g. C157 in the output capacitance bank. There should be only low-ESR, ceramic ones.  I followed the recommendation from the datasheet page 12: 0.8-1.2V Cout=300u including at least 47u ceramic. There is actually 330u tantal and 300 + 3x100uF ceramic. I will remove the tantal. Can you please increase the input capacitance according to RUv0a?  Add 2 \* 22uF | High | Fix |  |
|  | KS | C255 should be moved before the current monitoring resistor.  Correct, I will change that | Med | Fix |  |
|  | KS | A resistor should be added to set the output voltage ramp-up time.  I suppose a capacitor on the SS/TR pin?  Yes | High | Fix |  |
|  | KS | ILIM connection must be verified.  As I understand, by grounding ILIM, the current limit reduces from 15 to 12 A. 12 A is enough I think.  Ask Johan to test (KS asks or provides email address from Johan to MR) | High | Discus |  |
|  | KS | *I would also like to point out that a special remark should be added on the schematic close to the DC-DC converter that the layout has to be designed according to all the recommendations by TI. I can only say from experience that it's a lot of work to design it properly to achieve the expected performance in terms of output ripple.*  Will do that | High | Fix |  |
| 60 | KS | \*) 60/65 - About the DIP switch, please copy the connection from RUv0a  Ok | High | Fix |  |
|  | SV | Also regarding DIP switches: Should they have pullup resistors, or are there internal pullups in the FPGA? I don't see any pullups, and as far as I can tell the DIPSWITCH inputs on the FPGA will be left floating when the switches are off?  For the DIPswitch, I wanted to rely on the FPGA internal pull-up resisters. Later I realised that for improved radiation immunity, it is likely better to have strong (1kohm) external pull ups. (so it does not matter anymore if the pull-up/down config bit flips). So I would propose to introduce the external pull ups. |  |  |  |
| 61 | KS | \*) 61/65 no decoupling for X6,  Will add that | Med | Fix |  |
|  | ML | NC pin of U39 is not connected to a N/C box. | Low | Fix |  |
|  | ML | - L23, L24 seem to connect +2v5 to +3v3. I guess this is a SHORT-CIRCUIT. |  |  |  |
|  |  | why 2 power rails are connected to X6?  It allows the use of the 3,3V SE oscillator as well as the 2.5V differential. One (L24) should be NP | Med | Fix |  |
|  | KS | R187 to be verified with X6 datasheet, 100R seems wrong to me.  It is just a pull down. What do you propose?  I’d propose 1k | Med | Fix |  |
|  | SV | I noticed that INN0 goes to OUTPUT+, and INP0 goes to OUTPUT- on X6.  We will change symbol and check proper connection on sheet 61 and 62 | Med | Fix |  |
|  | MR | Change J54 and J53 to resistor jumpers | High | Fix |  |
| 62 | ML | - L22, L20 seem to connect +2v5 to +3v3. I guess this is a SHORT-CIRCUIT. |  |  |  |
|  | KS | \*) 62/65 L20/L22 - It will be a short! It can't be designed like that!  Yes, one L should be NP | Critical | Fix |  |
|  | ML | Pin 2 of component X5/7 is not connected to N/C box. | Low | Fix |  |
|  | ML | - X5/7 is double. |  |  |  |
|  | KS | I don't understand that. **It looks like 2 components are on top of each other.**  Will check this | High | Fix |  |
|  | KS | No decoupling for that oscillator.  Will add that | Med | Fix |  |
|  | ML | - Termination scheme between component X5/7 and U38 is not clear. |  |  |  |
|  | KS | \*) 62/65 - I don't understand the connection between X5 and U38. It looks like there is double 100R termination. The termination scheme between CLOCKDES6 and U38 seems wrong to me. Is there any reference for that?  I took it from figure 39 & 40 from  <https://www.silabs.com/documents/public/reference-manuals/si53xx-reference-manual.pdf>  Now it is indeed double. I will make the 100 ohm NP or remove it. | Med | Fix |  |
|  | ML | U38 symbol is confusing. | Med | Fix |  |
|  | ML | U38 has no component type. | High | Fix |  |
|  | MR | Consider the use of tristate-DIP switch | Med | Fix |  |
| 63 | PG | * The JTAG pinout is the Atmel AVR JTAG one, fine if this is the intended one. * Pin 4 is supposed to provide reference voltage if we want to comply to the standard (max 3 mA load)   The PROG\_MODE is for IGLOO2. So I think it should be disconnected. | Low | None |  |
|  | ML | J2 is overlayed with some other component: cannot be read. |  |  |  |
|  | SV | duplication of numbering on connector J2, hard to read | Med | Fix |  |
|  | KS | \*) 63/65 - J2 connector, there is something wrong with the numbering. Why there are 2 different connectors J2 and J31 for the JTAG? I am really worried about signal integrity of that chain.  In fact, there are 3 sources: SCA, J2 front panel connector and the PA3 programm connector. All these 3 devices will be located close to J2 (the front panel connector) | High | None |  |
|  | ML | - QS3VH126S1G has no component designator. => Place properly | Med | Fix |  |
|  | ML | Close to J2 there is a GND label which makes no sense. | Low | Fix |  |
|  | PG | Xilinx pinout JTAG with 1.5 supply voltage, on front panel, is OK, the TRST line is additional to Xilinx specs.  The TRST is there to allow a PA3 programmer to be connected via the frontpannel (using a patch cable.) The TRST is unconnected in the Xilinx programmer, so that should not give problems | Med | None |  |
| 64 | PG | * Following are suggestions NOT TO BE IMPLEMENTED unless agreed with Power Board team (they did fix the pinout) * [SCL1\_WRITE\_N, SCL1\_WRITE\_P] now on pins (10, 12) -> move to pin [12, 13] * [SDA1\_WRITE\_N, SDA1\_WRITE\_P] now on pins (13, 14) -> move to pin [20, 21] * [SCL2\_WRITE\_N, SCL2\_WRITE\_P] now on pins (16, 18) -> move to pin [22, 23] * [SDA2\_WRITE\_N, SDA2\_WRITE\_P] now on pins (20, 23) -> move to pin [24, 25] * [SCL2\_AUX\_WRITE\_N, SCL2\_AUX\_WRITE\_P] now on pins (24, 25) -> move to pin [26, 27] * [SDA2\_AUX\_WRITE\_N, SDA2\_AUX\_WRITE\_P] now on pins (26, 27) -> move to pin [28, 29] | Low | None |  |
|  | ML | There is a GND (label? net? comment?) over to pin 61 of the SN65MLVD080. | Med | Fix |  |
|  | PG | * Pins 1, 2, 29, 32 on both symbols (DE on SCL#/SDA# READ lines) are floating, should not to be tied to ground?   According to DS page 13, the outputs are ‘Z’ when DE floating | Med | None |  |
|  | PG | * Pin 33, is not a 1k resistor to ground suggested (as implemented in U11 and U12)? | Critical | Fix |  |
|  | KS | \*) 64/65 - how the decoupling capacitors are shared between different ICs?  Each of both ICs gets half the the capacitors  Can you please mark it on the schematic? | Low | None |  |
|  |  | 64/65 - J58 - I don't like connecting the power of the whole board over a jumper. I think it's worth considering to add here a 1mR resistor and current measuring circuit to have the knowledge of how much current the board draws.  I can change this to resistors   * O-ohm resistor | Med | Fix |  |
|  | KS | Is it necessary to have the possibility to choose 5V or 12V? Isn't 12V a baseline?  Maybe when operating multiple boards in VME, the 5V provides more power.  This should be discussed at WP10 | Med | None |  |
| 65 | KS | \*) I'd propose to add a separate RST signal for each of the GBTx and SCA chips.  This was the initial idea. However, connecting the individual switches to the PWRGOOD\_1V5 signal was not possible. Therefore, it was decided (in one of the WP10 meetings) to use only one switch.  I am not sure that this is a good idea. It should be discussed again. I don’t like the idea that the output from the DC-DC converter control the reset of the board. I’d propose to add serial resistors on the RST lines so that in case of any drama we can access them separately. | Med | None |  |
|  | KS | \*) 65/65 - I don't like that reset scheme. If a reset signal after power-up is required then I'd suggest using a dedicated reset signal generator IC that asserts a reset signal for a known interval of time.  This should then also be rad-tolerant  Yes, we must look for a component like that. It has to be discussed at WP-10  Reset switch mainly for testing purposes, not used in cavern. GBTx has its own power-on reset. External reset should not be connected to active circuits to incease SEU immunity. Decided: Do not use external reset chip.  Open: KS has doubts on connection to 1V5 powergood | Med | None  Open |  |
| PCB | KS | Additional ESD fingers 1Mohm to GND | Med | Fix |  |
|  | MR | 0603 AC coupling capacitors oke for high speed signals? | Med | Open |  |