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ITS upgrade

RUv1 manual

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Document History

Version	Date	Author	Section	Description
0.1	24-August-2017	M.J. Rossewij	-	First concept.

Contents

1 Introduction

This a preliminary version of the document describing the RUv1 hardware.

1.1 Block-schematic

1.2 Clocking scheme

1.3 Configuration scheme

2 Connectors

The table below gives an overview of the RUv1 connectors. More details are presented in the following subsections.

CONNECTORs		Type	Function/Intended for
J0	POWER	SL508-4-90B	Power-in for table top operation
J1	VME J1 style	DIN41612	Power-in for rack operation & alternative Power board control
J2	Transition Board	QFS-104-01-SL-D-RA	Interface to Alpide sensor modules via transition board
J3	VTRx	TYCO 1888247	Primary (sensor) data uplink & control/status link
J4	VTTx		Up to 2 optional (sensor) data uplinks
J5	VTRx		Downlink for receiving trigger/timing
J6	USB3	micro B SuperSpeed	USB3 connector for table top operation
J7	BUSY_AUX	ERF8-010-01-L-D-RA-L	BUSY signal and optional links for future applications
J8	JTAG	MOLEX_08783-1420	Programming FPGAs (compatible with Xilinx 20 pin connector)
J9	CAN	MOLEX087833-0420	Access in absence of DAQ/GBT system
J10	Power mezzanine Board	ERF8-030-05.0-L-DV-TR	Primary path for Power board control & LEDs
J11	JTAG	HTST-105-01-L-DV-A	Programming FPGAs (compatible with Microsemi connector)
J12	GBTx I2C interface	Boxed header 4x2	Access to GBTx registers using CERN USB-I2C dongle
TEST-CONNECTORs			
J13	Xilinx pinheader	TSM-110-04-T-DV	Connected to Bank47 (1,8V)
J14	PA3 pinheader		Connected to Bank 5 (3,3V)
J15	JitterCleaner_IN+	SMA	Alternative/external input for jitter cleaner
J16	JitterCleaner_IN -		
J17	clockBuffer_IN+		Alternative/external input for 1-8 LVDS clock buffer
J18	clockBuffer_IN -		
J19	clockBuffer_OUT -		1-8 LVDS clock buffer output 6
J20	clockBuffer_OUT+		
J21	XilinxIO -		Xilinx bank 68 (1V8) differential test IO
J22	XilinxIO+		
J23	FAN connector	MOLEX-22-11-2032	FAN power connector

2.1 J0, Power connector

For table top operation, Power can be applied on the J0. Voltage can range from 5…12V. Take care that the voltage applied is compatible with the FAN connected to J23. Typical settings:

Voltage (V)	Current (A)
5	3
12	1,5

REMARK: THE RUV1 J0 polarity is reversed to RUV0 !!!!!

J0 pinnout:

Pin	Function	
1,2	Power_In	
3,4	GND	

2.2 J1 VME style

The type and position of the J1 connector is compatible with the VME standard, including the location of the (GND, 5 & 12V) power pins. When using J1, the placement of the polyswitch-fuses determines which J1 power input is used:

Voltage (V)	Current (A)	F2	F3
5	3	PolySwitch 5A 2920L500/16MR	Absent
12 (DEFAULT)	1,5	Absent	PolySwitch 2A2 2920L200DR

REMARK: Do not place both Polyswitch fuses (F2&F3) as this results into a short
Also here, take care that the voltage selected is compatible with the FAN connected to J23.

The complete J1 pinout is shown below:

	VME-J1				J1 backplane		
	Row A	Row B	Row C		Row A	Row B	Row C
1.	D00	BBSY	D08		GNDA	GNDA	GNDA
2.	D01	BCLR	D09				
3.	D02	ACFAIL	D10				
4.	D03	BG0IN	D11				
5.	D04	BG0OUT	D12		SCL1_AUX_WRITE_N		SCL1_AUX_READ_N
6.	D05	BG1IN	D13		SCL1_AUX_WRITE_P		SCL1_AUX _READ_P
7.	D06	BG1OUT	D14		SDA1_AUX_WRITE_N		SDA1_AUX _READ_N
8.	D07	BG2IN	D15		SDA1_AUX_WRITE_P		SDA1_AUX _READ_P
9.	GND	BG2OUT	GND		GND		GND
10.	SYSCLK	BG3IN	SYSFAIL		SCL1_WRITE_N		
11.	GND	BG3OUT	BERR		GND		
12.	DS1	BR0	SYSRESET		SCL1_WRITE_P		
13.	DS0	BR1	LWORD		SDA1_WRITE_N		
14.	WRITE	BR2	AM5		SDA1_WRITE_P		SCL1_READ_N
15.	GND	BR3	A23		GND		SCL1_READ_P
16.	DTACK	AM0	A22		SCL2_WRITE_N		SDA1_READ_N
17.	GND	AM1	A21		GND		SDA1_READ_P
18.	AS	AM2	A20		SCL2_WRITE_P		SCL2_READ_N
19.	GND	AM3	A19		GND		SCL2_READ_P
20.	IACK	GND	A18		SDA2_WRITE_N	GND	SDA2_READ_N
21.	IACKIN	SERCLK	A17				SDA2_READ_P
22.	IACKOUT	SERDAT	A16				
23.	AM4	GND	A15		SDA2_WRITE_P	GND	
24.	A07	IRQ7	A14		SCL2_AUX_WRITE_N		SCL2_AUX_READ_N
25.	A06	IRQ6	A13		SCL2_AUX_WRITE_P		SCL2_AUX_READ_P
26.	A05	IRQ5	A12		SDA2_AUX_WRITE_N		SDA2_AUX_READ_N
27.	A04	IRQ4	A11		SDA2_AUX_WRITE_P		SDA2_AUX_READ_P
28.	A03	IRQ3	A10				
29.	A02	IRQ2	A09				
30.	A01	IRQ1	A08				
31.	-12 V	+5 V STDBY	+12 V				+12V
32.	+ 5 V	+5 V	+5 V		+5V	+5V	+5V

GNDA (& R234) was introduced to enable the use of 1:1 backplanes instead of a standard VME backplane.

The RUv1-J1 connector provides (besides power-in) also an alternative path for the Power board control signals (using differential MLVDS). As this is the secondary path, the MLVDS transceivers are by default disabled: R244…R249=Not placed. To enable, make R244=R246=R247=R249=1k. R245 & R248 provides the option to enable power module 1 and/or 2 via the VME backplane. In that case, make R244…R249=1k.

2.3 J2 Transition board

After inserting the transition board in J2, it can be fixated with 4 M2 bolt/nuts. The J2 pinout can be found in the schematics.

2.4 J3 VTRx

J3 allows the installation of a VTRx to provide the primary GBT transceiver path for data and control. The VTRx should be fixated with 2 M1.4 screws.

2.5 J4 VTTx

J4 allows the installation of a VTTx to provide up to 2 additional GBT uplink data channels. The VTTx should be fixated with 2 M1.4 screws.

2.6 J5 VTRx (single mode)

J5 allows the installation of a VTRx (-SingleMode) to provide a receive path for the trigger (and LHC bunch clock). The VTRx (-SingleMode) Tx channel is unconnected and the Rx channel is connected with GBTx2. The VTTx (-SingleMode) should be fixated with 2 M1.4 screws.

2.7 J6 Micro B USB3

J6 is a Micro B USB3 (super speed) receptable, intended for table op operation and/or when no GBT/DAQ system is available.

2.8 J7 BUSY-AUX connector

The BUSY_AUX connector has the following pinout:

pin	Signal	Pin	signal
1	GND	2	GND
3	BUSY_IN_P	4	BUSY_OUT_P
5	BUSY_IN_N	6	BUSY_OUT_N
7	GND	8	GND
9	AUX_dp0	10	AUX_dp1
11	AUX_dn0	12	AUX_dn1
13	GND	14	GND
15	AUX_dp2	16	AUX_dp3
17	AUX_dn2	18	AUX_dn3
19	GND	20	GND

The BUSY_OUT signal goes to the Xilinx US MGT27 transmitter and the BUSY_IN goes to the Xilinx US MGT27 receiver. The receiver is shared with the 27^{th} sensor receiver pair. The connectivity of the MGT27 receiver is selected by placing/removing the proper capacitors:

MGT27 receiver function	C319&C320	C526/C530
ALPIDE_DATA_MGT_27	Removed	Placed
BUSY_IN	Placed	Removed
Default (bad SI due to stubs)	Placed	Placed

The 4 AUX signals are connected to the Xilinx US FPGA select IO (e.g. LVDS) and routed as differential pairs. The direction (IN/OUT/BI) is determined by the firmware. These signals are intended for optional future use.

2.9 J8 JTAG connector (front panel)

The front panel JTAG connector is compatible with the Xilinx 20 pin connector. The SCA-JTAG, J8 and J10 can act as JTAG masters and are connected in parallel. Placing the Xilinx download cable automatically disconnects (using PGND to disable U19, the FET switch) the SCA JTAG master from the JTAG chain.

2.10 J9 CAN connector

This CAN is intended to provide an alternative patch to access the RU and Power board when the GBT/DAQ system is not available. The CAN connector has the following pinout:

pin	Signal	Pin	signal
1	CANL	2	GND
3	CANH	4	GND

There is no CAN bus termination on the RU.

2.11 J10 Power mezzanine

The main function of the power mezzanine is to provide the primary access path to the power board using several I2C busses. The power mezzanine also has 6 LEDS: LED[0:3] are connected to the Xilinx US FPGA and LED[4:5] go to the Microsemi PA3 FPGA. The power mezzanine can be fixated using 2 M2.5 bolts/nuts. The J10 pinout can be found in the schematics.

2.12 J11 JTAG connector (Microsemi-FlashPro compatible)

J11 allows direct connection of the microsemi FlashPro(4) download cable. When connecting the download-cable, the SCA-JTAG master is automatically disconnected (by disabling U19, the FET switch) from the JTAG chain. Jumper J11 also disabling U19 (and disconnects the SCA-JTAG) and provides improved GND connection to the FlasPro download cable.

2.13 J12 GBTx I2C connector

J12 provides a path to access and program the GBTx with the Cern configuration software by connecting the CERN USB-I2C dongle. To access to the GBTx from the dongle, the Xilinx I2C master and the SCA I2C[7] master must be disabled. If the SCA I2C lines cannot be disabled (e.g. when using SCA version 1), the SCA I2C can be disconnected by removing R277 & R278. By default, each GBTx is set to a unique I2C address using resistors:

device	Address1	Addres2	Address	FusePower	FusePulse
GBTx	R14=NP	R190=NP	0x1	R279	R280
GBTX1	R26=100Ω	R191=NP	0x3	R282	R283
GBTX2	R39=NP	R192=100Ω	0x5	R41	R287

As it is not known is the GBTx-EFUSE process can be controlles by I2C, individual resistors (shown above) can be placed/removed to provide the FusePower and FusePulse to an individual GBTx.

2.14 J13 Xilinx GPIO header

Provides access to 10 signals from Xilinx bank 47 (1,8V).

2.15 J14 PA3 GPIO header

Provides access to 10 signals from PA3 Bank 5 (3,3V). RUv1.0 has a patch that also header pin 9 (CE2) & 10 (R/B2) to the flash memory.

2.16 J15 & J16 Jitter Cleaner SMA differential input

To provide an external clock signal to the jitter cleaner. Intended for test purposes. Selection of the jitter cleaner input source is done by S10_A1 or CS signal (coming form PA3):

S10[1]	R162	CS	Jitter Cleaner source
0	NP	X	GBTx Clockdes6
T	0	0	
T	0	1	Oscillator X2 OUT or SMAJ15/J16 In
1	NP	X	

Furthermore resistors or capacitors must be placed on J44 and J45 in such a way that the SMA signal (and not the oscillator signal) is propagated to the jitter cleaner. Optionally, Oscillator X2 can be disabled by placing 1kΩ on R344 (default).

2.17 17 & J18 Jitter Cleaner output/clock buffer input

Provides a path for monitoring the jitter cleaner output or can act as an external input for the clockbuffer. In the latter case, the JitterCleaner output should be disabled by setting S10[4:3]=LM and the IN_SEL should be pulled high (with R341 or from the PA3).

2.18 J19 & J20 Clock Buffer SMA differential output

Clock buffer LVDS monitoring output.

2.19 J21 & J22 Xilinx SMA differential IO

Xilinx US differential test output. Connected to bank 68 (1V8).

2.20 J23 Fan Connector

The Fan connector was initially designed to be compatible with RUv0. To be compatible with the FANs ordered, it was decided to place the FAN connector reversed. After the reversal, the pinout is:

Pin	Signals
1	GND
2	J1_5V & powerIn(=5…12V) when F2 placed
3	J1_12V & powerIn(=5…12V) when F3 placed

When operating the RUv1 with 12V present J1 (Pin 31 row C), it might be needed to cut/disconnect pin3 from the connector J23.

3 Jumpers

The table below gives an overview of the RUv1 jumpers:

RefDes	Function	Default
J25	FX3 power 1V2	1-2 (GND)
J26	FX3 power 1V8	1-2 (GND)
J27	FX3 power 3V3	1-2 (GND)
J28	FX3 power VIO5	1-2 (FX3 1V8)
J29	JTAG2 bypass FX3	2-3 (bypass)
J30	JTAG2 bypass GBTx	1-2 (bypass)
J31	JTAG2 bypass GBTx1	1-2 (bypass)
J32	JTAG2 bypass GBTx2	1-2 (bypass)
J33	JTAG bypass PA3	1-2 (include)
J34	JTAG bypass Xilinx	1-2 (include)
J35	JTAG bypass JTAG2	2-3 (bypass)
J36	JTAG forward TRST2	2-3 (GND)
J37	JTAG forward TMS2	2-3 (GND)
J38	J38 forward TCK2 Terminate TCK	2-4 (GND) 1-3 not placed
J39	Disconnect SCA-JTAG & extra GND FlashPro cable	Not placed
J40	Power LED	Not placed
J41	GBTx configSelect	2-3 (GND, IC channel)
J42	GBTx1 configSelect	2-3 (1V5, I2C)
J43	GBTx2 configSelect	2-3 (1V5, I2C)
J44	JitterCleaner_CLKIN2- select SMA or X2 Oscillator	X2 Oscillator (see picture)
J45	JitterCleaner_CLKIN2+ select SMA or X2 Oscillator	

Default refers to the setting during the actual Alice experiment.

3.1 J25, J26 & J27 FX3 power 1V2, 1V8 & 3V3

The USB3 functionality is intended for stand-alone/table top operation (when GBT system in not available) and is therefore not qualified for a radiation environment. As in the actual (Alice) experiment all data/control data transfer will go via the GBTx links, the USB FX3 chip must be disabled (powered down) in order to avoid radiation related issues like latch-up (SEL). For this purpose are jumper J25-J27, which have their default setting to GND.

3.2 J28 FX3 power VIO5

J28 sets the voltage (1V5 or 1V8_USB3 or GND) on FX3-VIO5 rail/bank which powers the FX3 JTAG and I2C interface. The lowest voltage where the I2C serial EEPROM (U8, U9: 24FC1025 used to store the FX3 boot image) can operate on is 1,8V. All RUv1 devices in the JTAG chain operate on 1,5V (determined by the GBTx DIO power rail). So when doing a boundry scan test (only needed with the production test), the jumper should be set to 1,5V (FX3 booting from the I2C PROM might fail in this situation). When operating the RU in a table-top situation, FX3 booting from EEPROM requires J28 to be set to 1V8_USB3 (and J26 to 1V8). In the actual (Alice) experiment, the FX3 must be switched off (so J25…27) and J28 must be set to 1V8_USB3 (which is also to GND due to J26).

3.3 J29, J30 & J32 JTAG2 bypass FX3, GBTx, GBTx1 & GBTx2

These jumpers are used to include (or disable) JTAG by connecting TDI from corresponding IC to the daisy chain (or GND). The FX3 and GBTx JTAG functionality is limited to boundry scan and will therefore only be used for (production) test and not during the experiment. Therefore the default jumper position is to GND.

3.4 J33 JTAG bypass PA3

J33 includes (or bypasses) the PA3 in the primary JTAG chain. The PA3 JTAG provides besides boundry scan also the FPGA configuration interface. It is foreseen to be the primary path to reprogram the PA3

(from the SCA JTAG master) when the system is installed. Therefore the default configuration is to include the PA3 in the chain.

3.5 J34 JTAG bypass Xilinx

J34 includes (or bypasses) the Xilinx in the primary JTAG chain. The Xilinx JTAG provides besides boundry scan also access to the FPGA configuration logic. As this provides a path for scrubbing actions, the Xilinx JTAG is included in primary JTAG chain in the default configuration.

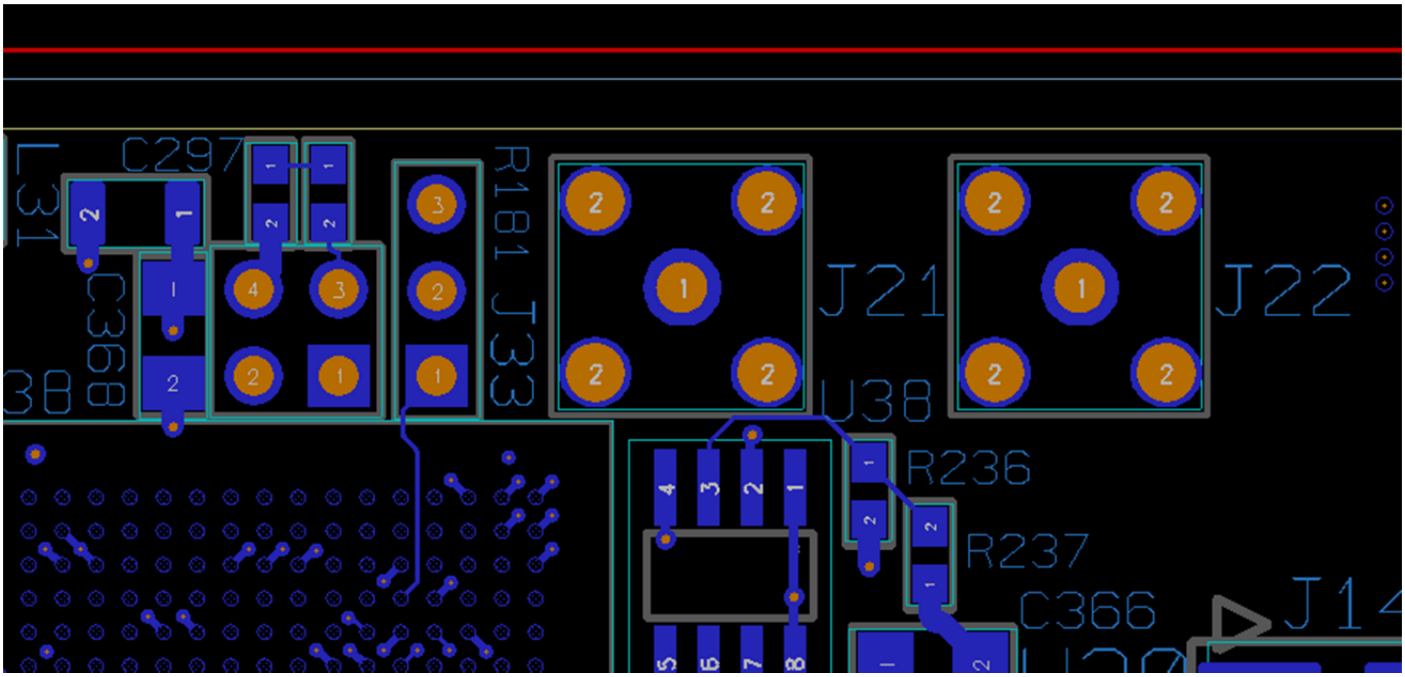
3.6 J35 JTAG bypass JTAG2

J35 allows to include the secondary JTAG chain (=JTAG2). As JTAG2 ICs (FX3 and GBTx) only support boundry scan, it should only be included with production test. The default configuration is therefore to bypass JTAG2.

3.7 J36, J37 & J38

J36, J37 & J38 are needed to forward the TRST, TMS and TCK to the secondary JTAG chain (=JTAG2). As JTAG2 ICs (FX3 and GBTx) only support boundry scan, it should only be enabled with production test. The default configuration is therefore force the JTAG2 signals to GND.

J38 in addition the option the terminate TCK (from the primary JTAG) with 68Ω and 100pF in series. Initial test showed that this termination network is not effective and it is therefore disabled in the defaults configuration.



3.8 J39 Disconnect SCA-JTAG & extra GND FlashPro cable

Placing J39 disables the FET switch (U19: QS3VH126S1G) which disconnects the SCA JTAG master from the JTAG chain. In addition, it provides an improved GND connection to the FlashPro cable. As the SCA-JTAG master is intended for accessing the FPGA configuration when the system is installed, the jumper should not be placed in the default configuration.

3.9 J40 POWER to INIT LED

J40 enables or disables the bicolored LED D2 which indicates the status of the INIT signal. As no light sources are allowed in the magnet during the experiment, the jumper must not be placed in the default configuration.

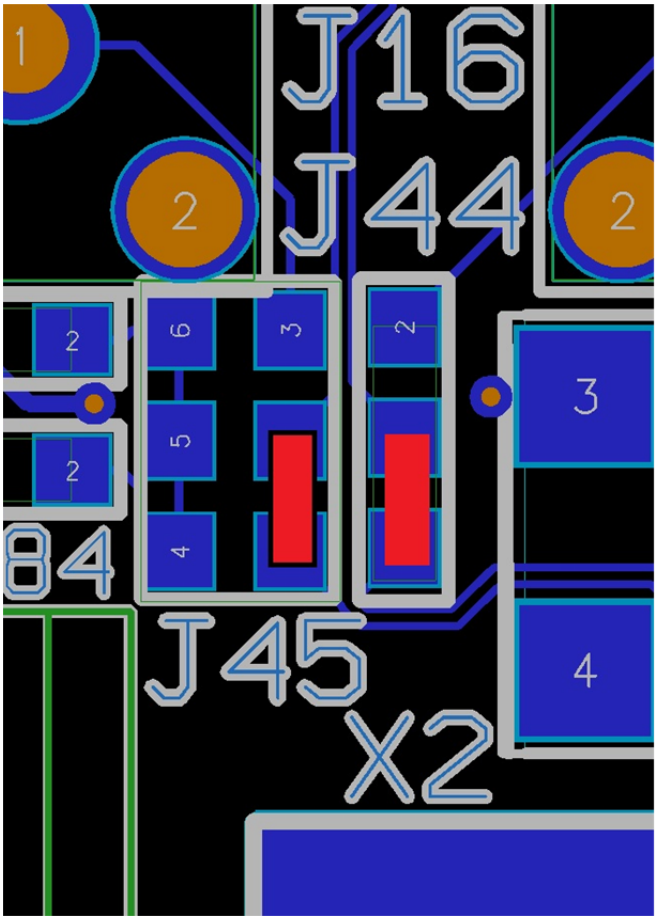
RUv1.0 has a bug causing the LED not to work properly. Jumper J40 should therefore never be placed on RUv1.0.

3.10 J41, J42 & J43 GBTx configSelect

J41, J42 & J42 select whether the GBTx, GBTx1 and GBTx2 are configured via the IC channel (optical link) or the GBTx I2C interface (using the Cern USB-I2C dongle or the Xilinx FPGA as I2C master). In the default configuration, GBTx is set to the IC channel (allowing it to be controlled directly from the control room GBT link) while GBTx1 and GBTx2 are controlled via I2C.

3.11 J44 & J45 JitterCleaner_CLKIN2 select SMA or X2 Oscillator

These are nit pin-header jumpers bet SMA resistor/capacitor selection circuits allowing the source of the JitterCleaner CLKIN2 input, i.e. the SMA connector or the X2 Oscillator. The default configuration is the X2 Oscillator with 100nF coupling as shown below:



4 Switches

The RU has the following switches

S0…S3	Push button connected to both PA3 and Xilinx Pushed =>HIGH (1V8) Relaxed => LOW (GND)
S4	Push button: Reset Jitter Cleaner (U18: Si5316)
S5	Push button: Reset GBTx, GBTx1 GBTx2 and SCA
S6	Push button: Pulls Xilinx PROGRAM signal low
S7	Push Button: Reset FX3 (U5: CYUSB3014)
S8	10 channel DIP switch connected to both PA3 and Xilinx ON position => High (1V8) OFF position => LOW (GND) Intended for testing purposed or to set a CAN bus address
S9	DIP switch for FX3 configuration (see below)
S10	DIP switch for jitter cleaner configuration (see below)

4.1 S9 FX3 configuration

S9 is an 8 channel DIP switch. Each channel has 3 states:

1. +: HIGH, pulled to 1V8
2. 0: Floating
3. -: LOW, pulled to GND

S9 channel	Function	Default
1	PMODE[0]	-
2	PMODE[1]	0
3	PMODE[2]	-
4	FSLC2	-
5	FSLC1	-
6	FSLC0	-
7 & 8	Unused	X

PMODE selects the FX3 boot source:

PMODE[2:0]	Boot from
F11	USB boot
F1F	I2C, On failure USB Boot is enabled
1FF	I2C only

RUv1 has the 19.2MHz crystal installed, therefore FSLC0…2 must be set to -. In fact, the FSCL pins refer to the CVVQ_FX3 power rail which is on RU connected to 3,3V. As S9 HIGH is 1,8V, this would possibly not work. Fortunate, all FSLC pins must be pulled down.

4.2 S10 JitterCleaner configuration

S10 is an 8 channel DIP switch. Each channel has 3 states:

1. +: High, pulled to VSI (2,5 or 3,3V)
2. 0: Middle/Floating
3. -: Low, pulled to GND

S10 channel	Name	Function	Default
1	CS	Clock Select	
2	DBL_BY	Output disable/bypass	
3	SFOUT[0]	Signal Format Select	M
4	SFOUT[1]		H
5	FRQSEL[0]	Frequency select	L
6	FRQSEL[1]		M
7	BWSEL[0]	PLL bandwidth Select	TBD
8	BWSEL[1]		TBD

CS: Clock Select

L	CLKIN1: GBTx CLOCKDES6
M	Selection controlled by PA3
H	CLKIN2: Oscillator X2 or external CLK via SMA J15/J16

DBL_BY: Output disable/bypass

L	CKOUT enabled
M	CKOUT disabled
H	Bypass mode with CKOUT enabled

SFOUTn: Signal Format Select

HM	LVDS
HL	CML
MH	LVPECL
ML	Low Swing LVDS
LH	CMOS
LM	Disabled
others	Reserved

FRQSEL: Frequency select

FREQSEL[1:0]	F_{MIN}(MHz)	F_{MAX}(MHz)
LL	19.38	22.28

LM	38,75	44.56
LH	77.5	89.13
ML	155	178.25
MM	310	356.5
MH	620	710

The optimal PLL bandwidth Select (BWSEL) needs to be determined experimentally.

5 LED

The RUv1.0 has one bi-colored LED (D2) indicating the XILINX FPGA INIT signals status:

RED	
GREEN	

6 Xilinx

The Xilinx has the following bank:

Bank	Voltage	Interface/functioin
0	1,5V	Configuration/Slave SelectMap
44	GND	Unused
45	1V8	FX3 interface (DQ[0:31], CTL[0:12], INT_n, CLK, RESET, UART_RX/TX)
46	1V8	GBTx SLVS (DIN[0:9], DOUT[0:9], DCLK[0:1])
47	1V8	GBTx1 SLVS (DIN[0:9]) GBTx CLOCKDES[2:3] LOCALCLK[2] AUX[0:3] differential signals LED[0:3] GPIO PINHEADER
48	1V8	GBTx2 SLVS (DIN[0:9], DOUT[0:9], DCLK[0:1]) PUSHBUTTON[0:3]
64	3V3	Alpide Sensor Control Interface (DCLK[0:5], DCTRL[0:5]) Power Board Interface (SCL1/2_(AUX)_READ/WRITE, SDA1/2_(AUX)_READ/WRITE,)
65	1V5	Slave SelectMap
66	1V8	Alpide Sensor Datal Interface (ALPIDE_DATA_GPIO[1:24])
67	1V5	GBTx/1/2 CMOS signals (TXRDY, RXRDY, RXDATAVALID, TXDATAVALID) I2C master to GBTx1/2 SCA (GPIO[0:11], I2C4 slave, SPI slave)
68	1V8	Alpide Sensor Datal Interface (ALPIDE_DATA_GPIO[0], ALPIDE_DATA_GPIO[25:27]) DIPSWITCH[0:9] PA3 single ended IO (PA3_IO[0:11]) PA3 diff. out (PA3_IO_d[0:4]) PA3 diff. in (PA3_IO_d[5:9])

7 PA3

The PA3 has the following banks:

Bank	Voltage	Interface/functioin
0	1V8	PA3 single ended IO (PA3_IO[0:11]) DIPSWITCH[0:9] PUSHBUTTON[0:3] LED[4:5]
1	1V5	Xilinx SelectMap (D[0:7], CCLK, CSI_B, DONE, INIT, PROGRAM, RDWR)
2	GND	Unused
3	GND	Unused
4	VSI	Jitter Cleaner Control signals (C1B, C2B, LOL, CS, RST)
5	3V5	Flash (DATA[0:7], CONTROL) CAN (D, R, LBK, RS) WATCHDOG/POWERON reset
6	1V5	SCA (GPIO[12:19], I2C0 slave, I2C5 slave)
7	2V5	Xilinx diff. in (FPGA_IN_d[0:4]) Xilinx diff. out (FPGA_OUT_d[5:9]) Clock input (CLOCKDES5, LOCAL_CLK) Clock Selection signal (IN_SEL) for Clock Buffer (U17:CDCLVD1212)

VSI is determined by the placement of L24 (3V3) or L25 (2V5).