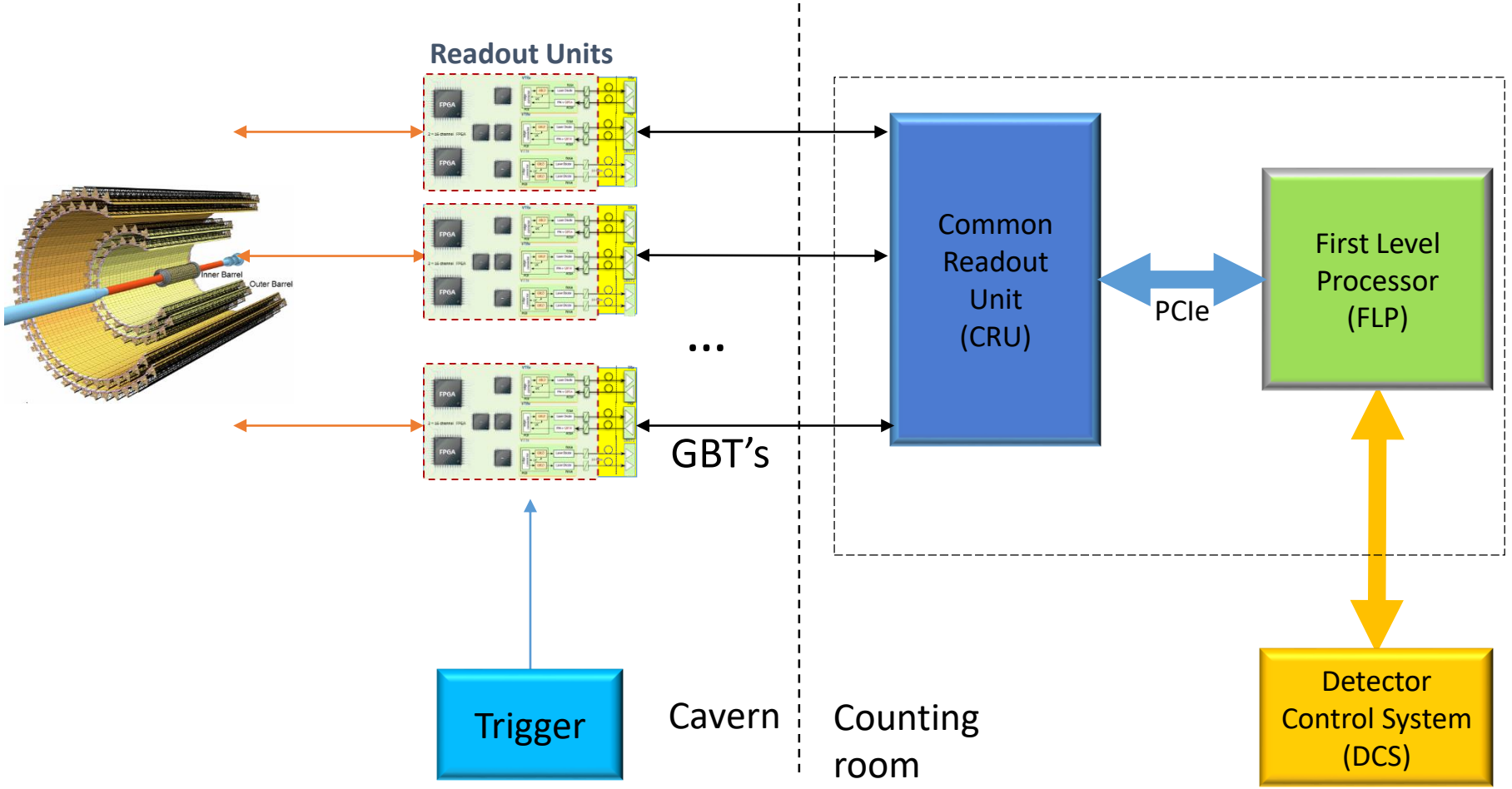
ITS Prototype Boards Progress Report

Joachim Schambach

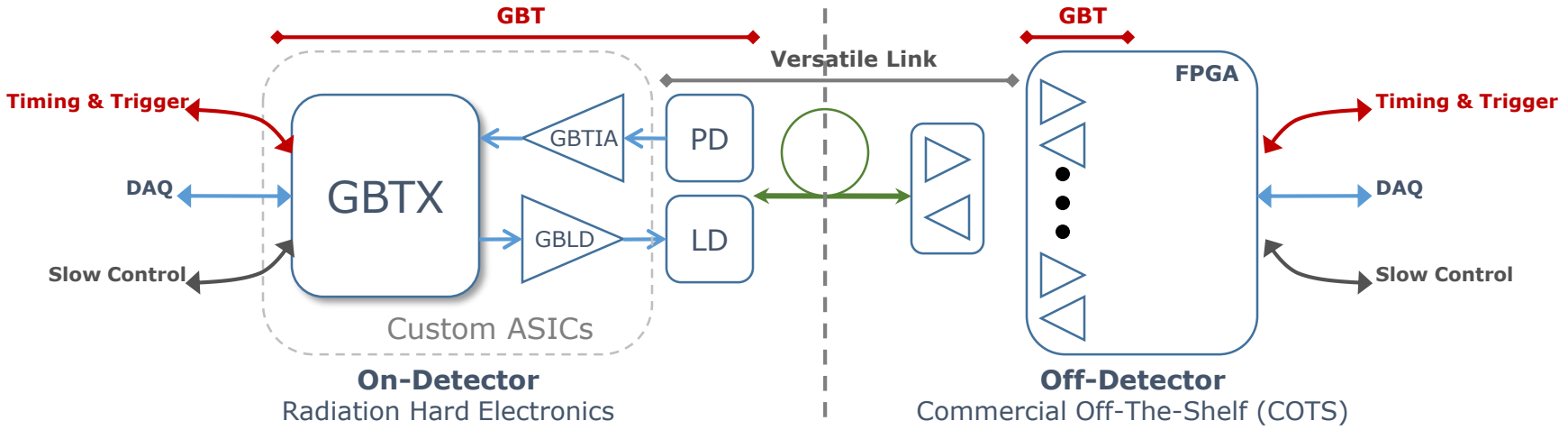
Joachim.Schambach@cern.ch

University of Texas at Austin

Readout Electronics – connections with ALICE



GigaBitTransceiver (GBT)

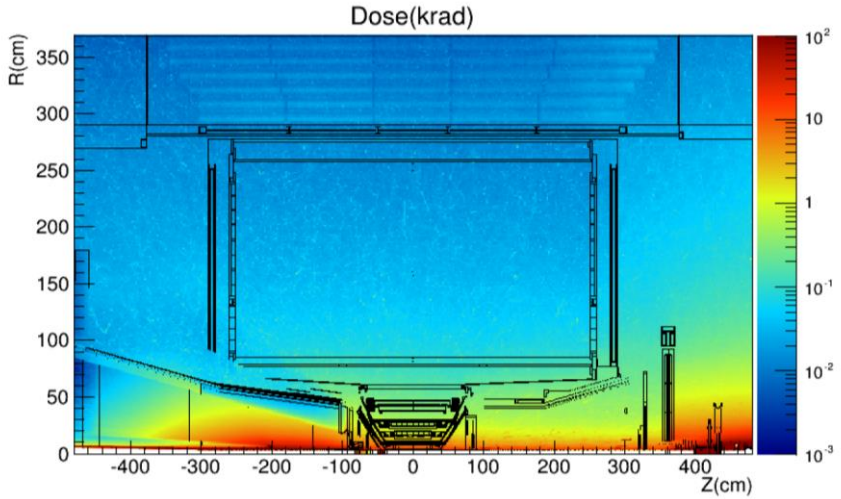


Development of an high speed bidirectional radiation hard optical link:

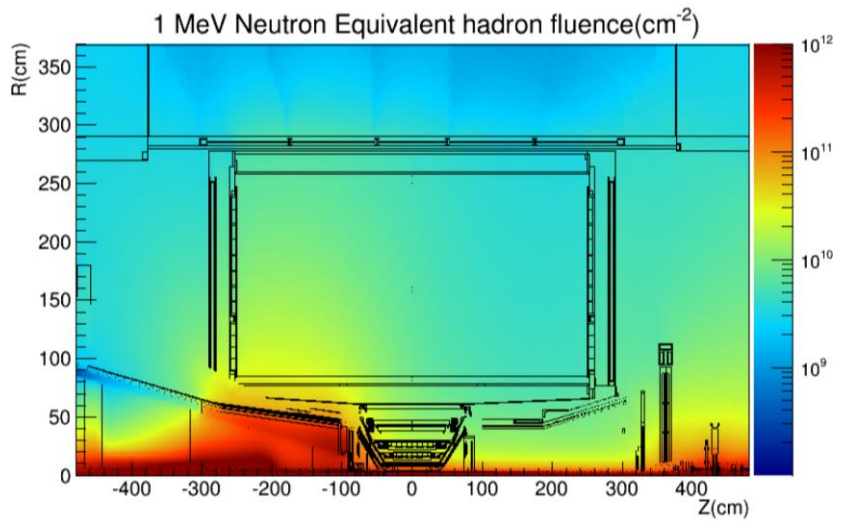
- *GBT project:*
  - ASIC design
  - Verification
  - Functionality testing
  - Packaging
- *Versatile link project:*
  - Opto-electronics
  - Radiation hardness
  - Functionality testing
  - Packaging

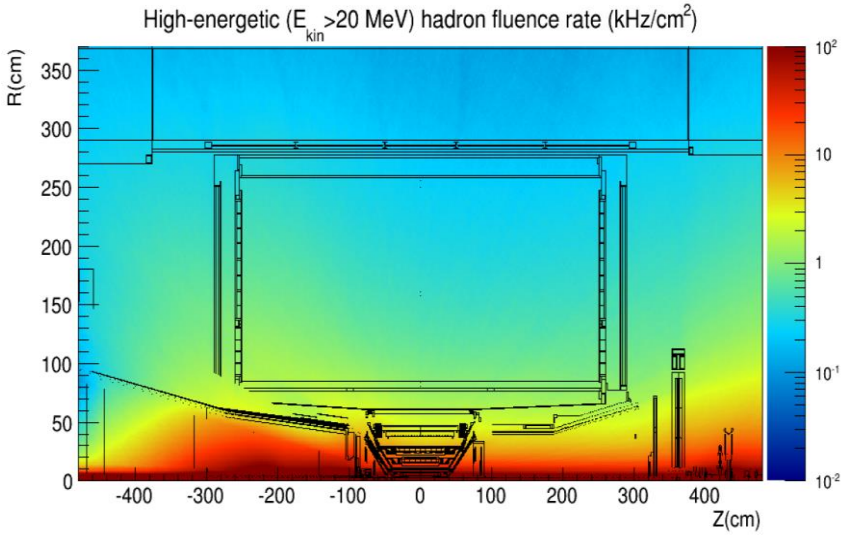
- The GBTX supports three frame types:
  - ***"GBT" Frame (3.28 Gb/s user bandwidth)***
  - ***"Wide Bus" Frame (3.52 Gb/s)***
  - ***"8B/10B" Frame (4.48 Gb/s)***
- GBT Frames include "Forward Error Correction"

Readout Electronics – Radiation Environment



At a distance of 5 meters, slightly off-axis from the collision centre (~90cm radius), a radiation tolerance of 5.7 kRad and 7×10^{11} 1MeVneq is still required.

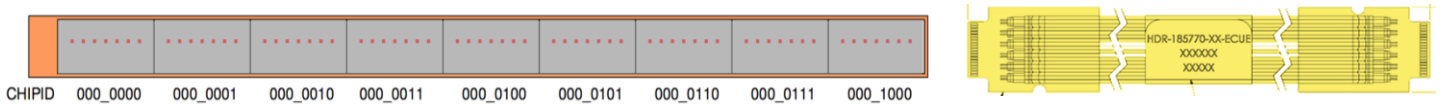




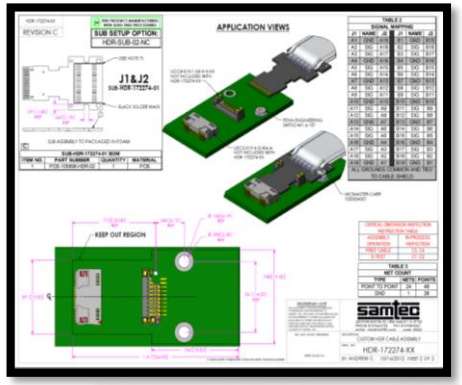
Readout Electronics – ITS high speed links

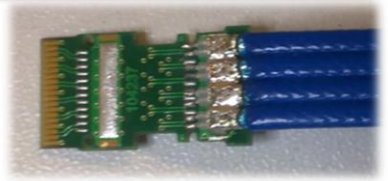
ILs

9 **data lines (1200Mb/s each)**, 1 **clock**, 1 **control**



Inner layers (0, 1, 2) staves: 9 masters for each stave

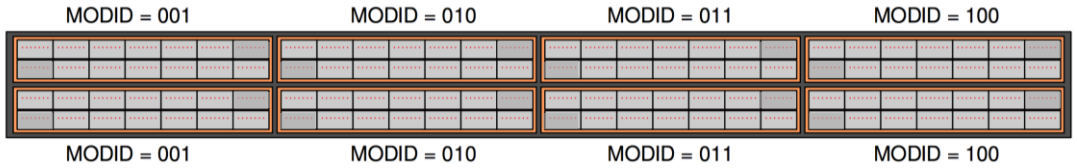


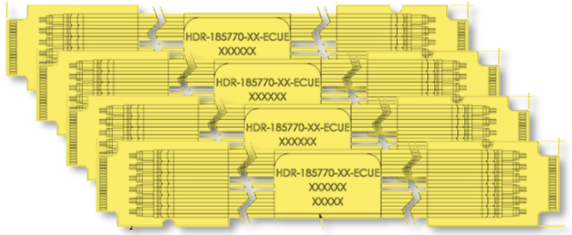


Samtec "Firefly"

MLs

(4+4+4+4) **data lines (400Mb/s each)**, (1+1+1+1) **clock**, (1+1+1+1) **control**

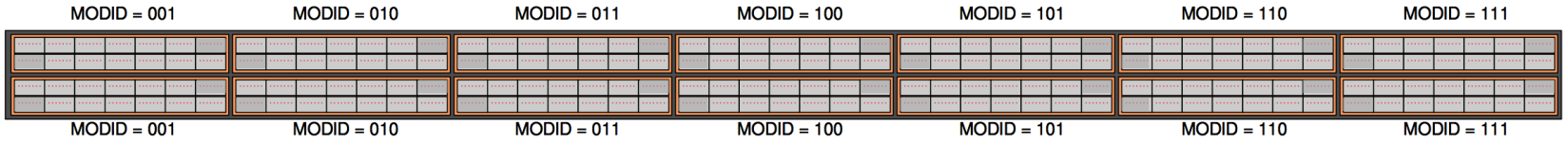


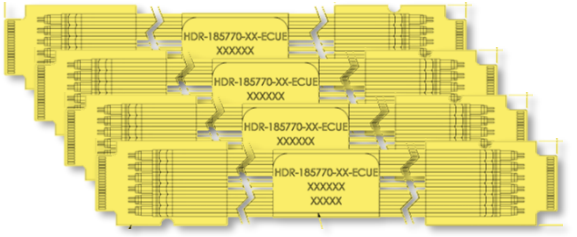


Mid layers (3, 4) staves: 8 modules, 112 sensors

OLs

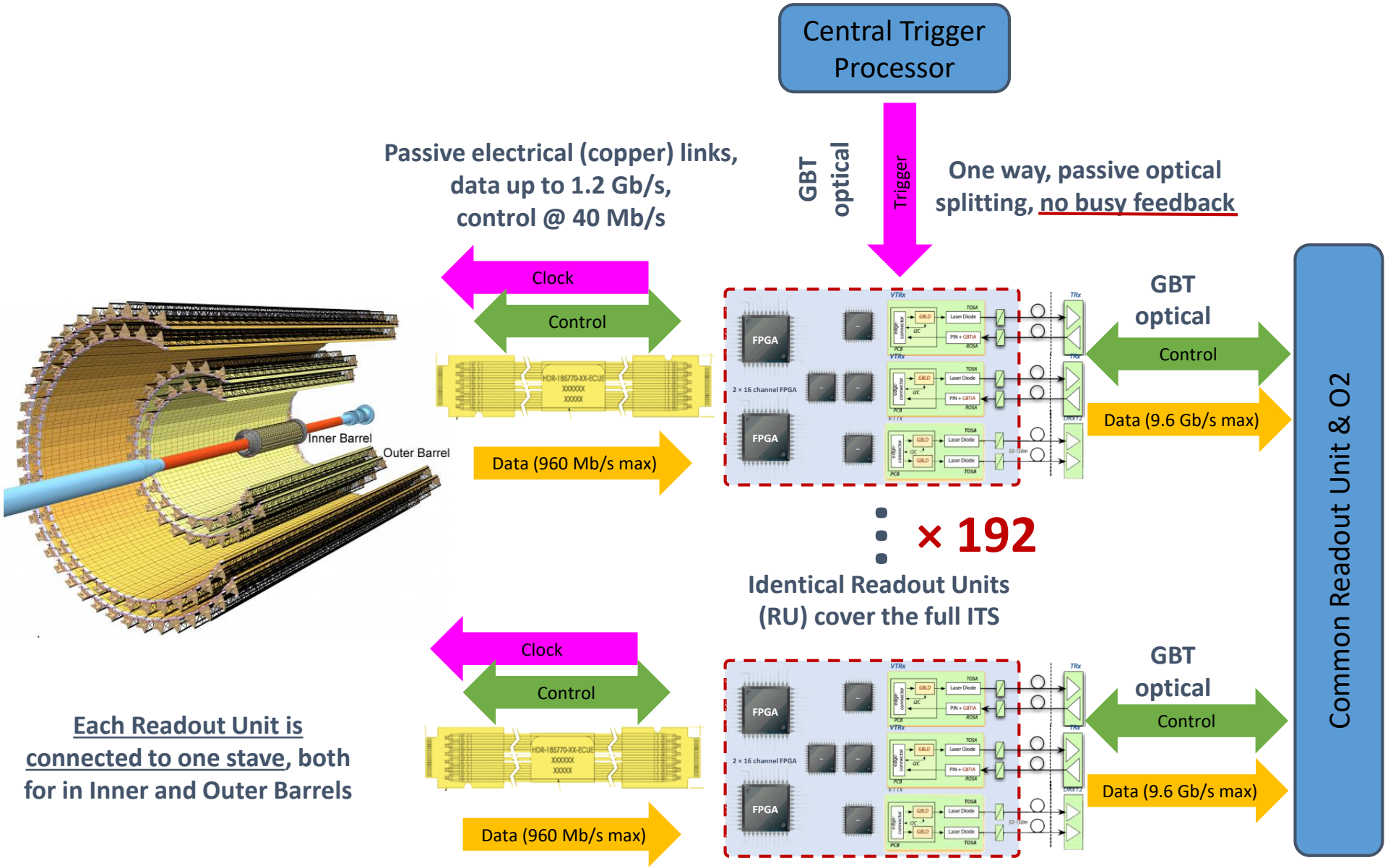
(7+7+7+7) **data lines (400 Mb/s each)**, (1+1+1+1) **clock**, (1+1+1+1) **control**



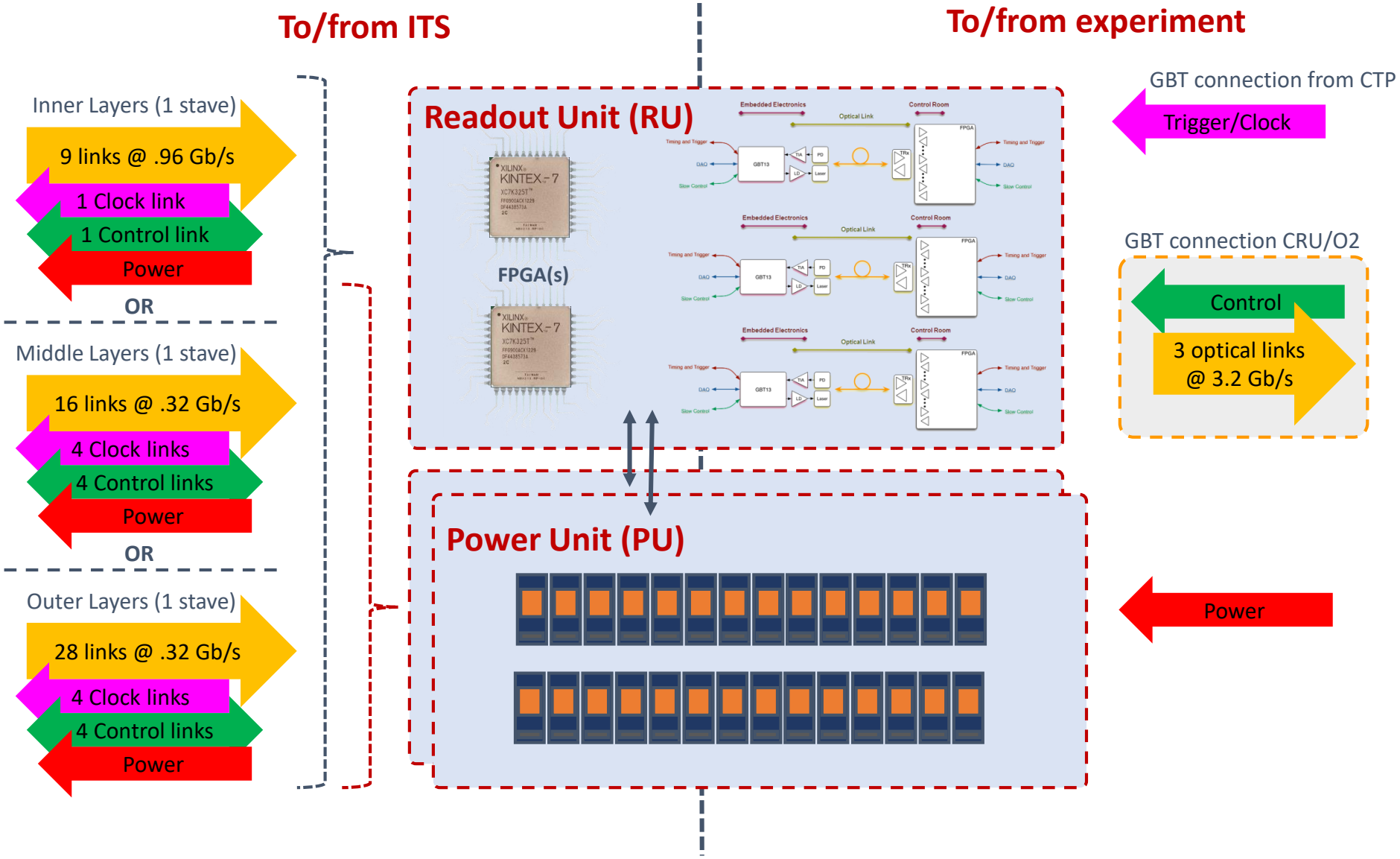


Outer layers (5, 6) staves: 14 modules, 196 sensors

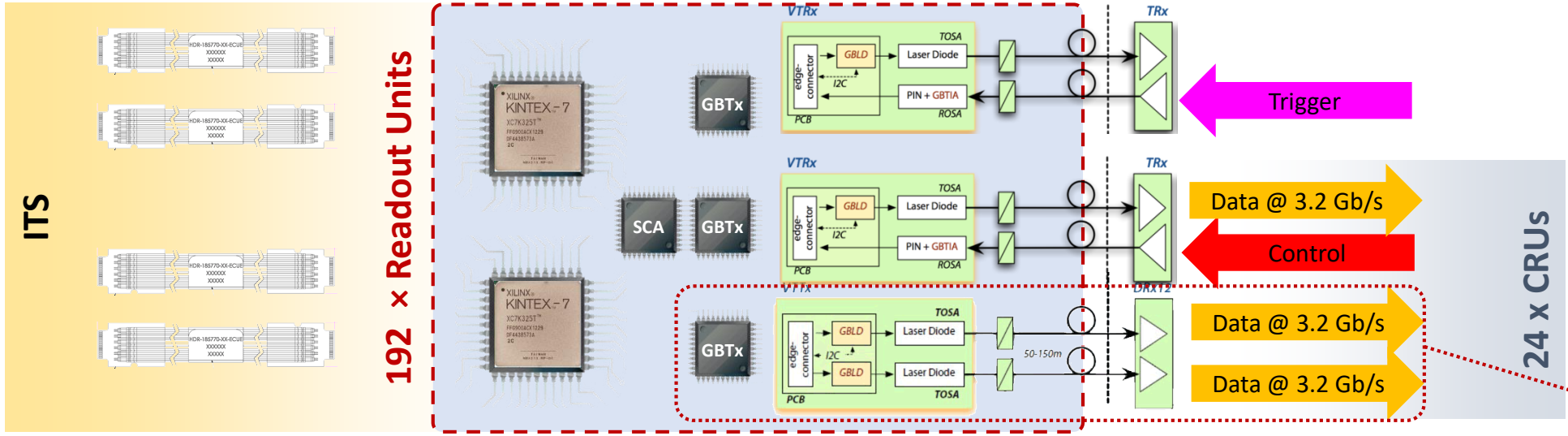
Readout Electronics Architecture – overview



Modular Readout Design



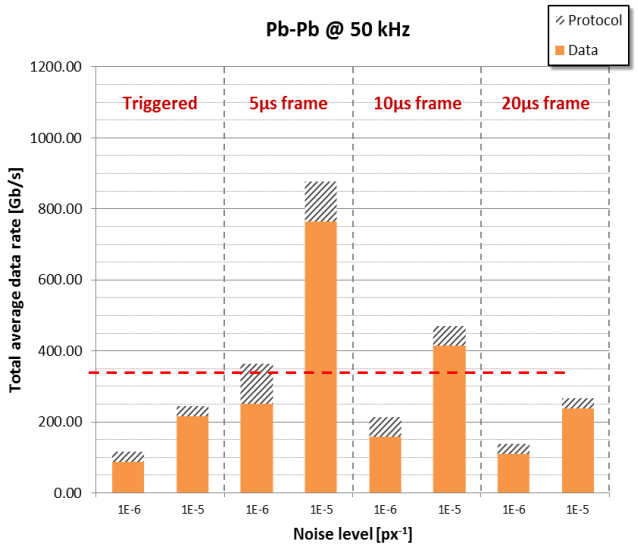
Readout Unit – Part Counts

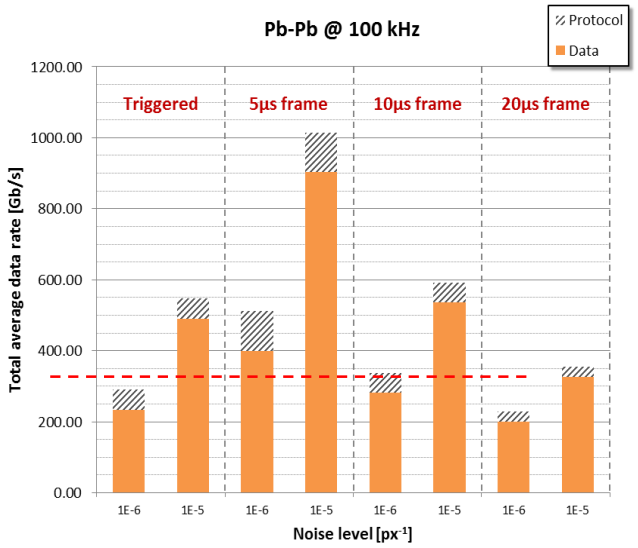


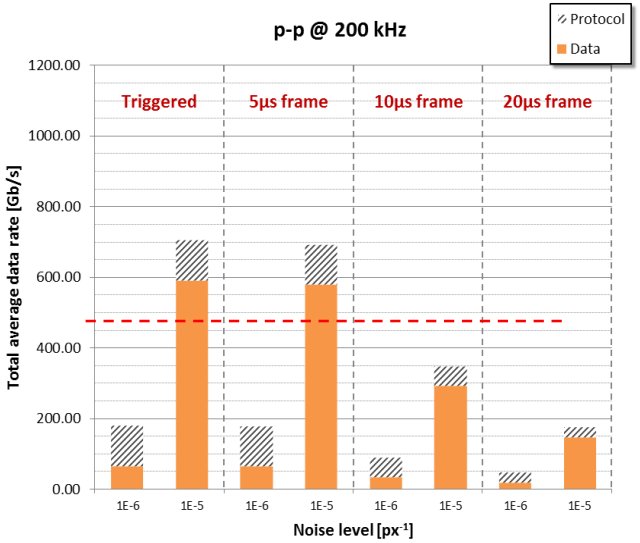
Layout			Power	Readout Units GBT connections						
Layer	Staves	FireFly Cables	**PUs** per layer	RUs per stave	**RUs** per layer	VTRx per layer	VTTx per layer	**TRG** fibers per layer	**Data** fibers per layer	**DCS** fibers per layer
0	12	12	3	1	12	24	12	12	36	12
1	16	16	4	1	16	32	16	16	48	16
2	20	20	5	1	20	40	20	20	60	20
3	24	96	48	1	24	48	24	24	72	24
4	30	120	60	1	30	60	30	30	90	30
5	42	168	168	1	42	84	42	42	126	42
6	48	192	196	1	48	96	48	48	144	48
Total		**624**	472		**192**	**384**	**192**	**192**	**576**	**192**

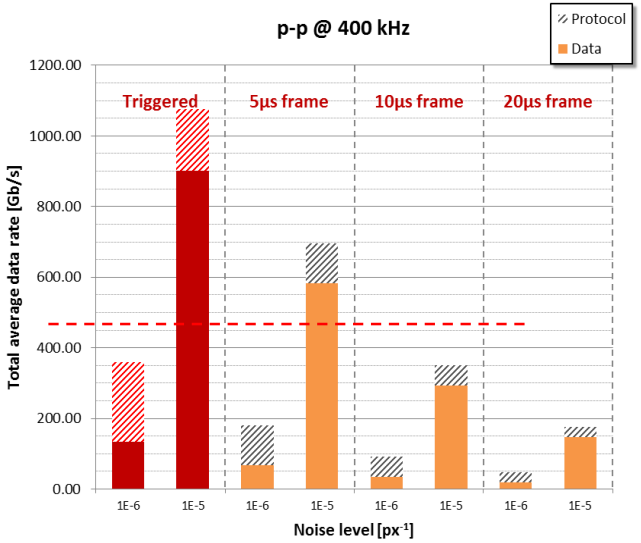
Not mandatory for "baseline" (Pb-Pb @ 50 kHz) operations.

Aggregate Data Rates







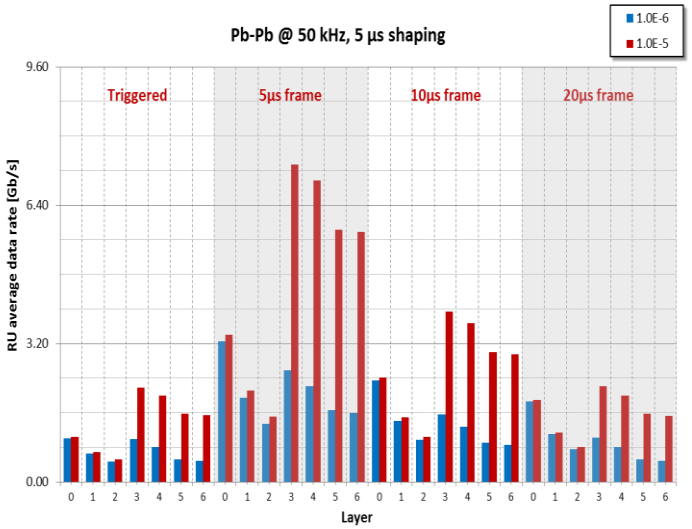


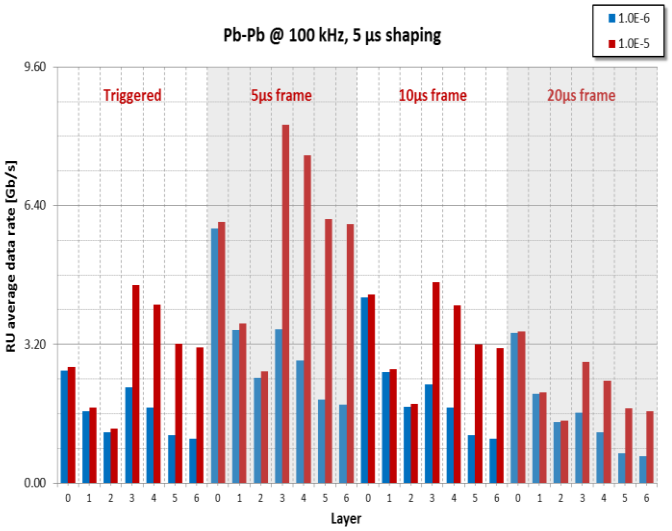
- Initial DAQ/O2 bandwidth: ~40 GB/s
- 400 kHz p-p triggered mode looses data in the simulation (red bars)

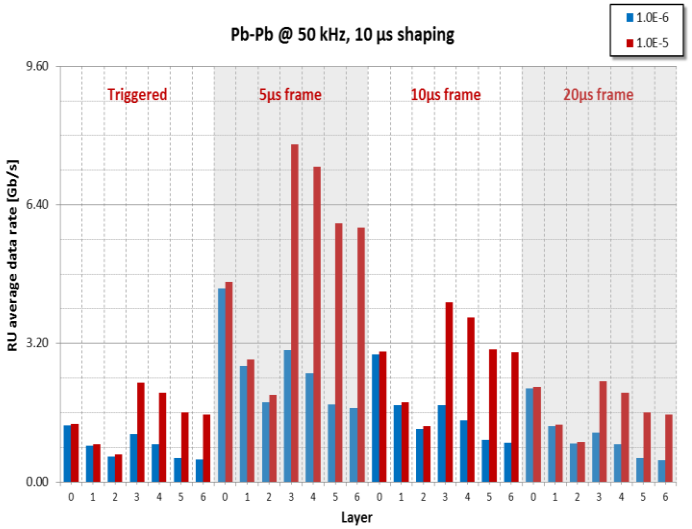
Take-away message:

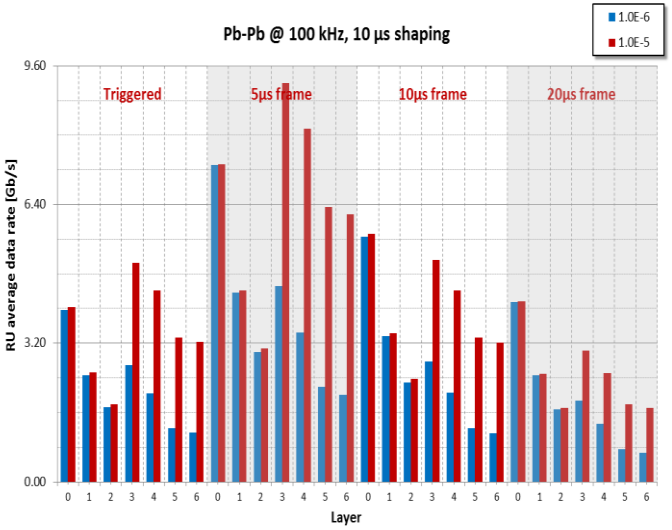
- All running conditions allow for scenarios that fit well within the allocated bandwidth

Pb-Pb Data Rates

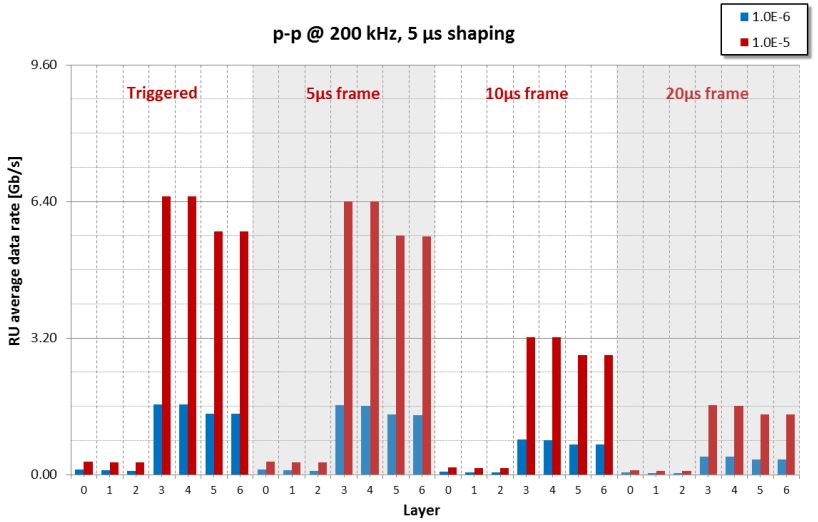


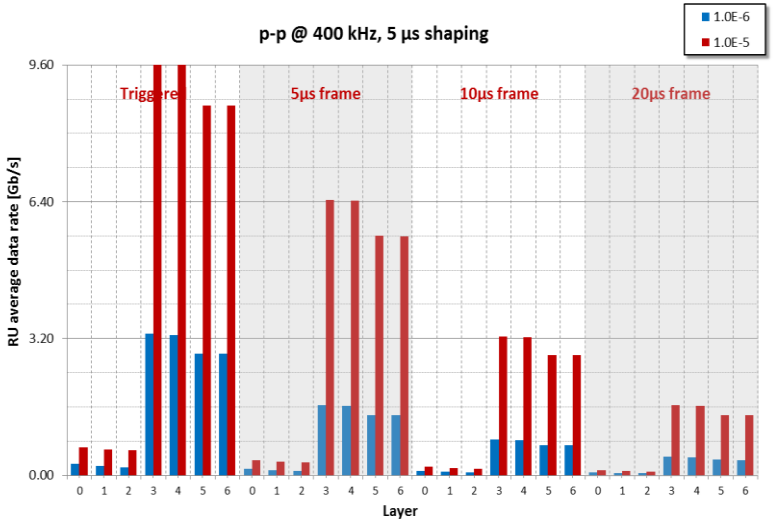


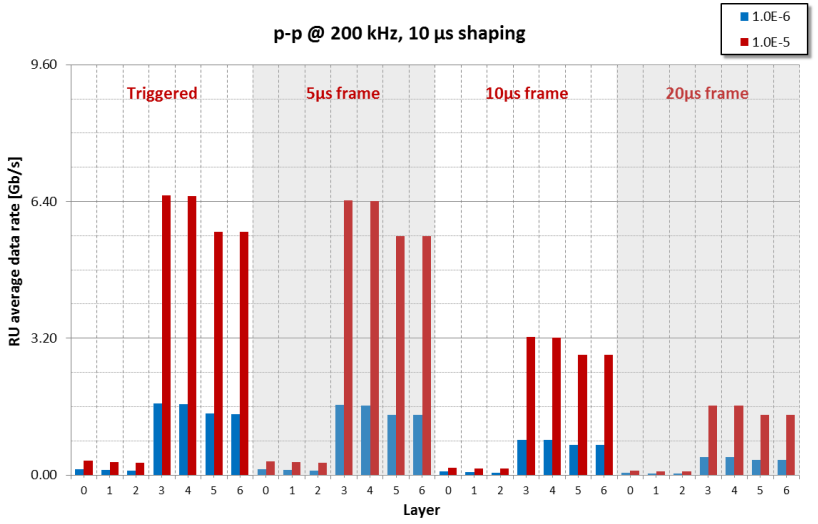


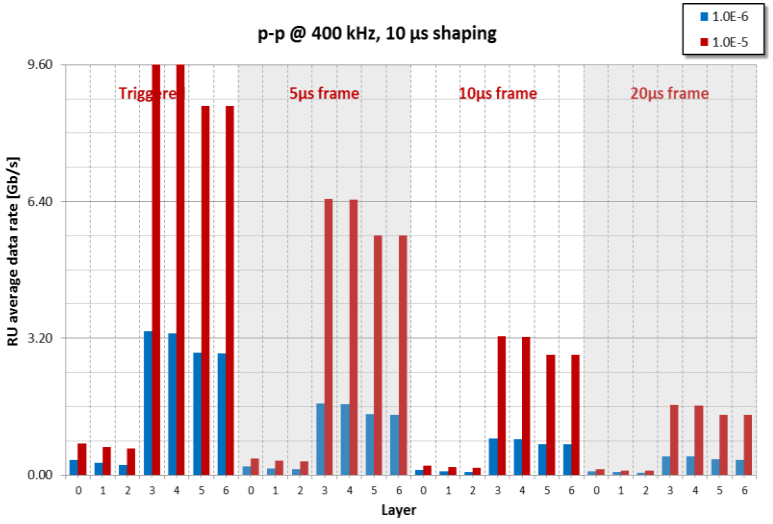


p-p Data Rates

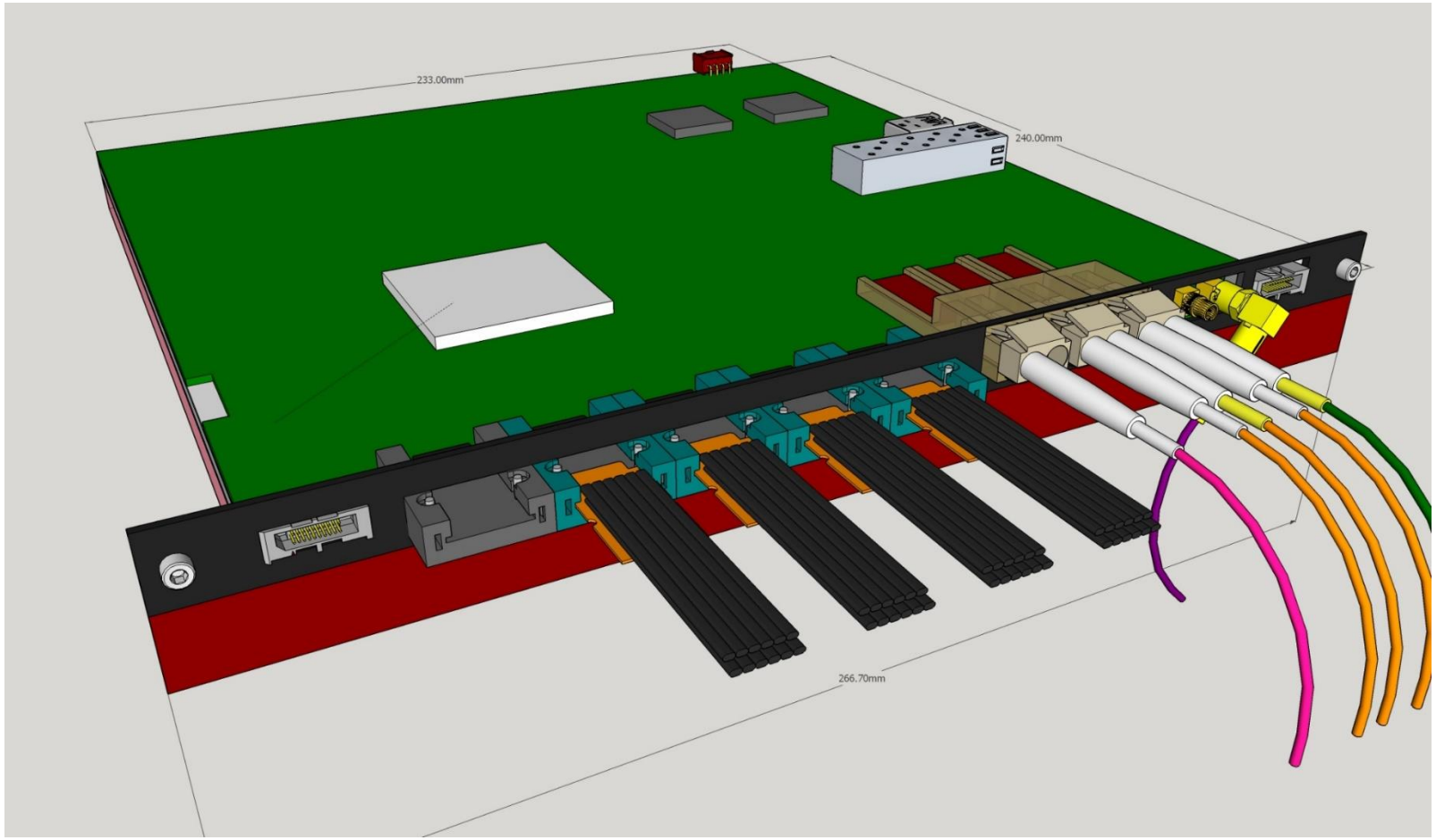






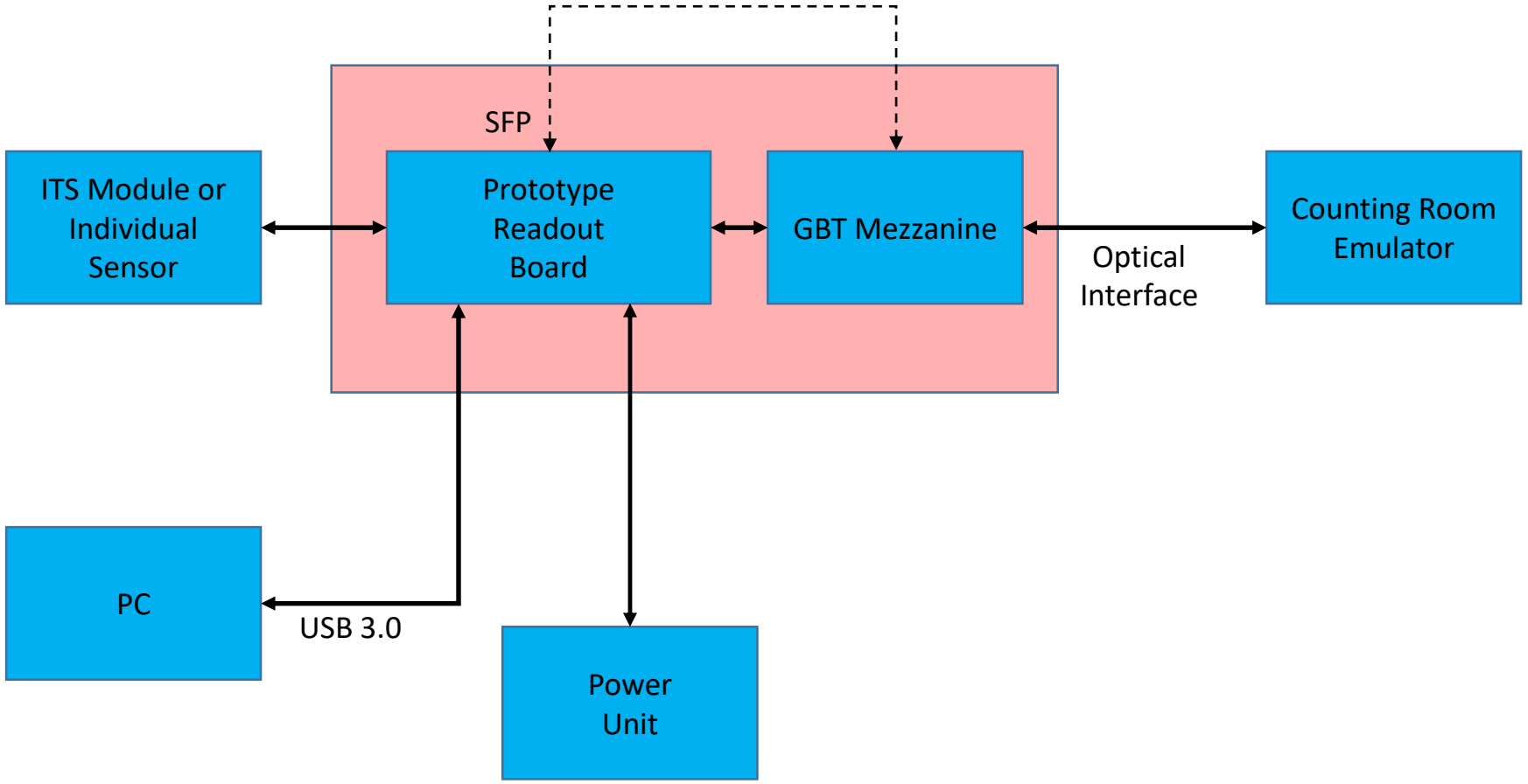


Readout Units – board physical dimensions estimate



- A **“standard” 233 × 160 mm² board** should fit all the electronics for the RU. There is room to increase the depth (>160 mm) if necessary.
- Power Connectors could be placed on the back, allowing for a cleaner wiring.

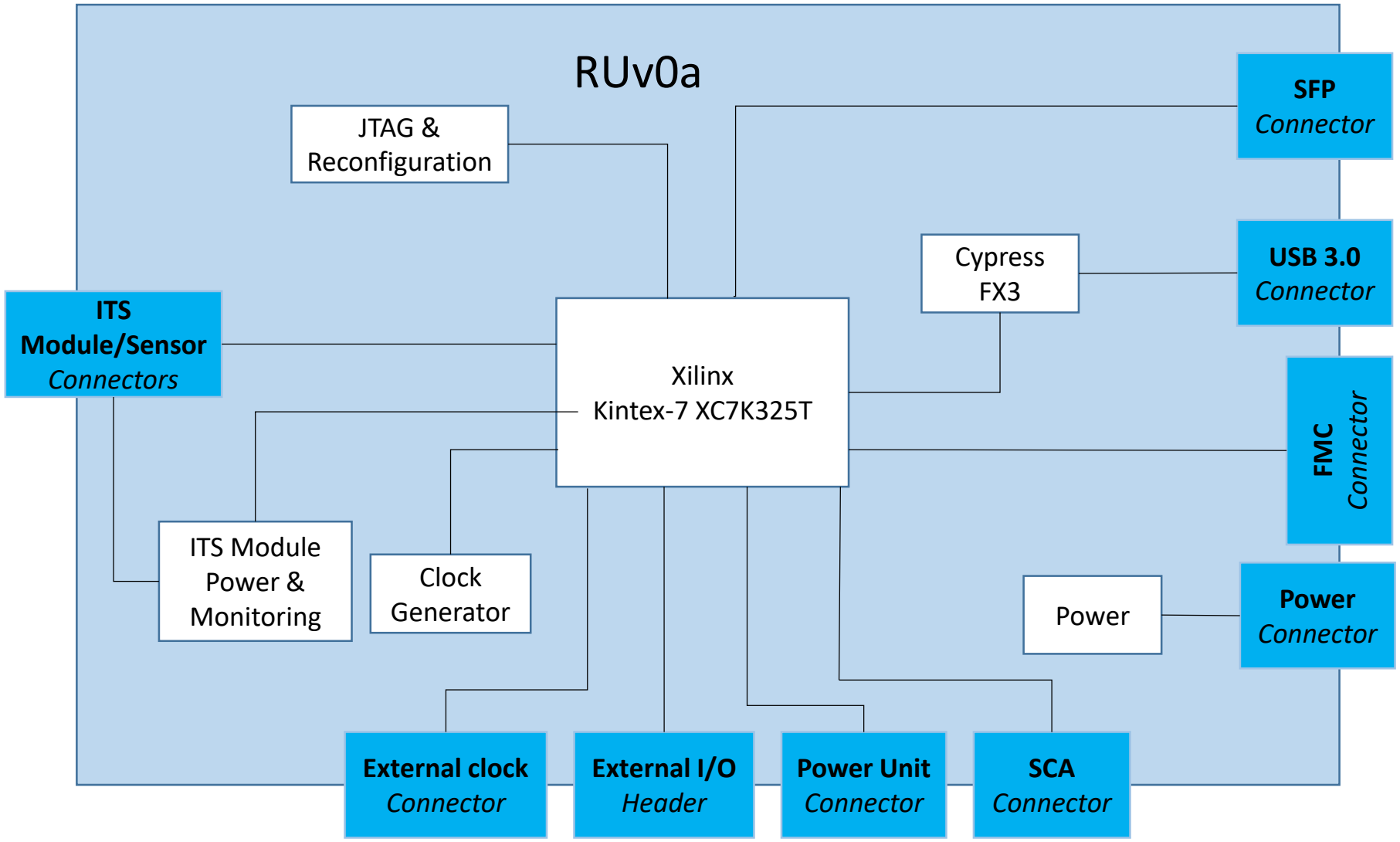
ITS Prototype Readout Platform Architecture



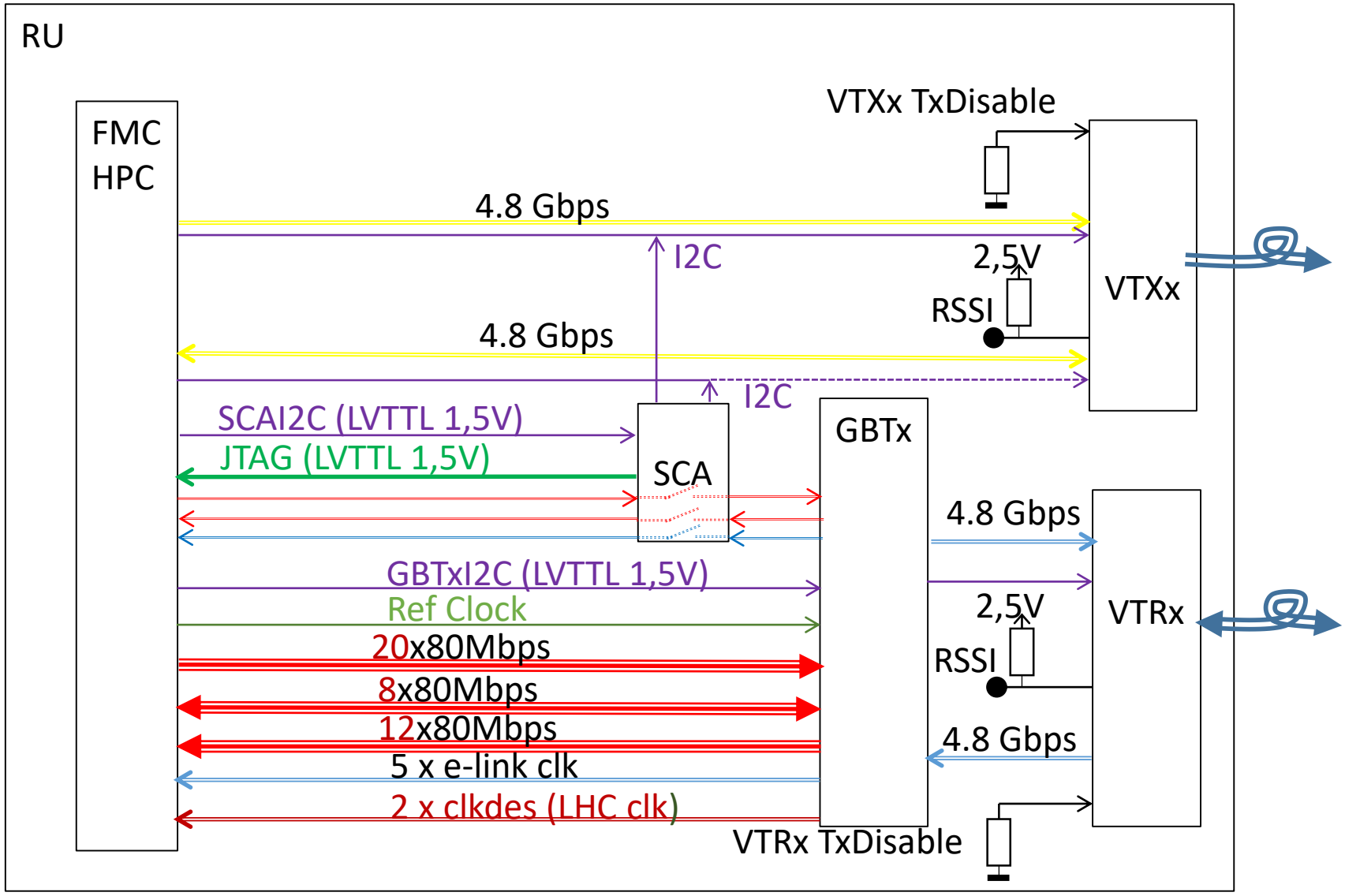
RU Prototype Motivations

- Test various connection schemes to ITS Sensors/Modules
- Provide readout for modules and sensors during production and testing
- Test interface FPGA-GBTx (with and without SLVS translators)
- Test FPGA implementation of GBT protocol
- Test various clocking schemes including clocks recovered by GBTx
- Provide interface to/from current PowerBoard prototype
- Test PowerBoard SCA interface
- Provide easy readout and control to/from a PC via USB
- Test FPGA architecture as a possible candidate for final RU
- Test interface to CRU
- Test various radiation effect mitigation techniques

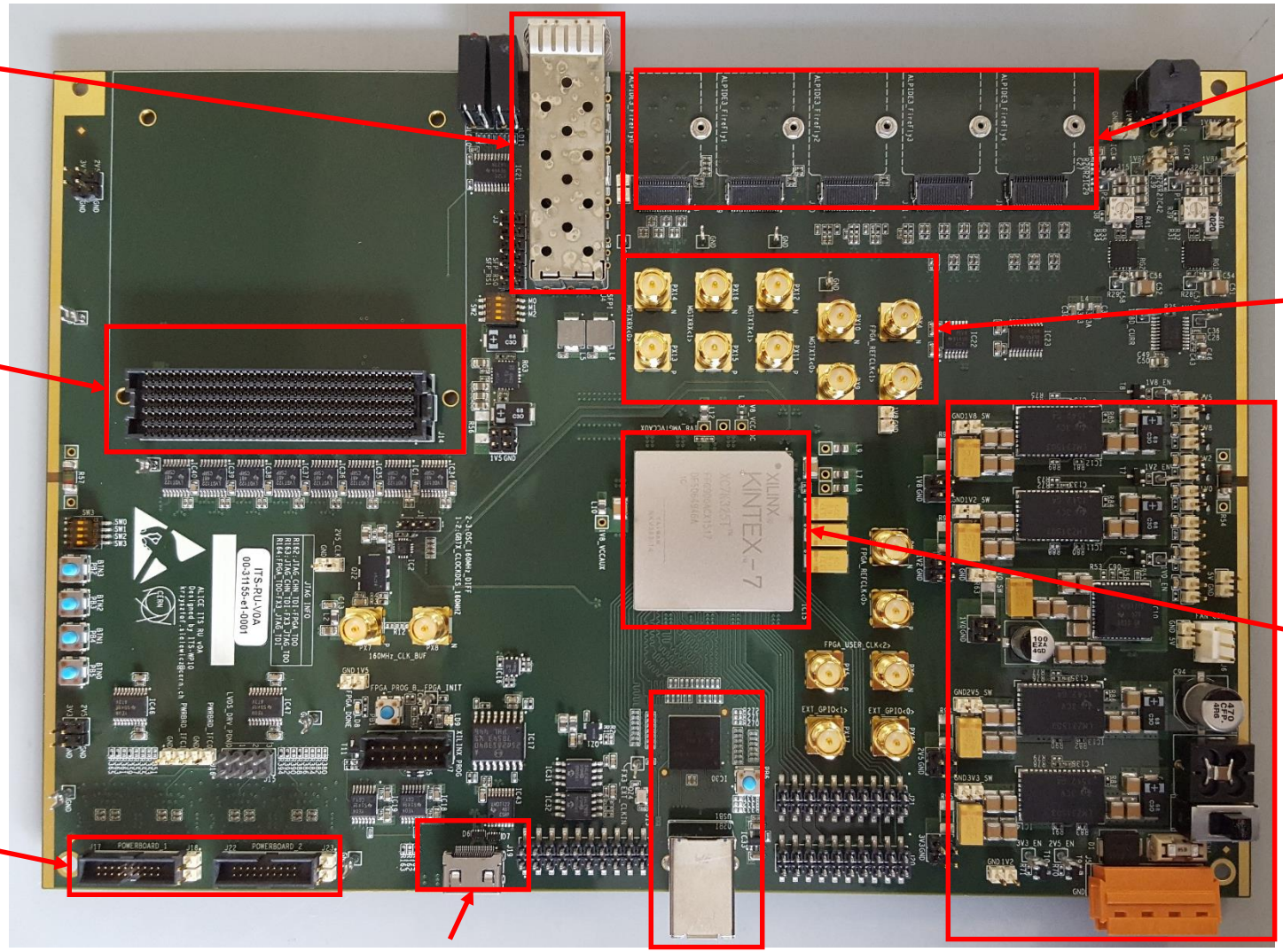
Prototype Readout Board “RUv0a”



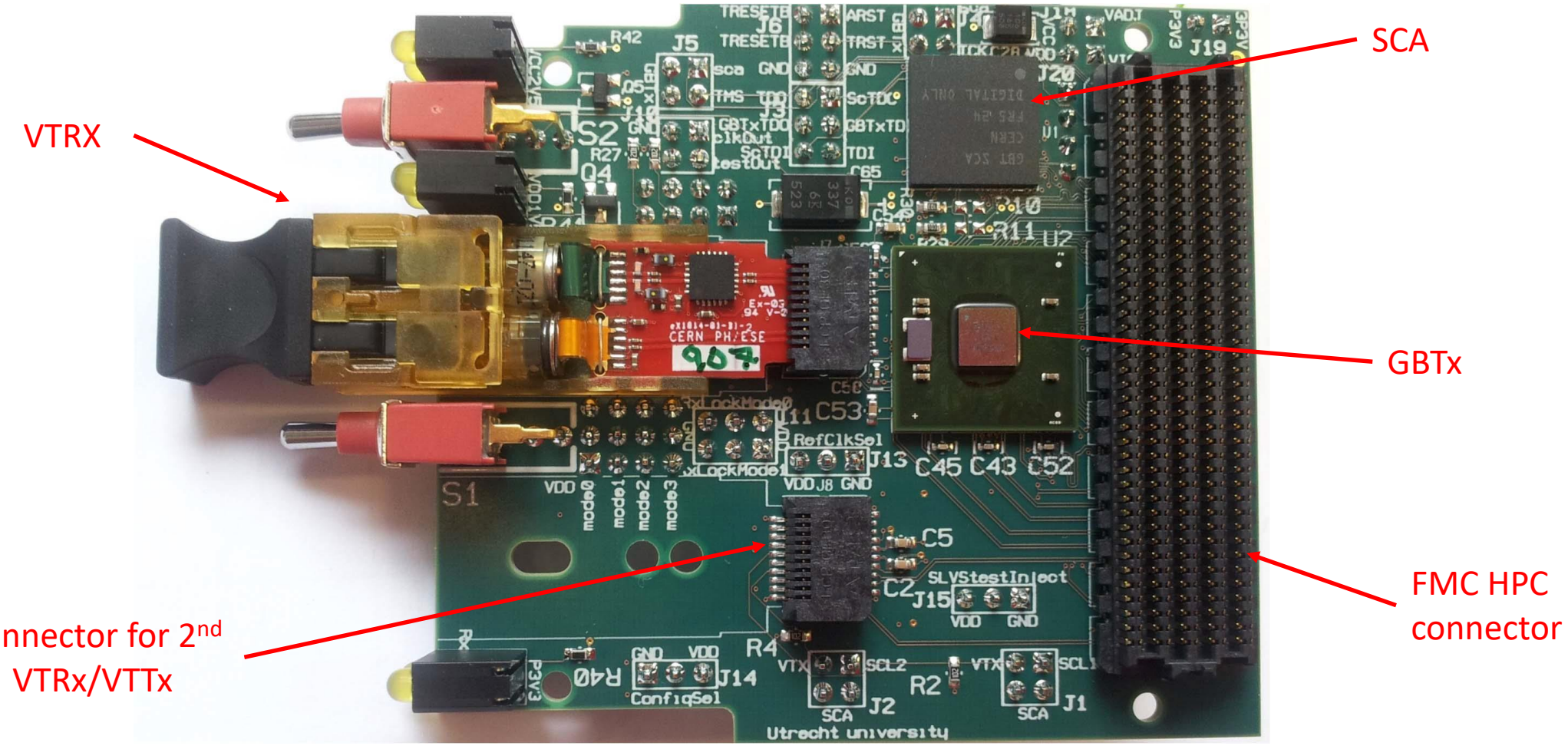
GBT FMC Mezzanine card



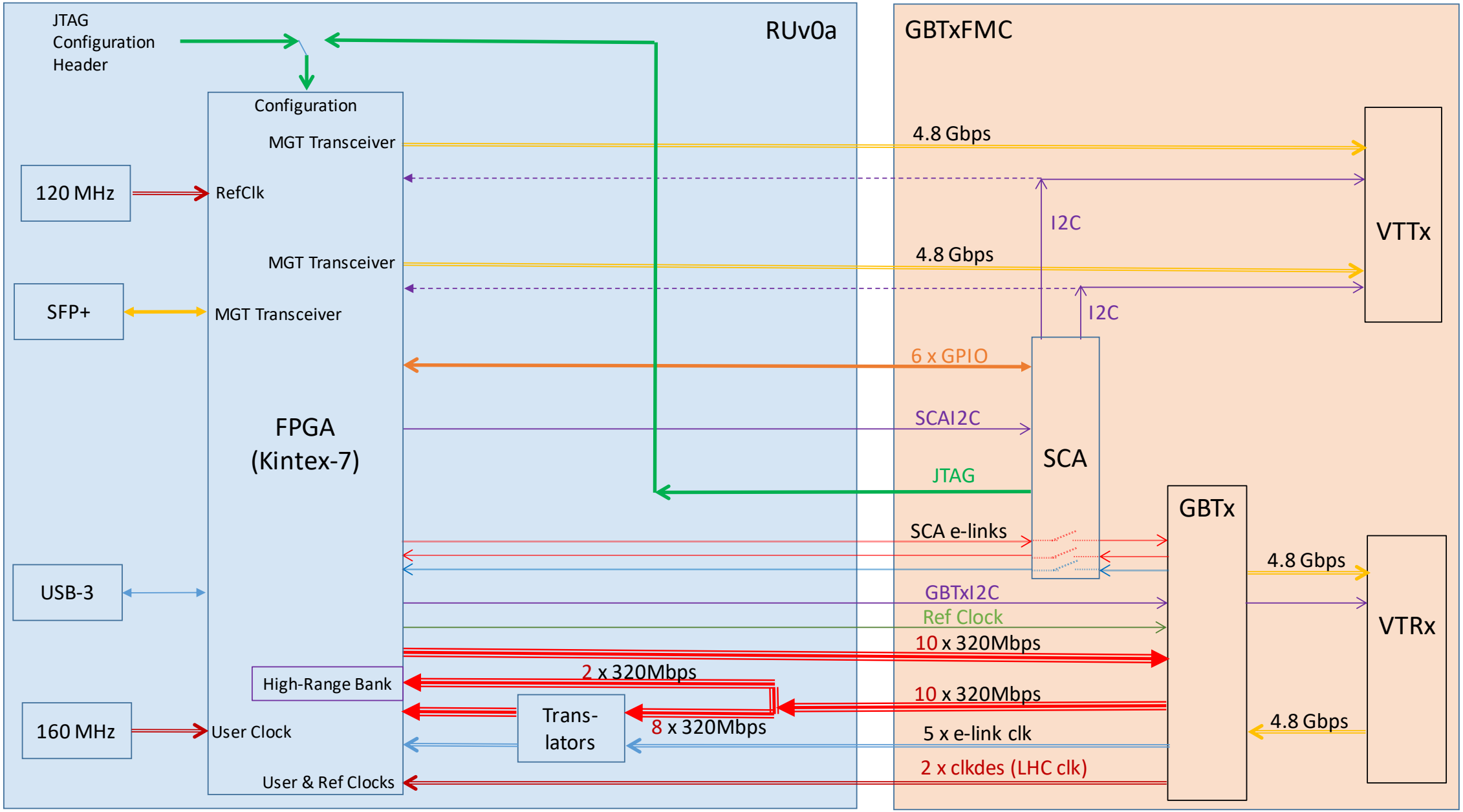
Readout Unit Prototype Version 0a (“RUv0a”)



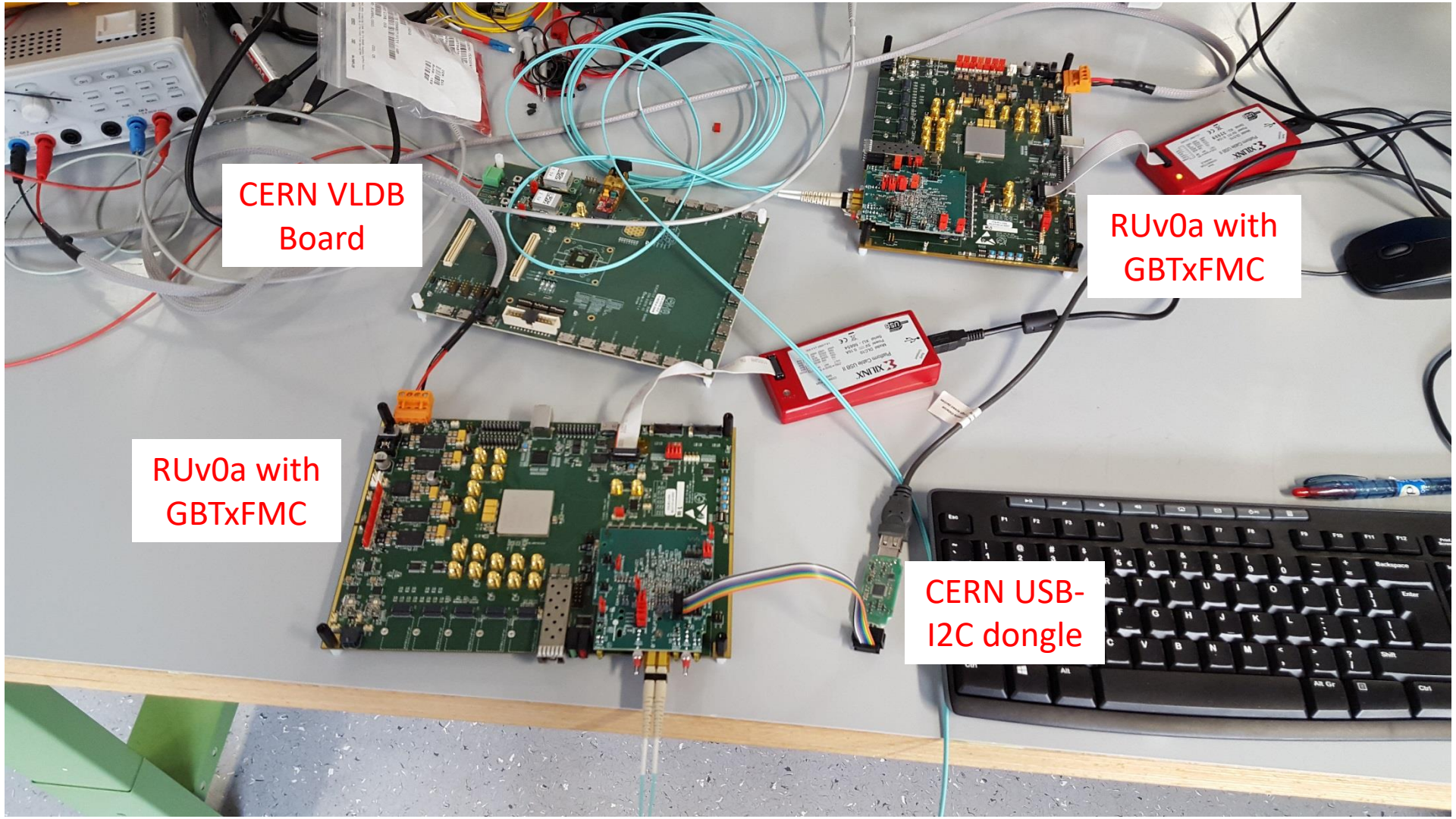
GBT FMC Mezzanine (“GBTxFMC”)



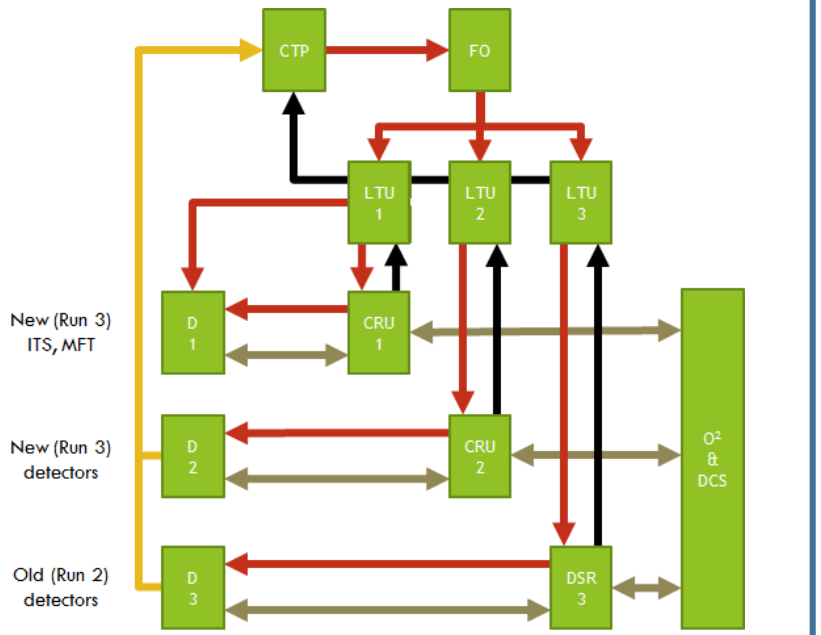
GBT Test Setup



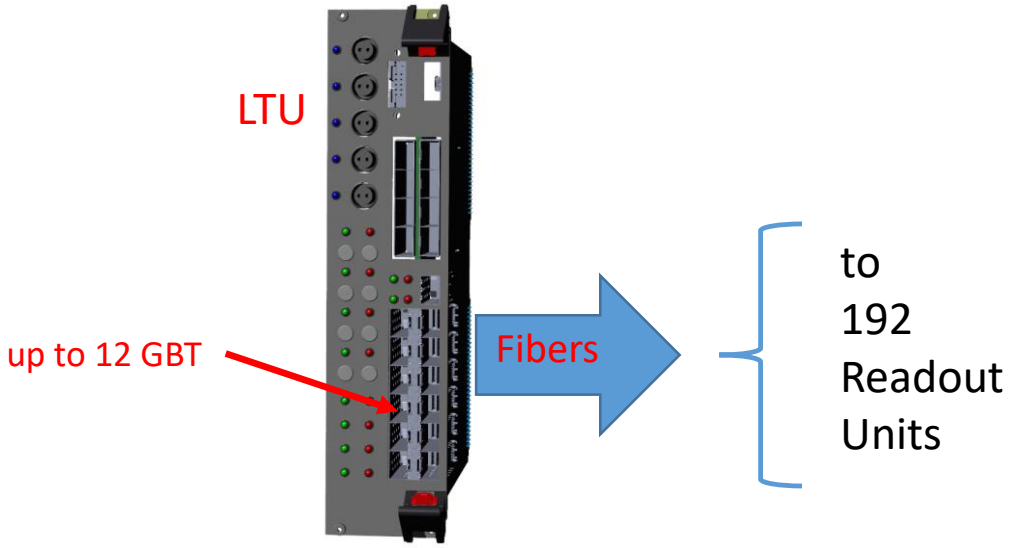
Test Setup


CERN VLDB Board
RUv0a with GBTxFMC
RUv0a with GBTxFMC
CERN USB-I2C dongle

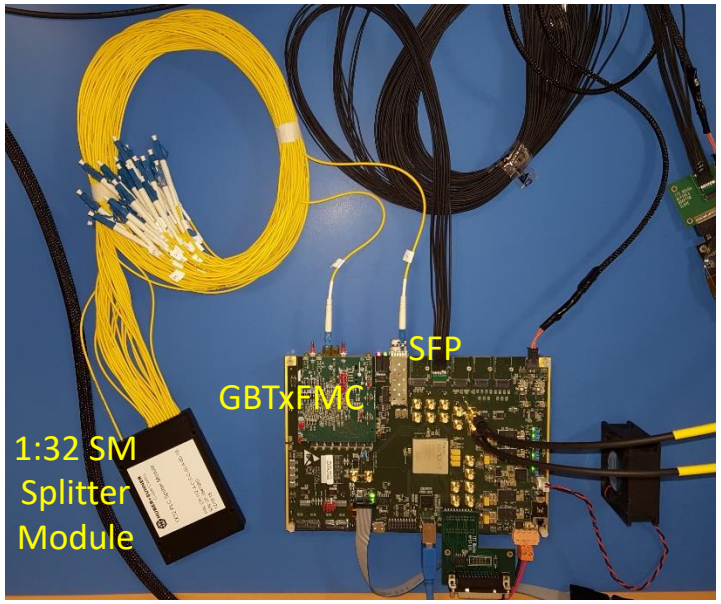
Trigger Distribution Tests



Trigger Distribution System Block Diagram



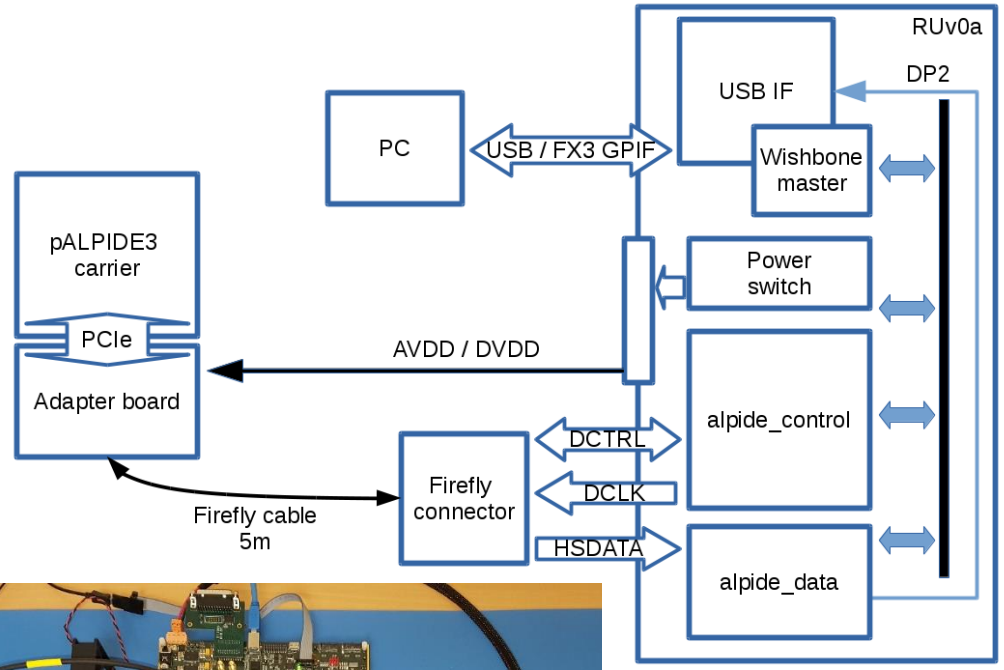
- Trigger received by GBT system via VTRx receiver and GBTx ASIC
- Need passive optical splitting from about LTU outputs to 192 RUs
- Ideally can split 1:32, then we would need 6 fiber outputs from LTU

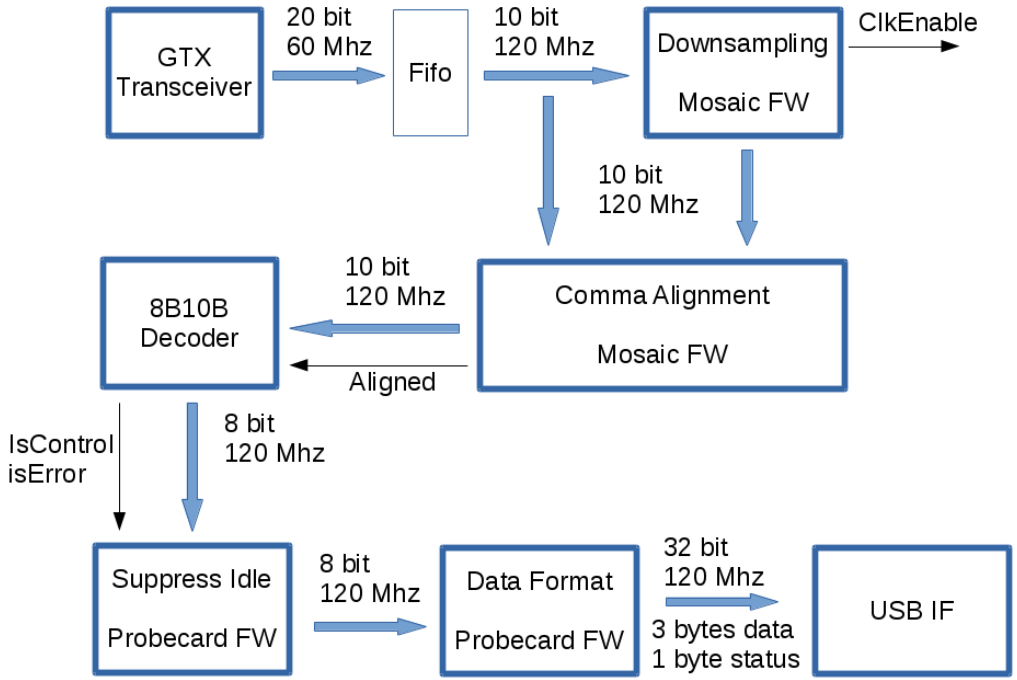


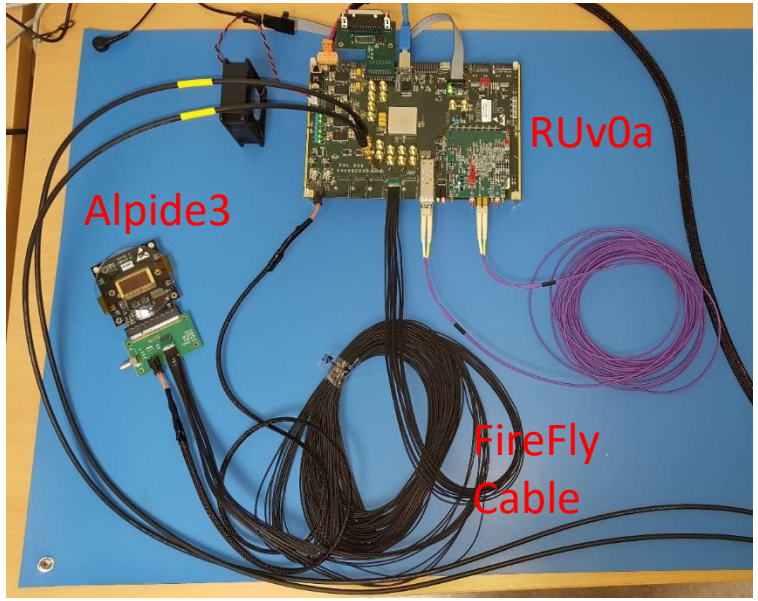
Test Setup

- Use RUv0a SFP as Tx and RUv0a GBTxFMC as Rx
- Firmware same as currently used for GBTx tests
- Need single-mode fiber equipment (including single-mode VTRx)
- Initial tests started, to be continued in Bergen

Alpide Readout

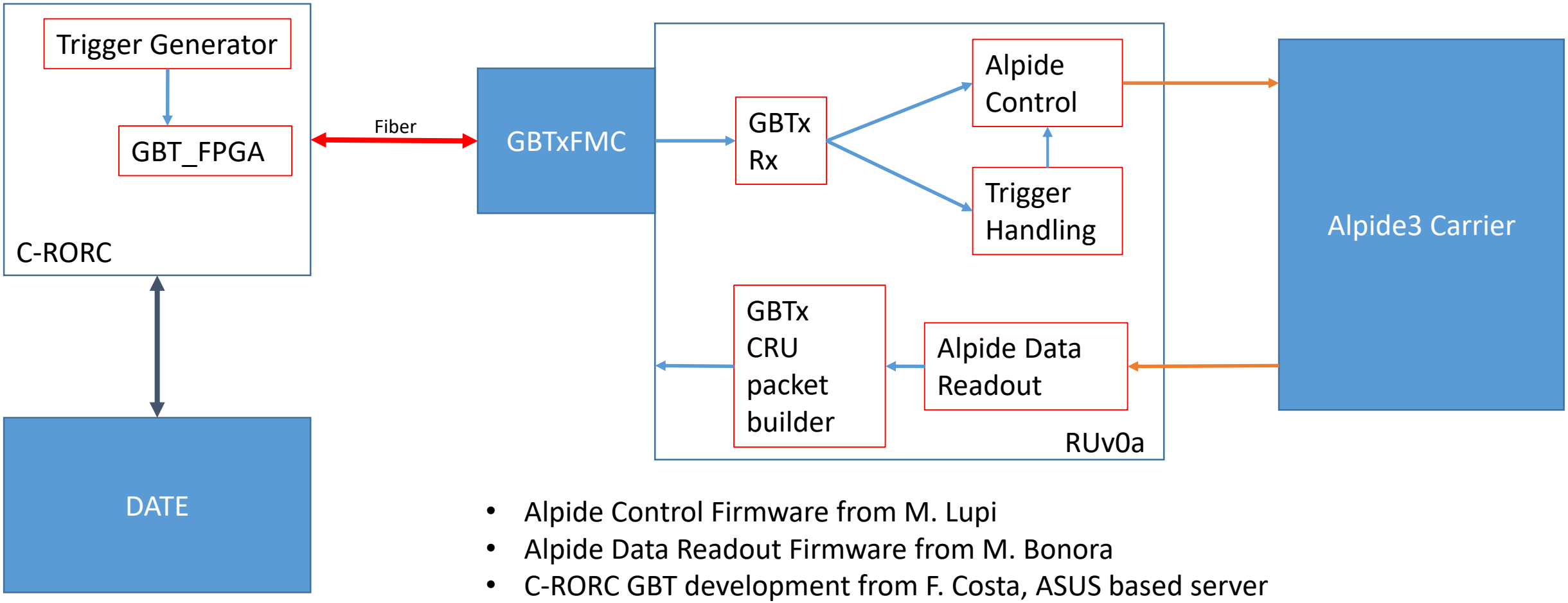






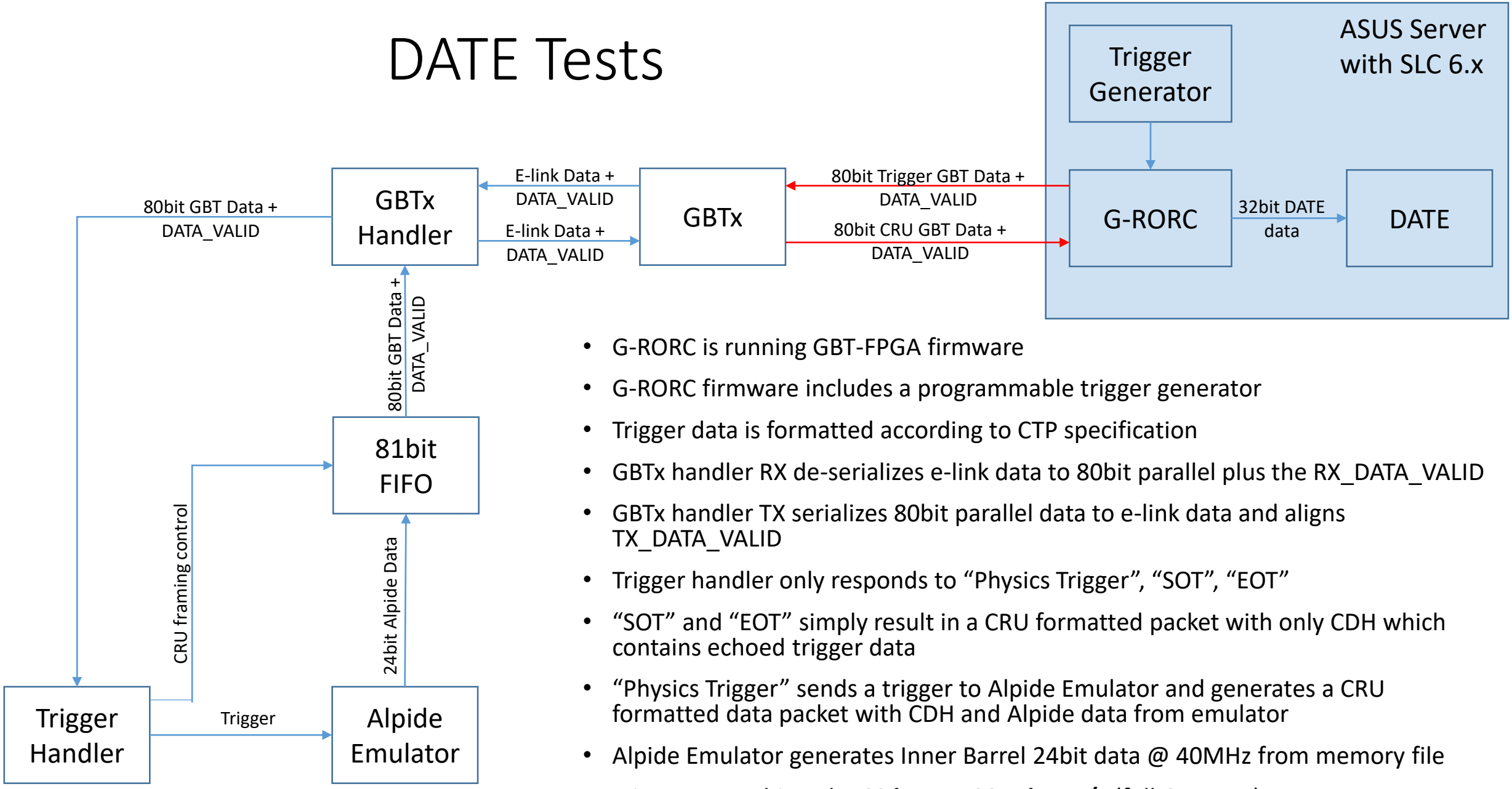
- Ported to setup in Austin, some issues debugged
- Control r/w stable, no problems
- Some issues with transceiver initialization, needs explicit reset
- Alpide high-speed readout at 1.2Gb/s (IB) & 0.4Gb/s (OB)
- Firmware tagged & distributed, about to be merged with main RUv0a firmware
- Implementation on IGLOO-2 started (Bergen)

Full Readout Chain



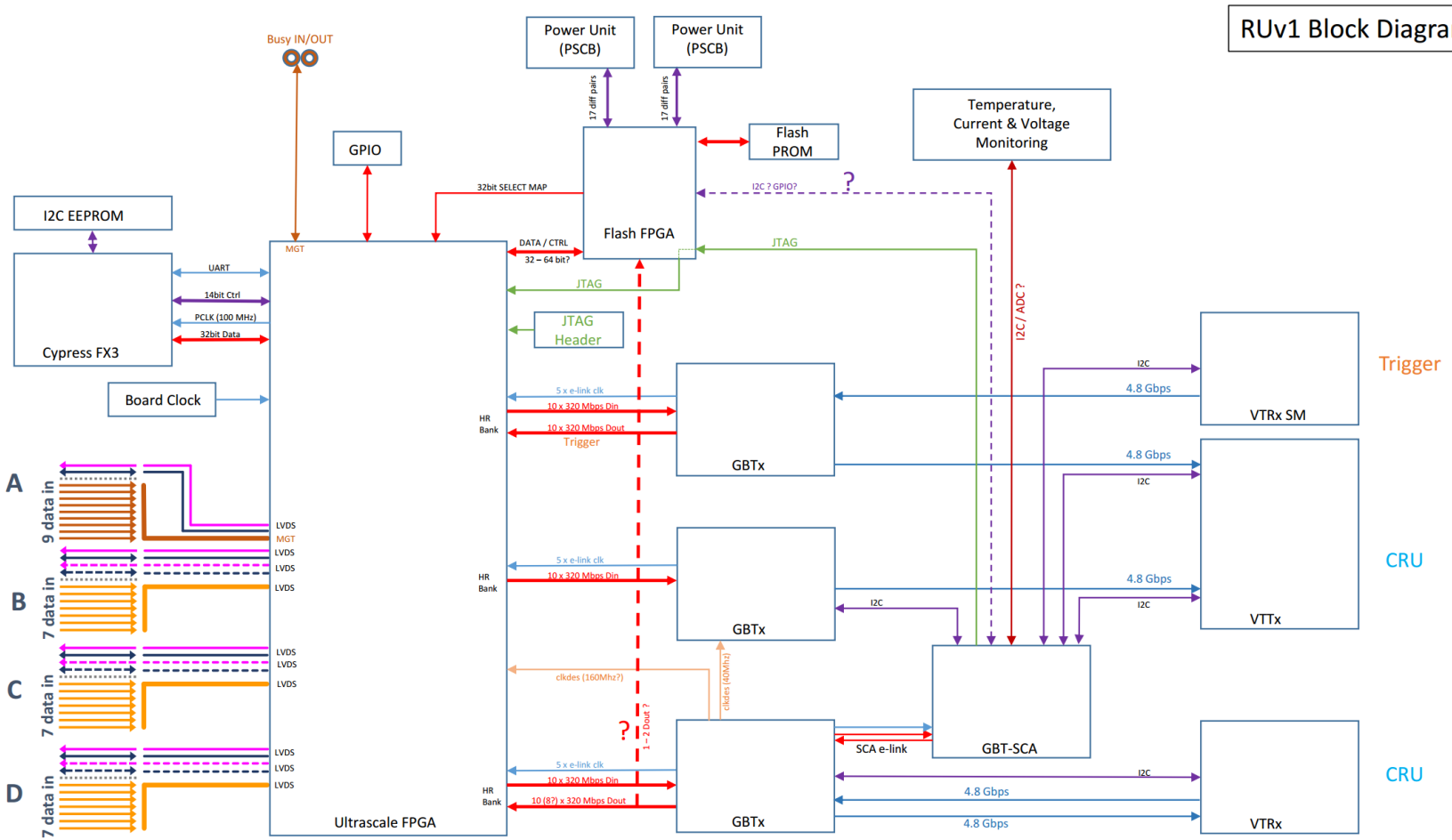
- Alpide Control Firmware from M. Lupi
- Alpide Data Readout Firmware from M. Bonora
- C-RORC GBT development from F. Costa, ASUS based server
- DATE software from DAQ group
- GBTx firmware from GBT tests (JS)

DATE Tests



- G-RORC is running GBT-FPGA firmware
- G-RORC firmware includes a programmable trigger generator
- Trigger data is formatted according to CTP specification
- GBTx handler RX de-serializes e-link data to 80bit parallel plus the RX_DATA_VALID
- GBTx handler TX serializes 80bit parallel data to e-link data and aligns TX_DATA_VALID
- Trigger handler only responds to “Physics Trigger”, “SOT”, “EOT”
- “SOT” and “EOT” simply result in a CRU formatted packet with only CDH which contains echoed trigger data
- “Physics Trigger” sends a trigger to Alpide Emulator and generates a CRU formatted data packet with CDH and Alpide data from emulator
- Alpide Emulator generates Inner Barrel 24bit data @ 40MHz from memory file
- Trigger rate achieved: **~60 kHz**, **~420 Mbytes/s** (full GBT rate)

RUv1 development: early block diagram concept



- SRAM based FPGA (Kintex 7 or Ultra Scale) with FLASH based small FPGA for scrubbing.
- On board FLASH for firmware storage & scrubbing
- Full set of GBT connections:
  - 3 GBTx chips
  - 2 VTRx
  - 1 VTTx
  - not necessary to mount them all on all the boards).
- Control of the Power Unit passes through the FLASH FPGA.
- Both FPGA in JTAG chain controlled by the SCA chip (rad-hard).

Prototype hardware for CRU emulation

- Arria 10 GX FPGA Development Kit from Altera (~$4.5k)
- Prototype Firmware from CRU group