Below are the technical specifications of the 84 staves and 60 Readout Units that will be provided by the ALICE experiment at CERN.

Ming please provide a Short description of the staves, role etc…(similar to the one for the readout units below)

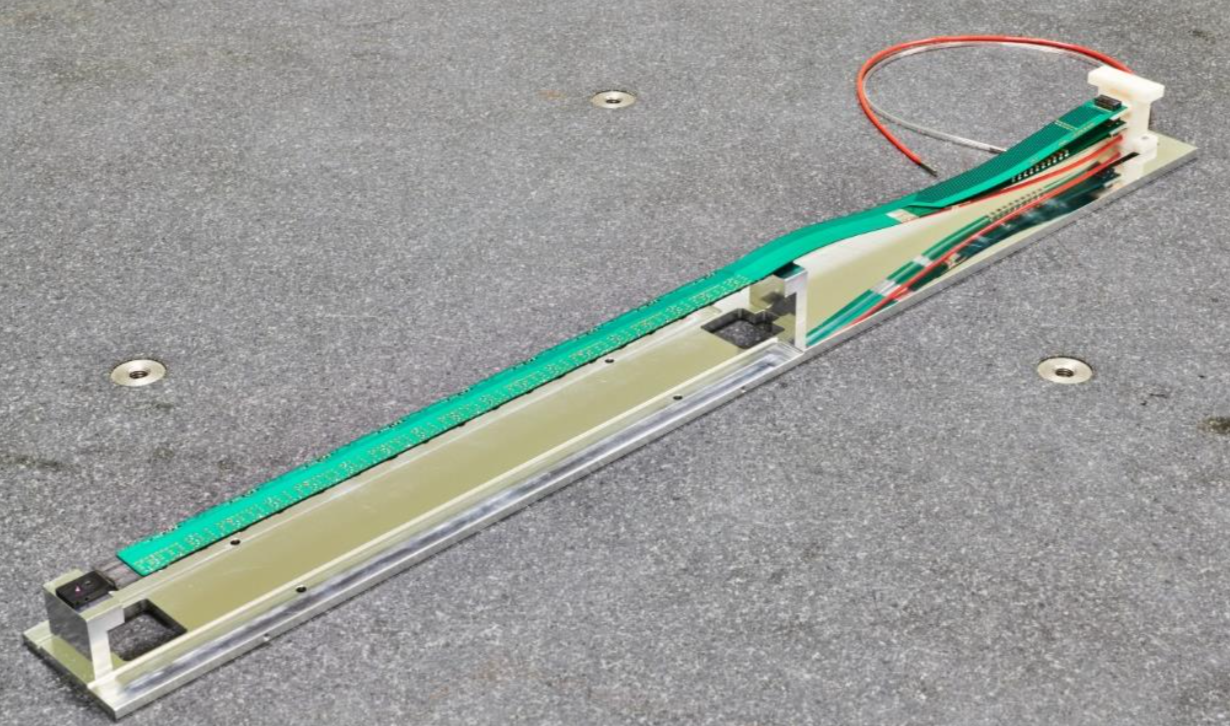


Figure 1. ALICE IB stave.

A stave is the basic element of the sPHENIX MVTX detector system, providing high precision spatial position measurements of charged particles traverse through the MAPS sensor layer. Each stave consists of the following items:

* 9 ALPIDE chips (silicon pixel sensors)
* One Flexible Printed Circuit (FPC), (to make a Hybrid Integrated Circuit/HIC with 9 sensors)
* Two FPC power extensions and connecters (for signal, analogy and digital power and also cooling)
* One carbone space frame (for mechanical support and also cooling)

An illustration of the staves is in Figure 1, with extended FPC power cables modified for sPHENIX:

The readout of the MVTX is comported of a FPGA-based Printed Circuit Boards called Readout Units. They control and read out the data from the detector, manage the local power distribution system and ensure connection with the counting room. Due to the sensors’ constrained power budget, which limits their data line driving capability, the readout electronics will be installed as closed as possible to the detector, in a radiation environment. The board will also operate in a magnetic field of 1.5 T.

Each Readout Board provided by CERN will consist of:

* 1 Xilinx FPGA part number XCKU060-1FFVA1156C (main programmable logic device).
* 1 Microsemi FPGA part number A3PE600L-FGG484M FP (auxilliary programmable logic device).
* 3 CERN custom made GBTx chips (transceivers for the connection to the counting house).
* 1 CERN custom made SCA chip (monitoring device).
* 3 SFP+ pod connectors (fiber optic connections).
* 2 ERF8-050-05.0-L-DV-TR Samtec connectors (sensor interface).
* Miniaturized passive components.
* VME J1 connector.

An illustration of the Readout Unit board is shown in Figure 2

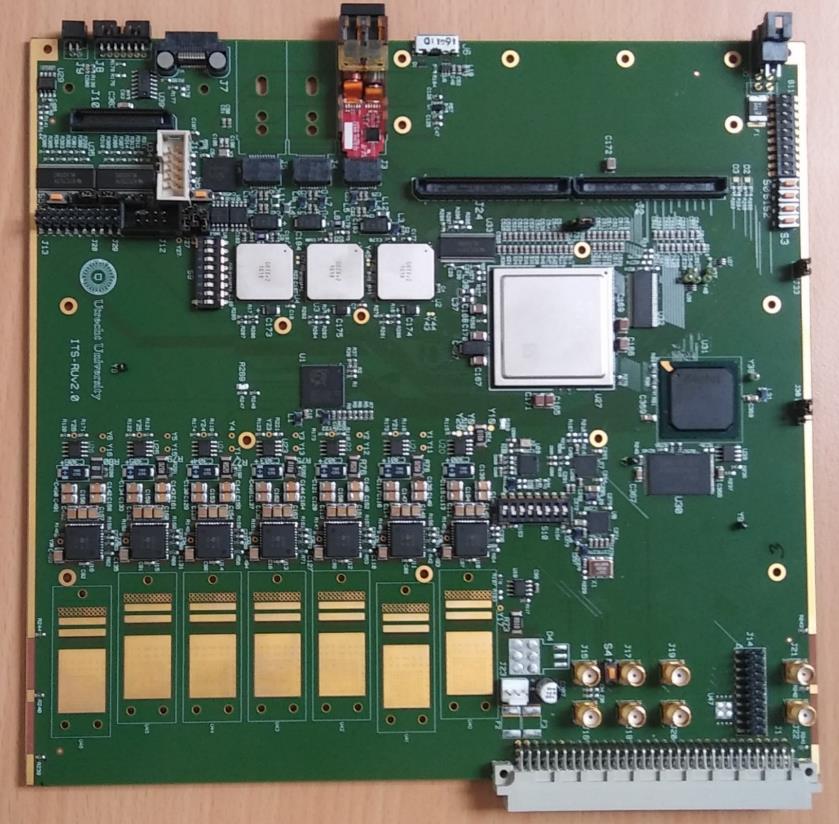


Figure 2: Readout Unit Board

The most complex components found on the board, and provided by CERN, are listed below.

* 1 Xilinx FPGA part number XCKU060-1FFVA1156C (main programmable logic device).
* 1 Microsemi FPGA part number A3PE600L-FGG484M FP (auxilliary programmable logic device).
* 3 CERN custom made GBTx chips (transceivers for the connection to the counting house).
* 1 CERN custom made SCA chip (monitoring device).
* 3 SFP+ pod connectors (fiber optic connections).
* 2 ERF8-050-05.0-L-DV-TR Samtec connectors (sensor interface).
* Miniaturized passive components.
* VME J1 connector.

The power mezzanine is attached to this main board via a high-density connector and provides the fan-out of the signals to the power board. It will be produced by UTA and it contains mainly the various connectors to connect to the Readout Unit on one side, and two ribbon cables on the other side. In addition, this board contains LEDs to indicate the status of the various logic in the Readout Unit. An illustration of the Power Mezzanine card is shown in Figure 2:



Figure 2: Power Mezzanine

The main components of the power mezzanine are:

* 1 Samtec shrouded terminal part number SHF-110-01-L-D-RA
* 2 Samtec edge rate terminal assemblies part number ERM8-030-02.0-L-DV
* 6 LED 0402 SMD, part number APG1005VGC-T-5MAV

The RU will be tested by Nikhef or UTA ???