

1 FELIX register map, version 3.4

Starting from the offset address of BAR0, BAR1 and BAR2, the register map for BAR0 expands from 0x0000 to 0x0430 for the PCIe control registers. BAR0 only contains registers associated with DMA. The offset for BAR0 is usually 0xFBB00000.

Address	PCIe	Name/Field	Bits	Type	Description
Bar0					
DMA_DESC					
0x0000	0,1	DMA_DESC_0			
		END_ADDRESS	127:64	W	End Address
		START_ADDRESS	63:0	W	Start Address
0x0010	0,1	DMA_DESC_0a			
		RD_POINTER	127:64	W	PC Read Pointer
		WRAP_AROUND	12	W	Wrap around
		READ_WRITE	11	W	1: fromHost/ 0: toHost
		NUM_WORDS	10:0	W	Number of 32 bit words
...					
0x00E0	0,1	DMA_DESC_7			
		END_ADDRESS	127:64	W	End Address
		START_ADDRESS	63:0	W	Start Address
0x00F0	0,1	DMA_DESC_7a			
		RD_POINTER	127:64	W	PC Read Pointer
		WRAP_AROUND	12	W	Wrap around
		READ_WRITE	11	W	1: fromHost/ 0: toHost
		NUM_WORDS	10:0	W	Number of 32 bit words
DMA_DESC_STATUS					
0x0200	0,1	DMA_DESC_STATUS_0			
		EVEN_PC	66	R	Even address cycle PC
		EVEN_DMA	65	R	Even address cycle DMA
		DESC_DONE	64	R	Descriptor Done
		CURRENT_ADDRESS	63:0	R	Current Address
...					
0x0270	0,1	DMA_DESC_STATUS_7			
		EVEN_PC	66	R	Even address cycle PC
		EVEN_DMA	65	R	Even address cycle DMA
		DESC_DONE	64	R	Descriptor Done
		CURRENT_ADDRESS	63:0	R	Current Address
0x0300	0,1	BAR0_VALUE	31:0	R	Copy of BAR0 offset reg.
0x0310	0,1	BAR1_VALUE	31:0	R	Copy of BAR1 offset reg.
0x0320	0,1	BAR2_VALUE	31:0	R	Copy of BAR2 offset reg.
0x0400	0,1	DMA_DESC_ENABLE	7:0	W	Enable descriptors 7:0. One bit per descriptor. Cleared when Descriptor is handled.
0x0410	0,1	DMA_FIFO_FLUSH	any	T	Flush (reset). Any write clears the DMA Main output FIFO
0x0420	0,1	DMA_RESET	any	T	Reset Wupper Core (DMA Controller FSMs)

Address	PCIe	Name/Field		Bits	Type	Description
0x0430	0,1	SOFT_RESET		any	T	Global Software Reset. Any write resets applications, e.g. the Central Router.
0x0440	0,1	REGISTER_RESET		any	T	Resets the register map to default values. Any write triggers this reset.
0x0450	0,1	FROMHOST_FULL_THRESH				
			THRESHOLD_ASSERT	22:16	W	Assert value of the FromHost programmable full flag
			THRESHOLD_NEGATE	6:0	W	Negate value of the FromHost programmable full flag
0x0460	0,1	TOHOST_FULL_THRESH				
			THRESHOLD_ASSERT	27:16	W	Assert value of the ToHost programmable full flag
			THRESHOLD_NEGATE	11:0	W	Negate value of the ToHost programmable full flag

Table 1: FELIX register map BAR0

BAR1 stores registers associated with the Interrupt vector. The offset for BAR1 is usually 0xFBA00000.

Address	PCIe	Name/Field		Bits	Type	Description
Bar1						
INT_VEC						
0x0000	0,1	INT_VEC_0				
			INT_CTRL	127:96	W	Interrupt Control
			INT_DATA	95:64	W	Interrupt Data
			INT_ADDRESS	64:0	W	Interrupt Address
...						
0x0070	0,1	INT_VEC_7				
			INT_CTRL	127:96	W	Interrupt Control
			INT_DATA	95:64	W	Interrupt Data
			INT_ADDRESS	64:0	W	Interrupt Address
0x0100	0,1	INT_TAB_ENABLE		7:0	W	Interrupt Table enable Selectively enable Interrupts

Table 2: FELIX register map BAR1

BAR2 stores registers for the control and monitor of HDL modules inside the FPGA other than Wupper. A portion of this register map's section is dedicated for control and monitor of devices outside the FPGA; as for example simple SPI and I2C devices. The offset for BAR2 is usually 0xFB900000.

Address	PCIe	Name/Field	Bits	Type	Description
Bar2					
Generic Board Information					
0x0000	0	REG_MAP_VERSION	15:0	R	Register Map Version, 3.4 formatted as 0x0304
0x0010	0	BOARD_ID_TIMESTAMP	39:0	R	Board ID Date / Time in BCD format YYMMDDhhmm
0x0020	0	BOARD_ID_SVN	15:0	R	Board ID SVN Revision
0x0030	0	STATUS_LEDS	7:0	W	Board GPIO Leds
0x0040	0	GENERIC_CONSTANTS			
		INTERRUPTS	15:8	R	Number of Interrupts
		DESCRIPTORS	7:0	R	Number of Descriptors
0x0050	0	NUM_OF_CHANNELS	7:0	R	Number of GBT Channels
0x0060	0	CARD_TYPE	63:0	R	Card Type: - 709 (0x2c5): VC709 - 710 (0x2c6): HTG710 - 711 (0x2c7): BNL711
0x0070	0	GBT_MAPPING	7:0	R	CXP-to-GBT mapping: 0: NORMAL CXP1 1-12 CXP2 13-24 1: ALTERNATE CXP1 1-4,9-12,17-20

Address	PCIe	Name/Field	Bits	Type	Description
0x0080	0	GENERATE_GBT	0	R	1 when the GBT Wrapper is included in the design
0x0090	0	OPTO_TRX_NUM	7:0	R	Number of optical transceivers in the design
0x00A0	0	TTC.EMU.CONST			
		GENERATE_TTC_EMU	1	R	1 when TTC emulator is generated
		TTC_TEST_MODE	0	R	1 when TTC Test mode is enabled
0x00B0	0	CR_INTERNAL_LOOPBACK_MODE	0	R	1 when Central Router internal loopback mode is enabled
0x00C0	0	INCLUDE_EPROC16			
		FRHOEPROC2	7	R	FromHost EPROC2 is included in Central Router
		FRHOEPROC4	6	R	FromHost EPROC4 is included in Central Router
		FRHOEPROC8	5	R	FromHost EPROC8 is included in Central Router
		FRHOEPROC16	4	R	FromHost EPROC16 is included in Central Router
		TOHOEPROC2	3	R	ToHost EPROC2 is included in Central Router
		TOHOEPROC4	2	R	ToHost EPROC4 is included in Central Router
		TOHOEPROC8	1	R	ToHost EPROC8 is included in Central Router
		TOHOEPROC16	0	R	ToHost EPROC16 is included in Central Router
0x00D0	0	WIDE_MODE	0	R	GBT is configured in Wide mode
0x00E0	0	DEBUG_MODE	0	R	0: SMA X3 is constant 0, SMA X4 is connected to clk40 (output). 1: Debug port module (SMA X3 and SMA X4) can be controlled using DEBUG_PORT_GBT and DEBUG_PORT_CLK
0x00F0	0	FIRMWARE_MODE	0	R	0: GBT mode 1: FULL mode
Central Router Controls					
0x1000	0,1	CR_TH_UPDATE_CTRL	any	T	See Central Router Doc
0x1010	0,1	CR_FH_UPDATE_CTRL	any	T	See Central Router Doc

Address	PCIe	Name/Field		Bits	Type	Description	
0x1020	0,1	FH_IC_PACKET_RDY			23:0	W	Rising edge indicates the complete packet can be read
0x1030	0,1	TIMEOUT_CTRL					
			ENABLE	32	W	1 enables the timeout trailer generation for ToHost mode	
			TIMEOUT	31:0	W	Number of 40 MHz clock cycles after which a timeout occurs.	
CR_GBT_CTRL							
EGROUP_TH							
0x1100	0,1	CR_TH_GBT00_EGROUP0_CTRL			63:0	W	See Central Router Doc, indices [5,6] are optimized out in wideMode
...							
0x1160	0,1	CR_TH_GBT00_EGROUP6_CTRL			63:0	W	See Central Router Doc, indices [5,6] are optimized out in wideMode
EGROUP_FH							
0x1170	0,1	CR_FH_GBT00_EGROUP0_CTRL			63:0	W	See Central Router Doc, indices [3,4] are optimized out in wideMode
...							
0x11B0	0,1	CR_FH_GBT00_EGROUP4_CTRL			63:0	W	See Central Router Doc, indices [3,4] are optimized out in wideMode
...							
EGROUP_TH							
0x2240	0,1	CR_TH_GBT23_EGROUP0_CTRL			63:0	W	See Central Router Doc, indices [5,6] are optimized out in wideMode
...							
0x22A0	0,1	CR_TH_GBT23_EGROUP6_CTRL			63:0	W	See Central Router Doc, indices [5,6] are optimized out in wideMode
EGROUP_FH							
0x22B0	0,1	CR_FH_GBT23_EGROUP0_CTRL			63:0	W	See Central Router Doc, indices [3,4] are optimized out in wideMode
...							
0x22F0	0,1	CR_FH_GBT23_EGROUP4_CTRL			63:0	W	See Central Router Doc, indices [3,4] are optimized out in wideMode
IC_FIFOS							
0x2400	0,1	FH_IC_FIFO_00					
			WE	any	T	Any write to this register will trigger a write to the FIFO	
			FULL	8	R	Full flag of the fifo, do not write if 1	
			DATAIN	7:0	W	Data input of fifo	
0x2410	0,1	TH_IC_FIFO_00					

Address	PCIe	Name/Field	Bits	Type	Description
		RE	any	T	Any write to this register will trigger a read enable from the fifo
		EMPTY	8	R	Empty flag of the fifo, do not read if 1
		DATAOUT	7:0	R	Data output of fifo
...					
0x26E0	0,1	FH_IC_FIFO_23			
		WE	any	T	Any write to this register will trigger a write to the FIFO
		FULL	8	R	Full flag of the fifo, do not write if 1
		DATAIN	7:0	W	Data input of fifo
0x26F0	0,1	TH_IC_FIFO_23			
		RE	any	T	Any write to this register will trigger a read enable from the fifo
		EMPTY	8	R	Empty flag of the fifo, do not read if 1
		DATAOUT	7:0	R	Data output of fifo
MINI_EGROUP_CTRL					
0x2700	0,1	EC_TOHOST_00			
		BIT_SWAPPING	3	W	0: two input bits of EC e-link are as documented, 1: two input bits are swapped
		ENCODING	2:1	W	Configures encoding of the EC channel
		ENABLE	0	W	Enables the EC channel
0x2710	0,1	EC_FROMHOST_00			
		BIT_SWAPPING	5	W	0: two output bits of EC e-link are as documented, 1: two output bits are swapped
		ENCODING	4:1	W	Configures encoding of the EC channel
		ENABLE	0	W	Configures the FromHost Mini egroup in EC mode
0x2720	0,1	TTC_TOHOST_00	0	W	Enables the ToHost Mini Egroup in TTC mode
...					
0x2B50	0,1	EC_TOHOST_23			
		BIT_SWAPPING	3	W	0: two input bits of EC e-link are as documented, 1: two input bits are swapped
		ENCODING	2:1	W	Configures encoding of the EC channel
		ENABLE	0	W	Enables the EC channel
0x2B60	0,1	EC_FROMHOST_23			

Address	PCIe	Name/Field	Bits	Type	Description
		BIT_SWAPPING	5	W	0: two output bits of EC e-link are as documented, 1: two output bits are swapped
		ENCODING	4:1	W	Configures encoding of the EC channel
		ENABLE	0	W	Configures the FromHost Mini egroup in EC mode
0x2B70	0,1	TTC_TOHOST_23	0	W	Enables the ToHost Mini Egroup in TTC mode
TTC_FANOUT_CTRL					
0x2B80	0,1	TTC_DELAY_00	3:0	W	Configures the FromHost TTC pipeline in the fanout selector
...					
0x2CF0	0,1	TTC_DELAY_23	3:0	W	Configures the FromHost TTC pipeline in the fanout selector
0x2D00	0,1	TTC_BUSY_TIMING_CTRL			
		PRESCALE	51:32	W	Prescales the 40MHz clock to create an internal slow clock
		BUSY_WIDTH	31:16	W	Minimum number of 40MHz clocks that the busy is asserted
		LIMIT_TIME	15:0	W	Number of prescaled clocks a given busy must be asserted before it is recognized
0x2D10	0,1	CR_FALLBACK_OPTIONS	63:0	W	Julias personal register with Hello Kitty options
Central Router Monitors					
CR_GBT_MON					
0x3000	0	CR_TH_GBT00_MON	63:0	R	See Central Router Doc
0x3010	0	CR_FH_GBT00_MON	63:0	R	See Central Router Doc
...					
0x32E0	0	CR_TH_GBT23_MON	63:0	R	See Central Router Doc
0x32F0	0	CR_FH_GBT23_MON	63:0	R	See Central Router Doc
0x3300	0,1	CR_STATIC_CONFIGURATION	0	R	Central Router Monitors
0x3310	0,1	CR_DEFAULT_EPROC_ENA0	14:0	R	Central Router Monitors
0x3320	0,1	CR_DEFAULT_EPROC_ENA1	14:0	R	Central Router Monitors
0x3330	0,1	CR_DEFAULT_EPROC_ENA2	14:0	R	Central Router Monitors
0x3340	0,1	CR_DEFAULT_EPROC_ENA3	14:0	R	Central Router Monitors
0x3350	0,1	CR_DEFAULT_EPROC_ENA4	14:0	R	Central Router Monitors
0x3360	0,1	CR_DEFAULT_EPROC_ENA5	14:0	R	Central Router Monitors
0x3370	0,1	CR_DEFAULT_EPROC_ENA6	14:0	R	Central Router Monitors
0x3380	0,1	CR_DEFAULT_EPROC_ENA7	14:0	R	Central Router Monitors
0x3390	0,1	CR_DEFAULT_EPROC_ENCODING0	14:0	R	Central Router Monitors
0x33A0	0,1	CR_DEFAULT_EPROC_ENCODING1	14:0	R	Central Router Monitors
0x33B0	0,1	CR_DEFAULT_EPROC_ENCODING2	14:0	R	Central Router Monitors
0x33C0	0,1	CR_DEFAULT_EPROC_ENCODING3	14:0	R	Central Router Monitors

Address	PCIe	Name/Field	Bits	Type	Description
0x33D0	0,1	CR_DEFAULT_EPROC_ENCODING4	14:0	R	Central Router Monitors
0x33E0	0,1	CR_DEFAULT_EPROC_ENCODING5	14:0	R	Central Router Monitors
0x33F0	0,1	CR_DEFAULT_EPROC_ENCODING6	14:0	R	Central Router Monitors
0x3400	0,1	CR_DEFAULT_EPROC_ENCODING7	14:0	R	Central Router Monitors
GBT Emulator Controls And Monitors					
0x4000	0	GBT_EMU_ENA			
		TOFRONTEND	1	W	Enable GBT dummy emulator ToFrontEnd
		TOHOST	0	W	Enable GBT dummy emulator ToHost
0x4010	0	GBT_EMU_CONFIG_WE_ARRAY	6:0	W	write enable array, every bit is one emulator RAM block
0x4020	0	GBT_EMU_CONFIG			
		WRADDR	45:32	W	write address bus
		WRDATA	15:0	W	write data bus
0x4030	0	GBT_FM_EMU_ENA_TOHOST	0	W	Enable FULL mode dummy emulator ToHost
0x4040	0	GBT_FM_EMU_CONFIG_WE_ARRAY	6:0	W	write enable array, every bit is one emulator RAM block
0x4050	0	GBT_FM_EMU_CONFIG			
		WRADDR	53:40	W	write address bus
		WRDATA	35:0	W	write data bus
0x4060	0	CR_FM_PATH_ENA	11:0	W	FULL mode CR enable array, every bit is one path
GBT Wrapper Controls					
0x5400	0	GBT_LOGIC_RESET	63:0	W	Not internally connected (?)
0x5410	0	GBT_GENERAL_CTRL	63:0	W	Alignment chk reset (not self clearing)
0x5420	0	GBT_MODE_CTRL			
		RX_ALIGN_TB_SW	2	W	RX_ALIGN_TB_SW
		RX_ALIGN_SW	1	W	RX_ALIGN_SW
		DESMUX_USE_SW	0	W	DESMUX_USE_SW
0x5480	0	GBT_RXSLIDE			
		S2312	59:48	W	RxSlide select [23:12]
		S1100	43:32	W	RxSlide select [11:0]
		M2312	27:16	W	RxSlide manual [23:12]
		M1100	11:0	W	RxSlide manual [11:0]
0x5490	0	GBT_TXUSRDY			
		B2312	27:16	W	TxUsrRdy [23:12]
		B1100	11:0	W	TxUsrRdy [11:0]
0x54A0	0	GBT_RXUSRDY			
		B2312	27:16	W	RxUsrRdy [23:12]
		B1100	11:0	W	RxUsrRdy [11:0]
0x54B0	0	GBT_GTTX_RESET			
		B0503	30:28	W	SOFT_RESET [5:3]
		B2312	27:16	W	GTTX_RESET [23:12]

Address	PCIe	Name/Field		Bits	Type	Description	
			B0200	14:12	W	SOFT_RESET [2:0]	
			B1100	11:0	W	GTTX_RESET [11:0]	
0x54C0	0	GBT_GTRX_RESET					
			B2312	27:16	W	GTRX_RESET [23:12]	
			B1100	11:0	W	GTRX_RESET [11:0]	
0x54D0	0	GBT_PLL_RESET					
			B0503	30:28	W	QPLL_RESET [5:3]	
			B2312	27:16	W	CPLL_RESET [23:12]	
			B0200	14:12	W	QPLL_RESET [2:0]	
			B1100	11:0	W	CPLL_RESET [11:0]	
0x54E0	0	GBT_SOFT_TX_RESET					
			B0503	30:28	W	SOFT_TX_RESET_ALL [5:3]	
			B2312	27:16	W	SOFT_TX_RESET_GT [23:12]	
			B0200	14:12	W	SOFT_TX_RESET_ALL [2:0]	
			B1100	11:0	W	SOFT_TX_RESET_GT [11:0]	
0x54F0	0	GBT_SOFT_RX_RESET					
			B0503	30:28	W	SOFT_RX_RESET_ALL [5:3]	
			B2312	27:16	W	SOFT_RX_RESET_GT [23:12]	
			B0200	14:12	W	SOFT_RX_RESET_ALL [2:0]	
			B1100	11:0	W	SOFT_RX_RESET_GT [11:0]	
0x5500	0	GBT_ODD_EVEN					
			B2312	27:16	W	OddEven [23:12]	
			B1100	11:0	W	OddEven [11:0]	
0x5510	0	GBT_TOPBOT					
			B2312	27:16	W	TopBot [23:12]	
			B1100	11:0	W	TopBot [11:0]	
0x5520	0	GBT_TX_TC_DLY_VALUE1			47:0	W	TX_TC_DLY_VALUE [47:0]
0x5530	0	GBT_TX_TC_DLY_VALUE2			47:0	W	TX_TC_DLY_VALUE [95:48]
0x5540	0	GBT_TX_OPT			47:0	W	TX_OPT
0x5550	0	GBT_RX_OPT			47:0	W	RX_OPT
0x5560	0	GBT_DATA_TXFORMAT					
			B4724	55:32	W	DATA_TXFORMAT [47:24]	
			B2300	23:0	W	DATA_TXFORMAT [23:0]	
0x5570	0	GBT_DATA_RXFORMAT					
			B4724	55:32	W	DATA_RXFORMAT [47:24]	

Address	PCIe	Name/Field		Bits	Type	Description
			B2300	23:0	W	DATA_RXFORMAT [23:0]
0x5580	0	GBT_TX.RESET				
			B2312	27:16	W	TX Logic reset [23:12]
			B1100	11:0	W	TX Logic reset [11:0]
0x5590	0	GBT_RX.RESET				
			B2312	27:16	W	RX Logic reset [23:12]
			B1100	11:0	W	RX Logic reset [11:0]
0x55A0	0	GBT_TX.TC.METHOD				
			B2312	27:16	W	TX time domain crossing method [23:12]
			B1100	11:0	W	TX time domain crossing method [11:0]
0x55B0	0	GBT_OUTMUX_SEL				
			B2312	27:16	W	Descrambler output MUX selection [23:12]
			B1100	11:0	W	Descrambler output MUX selection [11:0]
0x55C0	0	GBT_TC.EDGE				
			B2312	27:16	W	Sampling edge selection for TX domain crossing [23:12]
			B1100	11:0	W	Sampling edge selection for TX domain crossing [11:0]
0x55D0	0	GBT_TRANSCEIVER.POLARITY				
			TXPOLARITY	47:24	W	0: default polarity, 1: reversed polarity for transmitter of GTH channels
			RXPOLARITY	23:0	W	0: default polarity, 1: reversed polarity for the receiver of the GTH channels
0x5600	0	GBT_DNLNK.FO_SEL		31:0	W	ToHost FanOut/Selector. Every bitfield is a channel: 1 : GBT_EMU, select GBT Emulator for a specific CentralRouter channel 0 : GBT_WRAP, select real GBT link for a specific CentralRouter channel

Address	PCIe	Name/Field	Bits	Type	Description
0x5610	0	GBT_UPLNK_FO_SEL	31:0	W	ToFrontEnd FanOut/Selector. Every bitfield is a channel: 1 : GBT_EMU, select GBT Emulator for a specific GBT link 0 : TTC_DEC, select CentralRouter data (including TTC) for a specific GBT link
GBT Wrapper Monitors					
0x6600	0	GBT_VERSION			
		DATE	63:48	R	Date
		GBT_VERSION	47:32	R	GBT Version
		GTH_IP_VERSION	31:16	R	GTH IP Version
		RESERVED	15:3	R	Reserved
		GTHREFCLK_SEL	2	R	GTHREFCLK SEL
		RX_CLK_SEL	1	R	RX CLK SEL
0x6680	0	PLL_SEL	0	R	PLL SEL
		GBT_TXRESET_DONE			
		B2312	27:16	R	TX Reset done [23:12]
0x6690	0	B1100	11:0	R	TX Reset done [11:0]
		GBT_RXRESET_DONE			
		B2312	27:16	R	RX Reset done [23:12]
0x66A0	0	B1100	11:0	R	RX Reset done [11:0]
		GBT_TXFSMRESET_DONE			
		B2312	27:16	R	TX FSM Reset done [23:12]
0x66B0	0	B1100	11:0	R	TX FSM Reset done [11:0]
		GBT_RXFSMRESET_DONE			
		B2312	27:16	R	RX FSM Reset done [23:12]
0x66C0	0	B1100	11:0	R	RX FSM Reset done [11:0]
		GBT_CPLL_FBCLK_LOST			
		B2312	27:16	R	CPLL FBCLK LOST [23:12]
0x66D0	0	B1100	11:0	R	CPLL FBCLK LOST [11:0]
		GBT_CPLL_LOCK			
		B0503	30:28	R	QPLL LOCK [5:3]
		B2312	27:16	R	CPLL LOCK [23:12]
		B0200	14:12	R	QPLL LOCK [2:0]
0x66E0	0	B1100	11:0	R	CPLL LOCK [11:0]
		GBT_RXCDR_LOCK			
		B2312	27:16	R	RX CDR LOCK [23:12]
0x66F0	0	B1100	11:0	R	RX CDR LOCK [11:0]
		GBT_CLK_SAMPLED			

Address	PCIE	Name/Field	Bits	Type	Description
		B23:12	27:16	R	clk sampled [23:12]
		B11:0	11:0	R	clk sampled [11:0]
0x6700	0	GBT_RX_IS_HEADER			
		B23:12	27:16	R	RX IS HEADER [23:12]
		B11:0	11:0	R	RX IS HEADER [11:0]
0x6710	0	GBT_RX_IS_DATA			
		B23:12	27:16	R	RX IS DATA [23:12]
		B11:0	11:0	R	RX IS DATA [11:0]
0x6720	0	GBT_RX_HEADER_FOUND			
		B23:12	27:16	R	RX HEADER FOUND [23:12]
		B11:0	11:0	R	RX HEADER FOUND [11:0]
0x6730	0	GBT_ALIGNMENT_DONE			
		B23:12	27:16	R	RX ALIGNMENT DONE [23:12]
		B11:0	11:0	R	RX ALIGNMENT DONE [11:0]
0x6740	0	GBT_OUT_MUX_STATUS			
		B23:12	27:16	R	GBT output mux status [23:12]
		B11:0	11:0	R	GBT output mux status [11:0]
0x6750	0	GBT_ERROR			
		B23:12	27:16	R	Error flags [23:12]
		B11:0	11:0	R	Error flags [11:0]
0x6760	0	GBT_GBT_TOPBOT_C			
		B23:12	27:16	R	TopBot.c [23:12]
		B11:0	11:0	R	TopBot.c [11:0]
0x6800	0	GBT_FM_RX_DISP_ERROR1	47:0	R	Rx disparity error [47:0]
0x6810	0	GBT_FM_RX_DISP_ERROR2	47:0	R	Rx disparity error [96:48]
0x6820	0	GBT_FM_RX_NOTINTABLE1	47:0	R	Rx not in table [47:0]
0x6830	0	GBT_FM_RX_NOTINTABLE2	47:0	R	Rx not in table [96:48]
House Keeping Controls And Monitors					
0x7200	0	HK_CTRL_CDCE			
		REF_SEL	2	W	REF_SEL
		PD	1	W	PD
		SYNC	0	W	SYNC
0x7210	0	HK_CTRL_I2C			
		CONFIG_TRIG	1	W	i2c_config_trig
		CLKFREQ_SEL	0	W	i2c_clkfreq_sel
0x7220	0	HK_CTRL_FMC			
		SI5345_INSEL	6:5	W	Selects the input clock source 0 : FPGA (FMC LA01) 1 : FMC OSC (40.079 MHz) 2 : FPGA (FMC LA18)

Address	PCIe	Name/Field	Bits	Type	Description
		SI5345_A	4:3	W	Si5345 I2C address select 2 LSB (0x0:default, dev id 0x68)
		SI5345_OE	2	W	Si5345 active low output enable (0:enable)
		SI5345_RSTN	1	W	Si5345 active low output enable (0:reset)
		SI5345_SEL	0	W	Si5345 programming mode 1 : I2C mode (default) 0 : SPI mode
0x7300	0	MMCM_MAIN			
		LCLK_FORCE	3	W	force the use of the Local Clock in any circumstance, overrule automatic clock switch
		AUTOMATIC_CLOCK_SWITCH_ENABLED	1	R	1 when the automatic clock switch is enabled in the design
		OSC_SEL	1	R	Main MMCM Oscillator Select 1: TTC clock 0: Local clock
		PLL_LOCK	0	R	Main MMCM PLL Lock Status
0x7310	0	HK_MON			
		CDCE_PLL_LOCK	1	R	CDCE_PLL_LOCK
		I2C_ACK_ERROR	0	R	i2c_ack_error
0x7400	0	SPI_WR			
		SPI_WREN	any	T	Any write to this register triggers an SPI Write
		SPI_FULL	32	R	SPI FIFO Full
		SPI_DIN	31:0	W	SPI WRITE Data
0x7410	0	SPI_RD			
		SPI_RDEN	any	T	Any write to this register pops the last SPI data from the FIFO
		SPI_EMPTY	32	R	SPI FIFO Empty
		SPI_DOUT	31:0	R	SPI READ Data
0x7420	0	I2C_WR			
		I2C_WREN	any	T	Any write to this register triggers an I2C read or write sequence
		I2C_FULL	25	R	I2C FIFO full
		WRITE_2BYTES	24	W	Write two bytes
		DATA_BYTE2	23:16	W	Data byte 2
		DATA_BYTE1	15:8	W	Data byte 1
		SLAVE_ADDRESS	7:1	W	Slave address
		READ_NOT_WRITE	0	W	READ/ _i WRITE _{i/o}
0x7430	0	I2C_RD			

Address	PCIe	Name/Field	Bits	Type	Description
		I2C_RDEN	any	T	Any write to this register pops the last I2C data from the FIFO
		I2C_EMPTY	8	R	I2C FIFO Empty
		I2C_DOUT	7:0	R	I2C READ Data
0x7440	0	TTC.EMU			
		SEL	1	W	Select TTC data source 1 TTC Emu — 0 TTC Decoder
		ENA	0	W	Enable TTC data generator (10 bit counter)
0x7450	0	FPGA.CORE.TEMP	11:0	R	XADC temperature monitor for the FPGA CORE for FLX709, FLX710 temp (C)= $((\text{FPGA.CORE.TEMP} * 503.975) / 4096) - 273.15$ for FLX711 temp (C)= $((\text{FPGA.CORE.TEMP} * 502.9098) / 4096) - 273.8195$
0x7460	0	FPGA.CORE.VCCINT	11:0	R	XADC voltage measurement VCCINT = $(\text{FPGA.CORE.VCCINT} * 3.0) / 4096$
0x7470	0	FPGA.CORE.VCCAUX	11:0	R	XADC voltage measurement VCCAUX = $(\text{FPGA.CORE.VCCAUX} * 3.0) / 4096$
0x7480	0	FPGA.CORE.VCCBRAM	11:0	R	XADC voltage measurement VCCBRAM = $(\text{FPGA.CORE.VCCBRAM} * 3.0) / 4096$
0x7490	0	LMK.LOCKED	0	R	LMK Chip on BNL711 locked
0x74A0	0,1	FPGA.DNA	63:0	R	Unique identifier of the FPGA
0x74B0	0,1	FPGA.ENDPOINT	0	R	Endpoint of the FPGA
0x7500	0	DEBUG.PORT_GBT	6:0	W	Debug GBT data bit N (119..0) on SMA HTGx#3
0x7510	0	DEBUG.PORT_CLK	3:0	W	Debug clock and L1A port on SMA HTGx#4
0x7800	0	INT.TEST_2	any	T	Fire a test MSIx interrupt #2
0x7810	0	INT.TEST_3	any	T	Fire a test MSIx interrupt #3

Table 3: FELIX register map BAR2