P2: BANK 0 & BANK 44-46 FOR DDR1

P3: BANK 51-53 FOR DDR2

P4: BANK 70 (3.3V HR) & 71-73

P5: THE 12 QUADS OF 48 TX/RX LINKS

P6: PCIE CNT & 4 GTH QUADS

P7: BANK 65 (2.5V HR) & BANK 66-68

P8: POWER & GND FOR FPGA

P9: CDR & CLOCKS

P10: PEX8732 STATIONS 0&1

P11: PEX8732 CONTROL & POWER PINS

P12: DDR4 SODIMMS

P13: POWER: LTM463

P14: POWER: LTM4620A

P15: MINIPOD TX x4

P16: MINIPOD RX x4

P17: VOLTAGE/CURRENT/TEMPERATURE MONITOR & CNTS

NOTE

COMPANY BROOKHAVEN NATIONAL LABORATORY

TITLE

SIZE D REV SHEET TOP OF N

DRAWN KAI CHEN DATE 16/09/2015:15:14

Layout: Place resistor and capacitor for VREF
Underneath the FPGA via array
right next to the via

XCKU115FLVF1924

BANK 44

XCKU115FLVF1924

BANK 45

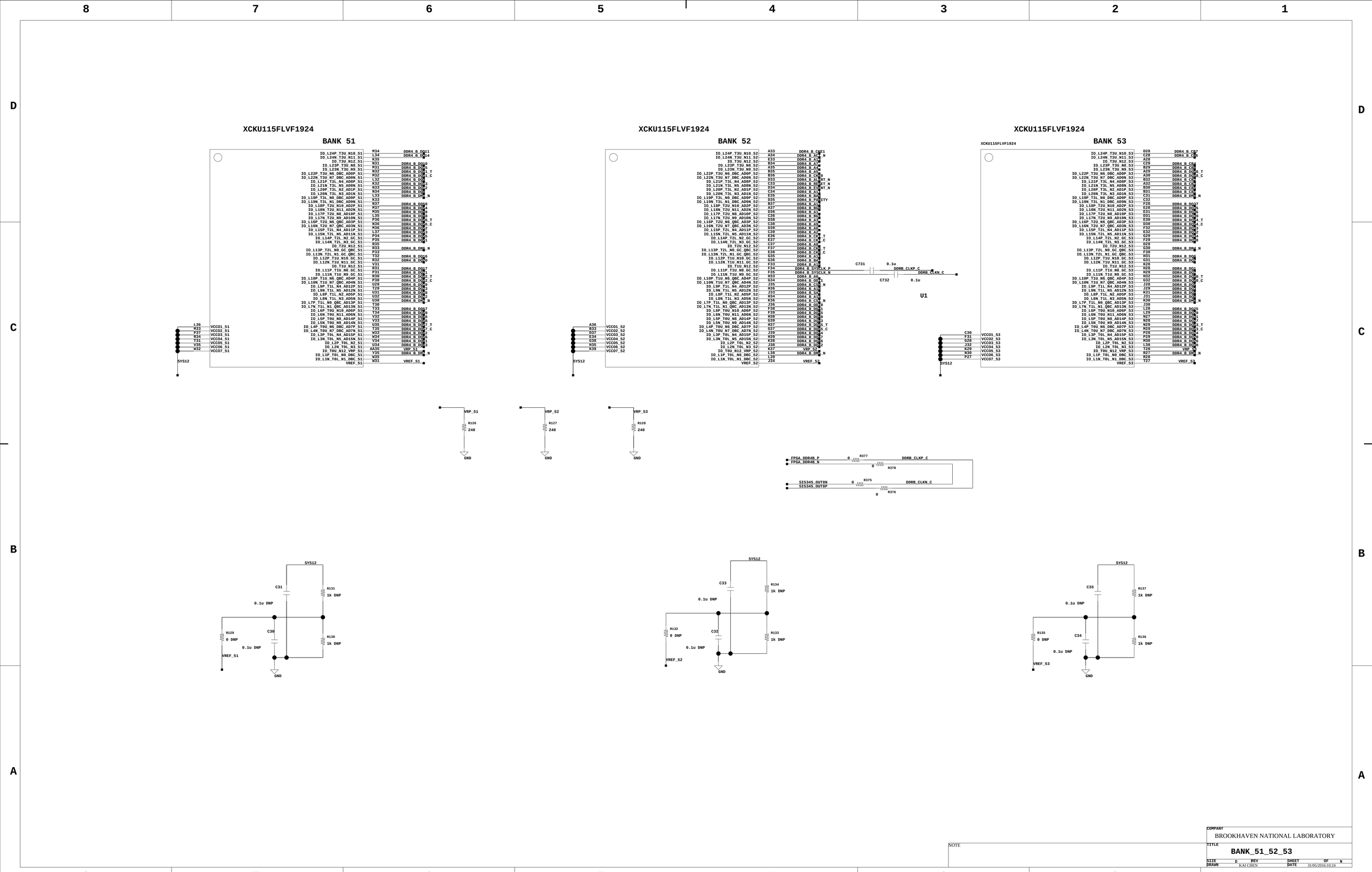
XCKU115FLVF1924

BANK 46

XCKU115FLVF1924

BANK 0

COMPANY	BROOKHAVEN NATIONAL LABORATORY
TITLE	BANK_0_44_45_46
SIZE	D
REV	
SHEET	1 OF N
DRAWN	KAI CHEN
DATE	24/03/2017:10:14
NOTE	



NOTE

COMPANY: BROOKHAVEN NATIONAL LABORATORY

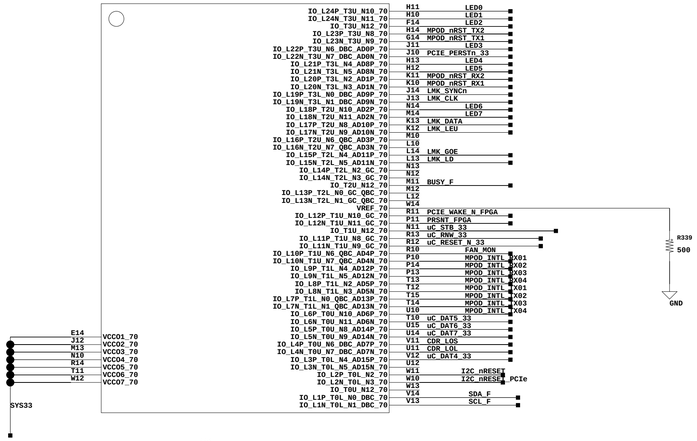
TITLE: BANK_51_52_53

SIZE: D | REV | SHEET | OF | N

DRAWN: KAI CHEN | DATE: 31/05/2016:10:24

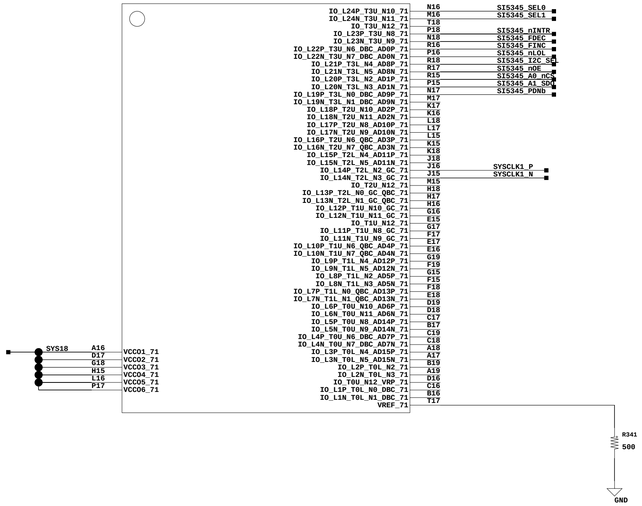
XCKU115FLVF1924

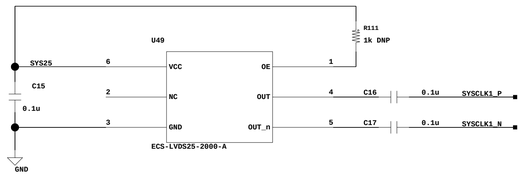
BANK 70



XCKU115FLVF1924

BANK 71





XCKU115FLVF1924

BANK 72

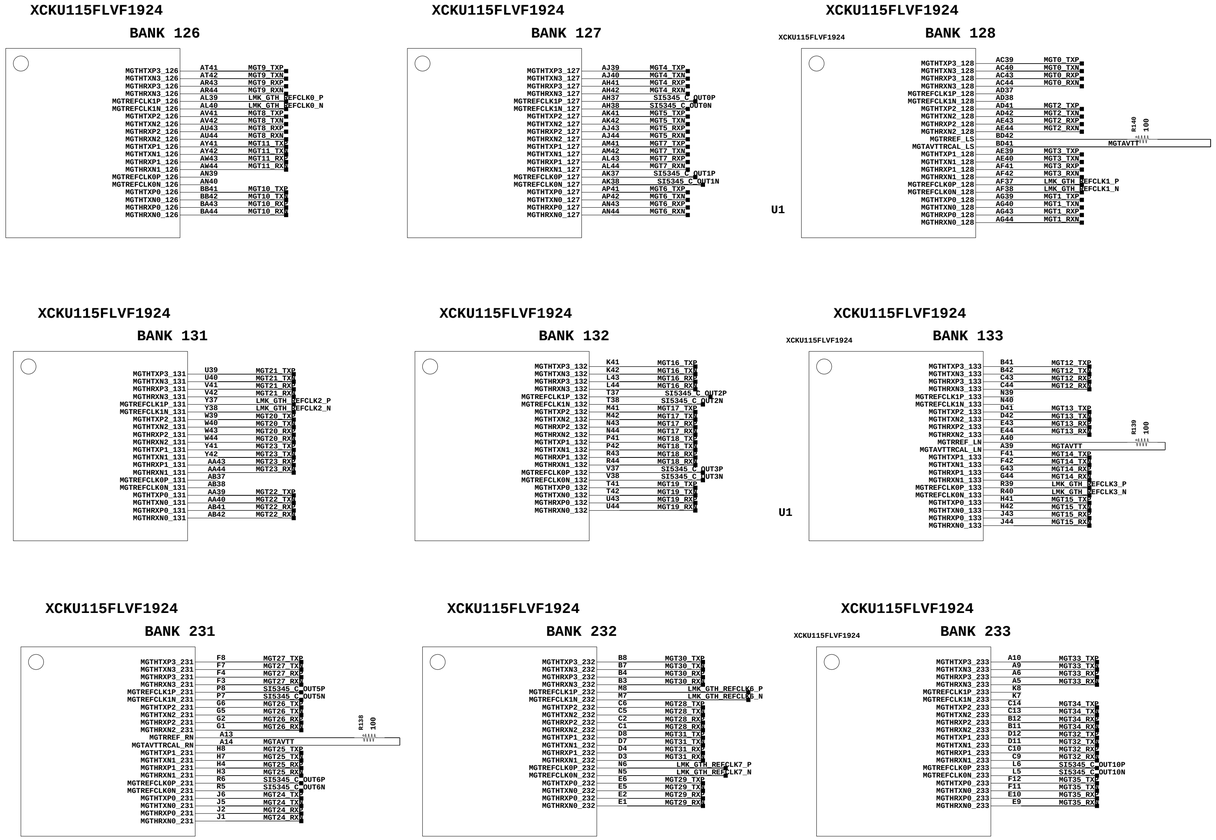


XCKU115FLVF1924

BANK 73



COMPANY	BROOKHAVEN NATIONAL LABORATORY
NOTE	
TITLE	BANK_70_71_72_73
SIZE D REV	SHEET OF N
DRAWN KAI CHEN	DATE 28/06/2016 14:40



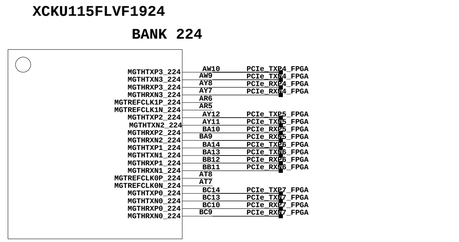
NOTE

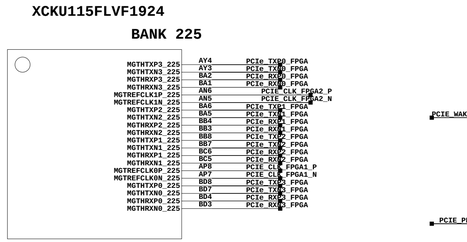
COMPANY: BROOKHAVEN NATIONAL LABORATORY

TITLE: GTH_FOR_DATA

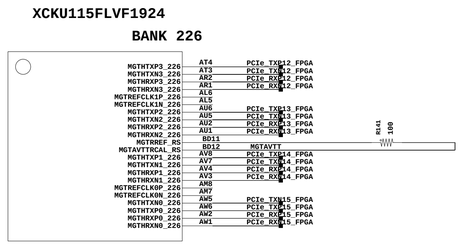
SIZE D REV SHEET OF N

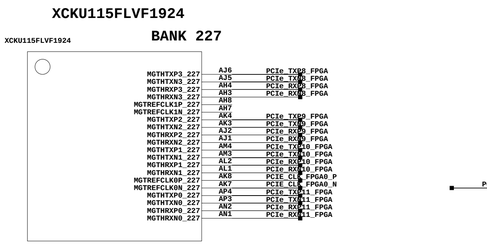
DRAWN KAI CHEN DATE 01/06/2016:10:02

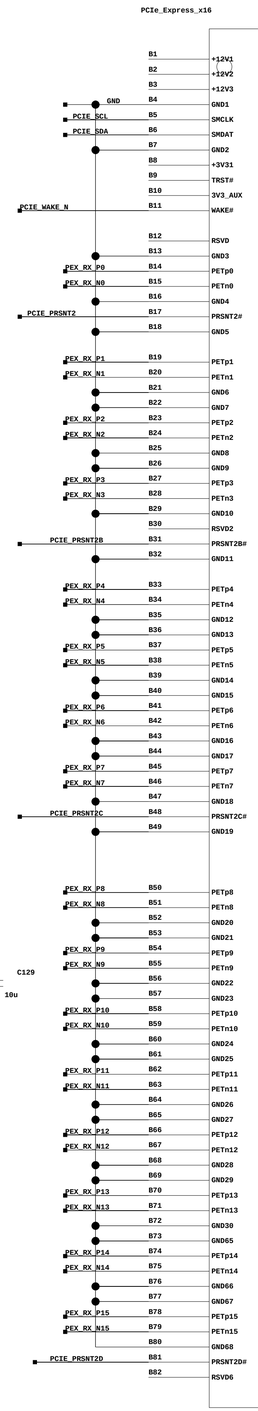


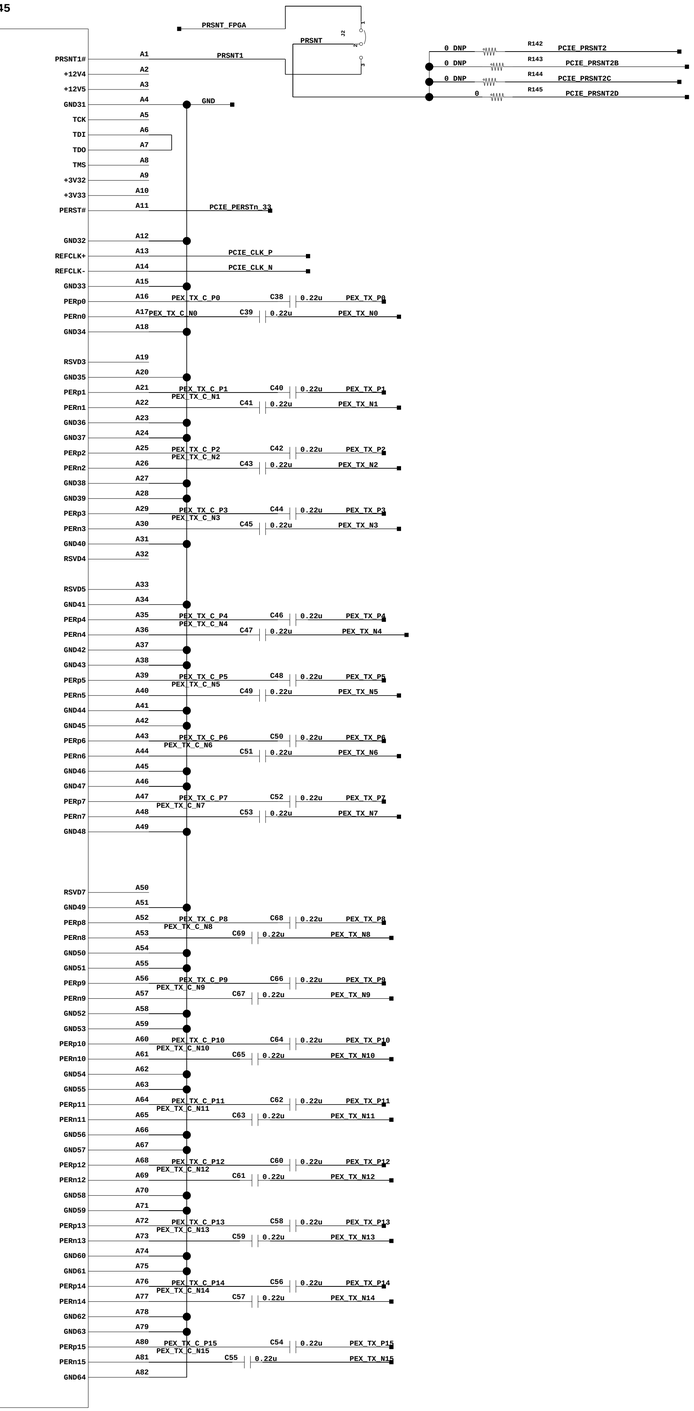


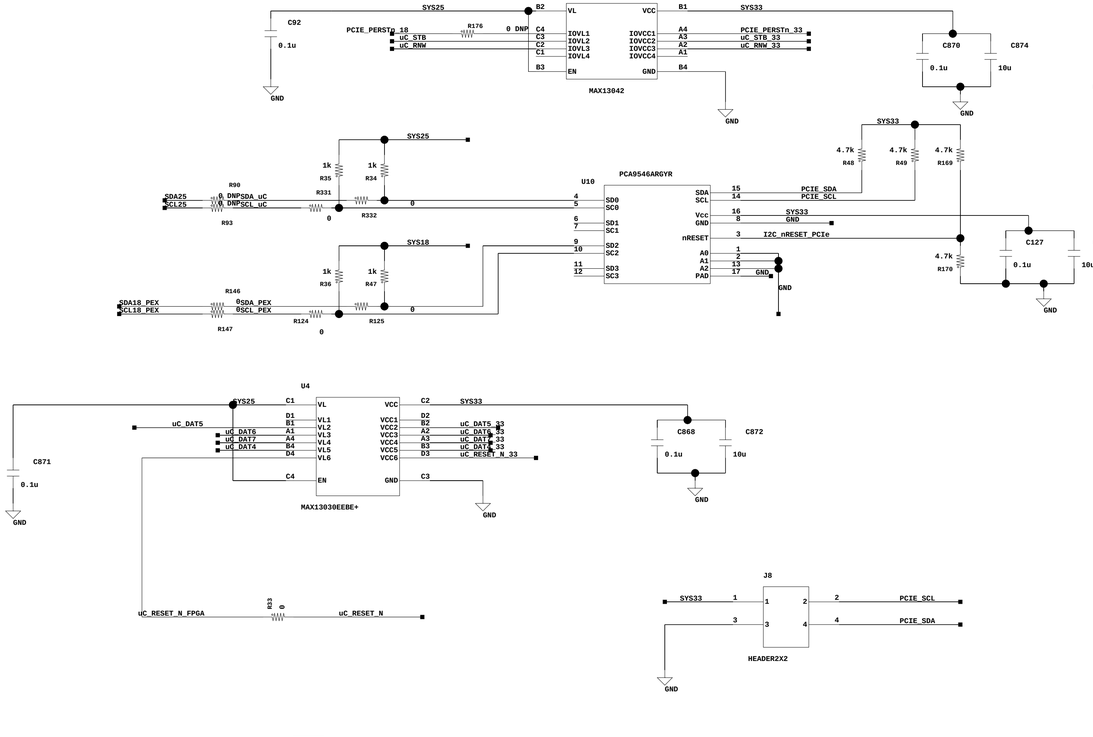
U1











NOTE

COMPANY: BROOKHAVEN NATIONAL LABORATORY

TITLE: PCIE GTH & EDGE

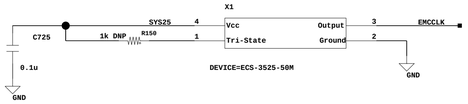
SIZE D REV SHEET OF N

DRAWN KAI CHEN DATE 24/03/2017:10:06

Layout: Place resistor and capacitor for VREF

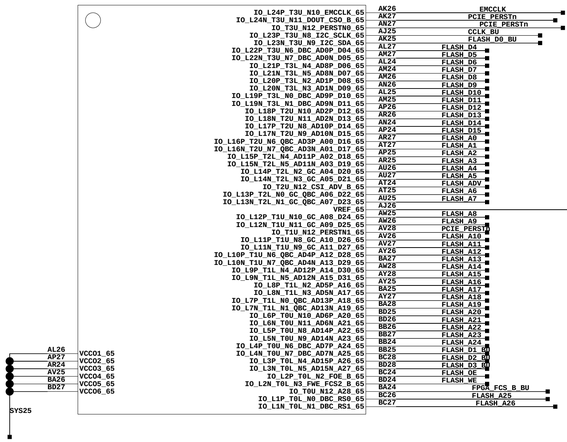
Underneath the FPGA via array

right next to the via



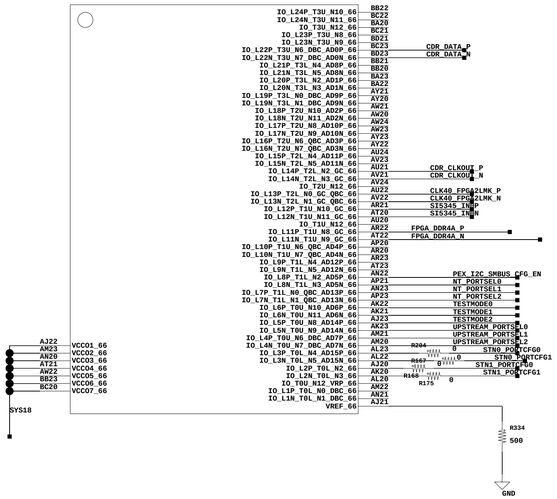
XCKU115FLVF1924

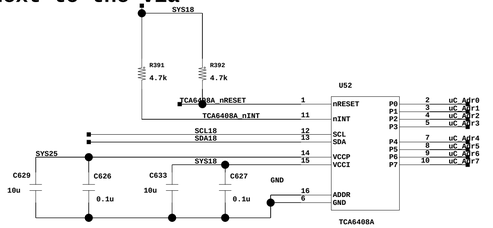
BANK 65

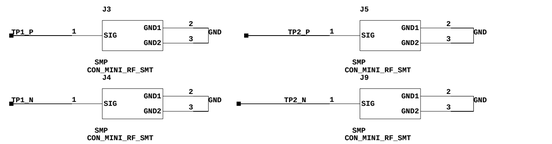


XCKU115FLVF1924

BANK 66

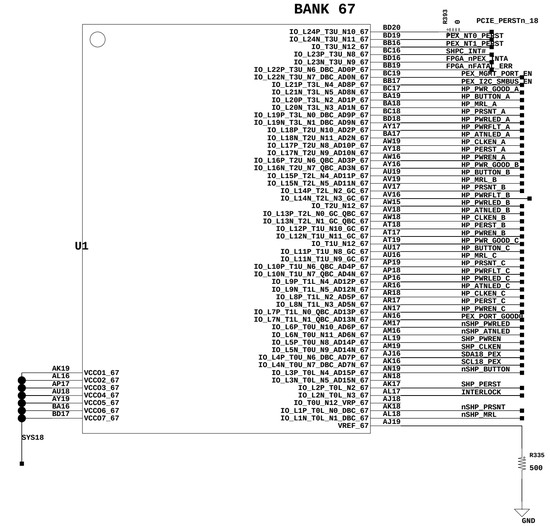






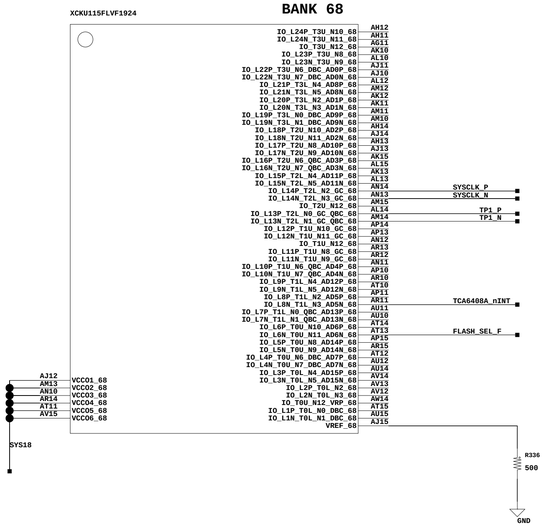
XCKU115FLVF1924

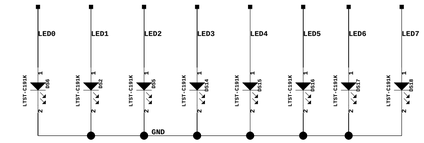
BANK 67

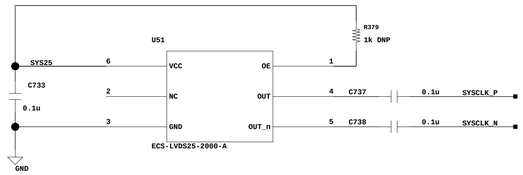


XCKU115FLVF1924

BANK 68

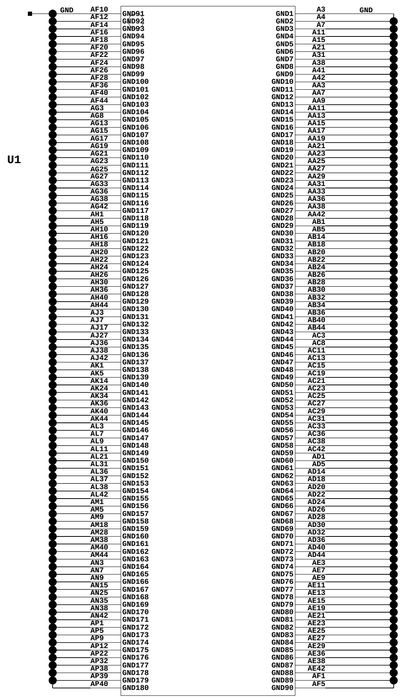


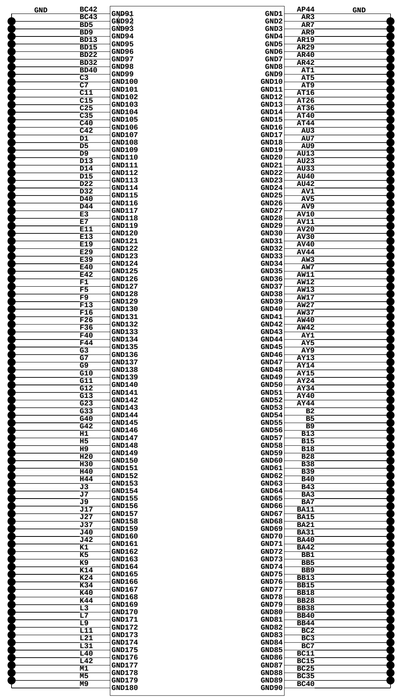


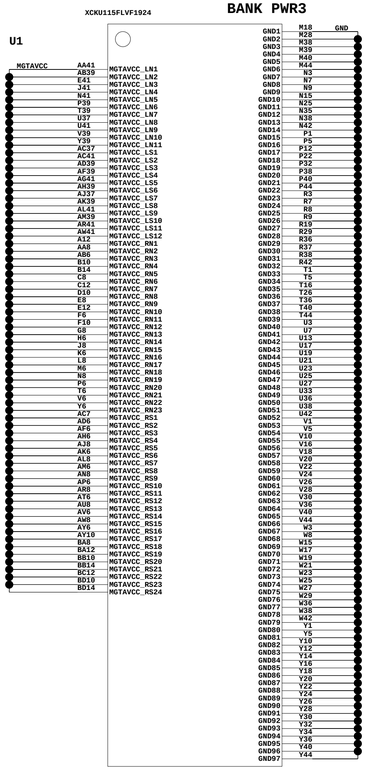


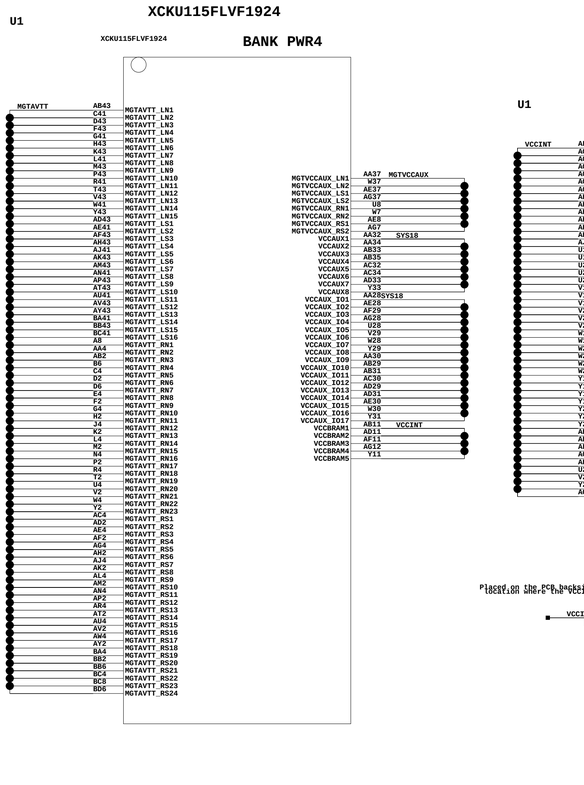
NOTE

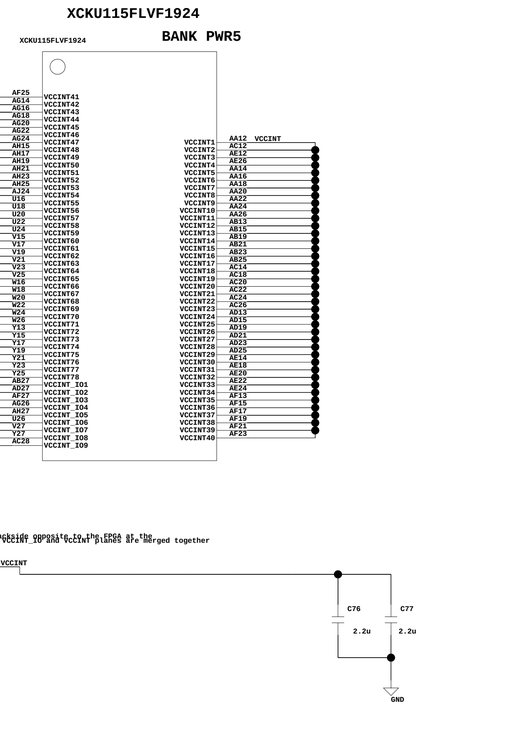
COMPANY	BROOKHAVEN NATIONAL LABORATORY
TITLE	BANK_65_66_67_68
SIZE D REV	SHEET OF N
DRAWN KAI CHEN	DATE 02/08/2016 12:59





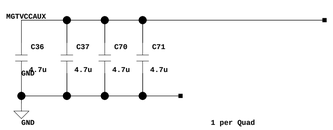






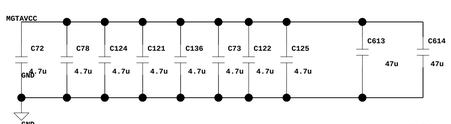
Placed on the PCB backside opposite to the FPGA if the VCCINT and the VCCAUX power planes are merged together

1 per Quad



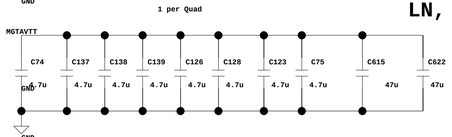
LN, LS, RN, RS: 4x1

1 per Quad



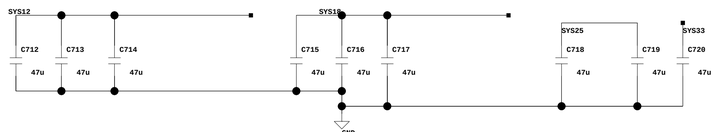
LN, LS, RN, RS: 4x2

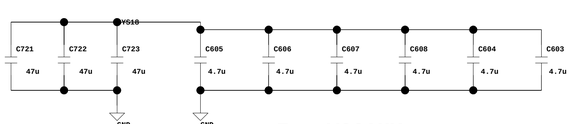
1 per Quad



LN, LS, RN, RS: 4x2

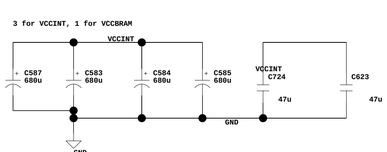
2 banks share one



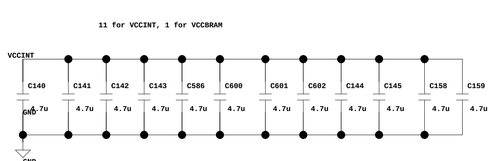


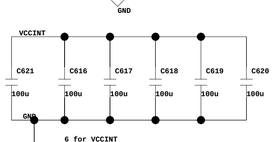
For VCCAUX

3 for VCCINT, 1 for VCCBRAM



11 for VCCINT, 1 for VCCBRAM



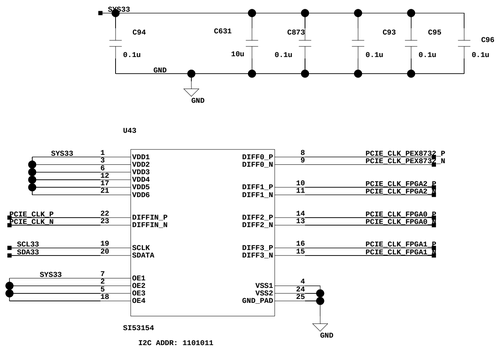


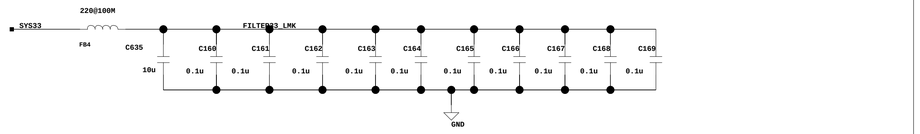
Can place any where close to FPGA

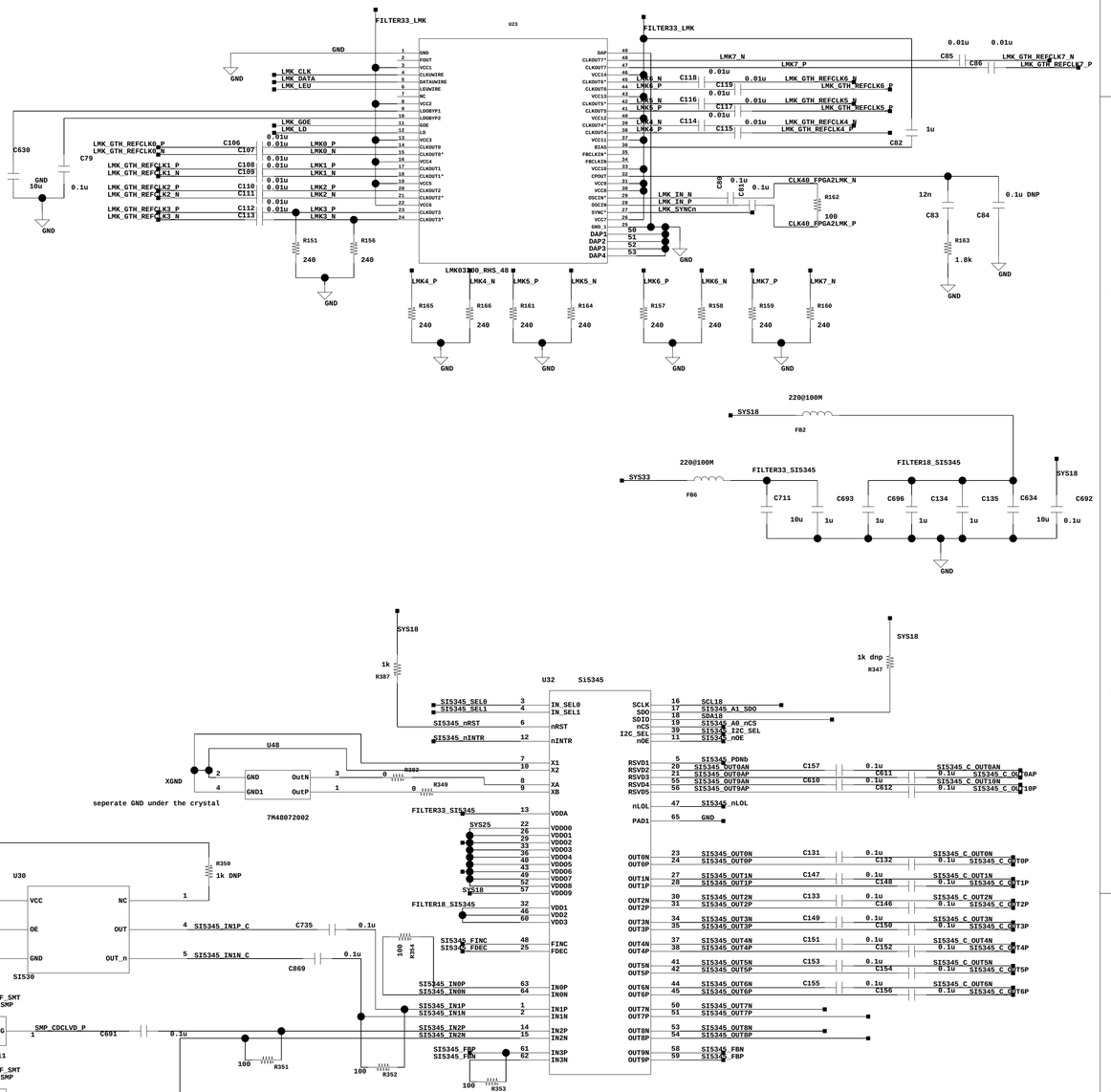


NOTE

COMPANY	BROOKHAVEN NATIONAL LABORATORY
TITLE	FPGA_POWER_PINS
SIZE D REV	SHEET OF N
DRAWN KAI CHEN	DATE 20/06/2016:14:43







NOTE

COMPANY	BROOKHAVEN NATIONAL LABORATORY				
TITLE	CLOCK				
SIZE	D	REV		SHEET	OF N
DRAWN	KAI CHEN			DATE	02/08/2016:09:47

PEX8732

U31

Station 0

PEX8732

R188 3k — REXT_A0
R189 3k
R190 3k — REXT_A1
R191 3k
R192 3k — REXT_A2
R193 3k
R194 3k — REXT_A3
R195 3k
R357 3k — REXT_CMU

GND

PCIE_CLK_PEX8732_P — PEX_REFCLKp
PCIE_CLK_PEX8732_N — PEX_REFCLKn

PEX_PETp[0]	AE5	PEX_TX_P0	
PEX_PETn[0]	AF5	PEX_TX_N0	
PEX_PERp[0]	AB5	PEX_RX_P0	
PEX_PERn[0]	AC5	PEX_RX_N0	
PEX_PETp[1]	AE6	PEX_TX_P1	
PEX_PETn[1]	AF6	PEX_TX_N1	
PEX_PERp[1]	AB6	PEX_RX_P1	
PEX_PERn[1]	AC6	PEX_RX_N1	
PEX_PETp[2]	AE7	PEX_TX_P2	
PEX_PETn[2]	AF7	PEX_TX_N2	
PEX_PERp[2]	AB7	PEX_RX_P2	
PEX_PERn[2]	AC7	PEX_RX_N2	
PEX_PETp[3]	AE8	PEX_TX_P3	
PEX_PETn[3]	AF8	PEX_TX_N3	
PEX_PERp[3]	AB8	PEX_RX_P3	
PEX_PERn[3]	AC8	PEX_RX_N3	
PEX_PETp[4]	AE10	PEX_TX_P4	
PEX_PETn[4]	AF10	PEX_TX_N4	
PEX_PERp[4]	AB10	PEX_RX_P4	
PEX_PERn[4]	AC10	PEX_RX_N4	
PEX_PETp[5]	AE11	PEX_TX_P5	
PEX_PETn[5]	AF11	PEX_TX_N5	
PEX_PERp[5]	AB11	PEX_RX_P5	
PEX_PERn[5]	AC11	PEX_RX_N5	
PEX_PETp[6]	AE12	PEX_TX_P6	
PEX_PETn[6]	AF12	PEX_TX_N6	
PEX_PERp[6]	AB12	PEX_RX_P6	
PEX_PERn[6]	AC12	PEX_RX_N6	
PEX_PETp[7]	AE13	PEX_TX_P7	
PEX_PETn[7]	AF13	PEX_TX_N7	
PEX_PERp[7]	AB13	PEX_RX_P7	
PEX_PERn[7]	AC13	PEX_RX_N7	
PEX_PETp[8]	AE14	PEX_TX_P8	
PEX_PETn[8]	AF14	PEX_TX_N8	
PEX_PERp[8]	AB14	PEX_RX_P8	
PEX_PERn[8]	AC14	PEX_RX_N8	
PEX_PETp[9]	AE15	PEX_TX_P9	
PEX_PETn[9]	AF15	PEX_TX_N9	
PEX_PERp[9]	AB15	PEX_RX_P9	
PEX_PERn[9]	AC15	PEX_RX_N9	
PEX_PETp[10]	AE16	PEX_TX_P10	
PEX_PETn[10]	AF16	PEX_TX_N10	
PEX_PERp[10]	AB16	PEX_RX_P10	
PEX_PERn[10]	AC16	PEX_RX_N10	
PEX_PETp[11]	AE17	PEX_TX_P11	
PEX_PETn[11]	AF17	PEX_TX_N11	
PEX_PERp[11]	AB17	PEX_RX_P11	
PEX_PERn[11]	AC17	PEX_RX_N11	
PEX_PETp[12]	AE19	PEX_TX_P12	
PEX_PETn[12]	AF19	PEX_TX_N12	
PEX_PERp[12]	AB19	PEX_RX_P12	
PEX_PERn[12]	AC19	PEX_RX_N12	
PEX_PETp[13]	AE20	PEX_TX_P13	
PEX_PETn[13]	AF20	PEX_TX_N13	
PEX_PERp[13]	AB20	PEX_RX_P13	
PEX_PERn[13]	AC20	PEX_RX_N13	
PEX_PETp[14]	AE21	PEX_TX_P14	
PEX_PETn[14]	AF21	PEX_TX_N14	
PEX_PERp[14]	AB21	PEX_RX_P14	
PEX_PERn[14]	AC21	PEX_RX_N14	
PEX_PETp[15]	AE22	PEX_TX_P15	
PEX_PETn[15]	AF22	PEX_TX_N15	
PEX_PERp[15]	AB22	PEX_RX_P15	
PEX_PERn[15]	AC22	PEX_RX_N15	

AE9	PEX_REFCLKp		
AF9	PEX_REFCLKn		
AE2	NC6		
AF2	NC7		
AE3	NC8		
AF3	NC9		
AE18	NC10		
AF18	NC11		
AA25	NC12		
AA26	NC13		

Y4	REXT_A0		
Y5	REXT_B0		
AC9	REXT_A1		
AB9	REXT_B1		
AC18	REXT_A2		
AB18	REXT_B2		
AB24	REXT_A3		
Y22	REXT_B3		
AB10	Y1	REXT_CMU	

PEX8732

U31

Station 1

PEX8732

R196 3k — REXT_A4
R197 3k
R198 3k — REXT_A5
R199 3k
R200 3k — REXT_A6
R201 3k
R202 3k — REXT_A7
R203 3k

GND

N4	REXT_A4		
N5	REXT_B4		
H3	REXT_A5		
G3	REXT_B5		
A3	REXT_A6		
C1	REXT_B6		
D9	REXT_A7		
E9	REXT_B7		
W1	NC14		
W2	NC15		
N2	NC16		
N1	NC17		
F1	NC18		
E1	NC19		
B9	NC20		
A9	NC21		

PEX_PETp[16]	U2	PEX_F_R0_P	C178	0.22u		PCIe_RXP0_FPGA
PEX_PETn[16]	U1	PEX_F_R0_N	C179	0.22u		PCIe_RXN0_FPGA
PEX_PERp[16]	U5	PEX_F_T0_P	C180	0.22u		PCIe_TXP0_FPGA
PEX_PERn[16]	U4	PEX_F_T0_N	C181	0.22u		PCIe_TXN0_FPGA
PEX_PETp[17]	T2	PEX_F_R1_P	C182	0.22u		PCIe_RXP1_FPGA
PEX_PETn[17]	T1	PEX_F_R1_N	C183	0.22u		PCIe_RXN1_FPGA
PEX_PERp[17]	T5	PEX_F_T1_P	C184	0.22u		PCIe_TXP1_FPGA
PEX_PERn[17]	T4	PEX_F_T1_N	C185	0.22u		PCIe_TXN1_FPGA
PEX_PETp[18]	R2	PEX_F_R2_P	C186	0.22u		PCIe_RXP2_FPGA
PEX_PETn[18]	R1	PEX_F_R2_N	C187	0.22u		PCIe_RXN2_FPGA
PEX_PERp[18]	R5	PEX_F_T2_P	C188	0.22u		PCIe_TXP2_FPGA
PEX_PERn[18]	R4	PEX_F_T2_N	C189	0.22u		PCIe_TXN2_FPGA
PEX_PETp[19]	P2	PEX_F_R3_P	C190	0.22u		PCIe_RXP3_FPGA
PEX_PETn[19]	P1	PEX_F_R3_N	C191	0.22u		PCIe_RXN3_FPGA
PEX_PERp[19]	P5	PEX_F_T3_P	C192	0.22u		PCIe_TXP3_FPGA
PEX_PERn[19]	P4	PEX_F_T3_N	C193	0.22u		PCIe_TXN3_FPGA
PEX_PETp[20]	M2	PEX_F_R4_P	C194	0.22u		PCIe_RXP4_FPGA
PEX_PETn[20]	M1	PEX_F_R4_N	C195	0.22u		PCIe_RXN4_FPGA
PEX_PERp[20]	M5	PEX_F_T4_P	C196	0.22u		PCIe_TXP4_FPGA
PEX_PERn[20]	M4	PEX_F_T4_N	C197	0.22u		PCIe_TXN4_FPGA
PEX_PETp[21]	L2	PEX_F_R5_P	C198	0.22u		PCIe_RXP5_FPGA
PEX_PETn[21]	L1	PEX_F_R5_N	C199	0.22u		PCIe_RXN5_FPGA
PEX_PERp[21]	L5	PEX_F_T5_P	C200	0.22u		PCIe_TXP5_FPGA
PEX_PERn[21]	L4	PEX_F_T5_N	C201	0.22u		PCIe_TXN5_FPGA
PEX_PETp[22]	K2	PEX_F_R6_P	C202	0.22u		PCIe_RXP6_FPGA
PEX_PETn[22]	K1	PEX_F_R6_N	C203	0.22u		PCIe_RXN6_FPGA
PEX_PERp[22]	K5	PEX_F_T6_P	C204	0.22u		PCIe_TXP6_FPGA
PEX_PERn[22]	K4	PEX_F_T6_N	C205	0.22u		PCIe_TXN6_FPGA
PEX_PETp[23]	J2	PEX_F_R7_P	C206	0.22u		PCIe_RXP7_FPGA
PEX_PETn[23]	J1	PEX_F_R7_N	C207	0.22u		PCIe_RXN7_FPGA
PEX_PERp[23]	J5	PEX_F_T7_P	C208	0.22u		PCIe_TXP7_FPGA
PEX_PERn[23]	J4	PEX_F_T7_N	C209	0.22u		PCIe_TXN7_FPGA
PEX_PETp[24]	B5	PEX_F_R8_P	C171	0.22u		PCIe_RXP8_FPGA
PEX_PETn[24]	A5	PEX_F_R8_N	C172	0.22u		PCIe_RXN8_FPGA
PEX_PERp[24]	E5	PEX_F_T8_P	C170	0.22u		PCIe_TXP8_FPGA
PEX_PERn[24]	D5	PEX_F_T8_N	C172	0.22u		PCIe_TXN8_FPGA
PEX_PETp[25]	B6	PEX_F_R9_P	C210	0.22u		PCIe_RXP9_FPGA
PEX_PETn[25]	A6	PEX_F_R9_N	C211	0.22u		PCIe_RXN9_FPGA
PEX_PERp[25]	E6	PEX_F_T9_P	C212	0.22u		PCIe_TXP9_FPGA
PEX_PERn[25]	D6	PEX_F_T9_N	C213	0.22u		PCIe_TXN9_FPGA
PEX_PETp[26]	B7	PEX_F_R10_P	C214	0.22u		PCIe_RXP10_FPGA
PEX_PETn[26]	A7	PEX_F_R10_N	C215	0.22u		PCIe_RXN10_FPGA
PEX_PERp[26]	E7	PEX_F_T10_P	C216	0.22u		PCIe_TXP10_FPGA
PEX_PERn[26]	D7	PEX_F_T10_N	C217	0.22u		PCIe_TXN10_FPGA
PEX_PETp[27]	B8	PEX_F_R11_P	C218	0.22u		PCIe_RXP11_FPGA
PEX_PETn[27]	A8	PEX_F_R11_N	C219	0.22u		PCIe_RXN11_FPGA
PEX_PERp[27]	E8	PEX_F_T11_P	C220	0.22u		PCIe_TXP11_FPGA
PEX_PERn[27]	D8	PEX_F_T11_N	C221	0.22u		PCIe_TXN11_FPGA
PEX_PETp[28]	B10	PEX_F_R12_P	C222	0.22u		PCIe_RXP12_FPGA
PEX_PETn[28]	A10	PEX_F_R12_N	C223	0.22u		PCIe_RXN12_FPGA
PEX_PERp[28]	E10	PEX_F_T12_P	C224	0.22u		PCIe_TXP12_FPGA
PEX_PERn[28]	D10	PEX_F_T12_N	C225	0.22u		PCIe_TXN12_FPGA
PEX_PETp[29]	B11	PEX_F_R13_P	C226	0.22u		PCIe_RXP13_FPGA
PEX_PETn[29]	A11	PEX_F_R13_N	C227	0.22u		PCIe_RXN13_FPGA
PEX_PERp[29]	E11	PEX_F_T13_P	C228	0.22u		PCIe_TXP13_FPGA
PEX_PERn[29]	D11	PEX_F_T13_N	C229	0.22u		PCIe_TXN13_FPGA
PEX_PETp[30]	B12	PEX_F_R14_P	C230	0.22u		PCIe_RXP14_FPGA
PEX_PETn[30]	A12	PEX_F_R14_N	C231	0.22u		PCIe_RXN14_FPGA
PEX_PERp[30]	E12	PEX_F_T14_P	C232	0.22u		PCIe_TXP14_FPGA
PEX_PERn[30]	D12	PEX_F_T14_N	C233	0.22u		PCIe_TXN14_FPGA
PEX_PETp[31]	B13	PEX_F_R15_P	C174	0.22u		PCIe_RXP15_FPGA
PEX_PETn[31]	A13	PEX_F_R15_N	C175	0.22u		PCIe_RXN15_FPGA
PEX_PERp[31]	E13	PEX_F_T15_P	C176	0.22u		PCIe_TXP15_FPGA
PEX_PERn[31]	D13	PEX_F_T15_N	C177	0.22u		PCIe_TXN15_FPGA

PEX8732

U31

NC

PEX8732

Y25 — NC30
Y23 — NC31
N23 — NC32
N22 — NC33
E24 — NC34
F18 — NC35
D18 — NC36
E18 — NC37
W24 — NC22
W25 — NC23
N25 — NC24
N26 — NC25
B24 — NC26
A24 — NC27
B18 — NC28
A18 — NC29

NC38	U25		
NC39	U26		
NC40	U22		
NC41	U23		
NC42	T25		
NC43	T26		
NC44	T22		
NC45	T23		
NC46	R25		
NC47	R26		
NC48	R22		
NC49	R23		
NC50	P25		
NC51	P26		
NC52	P22		
NC53	P23		
NC54	N25		
NC55	N26		
NC56	M22		
NC57	M23		
NC58	L25		
NC59	L26		
NC60	L22		
NC61	L23		
NC62	K25		
NC63	K26		
NC64	K22		
NC65	K23		
NC66	J25		
NC67	J26		
NC68	J22		
NC69	J23		
NC70	A22		
NC71	C22		
NC72	C23		
NC73	D22		
NC74	B21		
NC75	A21		
NC76	E21		
NC77	D21		
NC78	B20		
NC79	A20		
NC80	E20		
NC81	D20		
NC82	B19		
NC83	A19		
NC84	E19		
NC85	D19		
NC86	B17		
NC87	A17		
NC88	E17		
NC89	D17		
NC90	B16		
NC91	A16		
NC92	E16		
NC93	D16		
NC94	B15		
NC95	A15		
NC96	E15		
NC97	D15		
NC98	B14		
NC99	A14		
NC100	E14		
NC101	D14		

NOTE

COMPANY: BROOKHAVEN NATIONAL LABORATORY
TITLE: PEX_STATIONS
SIZE: D | REV | SHEET | OF | N
DRAWN: KAI CHEN | DATE: 03/08/2016:09:37

PEX8732

U31

CONTROL

PEX8732

SYS18

GND

10k R238 · 10k R237 · 10k R240 · 10k R239 · 10k R235

PCIE_PERSTn_18 → PEX_NT_PERST → PEX_NT1_PERST

SHPC_INT# — FPGA_nPEX_INTA — FPGA_nFATAL_ERR

1k R236 — PEX_JTAG_RSTn

JTAG_TRST# · JTAG_TCK · JTAG_TMS · JTAG_TDI · JTAG_TDO

PEX_EE_SK · PEX_EE_CSn · PEX_EE_DI · PEX_EE_DO

TESTMODE0 · TESTMODE1 · TESTMODE2

UPSTREAM_PORTSEL0 · UPSTREAM_PORTSEL1 · UPSTREAM_PORTSEL2

STN0_PORTCFG0 · STN0_PORTCFG1

STN1_PORTCFG0 · STN1_PORTCFG1

10k R243 · 10k R245 · 10k R205

PEX_MGMT_PORT_EN

0 R207

0 R208 DNP

PEX_I2C_SMBUS_CFG_EN

10k DNP R244 · 10k DNP R246 · 10k DNP R206

PEX_I2C_SMBUS_EN

PEX_PERST#	AC1	HP_PWR_GOOD_A_VS_MODE
PEX_NT_PERST#	AD25	HP_BUTTON_A_VS0_PERST#
NC5	F3	HP_MRL_A#_VS1_PERST#
SHPC_INT#	B3	HP_PRSNT_A#_VS2_PERST#
PEX_INTA#	D1	HP_PWRFLT_A#_VS1_FATAL_ERR#
FATAL_ERR#	C24	HP_PWRLED_A#_VS0_FATAL_ERR#
		HP_ATNLED_A#_VS0_PEX_INTA#
		HP_CLKEN_A#_VS1_PEX_INTA#
		HP_PERST_A#_VS2_PEX_INTA#
		HP_PWREN_A_VS2_FATAL_ERR#
JTAG_TRST#	C2	
JTAG_TCK	B2	
JTAG_TMS	B1	
JTAG_TDI	C3	
JTAG_TDO	G5	
EE_SK	E25	HP_PWR_GOOD_B_PORT_GOOD7#
EE_CS#	E26	HP_BUTTON_B#_PORT_GOOD2#
EE_DI	G23	HP_MRL_B#_PORT_GOOD4#
EE_DO	F26	HP_PRSNT_B#_PORT_GOOD6#
		HP_PWRFLT_B#_PORT_GOOD9#
		HP_PWRLED_B#_PORT_GOOD10#
		HP_ATNLED_B#_PORT_GOOD1#
		HP_CLKEN_B#_PORT_GOOD3#
		HP_PERST_B#_PORT_GOOD5#
		HP_PWREN_B_PORT_GOOD8#
TESTMODE0	Y6	
TESTMODE1	AD3	
TESTMODE2	AD4	
UPSTREAM_PORTSEL0	G24	
UPSTREAM_PORTSEL1	G25	
UPSTREAM_PORTSEL2	G26	
STN0_PORTCFG0	AD24	
STN0_PORTCFG1	AF24	
STN1_PORTCFG0	C4	
STN1_PORTCFG1	G1	
		HP_PWR_GOOD_C_PORT_GOOD11#
		HP_BUTTON_C#_VS3_PERST#
		HP_MRL_C#_VS4_PERST#
		HP_PRSNT_C#_VS5_PERST#
		HP_PWRFLT_C#_VS4_FATAL_ERR#
		HP_PWRLED_C#_VS3_FATAL_ERR#
		HP_ATNLED_C#_VS3_PEX_INTA#
		HP_CLKEN_C#_VS4_PEX_INTA#
		HP_PERST_C#_VS5_PEX_INTA#
		HP_PWREN_C_VS5_FATAL_ERR#
PORT_GOOD0#	D3	PEX_PORT_GOOD0
I2C_SDA1	AE25	PEX_MASTER_SDA
I2C_SCL1	AC25	PEX_MASTER_SCL
I2C_SDA0	E3	SDA_PEX
I2C_SCL0	G4	SCL_PEX
NC1	Y2	
NC2	AA9	
NC3	F9	
NC4	W4	
SPARE0	D2	
SPARE1	AA3	
SPARE2	AA2	
SPARE3	AA1	
THERMAL_DIODEn	AC24	PEX_DIODE_N
THERMAL_DIODEp	AF25	PEX_DIODE_P
STRAP_RESERVED8	C23	
STRAP_RESERVED9	C26	
STRAP_PLL_BYPASS#	Y26	
STRAP_MGMT_PORT_EN	G2	
STRAP_SERDES_MODE_EN#	W26	
STRAP_I2C_SMBUS_EN	F2	
STRAP_I2C_SMBUS_CFG_EN#	W6	
I2C_ADDR0	E2	
STRAP_PROBE_MODE#	Y21	
STRAP_NT_UPSTRM_PORTSEL0	A2	
STRAP_NT_UPSTRM_PORTSEL1	G6	
STRAP_NT_UPSTRM_PORTSEL2	AA18	
STRAP_GEN1_GEN2	H24	
STRAP_RESERVED1	N6	
STRAP_RESERVED2	N21	
STRAP_RESERVED3	W3	
STRAP_RESERVED16	AE24	

SYS18 — 10k R231 · 10k R232

SYS18 — 10k R209 DNP · 10k R211 · 10k R213 — TESTMODE0 · TESTMODE1 · TESTMODE2 — 10k R210 · 10k R212 · 10k R214 — GND

SYS18 — 10k R215 DNP · 10k R217 · 10k R219 — UPSTREAM_PORTSEL0 · UPSTREAM_PORTSEL1 · UPSTREAM_PORTSEL2 — 10k R216 · 10k R218 · 10k R220 — GND

SYS18 — 10k R221 DNP · 10k R223 · 10k R225 · 10k R227 · 10k R229 — STN0_PORTCFG0 · STN0_PORTCFG1 · STN1_PORTCFG0 · STN1_PORTCFG1 · GEN1_GEN2 — 10k R222 DNP · 10k R224 · 10k R226 DNP · 10k R228 · 10k R230 DNP — GND

SYS18 — 10k R362 · 10k R358 · 10k R360 — NT_PORTSEL2 · NT_PORTSEL1 · NT_PORTSEL0 — 10k R363 DNP · 10k R359 DNP · 10k R361 DNP — GND

SYS18 — 10k R242 · 10k R395

U42 — AT25256B

PEX_EE_CSn	1	CS_n	VCC
PEX_EE_DO	2	SO	HOLD_n
SYS18	3	WP_n	SCK
	4	VSS	SI
			PAD

	8	VCC	SYS18
	7	HOLD_n	
PEX_EE_SK	6	SCK	
PEX_EE_DI	5	SI	
	9	PAD	

C637 10u · C341 0.1u · C340 0.1u — GND

SYS18 — 4.7k R241 · 4.7k R394

U28 — TCA6416A

SHPC_INT#	24	nRESET	P00
	22	nINT	P01
PEX_MASTER_SDA	20	SDA	P02
PEX_MASTER_SCL	19	SCL	P03
			P04
			P05
			P06
			P07
	23	VCCI	
	21	VCCP	
			P10
			P11
			P12
			P13
	18	ADDR	P14
	9	GND	P15
	25	PAD	P16
			P17

1	nSHP_PWRLED	
2	nSHP_ATNLED	
3	SHP_PWREN	
4	SHP_CLKEN	
5	SHP_PERST	
6	INTERLOCK	
7		
8		
10		
11		
12		
13		
14	nSHP_PRSNT	
15	nSHP_MRL	
16	nSHP_BUTTON	
17		

C689 10u · C628 0.1u — GND

POWER

PEX8732

U31

PEX8732

SYS18 · PEX1P0VA · PEX0P9V

A1	VSS1	VSS572	AD21
A4	VSS2	VSS573	AD22
A23	VSS3	VSS574	AD23
A25	VSS4	VSS575	AE4
A26	VSS5	VSS576	AE23
B4	VSS6	VSS577	AF1
B23	VSS7	VSS578	AF4
C5	VSS8	VSS579	AF23
C6	VSS9	VSS580	AF26
C7	VSS10	VSS581	AA17
C8	VSS11	VSS582	AA19
C9	VSS12	VSS583	AA20
C10	VSS13	VSS584	AA21
C11	VSS14	VSS585	AA22
C12	VSS15	VSS586	AA23
C13	VSS16	VSS587	AB4
C14	VSS17	VSS588	AB23
C15	VSS18	VSS589	AC4
C16	VSS19	VSS590	AC21
C17	VSS20	VSS591	AD5
C18	VSS21	VSS592	AD6
C19	VSS22	VSS593	AD7
C20	VSS23	VSS594	AD8
C21	VSS24	VSS595	AD9
C22	VSS25	VSS596	AD10
D4	VSS26	VSS597	AD11
D23	VSS27	VSS598	AD12
E4	VSS28	VSS599	AD13
E23	VSS29	VSS600	AD14
F4	VSS30	VSS601	AD15
F5	VSS31	VSS602	AD16
F6	VSS32	VSS603	AD17
F7	VSS33	VSS604	AD18
F8	VSS34	VSS605	AD19
F10	VSS35	VSS606	AD20
F11	VSS36	VSS607	W13
F12	VSS37	VSS608	W14
F13	VSS38	VSS609	W15
F14	VSS39	VSS610	W16
F15	VSS40	VSS611	W17
F16	VSS41	VSS612	W18
F17	VSS42	VSS613	Y8
F19	VSS43	VSS614	Y10
F20	VSS44	VSS615	AA4
F21	VSS45	VSS616	AA5
F22	VSS46	VSS617	AA6
F23	VSS47	VSS618	AA7
G8	VSS48	VSS619	AA8
G19	VSS49	VSS620	AA10
H1	VSS50	VSS621	AA11
H2	VSS51	VSS622	AA12
H4	VSS52	VSS623	AA13
H5	VSS53	VSS624	AA14
H6	VSS54	VSS625	AA15
H7	VSS55	VSS626	AA16
H9	VSS56	VSS627	Y18
H10	VSS57	VSS628	Y20
H11	VSS58	VSS629	AB1
H12	VSS59	VSS630	AB2
H13	VSS60	VSS631	AB3
H14	VSS61	VSS632	AB5
H15	VSS62	VSS633	AB6
H16	VSS63	VSS634	AB7
H17	VSS64	VSS635	AB8
H18	VSS65	VSS636	AB9
H20	VSS66	VSS637	AB10
H21	VSS67	VSS638	AB11
H22	VSS68	VSS639	AB12
H23	VSS69	VSS640	AB13
H25	VSS70	VSS641	AB14
H26	VSS71	VSS642	AB15
J3	VSS72	VSS643	AB16
J8	VSS73	VSS644	AB17
J9	VSS74	VSS645	AB18
J10	VSS75	VSS646	AB20
J11	VSS76	VSS647	AC3
J12	VSS77	VSS648	AC5
J13	VSS78	VSS649	AC6
J17	VSS79	VSS650	AC7
J21	VSS80	VSS651	AC8
K24	VSS81	VSS652	AC9
K5	VSS82	VSS653	AC10
K6	VSS83	VSS654	AC11
K8	VSS84	VSS655	AC12
K9	VSS85	VSS656	AC13
K11	VSS86	VSS657	AC14
K13	VSS87	VSS658	AC15
K15	VSS88	VSS659	AC16
K16	VSS89	VSS660	AC17
K18	VSS90	VSS661	AC18
K19	VSS91	VSS662	AC19
K20	VSS92	VSS663	AC20
K22	VSS93	VSS664	AC22
L5	VSS94	VSS665	AD1
L8	VSS95	VSS666	AD2
L10	VSS96	VSS667	AD24
L12	VSS97	VSS668	AD26
L13	VSS98	VSS669	AE2
L15	VSS99	VSS670	AE3
L19	VSS100	VSS671	AE5
L24	VSS101	VSS672	AE6
M5	VSS102	VSS673	AE7
M8	VSS103	VSS674	AE8
M10	VSS104	VSS675	AE9
M11	VSS105	VSS676	AE10
M13	VSS106	VSS677	AE11
M15	VSS107	VSS678	AE12
M19	VSS108	VSS679	AE13
M24	VSS109	VSS680	AE14
N5	VSS110	VSS681	AE15
N8	VSS111	VSS682	AE16
N10	VSS112	VSS683	AE17
N11	VSS113	VSS684	AE18
N13	VSS114	VSS685	AE19
N15	VSS115	VSS686	AE20
N19	VSS116	VSS687	AE21
N24	VSS117	VSS688	AE22
P5	VSS118	VSS689	AF2
P8	VSS119	VSS690	AF3
P10	VSS120	VSS691	AF5
P11	VSS121	VSS692	AF6
P13	VSS122	VSS693	AF7
P15	VSS123	VSS694	AF8
P19	VSS124	VSS695	AF9
P24	VSS125	VSS696	AF10
R5	VSS126	VSS697	AF11
R8	VSS127	VSS698	AF12
R10	VSS128	VSS699	AF13
R11	VSS129	VSS700	AF14
R13	VSS130	VSS701	AF15
R15	VSS131	VSS702	AF16
R19	VSS132	VSS703	AF17
R24	VSS133	VSS704	AF18
T5	VSS134	VSS705	AF19
T8	VSS135	VSS706	AF20
T10	VSS136	VSS707	AF21
T11	VSS137	VSS708	AF22
T13	VSS138	VSS709	AG1
T15	VSS139	VSS710	AG2
T19	VSS140	VSS711	AG3
T24	VSS141	VSS712	AG4
U5	VSS142	VSS713	AG5
U8	VSS143	VSS714	AG6
U10	VSS144	VSS715	AG7
U11	VSS145	VSS716	AG8
U13	VSS146	VSS717	AG9
U15	VSS147	VSS718	AG10
U19	VSS148	VSS719	AG11
U24	VSS149	VSS720	AG12
V5	VSS150	VSS721	AG13
V8	VSS151	VSS722	AG14
V10	VSS152	VSS723	AG15
V11	VSS153	VSS724	AG16
V13	VSS154	VSS725	AG17
V15	VSS155	VSS726	AG18
V19	VSS156	VSS727	AG19
V24	VSS157	VSS728	AG20
W5	VSS158	VSS729	AG21
W8	VSS159	VSS730	AG22
W10	VSS160	VSS731	AH3
W11	VSS161	VSS732	AH5
W12	VSS162	VSS733	AH6
Y5	VSS163	VSS734	AH7
Y8	VSS164	VSS735	AH8
Y10	VSS165	VSS736	AH9
Y11	VSS166	VSS737	AH10
Y13	VSS167	VSS738	AH11
Y15	VSS168	VSS739	AH12
Y19	VSS169	VSS740	AH13
Y24	VSS170	VSS741	AH14
AA5	VSS171	VSS742	AH15
AA8	VSS172	VSS743	AH16
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AA13	VSS175	VSS746	AH19
AA15	VSS176	VSS747	AH20
AA18		VSS748	AH21
AB19		VSS749	AH22
AB21		VSS750	AH23
AB24		VSS751	AH24
AC23		VSS752	AH25
AD25		VSS753	AH26
AE26		VSS754	AJ1
AF23		VSS755	AJ2
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AH23		VSS760	AJ7
AH26		VSS761	AJ8
AJ25		VSS762	AJ9
AK1		VSS763	AJ10
AK2		VSS764	AJ11
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AK4		VSS766	AJ13
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AK7		VSS769	AJ16
AK8		VSS770	AJ17
AK9		VSS771	AJ18
AK10		VSS772	AJ19
AK11		VSS773	AJ20
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AK13		VSS775	AJ22
AK14		VSS776	AJ23
AK15			AJ24
AK16			AK26
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AK18			
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AK20			
AK21			
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AK23			
AK24			
AK25			
AK26			

PEX_PERST#	AC1	VDD18_1	VDD18A_1
PEX_NT_PERST#	AD25	VDD18_2	VDD18A_2
NC5	F3	VDD18_3	VDD18A_3
SHPC_INT#	B3	VDD18_4	VDD18A_4
PEX_INTA#	D1	VDD18_5	VDD18A_5
FATAL_ERR#	C24	VDD18_6	VDD18A_6
		VDD18_7	
		VDD18_8	
		VDD18_9	
		VDD18_10	
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		VDD18_15	
		VDD18_16	
		VDD18_17	
		VDD18_18	
		VDD18_19	
		VDD18_20	

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		VDD09_2	VDD09A_2
		VDD09_3	VDD09A_3
		VDD09_4	VDD09A_4
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			VDD09A_55
			VDD09A_56

SYS18 — C262 0.01u · C241 0.1u · C263 0.01u · C242 0.1u · C264 0.01u · C243 0.1u · C265 0.01u · C244 0.1u · C266 0.01u · C245 0.1u — GND

SYS18 — C267 0.01u · C235 0.1u · C268 0.01u · C236 0.1u · C269 0.01u · C237 0.1u · C270 0.01u · C238 0.1u · C271 0.01u · C239 0.1u · C240 4.7u — GND

PEX1P8VA — C272 0.01u · C246 0.1u · C273 0.01u · C247 0.1u · C274 0.01u · C248 0.1u · C249 4.7u — GND

PEX0P9V — C334 0.01u · C332 0.1u · C335 0.01u · C333 0.1u · C321 0.01u · C309 0.1u · C322 0.01u · C310 0.1u · C323 0.01u · C311 0.1u · C324 0.01u · C312 0.1u · C325 0.01u · C313 0.1u · C330 0.01u · C315 0.1u · C331 0.01u · C316 0.1u · C326 0.01u · C317 0.1u · C327 0.01u · C318 0.1u · C328 0.01u · C319 0.1u · C329 0.01u · C320 0.1u · C314 4.7u — GND

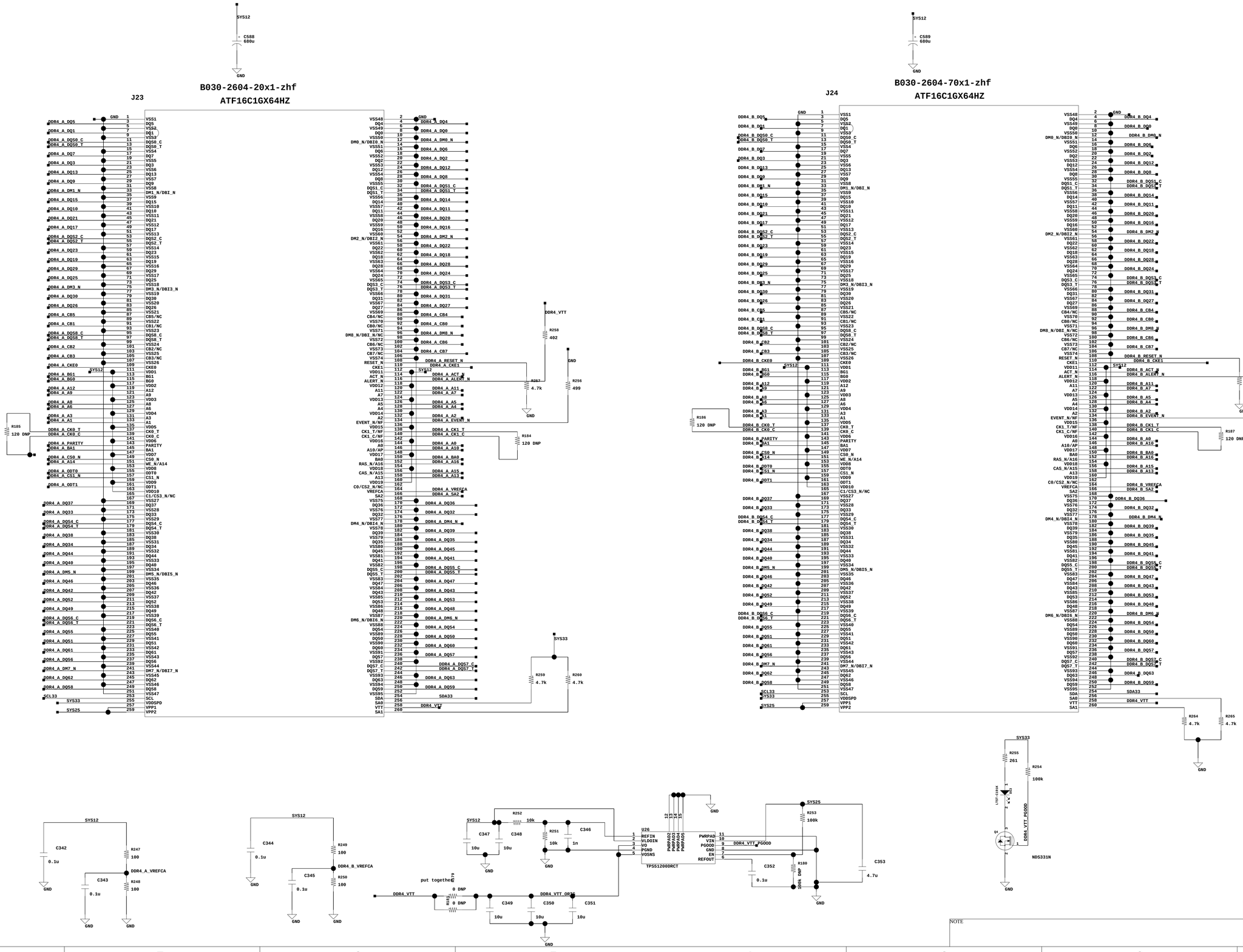
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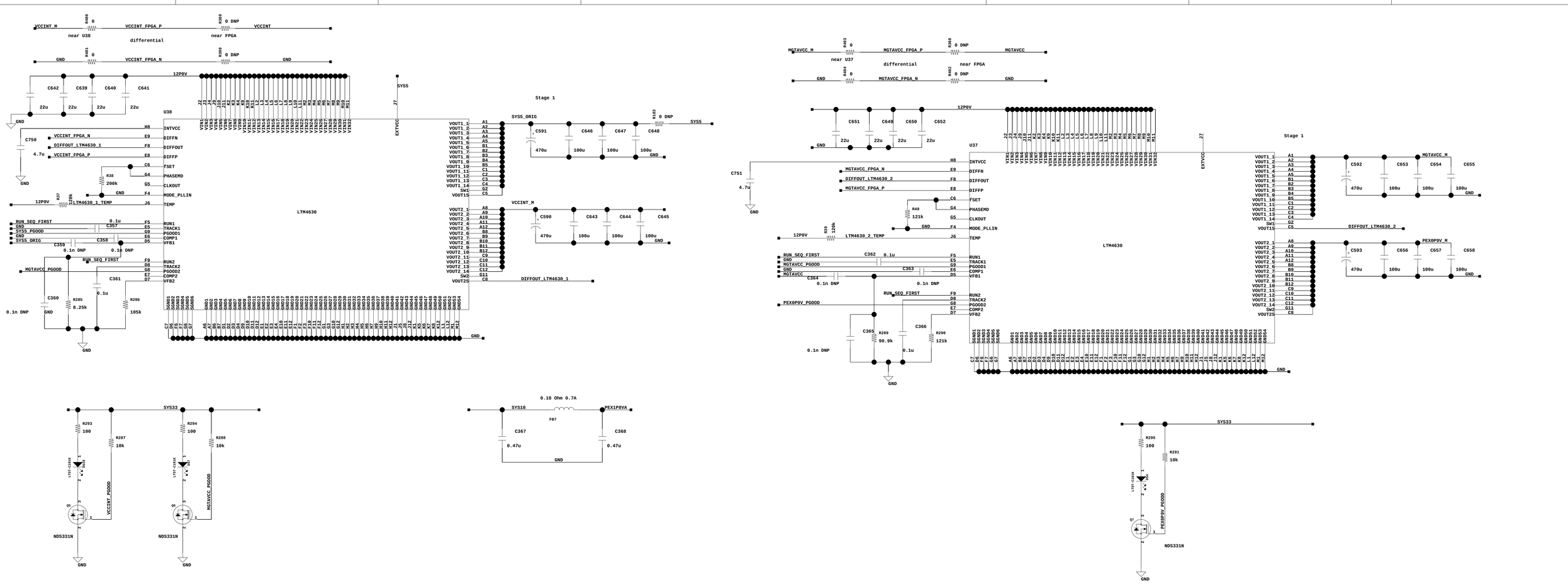
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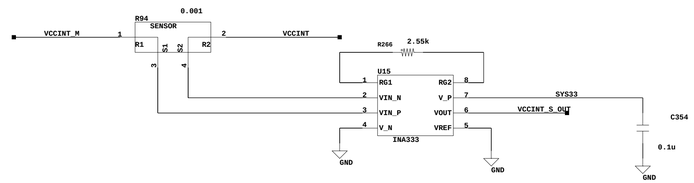
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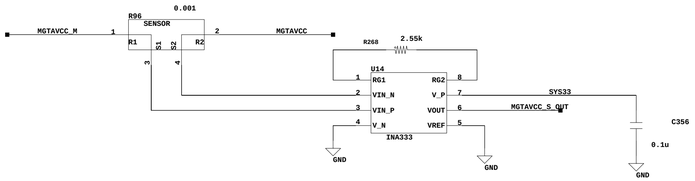
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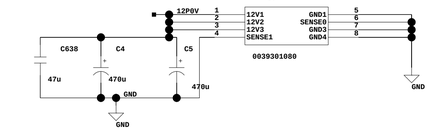
COMPANY	BROOKHAVEN NATIONAL LABORATORY
TITLE	PEX_PWR_CTRL
SIZE	D
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OF	
N	
DRAWN	KAI CHEN
DATE	24/03/2017:10:09

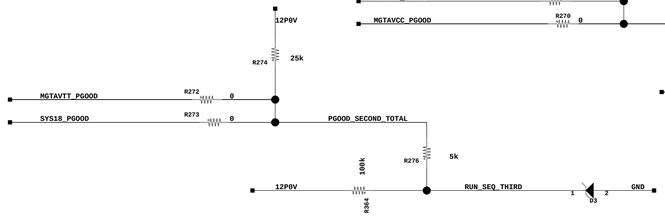

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J23
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C589
680u
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J24
DDR4_VTT
R258
402
R257
4.7k
R256
499
R259
4.7k
R260
4.7k
SYS33
R263
402
R262
4.7k
R261
499
R264
4.7k
R265
4.7k
R185
120 DNP
R184
120 DNP
R186
120 DNP
R187
120 DNP
SYS12
C342
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R247
100
DDR4_A_VREFCA
C343
0.1u
R248
100
SYS12
C344
0.1u
R249
100
DDR4_B_VREFCA
C345
0.1u
R250
100
SYS12
R252
10k
C347
10u
C348
10u
R251
10k
C346
1n
U26
REFIN
VLDOIN
VO
PGND
VDSNS
PWRPAD
VIN
PGOOD
GND
EN
REFOUT
DDR4_VTT_PGOOD
SYS25
R253
100k
C352
0.1u
R180
100K DNP
C353
4.7u
put together
R182
0 DNP
R183
0 DNP
DDR4_VTT
DDR4_VTT_ORG
C349
10u
C350
10u
C351
10u
SYS33
R255
261
R254
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Q4
NDS331N
DDR4_VTT_PGOOD
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BROOKHAVEN NATIONAL LABORATORY
TITLE
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DATE
03/08/2016:23:34

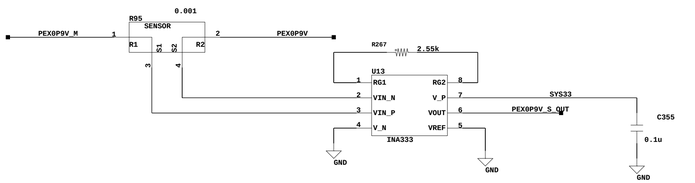


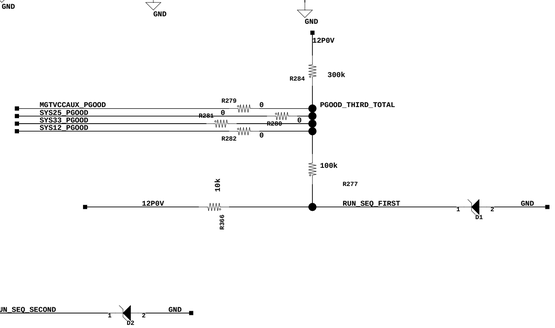








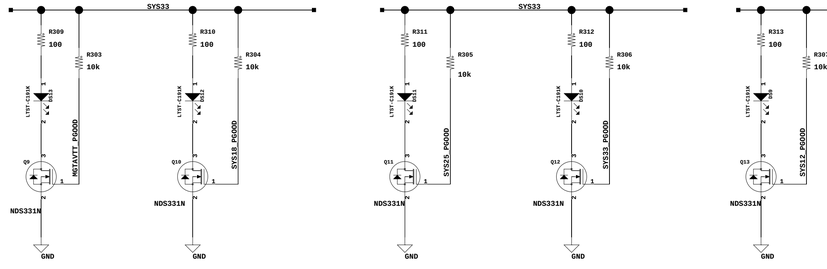


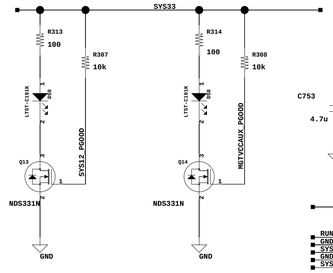


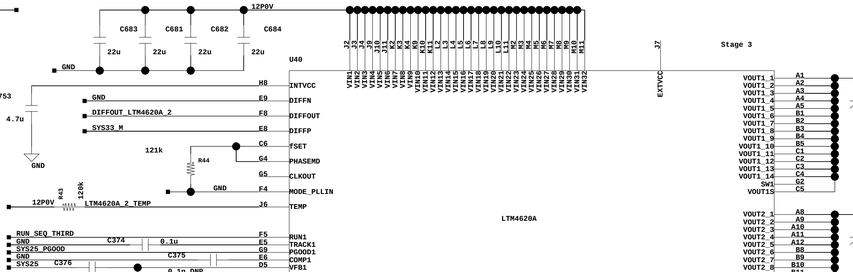


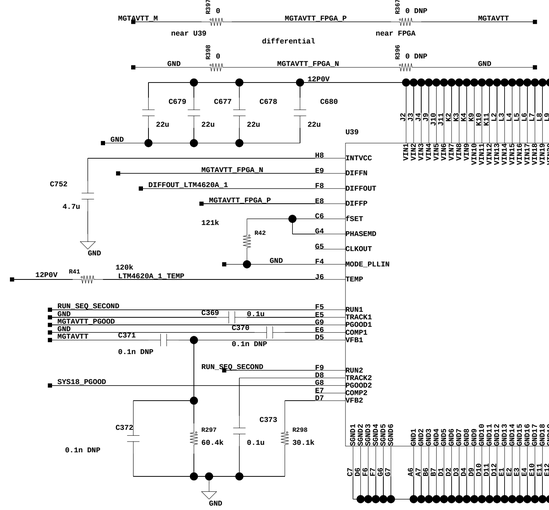
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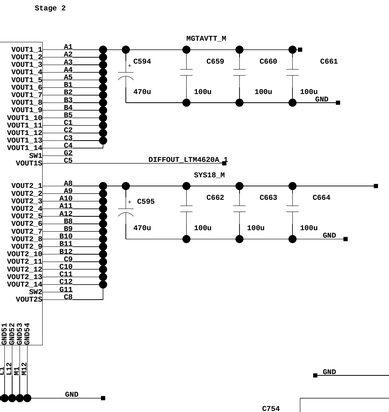
COMPANY	BROOKHAVEN NATIONAL LABORATORY		
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DRAWN	KAI CHEN	DATE	01/08/2016:16:44

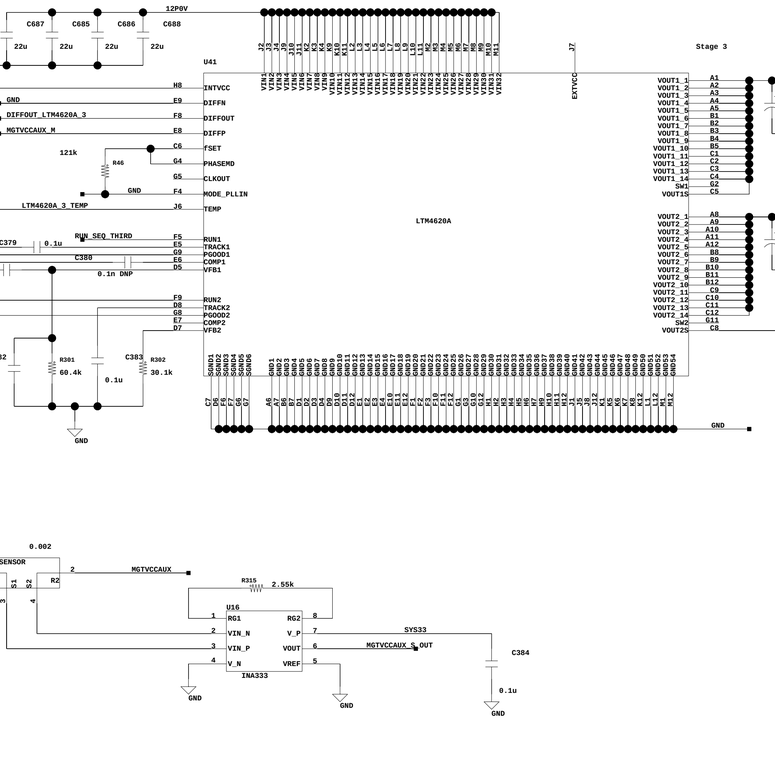


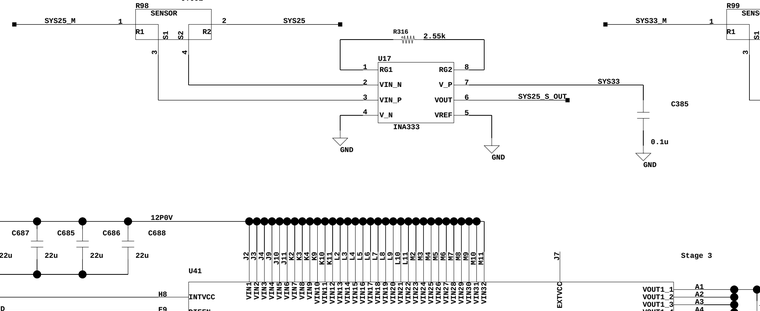


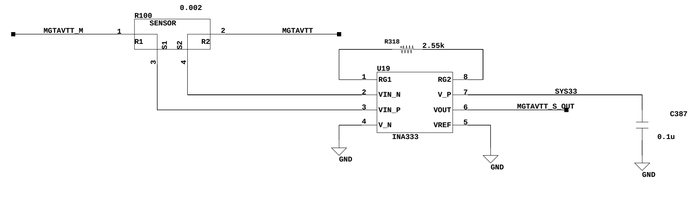


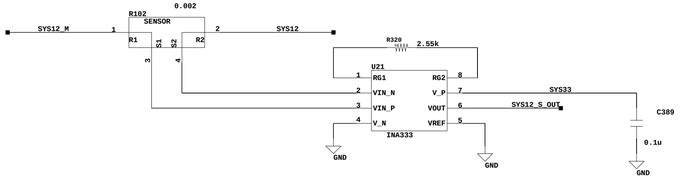






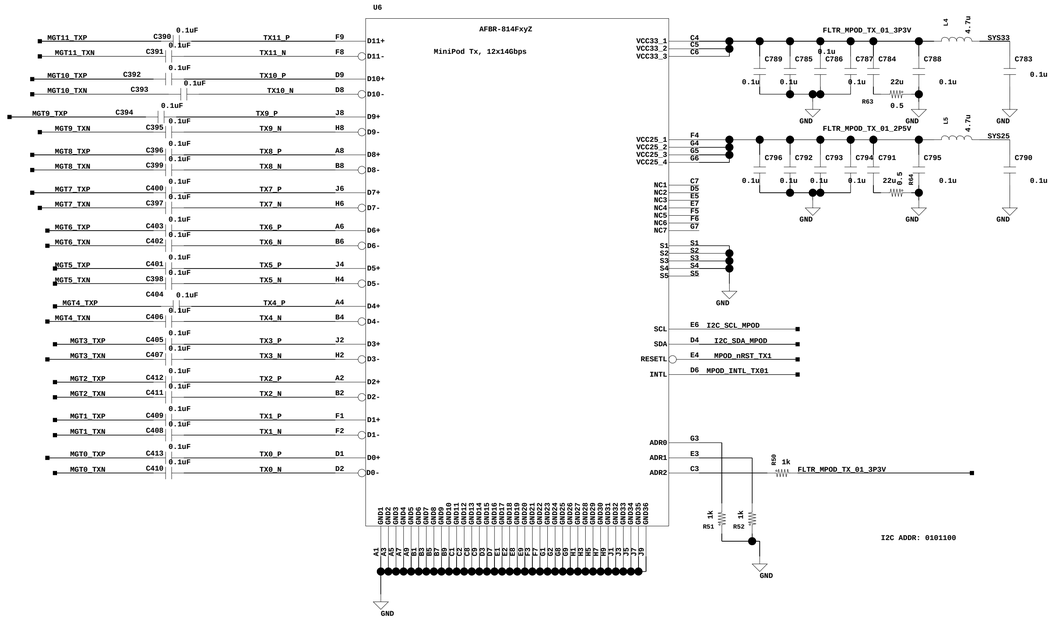


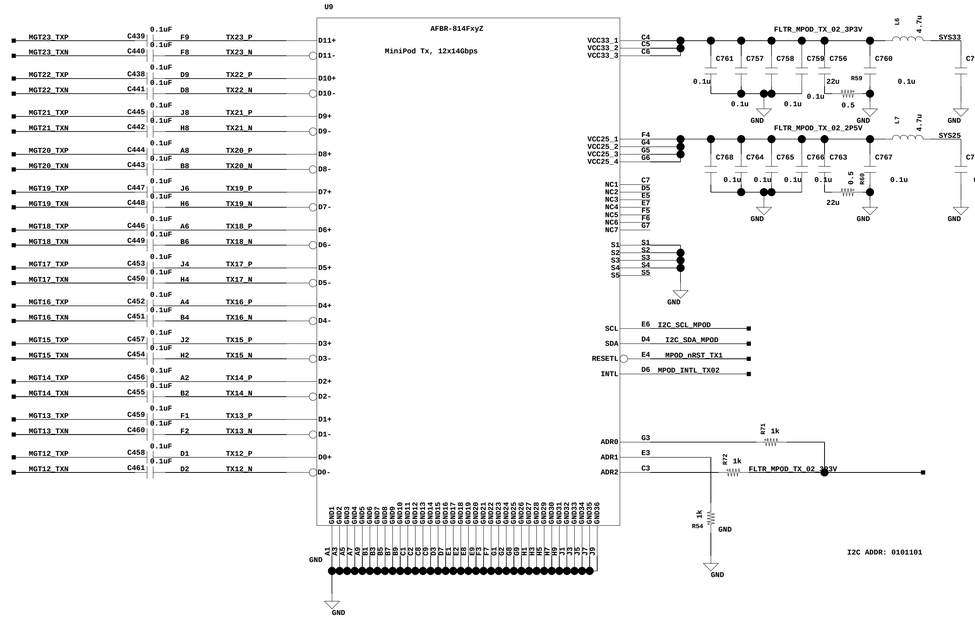


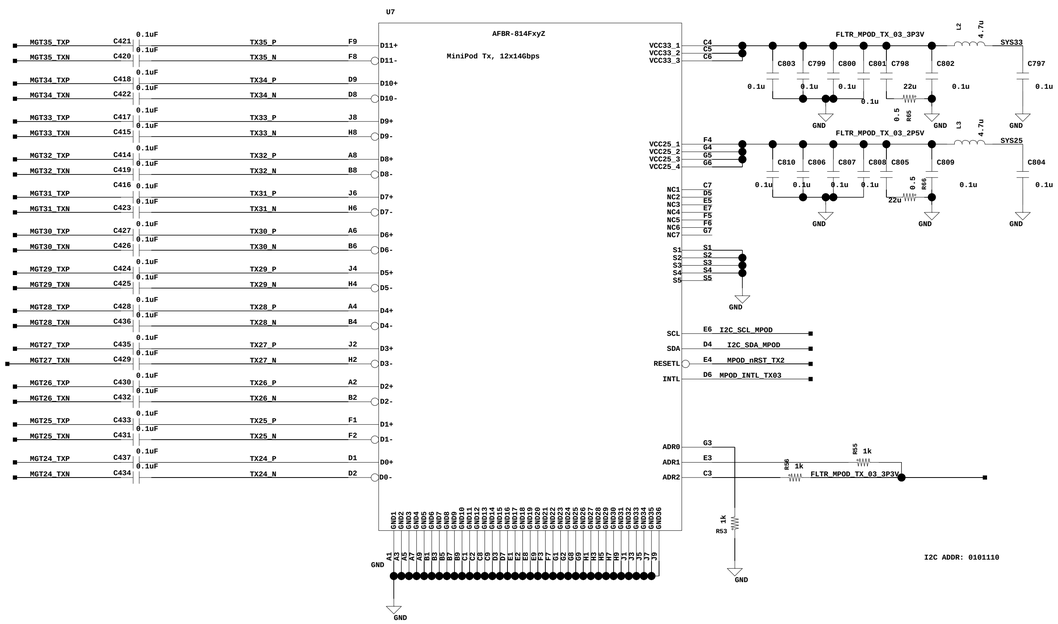


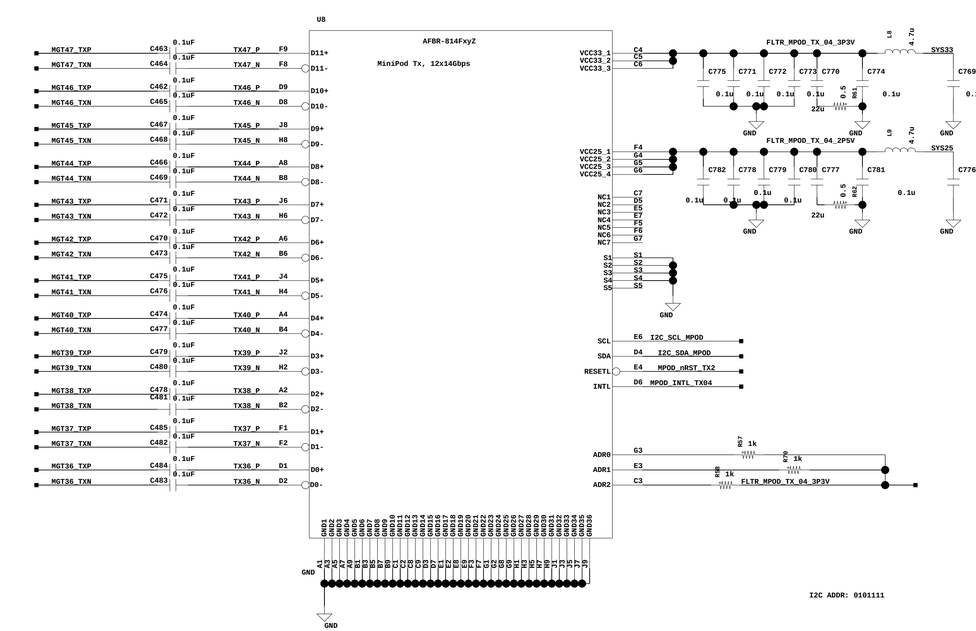
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COMPANY	BROOKHAVEN NATIONAL LABORATORY		
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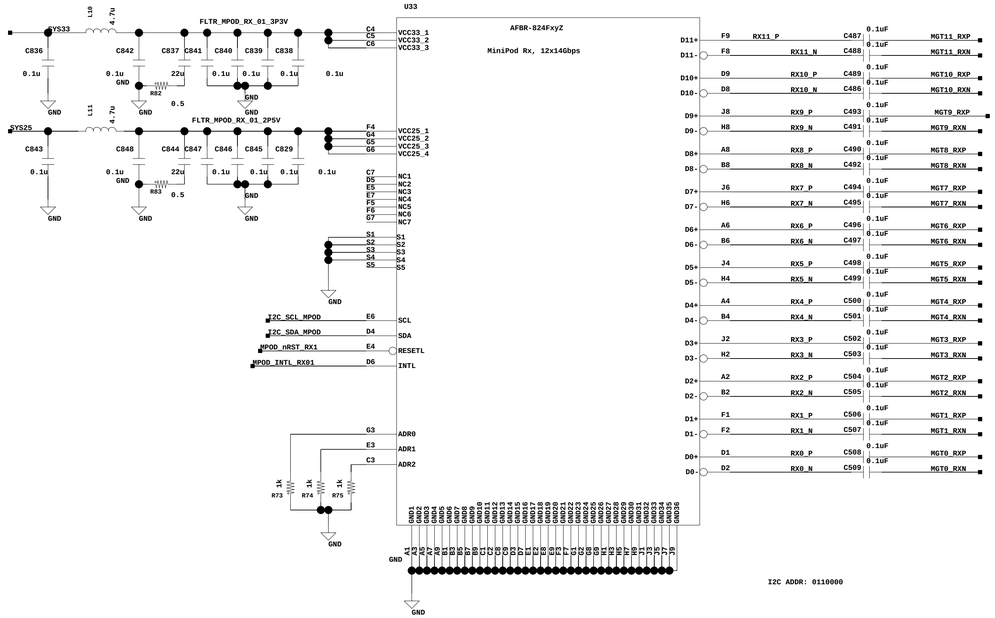


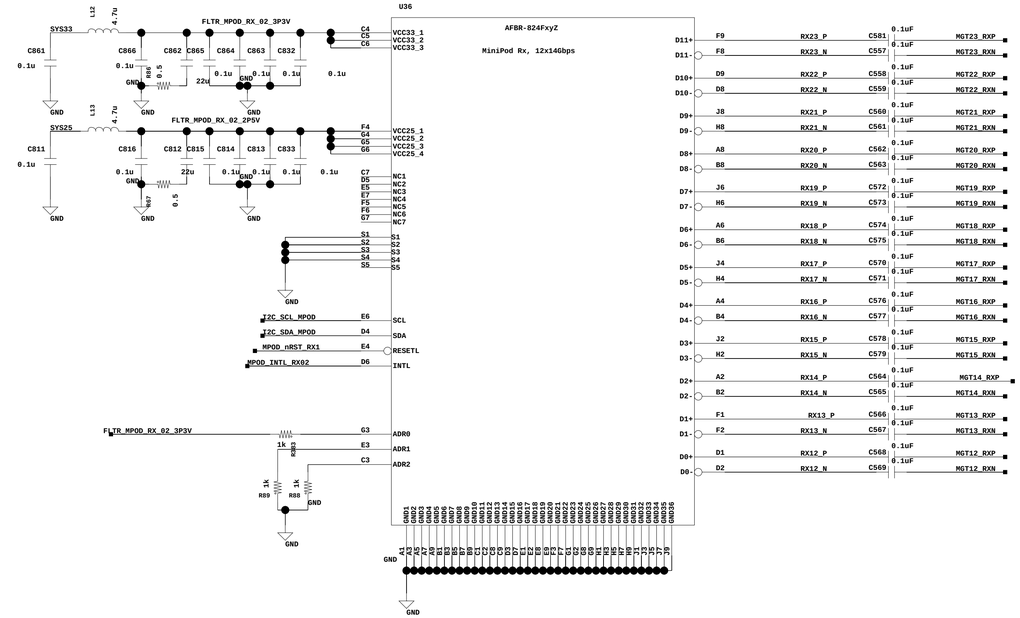


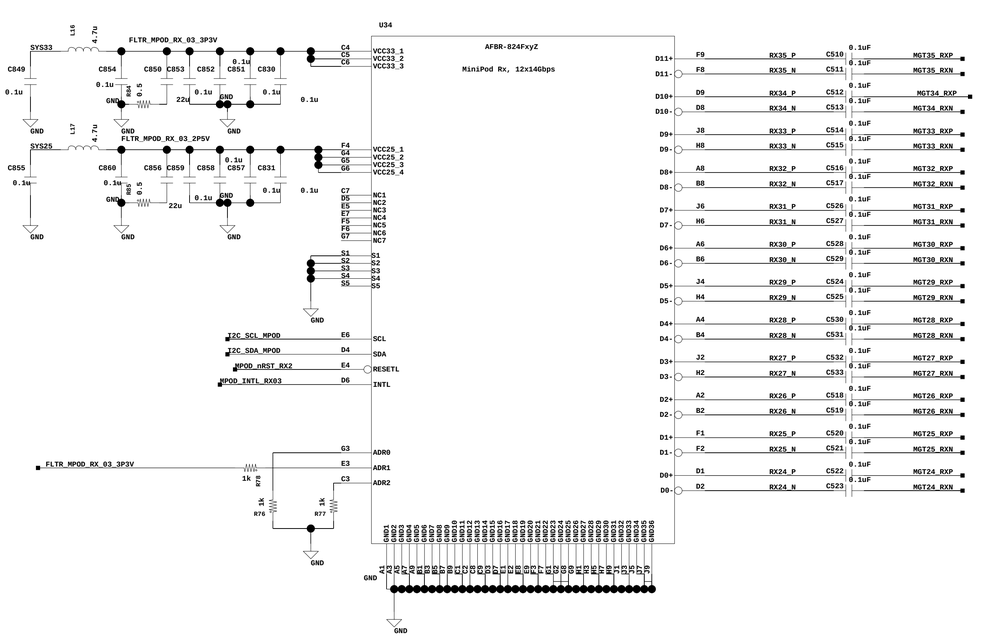


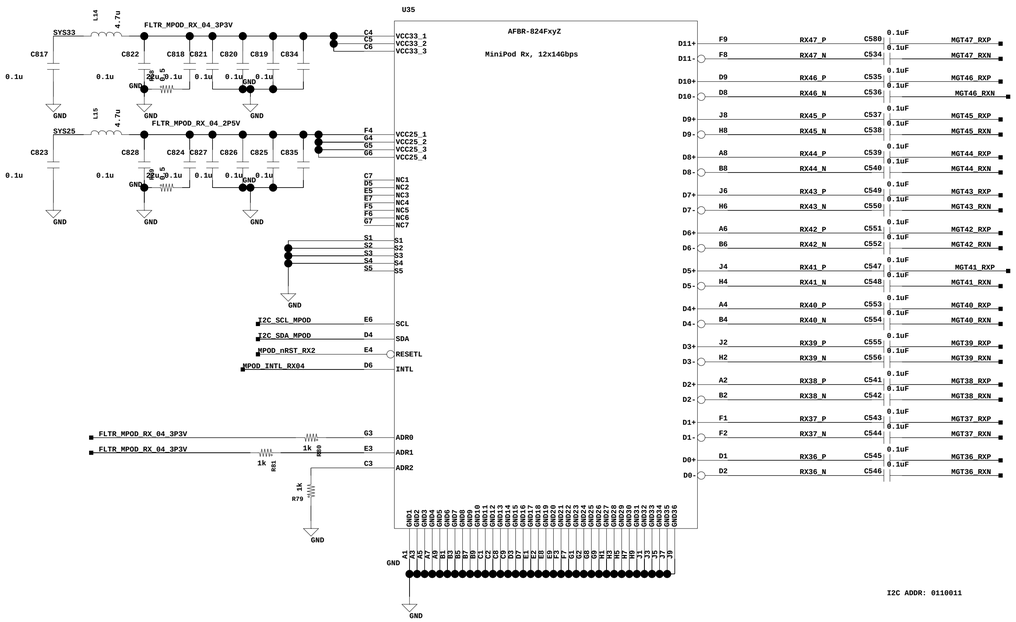
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COMPANY	BROOKHAVEN NATIONAL LABORATORY
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DRAWN KAI CHEN	DATE 13/05/2016 15:01







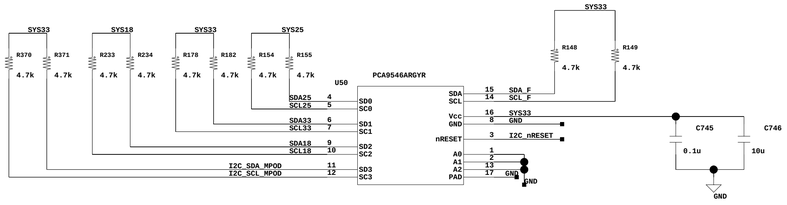


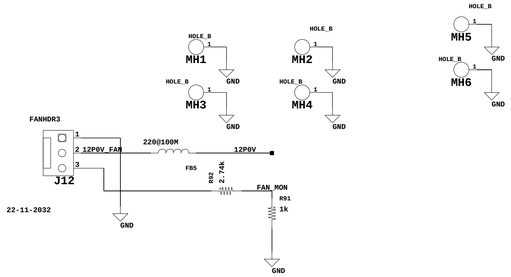
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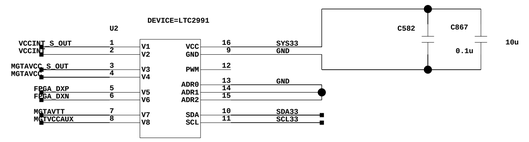
COMPANY
BROOKHAVEN NATIONAL LABORATORY

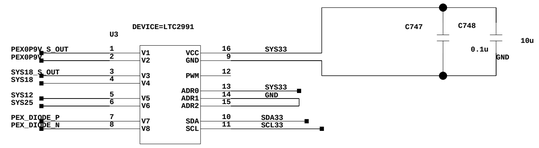
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COMPANY
BROOKHAVEN NATIONAL LABORATORY

TITLE

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