ALICE
Internal Note

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ALICE COMMON READ-OUT UNIT
ALICE-CRU

CRU User Requirements

Issue:	Draft
Revision:	v0.8
Reference:	CRU
Created:	30/11/2015
Last modified:	28/11/2016

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Abstract

This document enumerates the ALICE CRU (Common Read-out Unit) user requirements.

Document Status Sheet

1. Document Title: CRU User Requirements			
2. Document Reference Number: CRU			
3. Issue	**4. Revision**	**5. Date**	**6. Reason for change**
Working Draft	v0.3	22 January 2016	Initial thinking
Working Draft	v0.4	01 March 2016	Evolution of the thinking
Working Draft	v0.5	09 March 2016	Chapters 3.1, 3.3, and 3.4 updated
Working Draft	v0.6	11 March 2016	Chapters 3.1, 3.2, 3.5, 3.6, and 3.7 updated
Working Draft	v0.7	14 June 2016	Chapters 3.10 added; 3.11, 6, and 7 updated
Working Draft	v0.8	28 October 2016	Chapter 3.x updated

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1 Introduction

To cope with the increasing luminosity of the CERN Large Hadron Collider (LHC), the ALICE experiment is planning a major upgrade of the detectors during the Long Shutdown-2 (LS2) period, which is at present foreseen to start in mid-2018. The increased luminosity will significantly enhance the physics reach of the experiment. The luminosities for Pb-Pb collisions will increase from $1x10^{27}$ $cm^{-2}s^{-1}$ to $6x10^{27}$ $cm^{-2}s^{-1}$ corresponding to collision rates of 50 kHz. The upgrade strategy is based on collecting greater than 10 nb^{-1} of Pb-Pb ion collisions. ALICE will also collect 6 pb^{-1} of p-p collisions and 50 nb^{-1} of p-Pb collisions, both at a leveled collision rate of 200 KHz. Due to this increased interaction rate there will be manifold increase in the traffic of experimental data, hence the need for increased readout rate.

The maximum readout rate of the present ALICE detector is 500 Hz of Pb-Pb events but the overall goal is to readout 50 kHz Pb-Pb collisions and 200 kHz p-p and p-Pb collisions. Hence the detectors and electronics needed to be upgraded to handle the higher high rates. To tackle this requirement, a new approach based on Common Readout Unit (CRU) is being developed for data concentration and multiplexing

2 Upgrade Architecture

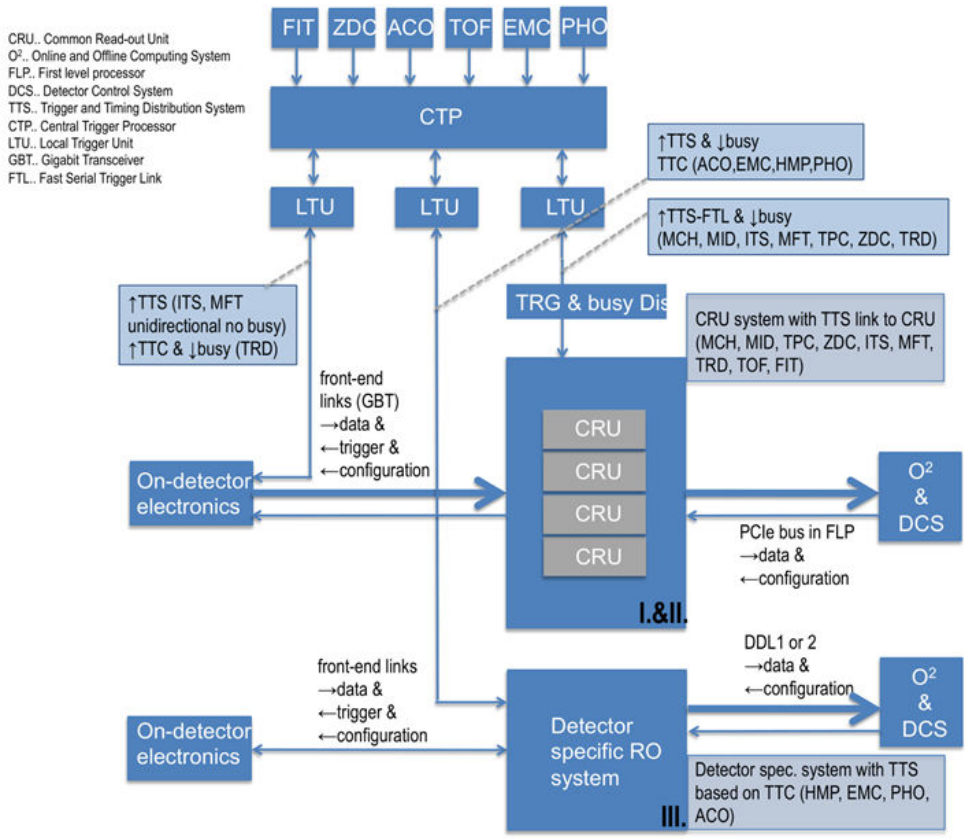

Figure 1: Upgrade Architecture

Figure 1 shows the ALICE upgrade architecture for LS2. The detectors can be grouped into three groups based on CRU usage:

I. The CRU delivers the LHC clock, the trigger information, and participates in the data taking.

II. The CRU only participates in the data taking.

III. The detector in this group will not use the CRU in any way.

3 Requirements from the Detectors

The following ALICE detectors plan to use CRU after the upgrade of the ALICE their read-out and trigger system:

ACO	ALICE Cosmic Ray Detector
FIT	Fast Interaction Triggr detector (of ALICE)
ITS	Inner Tracking System detectors (of ALICE)
MCH	Muon Chambre detector (of ALICE)
MFT	Muon Forward Tracking (of ALICE)
MID	Muon Identifier detector (of ALICE)
TOF	Time of Flight detector (of ALICE)
TPC	Time Projection Chambre detector (of ALICE)
TRD	Transition Radiation Detector (of ALICE)
ZDC	Zero Degree Calorimeter detector (of ALICE)

In the following chapters the detector requirements for the CRU functionality are specified.

3.1 TPC

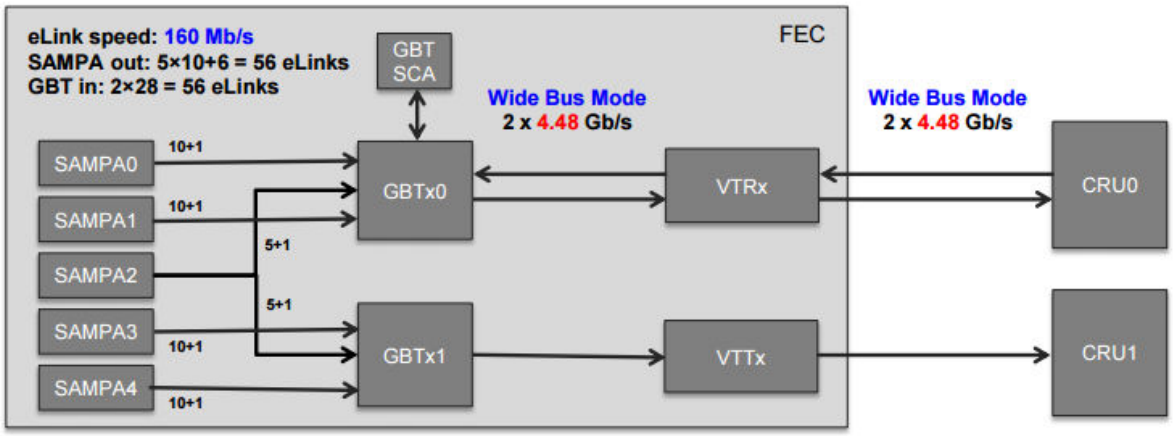

Figure 2: TPC Front-End Card Block Diagram

The TPC front-end (FE) card will contain: 5 SAMPA ASIC, 2 GBTx ASIC, 1 GBT-SCA, 1 VTRx, 1 VTTx (see Figure 2). The requirements can be summarized in the following points:

1. The CRU shall support 1 GBT downlink (CRU->FE direction) in GBT mode (80 bit payload) and 2 GBT uplinks (FE->CRU direction) in Wide Bus mode (112 bit payload) per front-end card.
2. A single CRU shall support at least 20 GBT downlinks and 20 GBT uplinks.
3. The CRU shall provide the LHC clock for the FE over the GBT downlink. The recovered LHC clock output from the GBTx ASIC must have a constant and deterministic phase relation to the original LHC clock between each GBT links, CRU units, power-on cycles and firmware updates. The maximum acceptable LHC jitter is 300 ps (RMS) and the clock skew should not exceed 1 ns (peak-to-peak).
4. The CRU shall provide the readout control for the FE over the GBT downlink where the readout control bits are based on the raw trigger information bits received from the LTU. The readout control bits must be delivered with constant latency.
5. The CRU's GBT stage shall accept the incoming GBT link working in the Wide Bus mode and pass forward the extracted 112 bit payload with additional status information to the TPC specific User Logic.
6. The CRU's PCIe DMA stage shall accept the outgoing traffic from the TPC specific User Logic and deliver the TPC data to the memory of FLP servers.
7. The CRU shall provide access to the GBTx ASIC registers and to the GBT-SCA features for TPC specific Linux applications.
8. The CRU shall support the TPC Safety Module response time requirements.

3.2 MCH

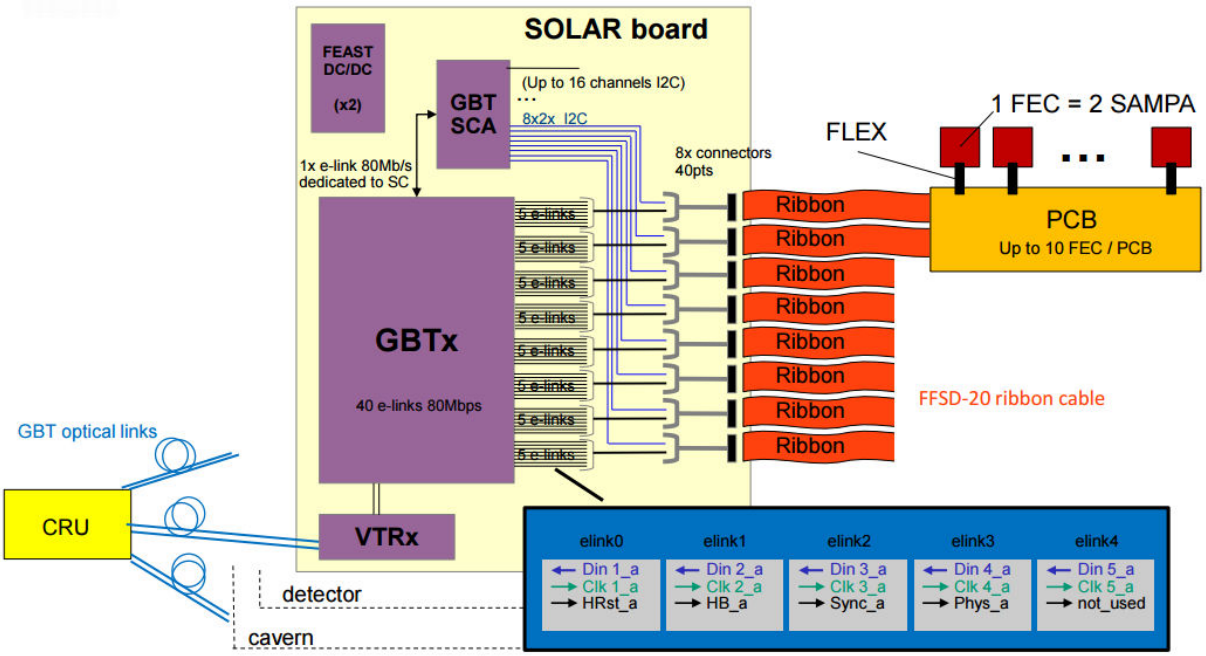

Figure 3: MCH SOLAR Front-End Card Block Diagram

The MCH front-end card will contain: 1 GBTx ASIC, 1 GBT-SCA, 1 VTRx (see Figure 4). The CRU shall support the following features:

1. LHC clock distribution over the GBT downlink with constant and deterministic phase between GBT links, CRU units, power cycles and firmware updates. The acceptable LHC clock parameters: the jitter should be better than 1 ns (peak-to-peak) and the skew also should be better than 1 ns (peak-to-peak).
2. Readout control distribution over the GBT downlink with constant latency. The trigger latency should be less than 5 us.
3. Accepting the incoming SAMPA serial packages and passing them forward to the MCH specific User Logic firmware portion.
4. The CRU's PCIe DMA stage shall accept the outgoing traffic from the MCH specific User Logic and deliver the MCH data to the memory of the FLP servers.
5. The CRU shall provide access to the GBTx ASIC registers and to the GBT-SCA features for MCH specific Linux applications.

3.3 MID

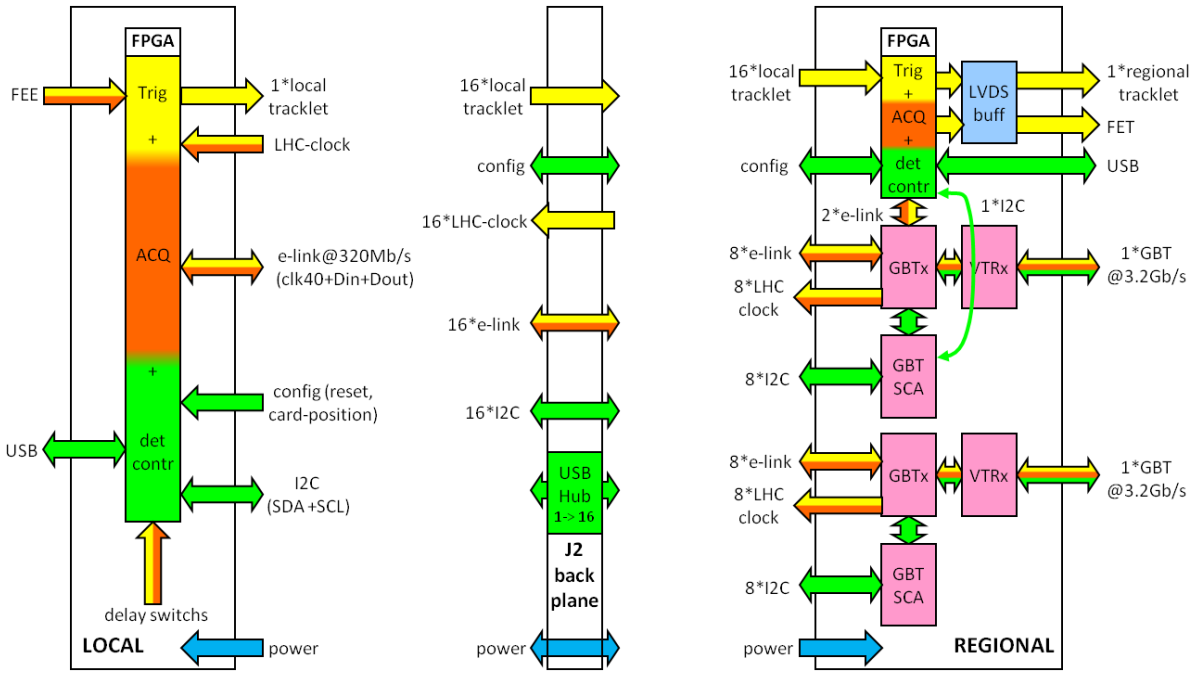

Figure 4: MID Front-End Card Block Diagram

The MID Regional card will contain: 2 GBTx ASIC, 2 GBT-SCA, 2 VTRx (see Figure 4). The CRU shall support the following features:

1. LHC clock distribution over the GBT downlink with constant and deterministic phase between GBT links, CRU units, power cycles and firmware updates. The maximum acceptable LHC clock jitter and skew should be of order of ~100 ps (the exact numbers are not yet specified).
2. Readout control distribution over the GBT downlink with constant latency.
3. Accepting the incoming MID front-end card specific detector data and pass forward the MID specific User Logic firmware portion.
4. The CRU's PCIe DMA stage shall accept the outgoing traffic from the MID specific User Logic and deliver the MID data to the memory of the FLP servers.
5. The CRU shall provide access to the GBTx ASIC registers and to the GBT-SCA features for MID specific Linux applications.

3.4 TOF

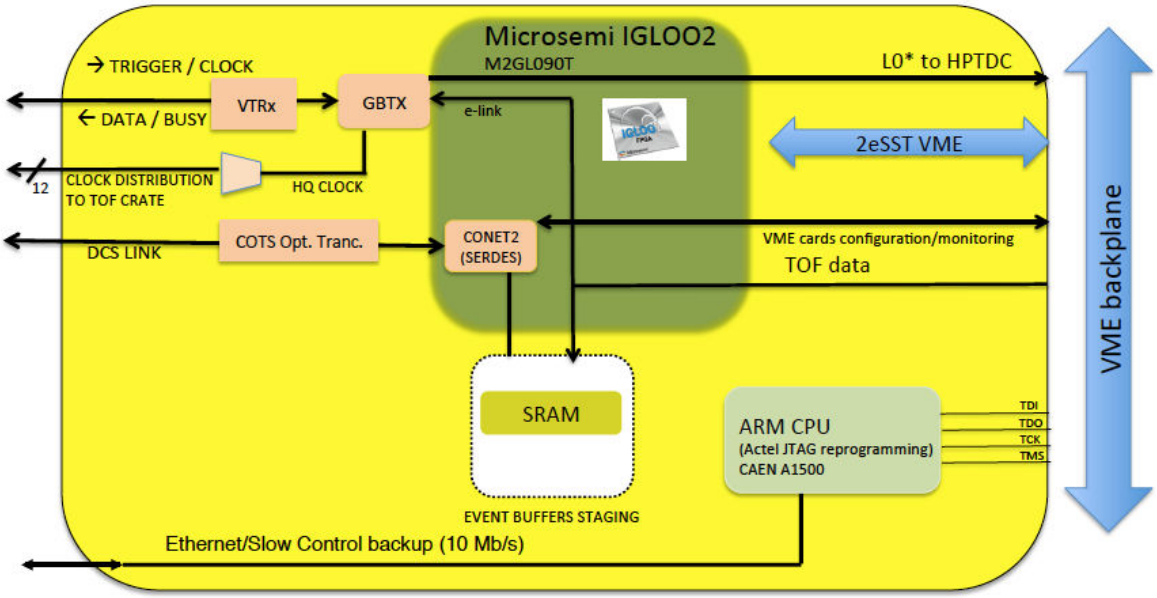

Figure 5: TOF DRM2 Front-End Card Block Diagram

The TOF front-end card will contain: 1 GBTx ASIC, 1 VTRx (see Figure 5). The CRU shall support the following features:

1. LHC clock distribution over the GBT downlink with constant and deterministic phase between GBT links, CRU units, power cycles and firmware updates. The maximum acceptable LHC clock skew is 100 ps (peak-to-peak)
2. The current LHC clock jitter is 17 ps. For Run3 the maximum acceptable LHC clock jitter is 15 ps (RMS) at the output of the GBTx.
3. Trigger information distribution with constant latency over the GBT downlink. The maximum acceptable trigger delay is 15 us.
4. Accepting the incoming CDH/SDH packages with TOF detector data payload and delivering them to the FLP server's memory.
5. The BUSY signal will be embedded into the incoming TOF packages and it must be extracted by the CRU and delivered to the trigger system (LTU).

Additional requirements:

6. The current LHC clock jitter is 17 ps. The CRU shall be able to achieve this value.
7. Even in case of absence of signal from the LTU the CRU should be able to self-generate random triggers at fixed and programmable rate encoding the GBTx information. This feature will be particularly important for lab test, debug purposes or - simply - to have the possibility to have standalone runs if the CTP/LTU systems are not available.
8. The CRU in case of absence of clock from the LTU should have a local backup clock at 40 MHz distributed in its GBTx outputs. The switch from one clock to another should be carefully controlled and it shall always be possible to know which clock is distributed (local or coming from LTU).

9. When the TOF front-end will send a BUSY condition this should be propagated up to the CTP via some fan-in, so the CTP will see just that a whole detector is busy. But it will be fundamental for the detector to have the possibility to easily read out which are the specific links setting the busy.
10. In the case of communication problems with one or multiple GBT links it is important to have the possibility to detect the problematic links.
11. Supporting multiple events per CDH/SDH package. To optimize readout time it may require sending not single events but a package of 10 events all together.

3.5 ITS

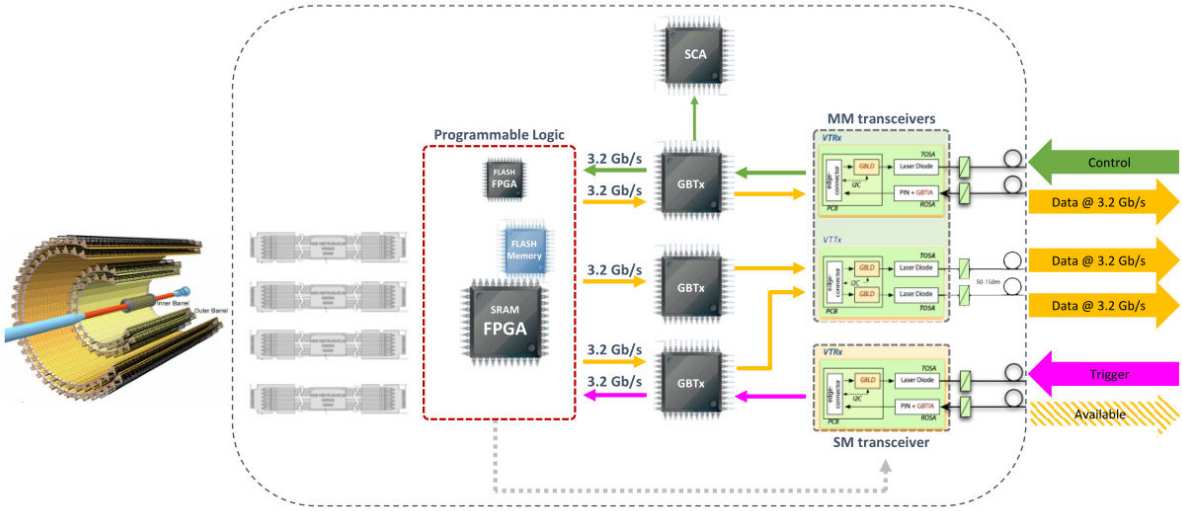

Figure 6: ITS Front-End Card Block Diagram

The ITS front-end card will contain: 3 GBTx ASIC, 1 GBT-SCA, 2 VTRx, 1 VTTx (see Figure 6). The requirements can be summarized in the following points:

1. The CRU shall support 1 GBT downlink (CRU->FE direction) in GBT mode (80 bit payload) and 3 GBT uplinks (FE->CRU direction) in GBT mode (80 bit payload) per front-end card.
2. LHC clock distribution over the GBT downlink with constant and deterministic phase between GBT links, CRU units, power cycles and firmware updates. The LHC clock skew should be less than ¼ clock period (~6 ns). The LHC clock jitter is not critical; it should be good enough to feed the clock regenerator PLL.
3. The ITS will utilize the GBT downlink for packet based communication to deliver large amount of configuration data to the front-end card. This packet based slow control must be supported in both direction between the front-end card and the CRU.
4. The CRU shall accept the incoming CDH/SDH packages with the ITS detector data payload and deliver them either to the FLP server's memory or to the ITS specific user logic for further processing.
5. The ITS require some kind of broadcast ability which allows coordination between the front-end cards. This can be a specific trigger bit sent by the LTU or a specific packet sent by the CRU. The advisable implementation depends on the timing requirements.

6. The CRU shall provide access to the GBTx ASIC registers and to the GBT-SCA features for ITS specific Linux applications.

3.6 MFT

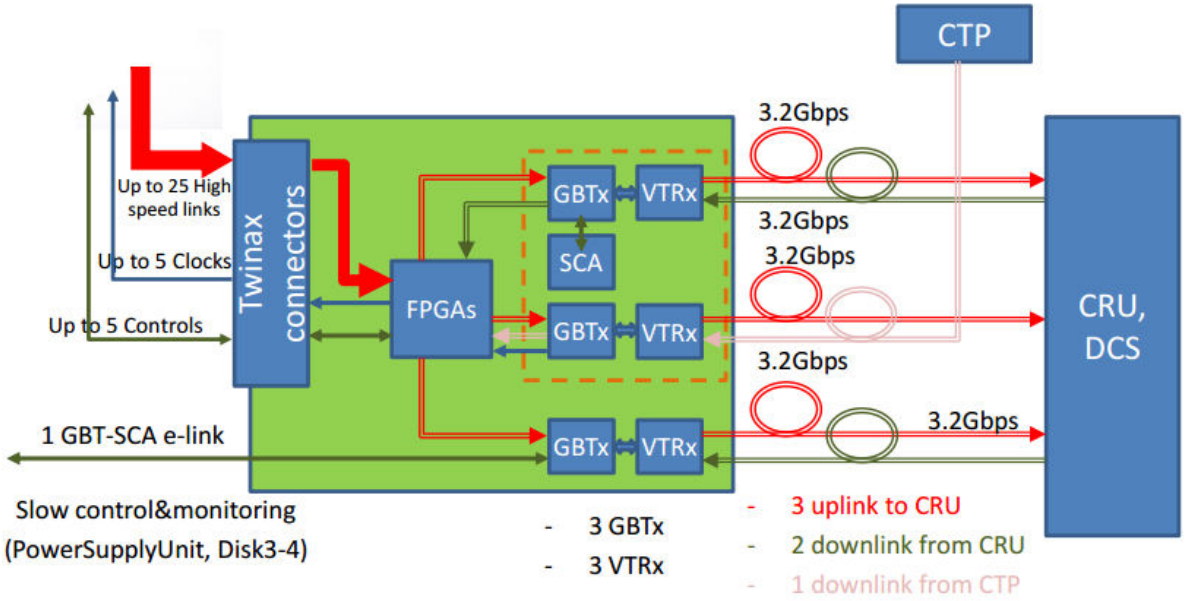

Figure 7: MFT Front-End Card Block Diagram

The MFT front-end card will contain: 3 GBTx ASIC, 1 GBT-SCA, 2 VTRx, 1 VTTx (see Figure 6). The requirements can be summarized in the following points:

1. The CRU shall support 2 GBT downlink (CRU->FE direction) in GBT mode (80 bit payload) and 3 GBT uplinks (FE->CRU direction) in GBT mode (80 bit payload) per front-end card.
2. The CRU shall support at least 36 GBT Links.
3. LHC clock distribution over the GBT downlink with constant and deterministic phase between GBT links, CRU units, power cycles and firmware updates. The LHC clock skew should be less than ¼ clock period (~6 ns). The LHC clock jitter is not critical; it should be good enough to feed the clock regenerator PLL.
4. The MFT will utilize the GBT downlink for packed based communication to deliver large amount of configuration data to the front-end card. This packet based slow control must be supported in both direction between the front-end card and the CRU.
5. The CRU shall accept the incoming CDH/SDH packages with the MFT detector data payload and deliver them to the FLP server's memory.
6. The CRU shall provide access to the GBTx ASIC registers and to the GBT-SCA features for MFT specific Linux applications.

3.7 TRD

The TRD front-end card will communicate with the CRU over existing 2.5 Gb/s, 8B/10B encoded, unidirectional optical links using a TRD specific protocol. The CRU shall support the following features:

1. Compatibility with the optical transceivers used by the TRD detector. But since on the CRU side the only option is the Avago MiniPOD then this must be solved on the TRD side.
2. The CRU firmware shall be modular enough to allow replacing the GBT protocol in the input stage with the TRD specific custom protocol.
3. The CRU firmware shall support a TRD specific User Logic for data processing.
4. The PCIe stage shall accept the processed TRD data and deliver it to the FLP server memory.
5. Ability to buffer up to 1.5 MB (12 Mbit) detector data.
6. Accept at least 30 input links per CRU to reach the 60 input links per FLP which is required to handle one TRD supermodule.

3.8 FIT

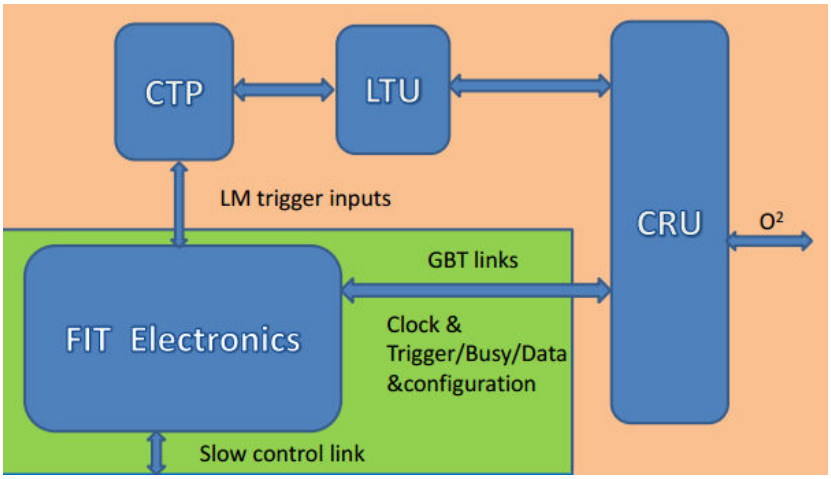

Figure 8: FIT System Diagram

The CRU shall support the following features:

1. LHC clock distribution over the GBT downlink with constant and deterministic phase between GBT links, CRU units, power cycles and firmware updates. The maximum acceptable LHC jitter is 30 ps (RMS) at the GBTx and the clock skew should be better than 50-100 ps (peak-to-peak).
2. Trigger information distribution with constant latency over the GBT downlink.
3. Accepting the incoming CDH/SDH packages with FIT detector data payload and delivering them to the FLP server's memory.
4. The BUSY signal will be embedded into the incoming FIT packages and it must be extracted by the CRU and delivered to the trigger system (LTU).
5. The CRU shall provide access to the GBTx ASIC registers and to the GBT-SCA features for FIT specific Linux applications.

3.9 ZDC

The CRU shall support the following features:

1. LHC clock distribution over the GBT downlink with constant and deterministic phase between GBT links, CRU units, power cycles and firmware updates. The maximum acceptable LHC jitter is 200 ps (RMS) at the GBTx and the clock skew should be better than 500 ns (peak-to-peak).
2. Trigger information distribution with constant latency over the GBT downlink. The trigger latency should be less than 1.5-2 us.
3. Accepting the incoming CDH/SDH packages with FIT detector data payload and delivering them to the FLP server's memory.
4. The CRU shall provide access to the GBTx ASIC registers and to the GBT-SCA features for ZDC specific Linux applications.

3.10 ACO

The CRU shall support the following features:

1. LHC clock distribution over the GBT downlink with constant and deterministic phase between GBT links, CRU units, power cycles and firmware updates. The maximum acceptable LHC jitter is 250 ps (RMS) at the GBTx and the clock skew should be better than 24 ns (peak-to-peak).
2. Trigger information distribution with constant latency over the GBT downlink. The trigger latency should be less than 1 us.
3. Accepting the incoming CDH/SDH packages with FIT detector data payload and delivering them to the FLP server's memory.
4. The CRU shall provide access to the GBTx ASIC registers and to the GBT-SCA features for ACO specific Linux applications.

3.11 Summary

Table 9 summarizes the detector specific requirements.

Det.	Link type	Device on sending card	No. of links		No. of CRU	TTS through CRU	Busy through CRU	Using of GBT Downlink (e-links)	Using of GBT Uplink (e-links)	Cluster Finder	SDH by CRU	DCS through CRU
			bidir	unidir								
TPC	GBT (GBTx)	ASIC (SAMPA)	7200	7200	360	yes	yes	RO-CTRL: 1x (or 5x) 4 signals @ 80 Mb/s (trig, HB, sync, rst)	28 x 160 Mb/s serial links (SAMPA raw data streams)	yes	yes	GBT ctrl. ch. + SCA (I2C)
MCH	GBT (GBTx)	ASIC (SAMPA)	550	-	25	yes	yes	RO-CTRL: 8 x 5 signals @ 80 Mb/s (HRst, HB, Sync, Phys, x)	40 x 80 Mb/s serial links (SAMPA packets)	-	yes	GBT ctrl. ch. + SCA (I2C)
MID	GBT (GBTx)	FPGA (8x Max10, 2x CyclonV)	32	-	2	yes	yes	RO-CTRL: 10 x 1 bit stream @ 320 Mb/s (RO commands (8 bit serially)	10 x 320 Mb/s serial links	-	yes	GBT ctrl. ch. +SCA (I2C, JTAG, ADC)
TOF	GBT (GBTx)	FPGA (Igloo2)	72	-	3	yes	yes	80 bits of TTS @ 40 MHz	parallel mode, packets (w/ SDH + data) (or single words for control)	-	-	NO (Custom optical link)
FIT	GBT (GBTx)	FPGA (Virtex6)	22	-	2	yes	yes	80 bits of TTS @ 40 MHz (?)	parallel mode, packets (w/ SDH + data) (or single words for control)	-	-	?
ZDC	GBT (GBTx)	FPGA (Virtex5,6)	1	-	1	yes	-	80 bits of TTS @ 40 MHz (?)	parallel mode, packets (w/ SDH + data) (or single words for control)	-	-	?
ACO	GBT (GBTx)	?	1	-	1	yes	-	80 bits of TTS @ 40 MHz (?)	parallel mode, packets (w/ SDH + data) (or single words for control)			
ITS	GBT (GBTx, FPGA)	FPGA (Kintex7)	192	384	24	only clock	yes	parallel mode, packets (w/ DCS payload) (or single words for control)	parallel mode, packets (w/ SDH + data) (or single words for control)	yes	yes	GBT ctr. ch. (I2C, JTAG) + GBT down- and uplinks
MFT	GBT (GBTx, FPGA)	FPGA (Kintex7)	80	80	10	only clock	yes	parallel mode, packets (w/ DCS payload) (or single words for control)	parallel mode, packets (w/ SDH + data) (or single words for control)	?	?	GBT ctr. ch. (I2C, JTAG) + GBT down and uplinks
CTP	GBT (GBTx, FPGA)	FPGA (Kintex7)	2	-	1	-	-	parallel mode, packets (w/ DCS payload) (or single words for control)	parallel mode, packets (w/ SDH + data) (or single words for control)	-	-	NO (Eth link)
TRD	custom 8B/10B	ASIC	-	1044	54	-	yes	No downlinks!	No GBT - custom 2.5 Gb/s 8B/10B optical links, raw data stream	yes	yes	NO (Eth link)

Table 9: Summary of the Detector Specific Requirements

4 Requirements from the Trigger and Timing System

Each CRU is connected to a detector specific LTU over a bidirectional link. Where the LTU -> CRU direction is used for LHC clock and trigger information distribution and the CRU -> LTU direction is used for propagating back the detector busy information.

The CRU shall support the following features:

1. Ability to reconstruct the LHC clock from the incoming protocol from the LTU with deterministic phase and propagate it toward the front-end cards over the GBT downlinks.
2. Ability to access the front-end GBTx ASIC registers over the GBT links and provide software tools to adjust the reconstructed LHC clock phase on the front-end card.
3. Ability to extract the trigger information from the incoming protocol from the LTU with deterministic delay and deliver it either to the detector specific read-out logic or directly to the front-end cards through the GBT links.
4. Ability to propagate the detector busy information back to the LTU. The source of the busy information can be the CRU firmware itself in the case the responsible logic is implemented in the CRU firmware or the front-end card when the busy is embedded into the incoming CDH/SDH packages generated by the front-end.

5 Requirements from the DCS

1. The CRU firmware and software shall provide a generic interface which is accessible on the FLP server on Linux application level which allows any DCS related application to access the DCS related front-end functionality in a transparent way.

6 Requirements from the O2/DAQ

1. CRUs shall provide formatted data packages to the FLP computers with standardized common data headers called SDH.
2. Data strems shall be segmented by heartbeats.
3. Busy states in data read-out and streaming shall be recognized and communicated to the trigger system to build drop maps.
4. A read-out throttle mechanism shall be implemented. (Specified as a system level requirement in ALICE Tech Note)

7 General Firmware Related Requirements

1. The CRU firmware shall be based around a modular and extendable architecture. It shall be not a closed monolithic architecture. The CRU firmware shall be extendable by the detector teams with their detector specific code for the data processing.
2. The CRU team shall provide a generic (common) firmware implementation which supports as many detectors as possible (detectors which support the standard protocol and there is no need for data processing inside the CRU).
3. The CRU firmware shall support the remote firmware upgrade and functionality control.
4. As a requirement from the experiment, all CRUs shall provide a proven, „fall-back” data path bypassing the detector specific data processing but move unmodified raw data (a.k.a. link data) in standard ALICE data packets to the FLP memory.

5. The capability of switching back („fall back”) to the secure raw data (link data) taking mode be always available without firmware up/downgrade procedure.

8 General Software Related Requirements

1. The CRU team shall provide at least two level of software support:
    a. API level for the detector specific applications (like measurement control, DCS, …)
    b. Command line tools for configuring, testing, and debugging of components
2. The CRU driver and API layer shall provide support for accessing the underlying features from multiple threads and processes. The API shall guarantee that the critical resources shared correctly between the parallel users (like the DAQ and the DCS software and the detector specific user logic firmware shall be able to use the GBT-SCA slow control channel in parallel).
3. The CRU software shall support the remote firmware upgrade and functionality control.