CRU Firmware Overview

ALICE Common Read-out Unit (CRU)

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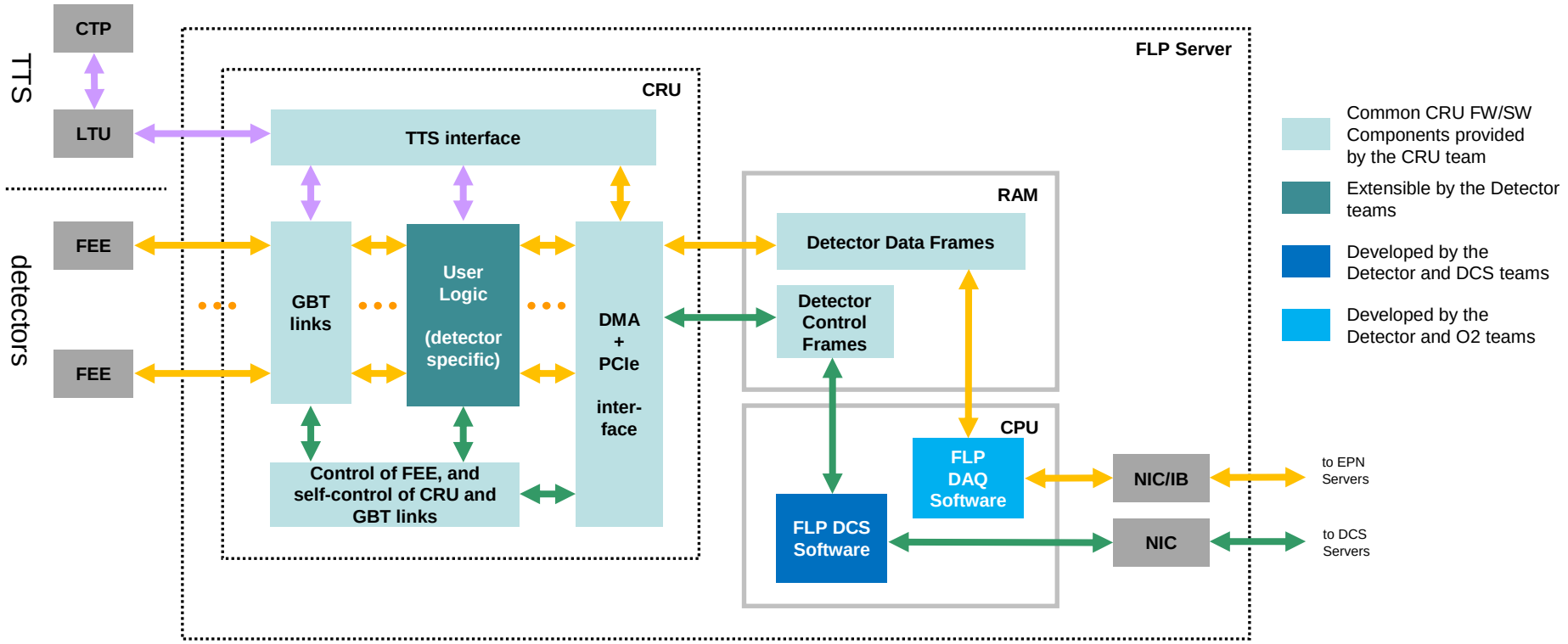
Overview

CRU Overview



Main Tasks of the CRU:

- Deliver the trigger, timing and read-out control information to the Front-End Electronics
- Deliver detector data to the O2 (FLP Servers) with and/or without processing in the CRU FPGA
- Transport detector control information between between the FLP Servers (DCS) and the FEE
- Take part of the Busy / Drop / Throttle mechanism of the detectors read-out

Characterization of the Links of the CRU

Trigger&Timing Downlink (LTU → CRU), 1 link / CRU:

- Technology: 10G PON, 9.6 Gbps, 8B/10B, point-multipoint
- Deterministic latency
- Payload: trigger and throttling (drop-maps) information from the Local Trigger Units (LTU)

Trigger&Timing Uplink (CRU → LTU): 1 link / CRU

- Technology: 10G PON, 2.4 Gbps, multipoint-point with Time Division Multiplexing (TDM)
- Payload: propagating busy and throttling information from CRU to the Local Trigger Units (LTU)

Detector Downlinks (CRU → Detector FEE): 24/36 links /CRU

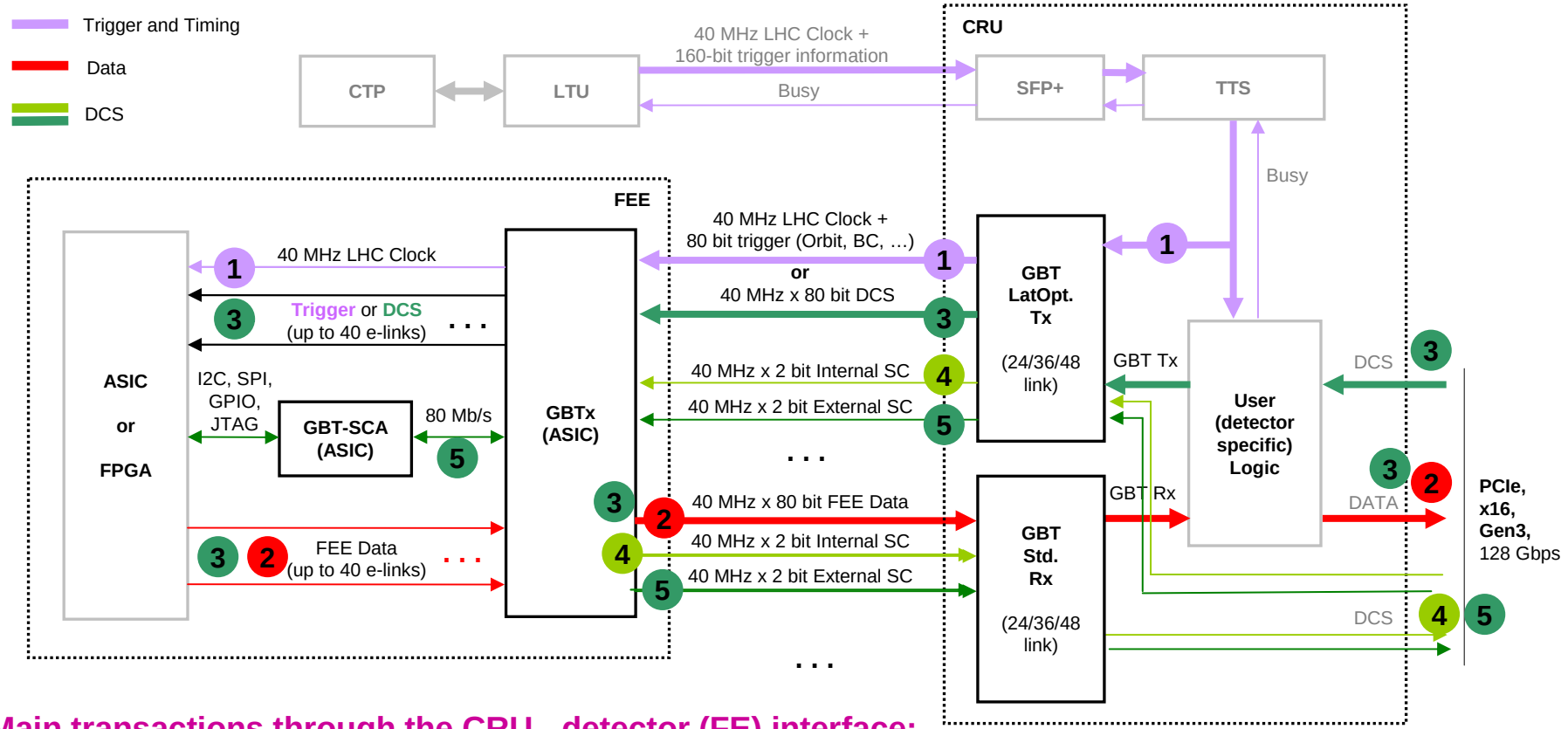
- Technology: 4.8 Gb/s rad-hard GBT links in GBT mode with Forward Error Correction (FEC)
- Deterministic latency
- Payload: LHC Clock & Trigger distribution to detectors, slow control

Detecor Uplinks (Detector FEE → CRU): 24/36 links /CRU

- Technology: 4.8 Gbps rad-hard GBT links in GBT mode w/FEC, or in Wide Bus mode
- Deterministic latency
- Payload: Detector data taking, slow control

Detector Interface (GBT)

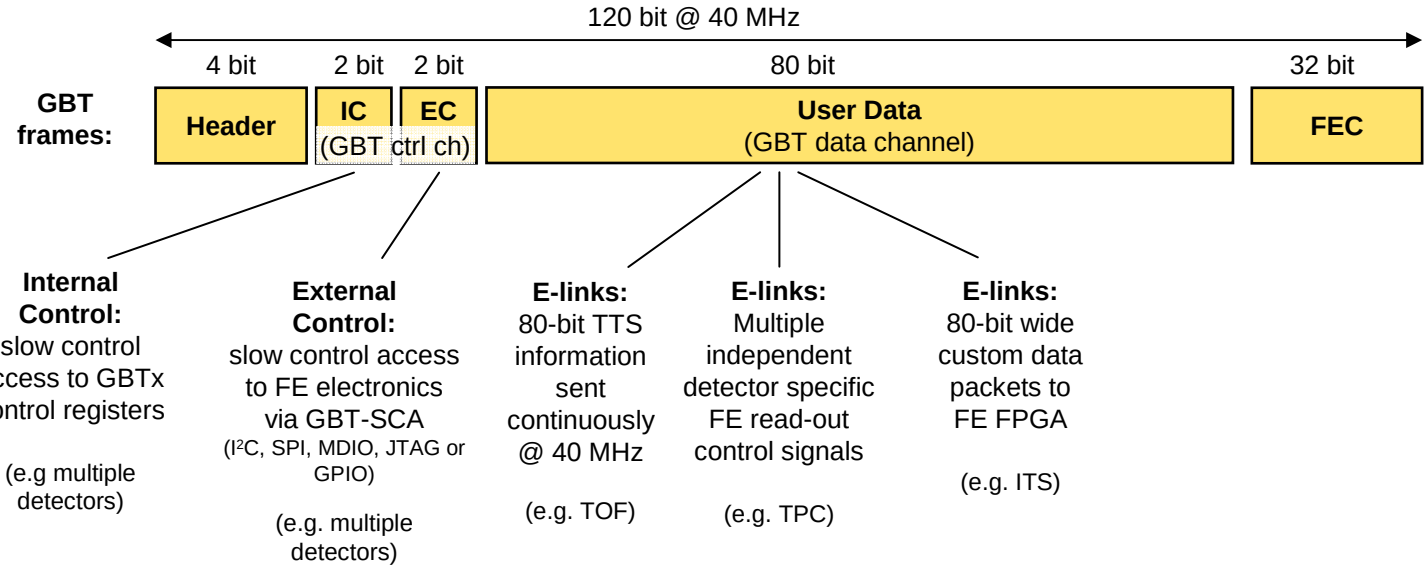
Communication Forms through the CRU – FE Interface



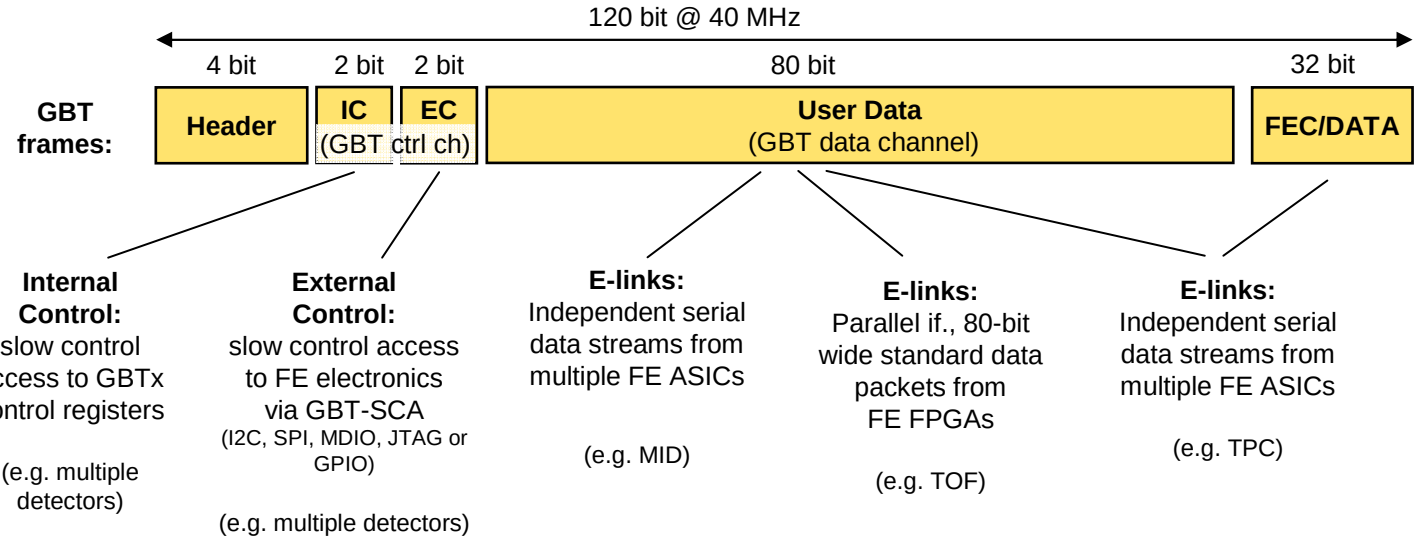
- **Main transactions through the CRU - detector (FE) interface:**
  - 1 Delivering the TTS information or Read-out Control from CRU to FE via GBT
  - 2 Receiving the detector data in multiple serial or parallel form from the FE via GBT
  - 3 Communicating custom packets between the CRU and the FE FPGA in parallel form via GBT
  - 4 Sending and receiving packets to and from the GBTx internal register block (GBT control)
  - 5 Sending and receiving slow control packets to and from GBT-SCA ASIC (detector control)

GBT Frames vs. Different CRU – FE Communication Forms

GBT Downlink
(CRU -> FE)



GBT Uplink
(FE -> CRU)



Trigger & Timing Distribution (Clocking scheme)

Trigger Downlink: 10G PON Receiving

- **Status of the 10G PON link testing and verification**
  - **LTU emulator with 10G PON: Xilinx KC705 and Kintex Ultrascale boards**

    (w/ support and instrumentation from the electronics group)
  - **CRU emulator: ALTERA and REFLEX Arria10 Development Boards (with Engineering Samples of A10.)**
  - **Development and verification Status**
    - 10G PON receiving: FW implemented in Arria 10 FPGA (w/ ES2)
    - Uplink (Busy) is not yet implemented, will be based on the reference design from CERN electronics group
    - Ligent OLT and ONU modules, passive splitters and attenuators were used in the tests
    - Recovered clocks and data have been characterized in A10
    - Additional (external) jitter-cleaner PLLs were also connected and tested
  - **Quality of the recovered LHC clock**
    - Jitter analysis showed good results for the 240 MHz clock recovered from 10G PON.
    - Performance of different external jitter cleaners (on a separate PCB) have been analyzed. Final selection of on-board jitter cleaner have to be made together with LHCb.

Detector Downlinks – Trigger and Timing Distribution

- **Detecor links, downlink direction:**
  - CRU shall delivers Timing (LHC clock), Trigger, and FEE read-out control information with *deterministic latency*.
  - Detectors fall into two categories:

Category A: trigger forwarding only in CRU

(e.g. TOF, ...)

- LHC clock and trigger payload received from the Local Trigger Unit (LTU) via 10G PON
- Trigger payload is extracted
- Part of the trigger payload is forwarded to the FEE
- FEE decodes the trigger infomation itself and controls the digitizer ASICs locally (local read-out control).

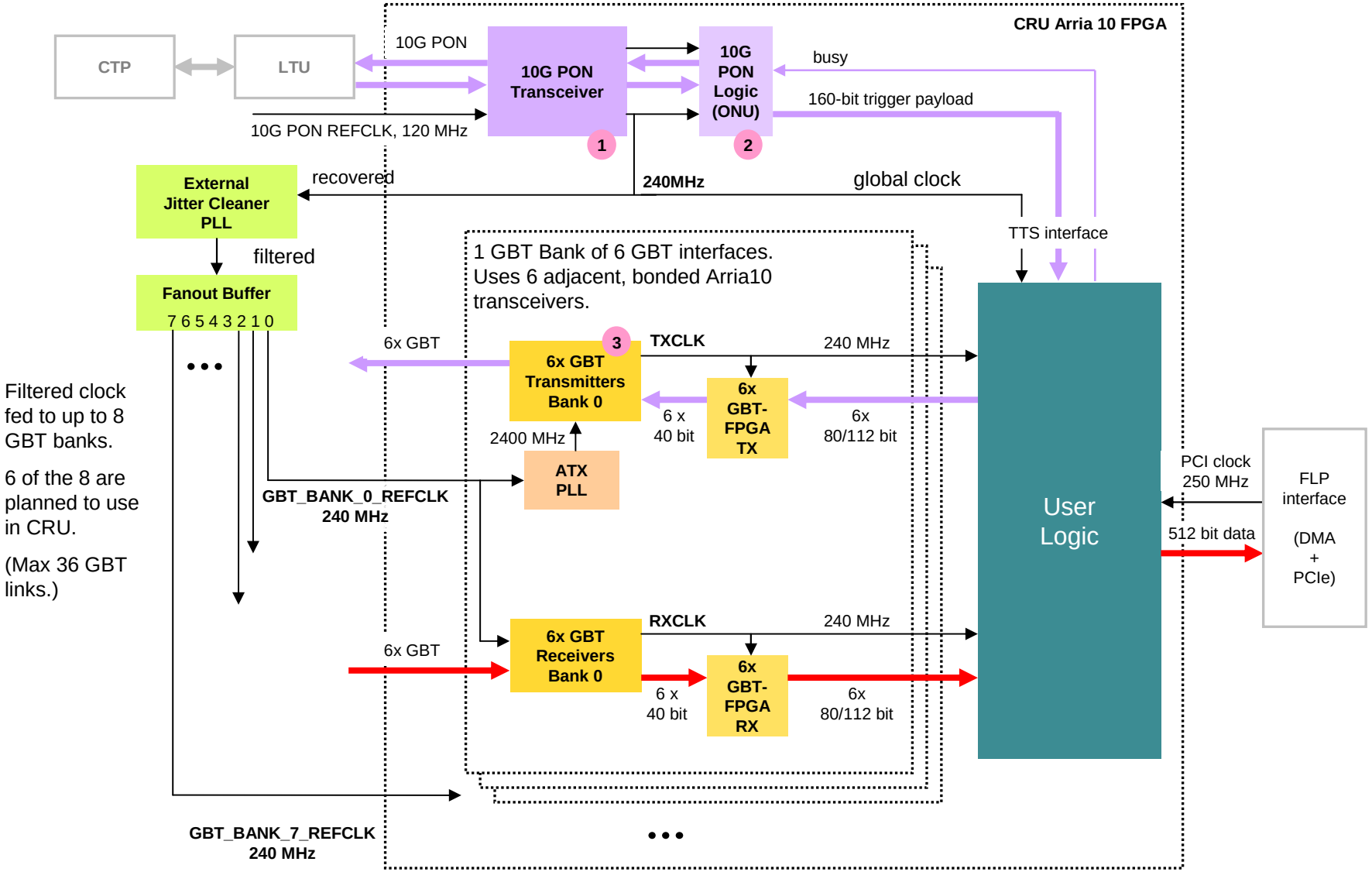
Category B: tigger preprocessing in CRU

(e.g TPC, MCH, MID)

- LHC clock and trigger payload received from the Local Trigger Unit (LTU) via 10G PON
- Trigger payload is extracted
- Trigger information is decoded and processed in the CRU
- Direct control signals of the digitizer ASICs sent to the FEE from the CRU (remote read-out control).

- **The two cases differ only in the *meaning* of the forwarded signals (i.e. raw trigger information (TTS payload) vs. direct read-out control signals of the FEE ASICs.**
- **The timing quality requirements for the transmission in both cases are *equally strict*!**
- **The key technical question in both cases is the distribution and transmission of the 40 MHz LHC clock with *deterministic phase.***

LHC Clock Recovery and Distribution

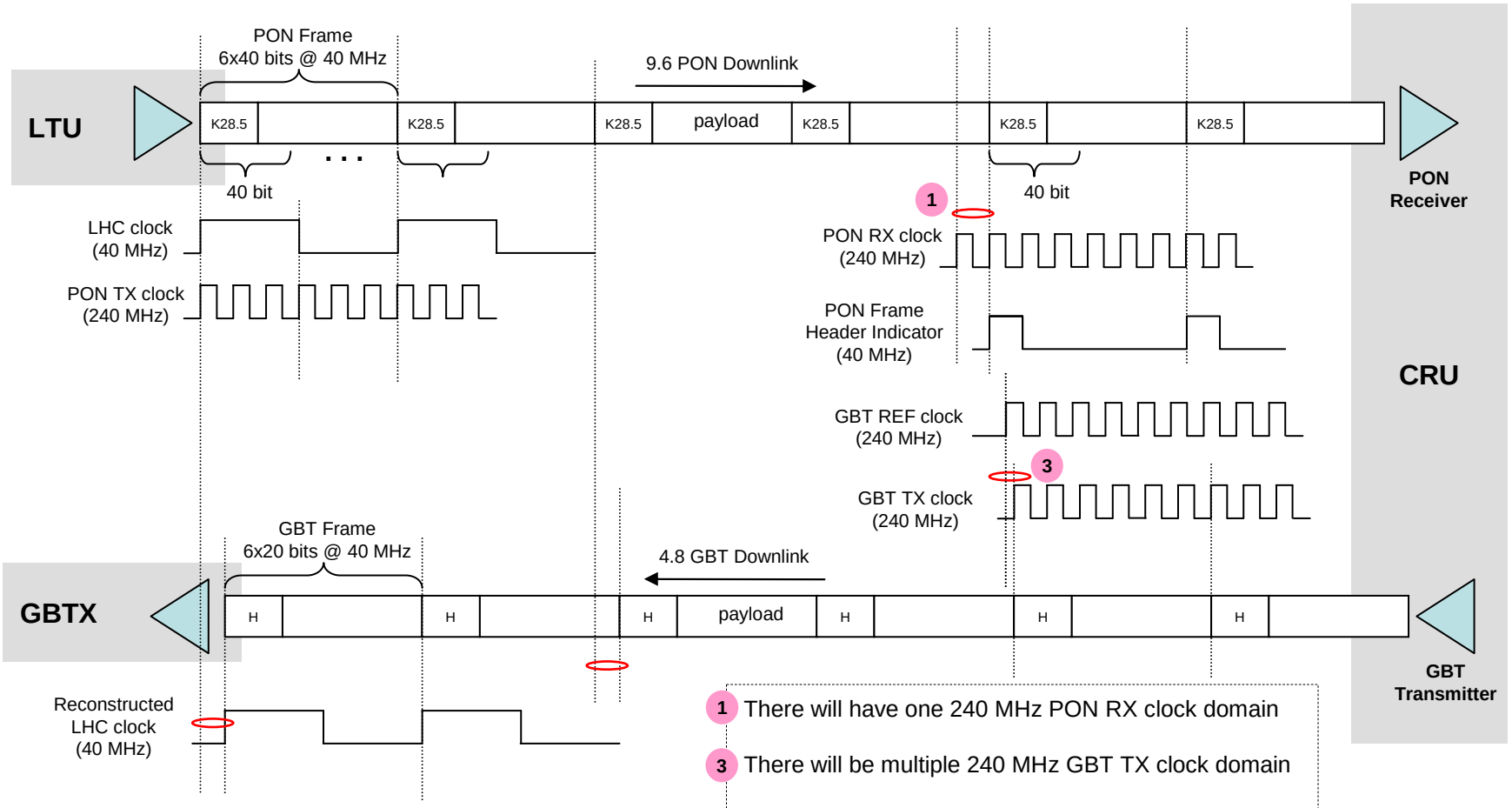


Filtered clock fed to up to 8 GBT banks.

6 of the 8 are planned to use in CRU.

(Max 36 GBT links.)

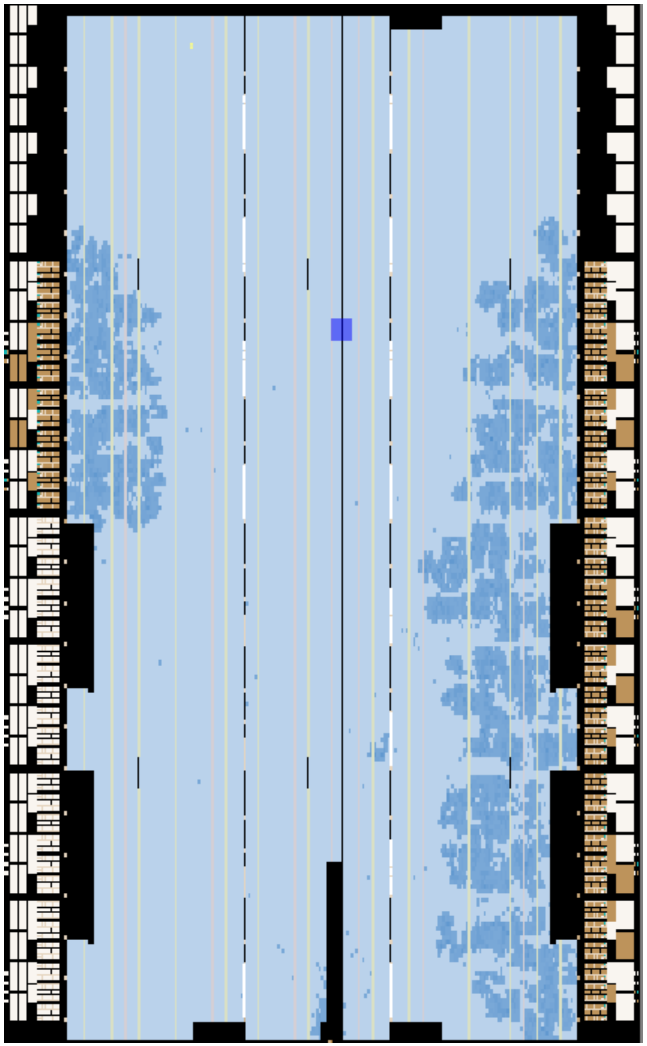
LHC Clock Distribution (2)



Challanges in Clock Distribution

Challanges	Solutions	Verification
1) 240 MHz 10G PON RX clock phase uncertainty Derived from 9.6 Gb/s 10G-PON link clock uncertainity: 360 deg /40 = up to 40x 104 ps	Detect the PON coma position in the RX parallel data and control: Receiver RX PMA Clock Slip, PMA reset	Demonstarted and tested with different Xilinx (LTU emulator) and Arria 10 (CRU) dev boards
2) 40 MHz Recovered LHC clock phase uncertainty Derived from 240 MHz recovered clock, uncertainity: 360 deg / 6 = up to 6x 4.17 ns	Detect the phase difference between 40 MHz rising edge and the PON coma position and control: PLL reset, dynamic phase shifting	40 MHz lock is not needed any more.
3) 120 MHz GBT-FPGA TX clock phase uncertainty Derived from 4.8 Gb/s GBT link clock, uncertainity: 360 deg / 20 = up to 20x 417 ps	Measure the relative phase difference between the PON RX clock and the GBT TX clock with undersampling technique, and set the right pahse with multiple resets of transmitter PMA	A10 transceiver feature: autonomous *„PLL Feedback Compensation".* No need for an own phase difference measurement and correction! (But 240 MHz clocking is needed.) Tested in A10 by the electronics group.
4) FPGA Routing	Floorplanning	t.b.d.
5) Cable length differences and other constant link-to-link skews in the downlink side	GBTx ASIC Phase-Shifter	Proven in GBT project.
6) Process-Voltage-Temperature (PVT) variations	First it should be measured to study the impact.	We now have plan for temperature dependency measurements with the electronics group.

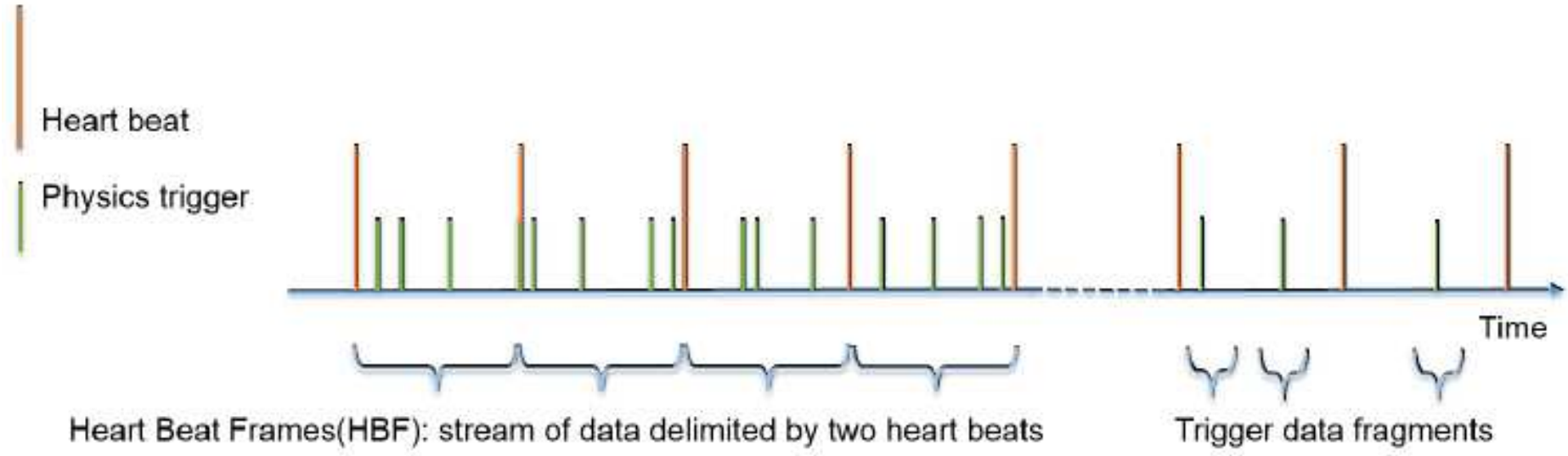
P&R Results: 48 x TX (GBT Mode) + 48 x RX (GBT Mode / WB)



- **CRU team has modified the GBT-FPGA *code* and the GBT-link-to-User-Logic *interface***
  - **to eliminite the 40 MHz interface clock, and**
  - **to have a single clock frequency of 240 MHz in the GBT-FPGA firmware.**
- **This was done in two steps:**
  - **First we increased the clock frequency to 120 MHz. Timing analysis completed and showed good results.**
  - **Now we are working on further increase it to a clean 240 MHz operation.**
- **Development tasks in progress:**
  - **Upgrade our firmware to the latest GBT-FPGA 4.0 code base received from the CERN electronics group**
  - **Modify the internal operation up to 240 MHz.**

Data Flow

Continuous readout : the Heart Beat trigger



The continuous read-out mode of some detectors will be a substantial change from current practice.

Data will not be delimited by *physics triggers* but it is composed of several *continuous* data streams transferred to the computing system.

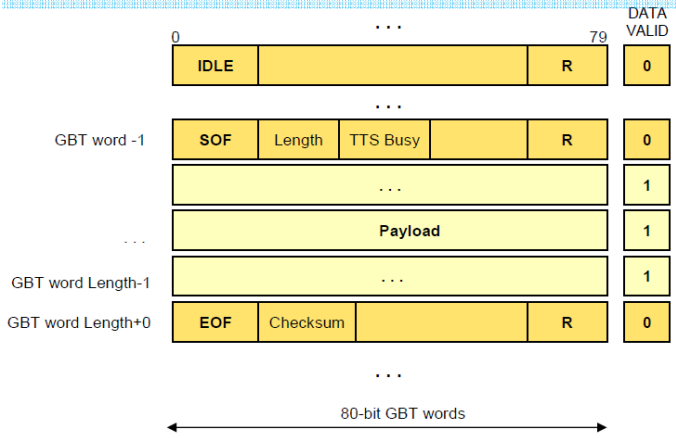
Artificial *heart beat triggers* or 'heart beats' will be generated by the trigger system at constant frequency (e.g. 10 kHz), used for chopping the continuous data flow into manageable Heart Beat Frames (HBF).

FEE – CRU Data Sending Modes

Detectors FEE can send data . . .

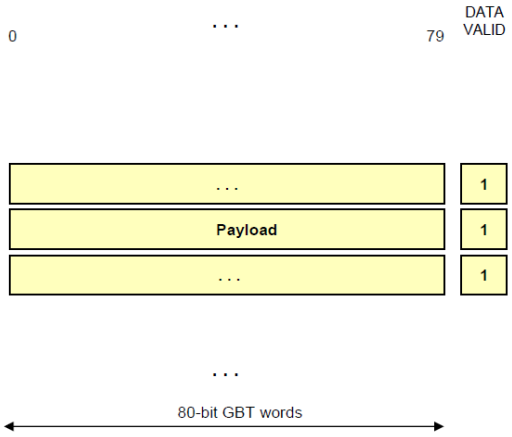
With packets protocol
(e.g. TOF, ITS, etc.):

- For every trigger (physics or heart beat) the detector generate a packet:
  - ***SOP*** (Start of Packet)
  - **PAYLOAD**
  - ***EOP*** (End Of Packet)
- Within the packet the data is tagged with event identification

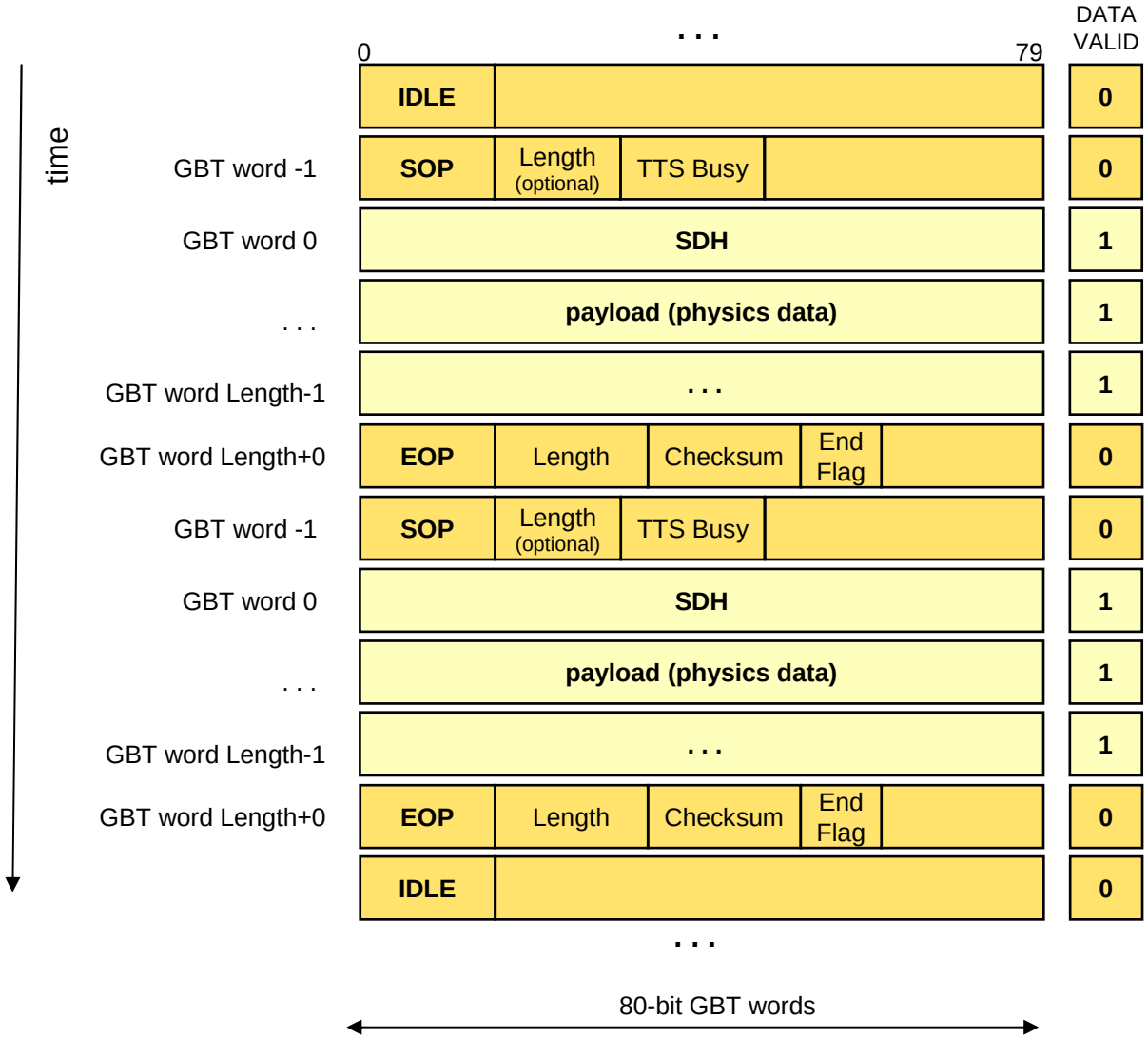


With continuous streaming
(e.g. TPC):

- The detector produces a continuous, unsegmented flow of data.
- It is the responsibility of the CRU to packetize the information and tag the data adding event identification

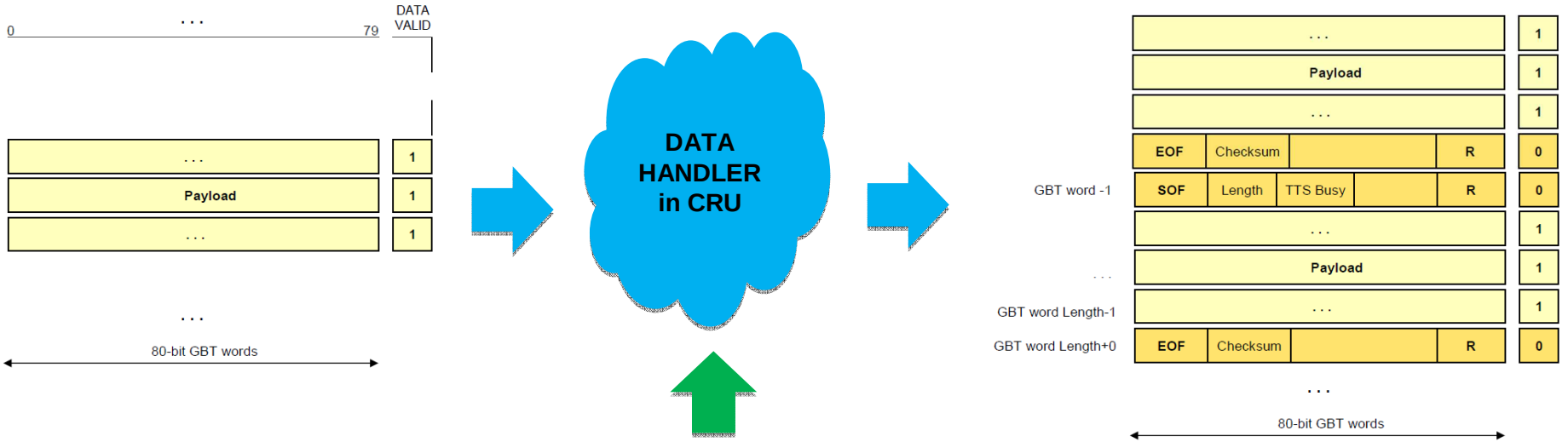


Detectors Sending standard data packets



SDH = Single Data Header,
former Common Data Header (CDH)

From continuous to packets...

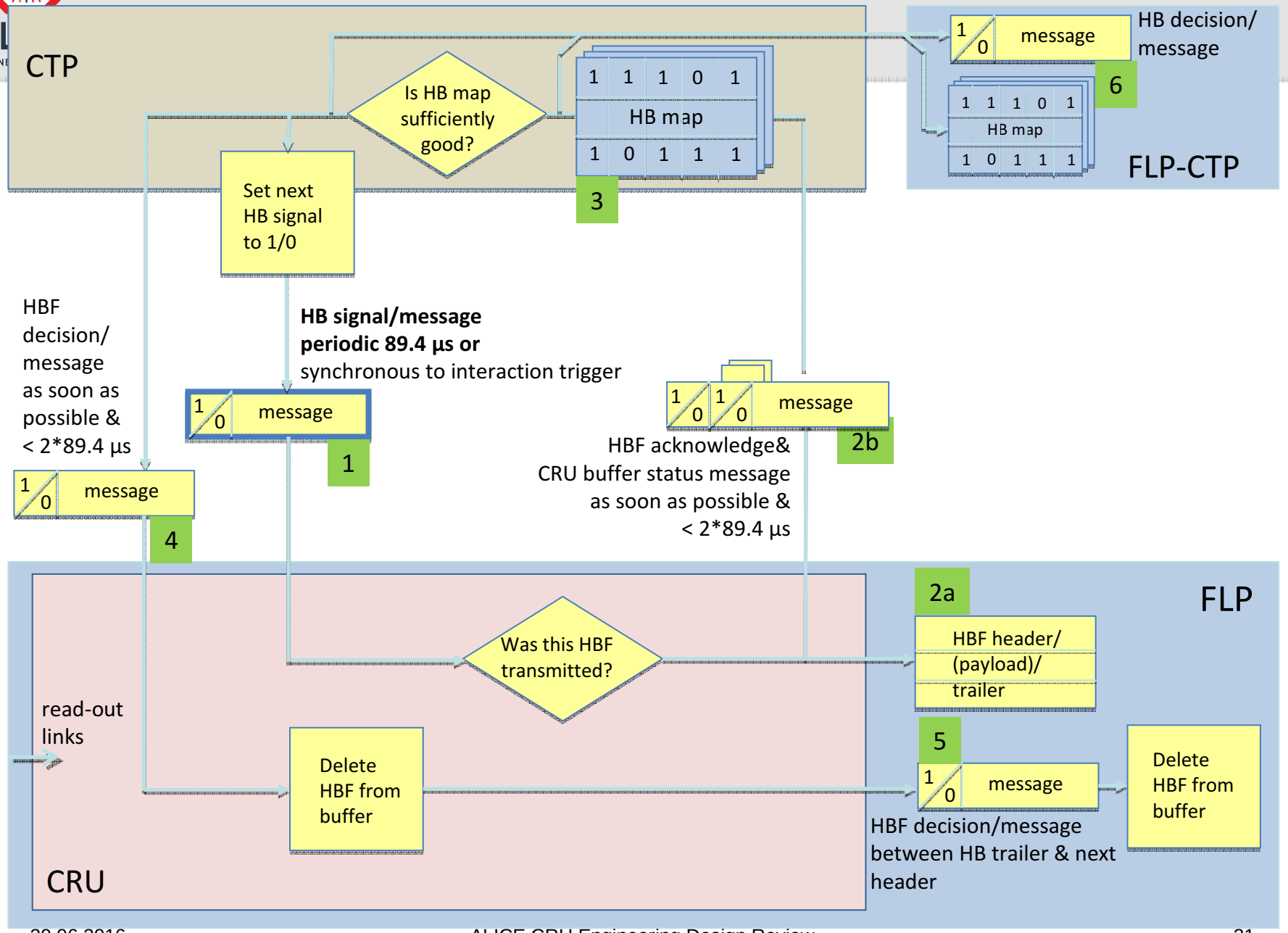


data rate in input:
1 GBT Word @ **40 MHz**

data rate in output:
1 GBT word @ **240 MHz**

The writing frequency to the data handler (40 MHz) is lower than the reading frequency from the data handler (240 MHz), so it is possible to add extra words (e.g. delimiters, header words, etc) into the continuous flow, without loosing any data.

Busy / Drop / Throttle Mechanism

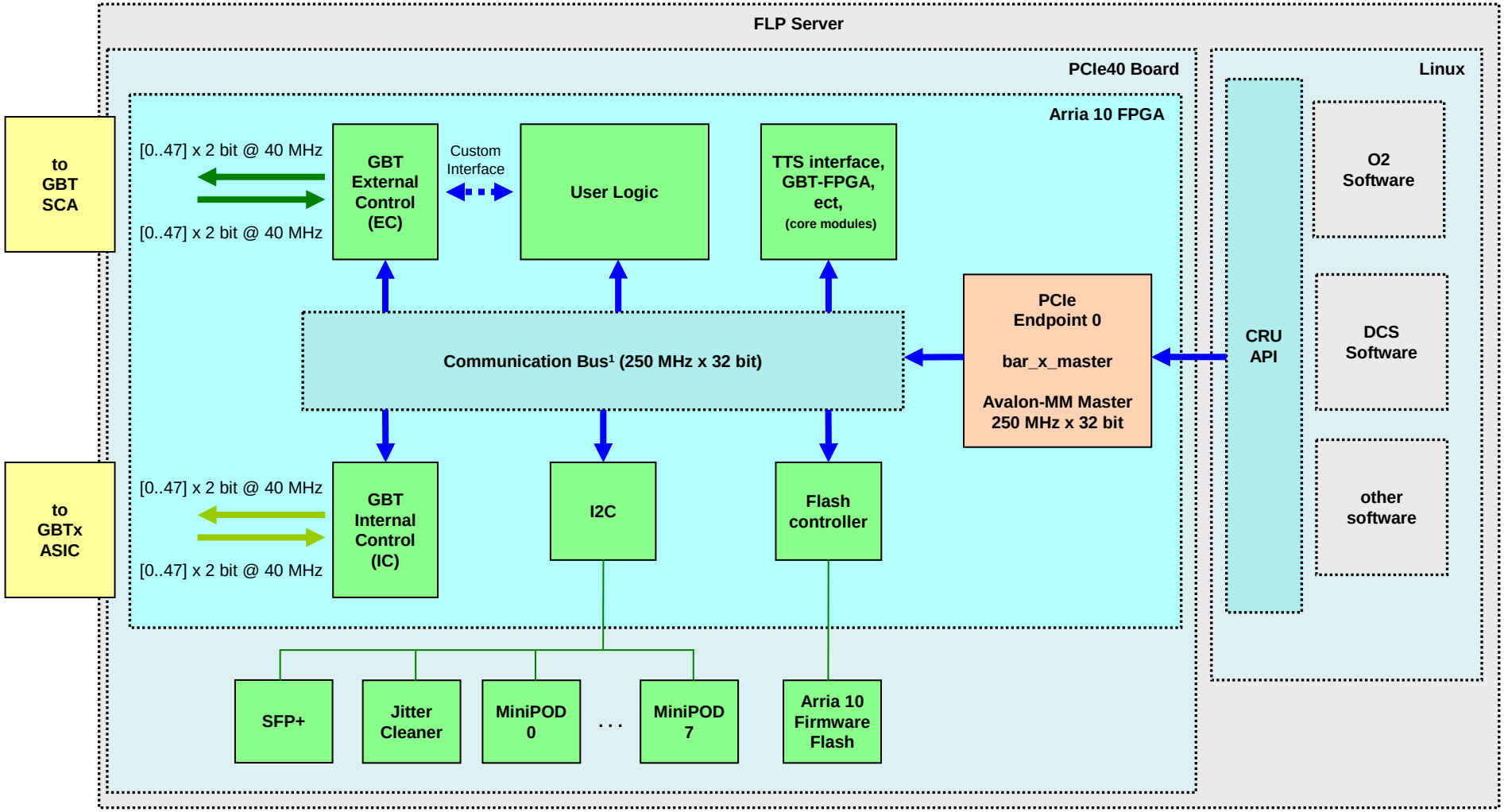


The Control Domain

CRU Control Tasks

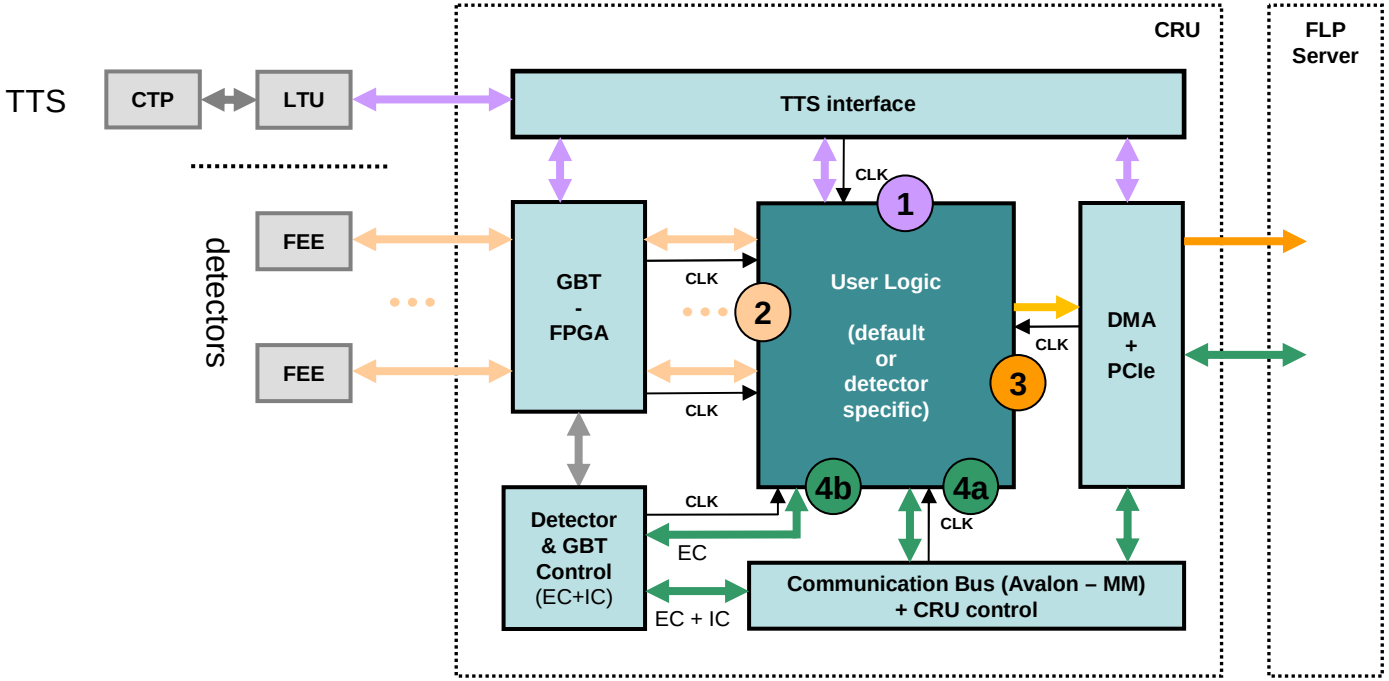
- **Controlling of the Detector / FEE**
  - **Controlling FEE through GBT-SCA over the External Control (EC) field of GBT control channel**
    - A GBT-SCA provides: 16x I2C master, SPI master, JTAG master, and GPIO
  - **Controlling FEE by sending custom CRU packets over the GBT data channel**
    - e.g. downloading large data blocks to FEE
- **Controlling of the GBT Link**
  - **Configuring GBTx over the Internal Control (IC) field of GBT control channel**
    - GBT front-end side features: LHC clock phase adjustment, laser driver, loopback, …
- **Controlling of the CRU itself**
  - **Controlling of FPGA firmware modules**
    (TTS interface, GBT-FPGA, FLP interface, and User Logic)
  - **Controlling of on-board components**
    (Optical transceivers, external PLLs, Firmware Flash, etc …)

CRU Slow Control Architecture



User Logic

CRU User Logic Interfaces – I.



- **The CRU User Logic has the following firmware interfaces:**
  - (1) TTS interface (downlink and uplink)
  - (2) GBT-FPGA interface (downlinks and uplink)
  - (3) FLP data streaming interafce (uplink only)

    Control Interfaces: (4a) Avalon-MM Slave Interface and (4b) Custom interface for detector control
- **All the User Logic interfaces are clocked from the CRU framework**
- **A detailed description of the interface signals can be found in the „*CRU Specification*" document (presently v0.7)**

User Logic Interfaces – II.

1

- TTS RX (downlink)
  - Raw trigger information
  - Stream without handshake
  - 240 MHz clock, 184-bits data @ 40 MHz
- TTS TX (uplink)
  - Busy information,
  - Stream with handshake

3

- FLP Data Streaming (uplink only)
  - Detector data
  - Stream with handshake
  - 250 MHz clock, 512-bit data @ 250 MHz

2

- GBT TX (downlink)
  - Trigger, read-out, custom packets
  - Streams without handshake
  - 240 MHz clock, 80-bits data @ 40 MHz
- GBT RX (uplink)
  - Detector data, custom packets
  - Streams without handshake
  - 240 MHz clock, 80/112-bits data @ 40 MHz

4a

- Control Interface - PCIe (up/downlink)
  - Avalon-MM Slave
    - User logic control
    - Register based interface
    - 250 MHz clock, 32-bit data

4b

- FEE Control Interface:
  - Custom interface
    - Prority acces to the GBT external control channel

Inside the User Logic...

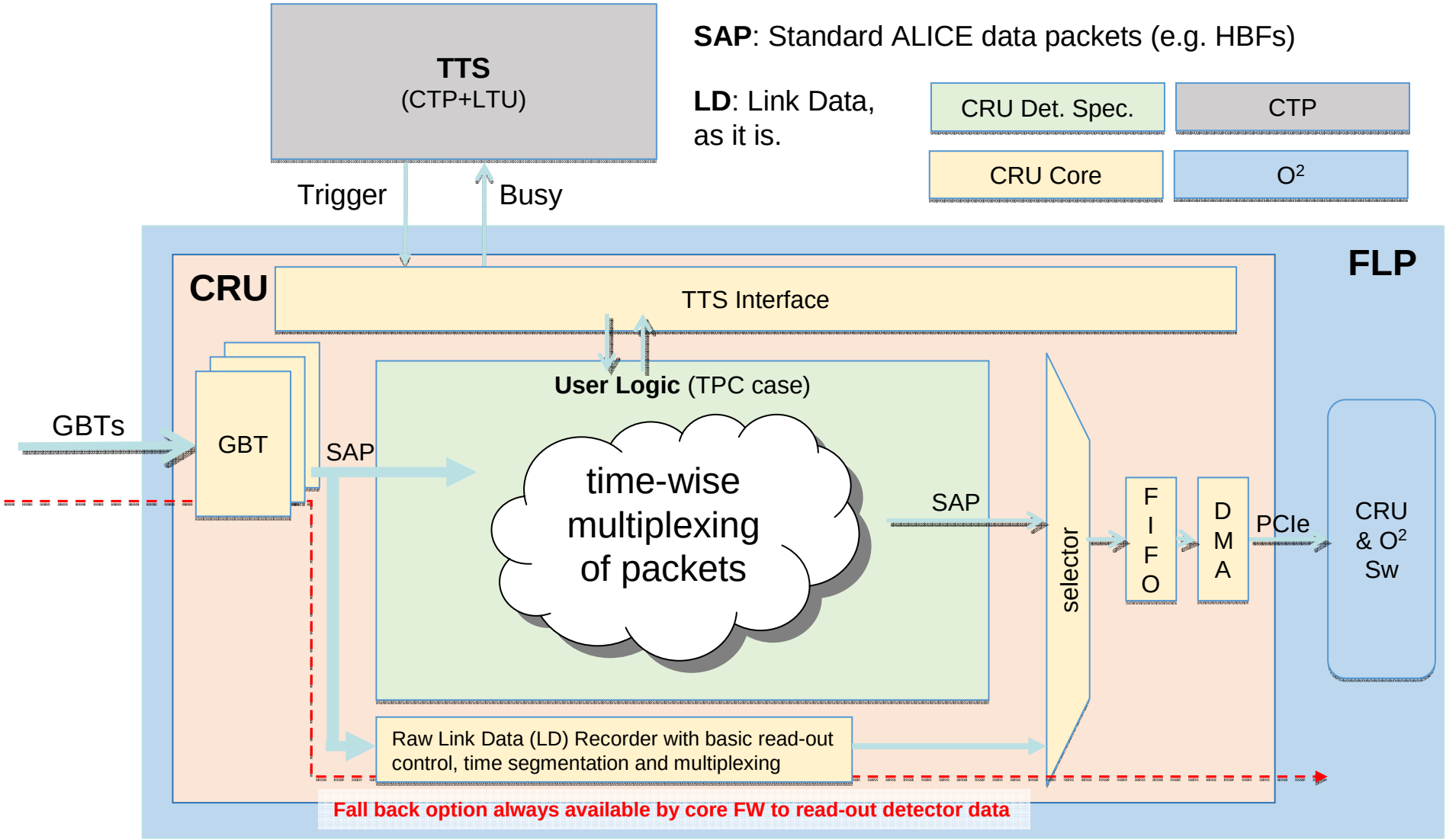
Data types	TPC	TRD	ITS	others
Link Data as it is (a fall-back option)	**Link data (LD)** (GBT frames payload data + FEC)	**Link data (LD)** (custom frames)	**Link data (LD)** (GBT frames payload data + FEC)	**Link data (LD)** (GBT frames payload data + FEC)
PL1	Extracted and sorted, but **unmodified raw data (UR)**	**t.b.d.**	**t.b.d.**	**t.b.d.**
PL2	**Baseline correction (BC)**	**t.b.d.**	**t.b.d.**	**t.b.d.**
PL3	**Zero Suppressing (ZS)**	**t.b.d.**	**t.b.d.**	**t.b.d.**
PL4	**Cluster Finder (CF)**	**t.b.d.**	**t.b.d.**	**t.b.d.**
PL5	**n.a.**	**t.b.d.**	**t.b.d.**	**t.b.d.**

Transmitted to FLP via...

Link Data (i.e. GBT Frame) **Recorder in core logic** (central team)

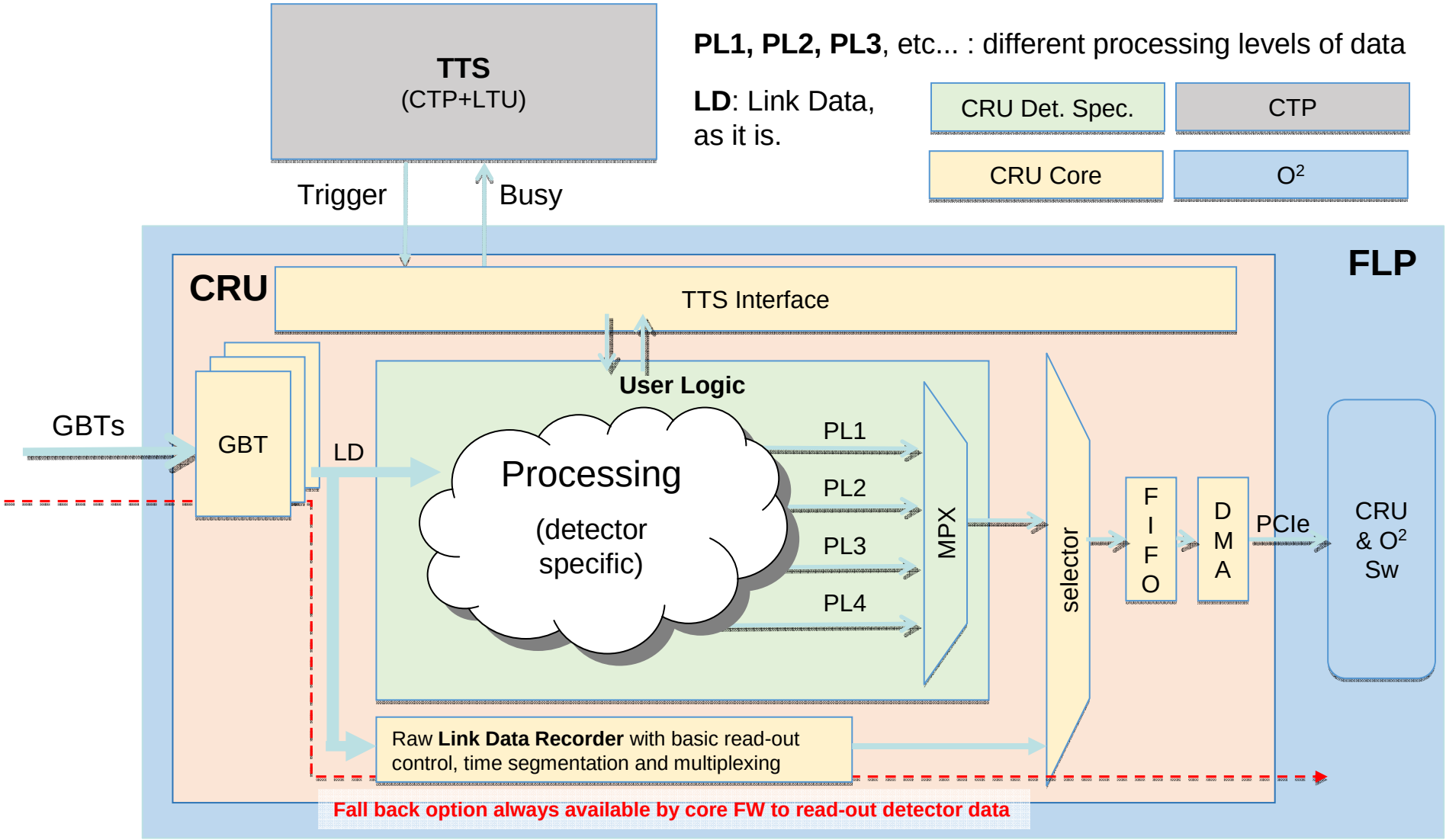
User Logic (detector teams)

Example 1 – Default User Logic
(developed by the central CRU team)



Example 2 – User Logic with Processing

(developed by detector CRU teams)



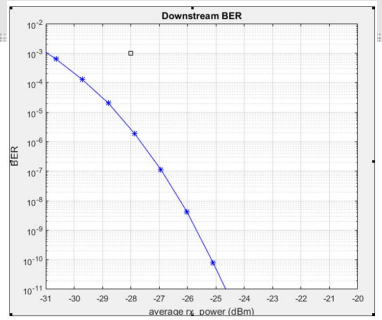
Thank you!

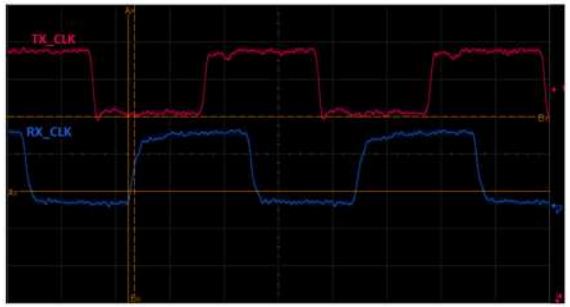
Reserved Slides

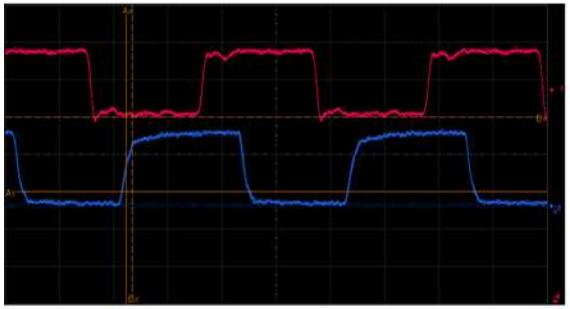
LTU to CRU: 10G PON

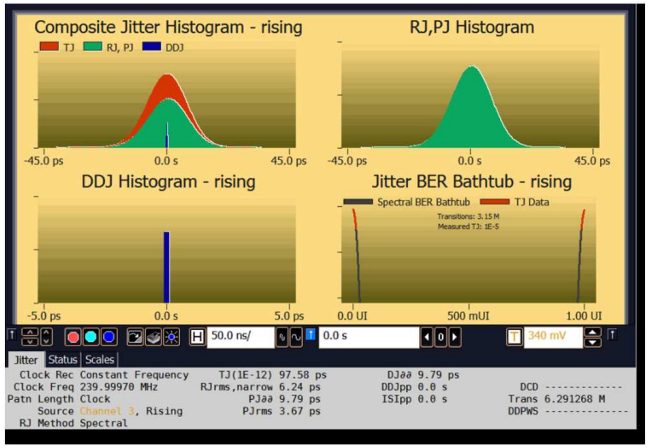
- **10G PON link testing and verification status**
  - **LTU emulator with 10G PON: Xilinx KC705 and Kintex Ultrascale boards**
    - Support and Instrumentation from the electronics group
  - **CRU emulator: ALTERA and REFLEX Arria10 Development Boards (with Engineering Samples of A10.)**
    - 10G PON receving: FW implemented in both Arria 10 hardware (w/ ES2)
    - Uplink (Busy) is not yet implemented
    - Ligent OLT and ONU modules, passive splitters and attenuators were used.
    - Recovered clocks and data got characterized
    - Additional (external) jitter-cleaner PLLs were also connected and tested

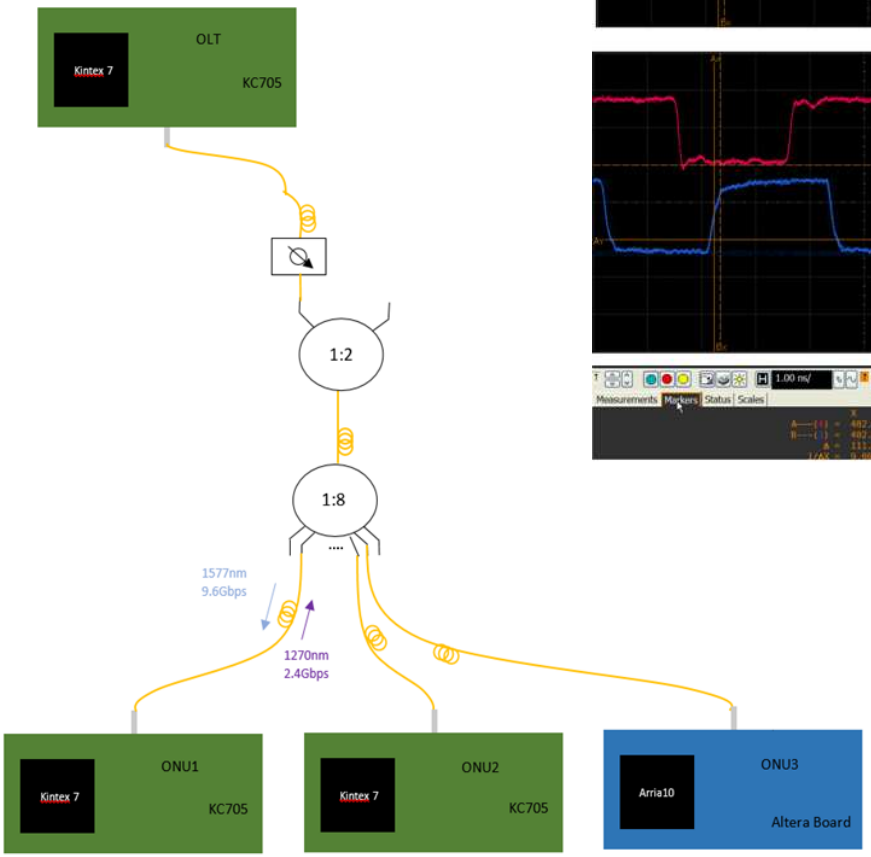
Qualification of 10G PON Receiving in Arria 10

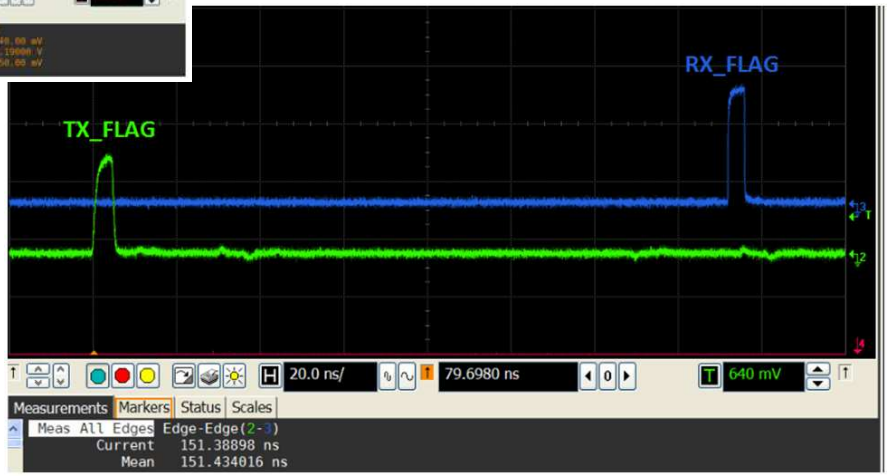












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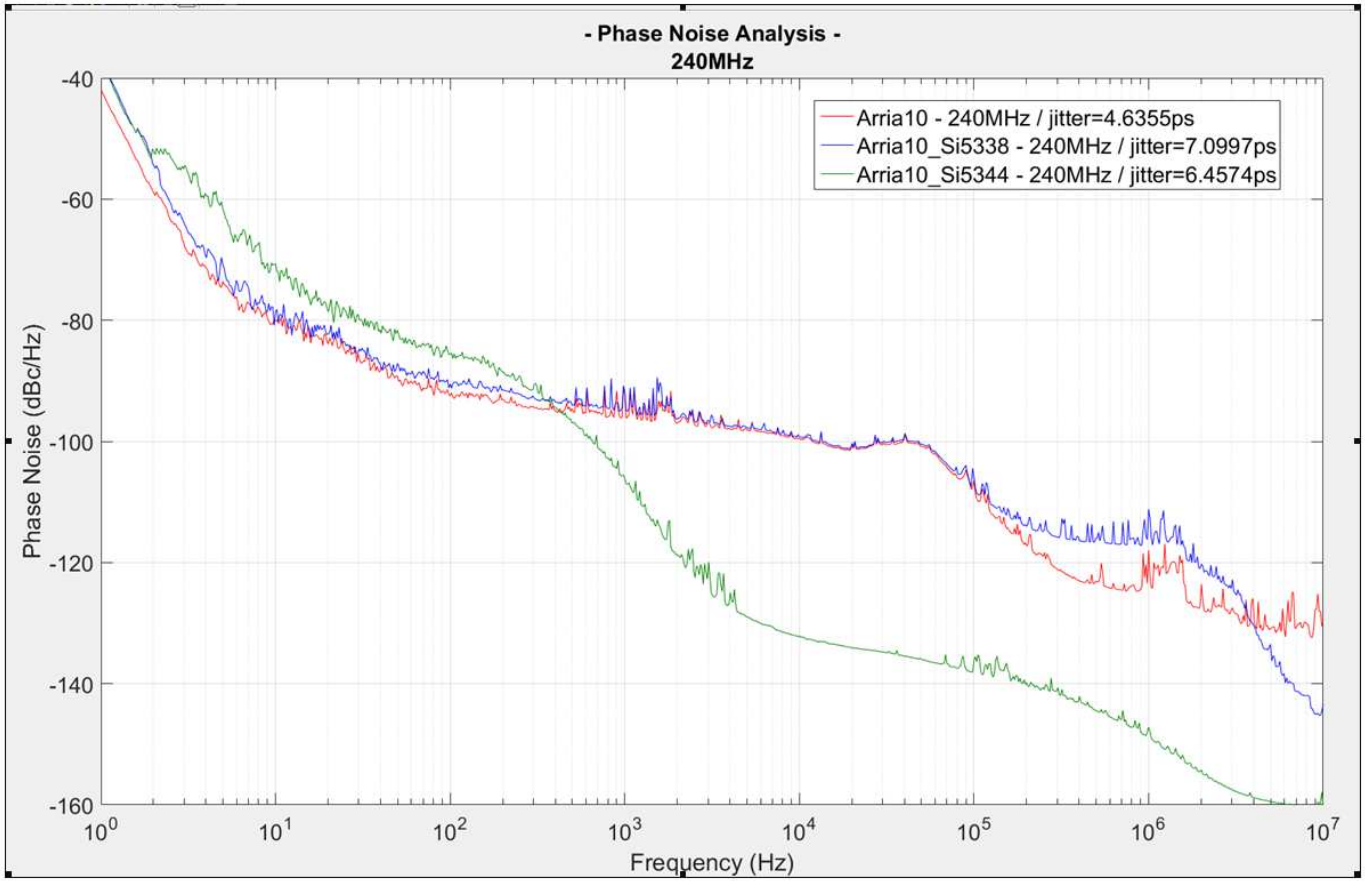
A10 internal PLL (ATX PLL) vs. external jitter cleaners



CRU FW Resource Usage Numbers