pALPIDEfs datasheet

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Version: 1.0b

Last edited: 24/03/2014

# Preamble

The pALPIDEfs is one of several chips implemented in the context of the microelectronics R&D for the ALICE ITS Upgrade, as part of a path towards the design of the ALPIDE chip that will target all the requirements of the ITS Upgrade. Each of those chips focuses on different development aspects. The pALPIDEfs chip is not intended to be a complete prototype of the final ALPIDE and its design did not aim to fulfil the complete set of the requirements. The pALPIDEfs chip has been designed mainly to explore microelectronics and system aspects related to the integration of a large scale (~3×1.5 cm2) MAPS chip and to the physical and electrical interconnection of such a chip on flex printed circuits.

The purpose of this document is to provide technical information for the integration of test systems and evaluation boards based on the pALPIDEfs chip.

# Table of Contents

[Preamble 1](#_Toc382993891)

[Table of Contents 2](#_Toc382993892)

[Introduction 4](#_Toc382993893)

[Block diagram and chip interfaces 5](#_Toc382993894)

[Floorplan 6](#_Toc382993895)

[Interface signals 7](#_Toc382993896)

[Supply and ground nets 9](#_Toc382993897)

[Recommended operating conditions 9](#_Toc382993898)

[Electrical characteristics 10](#_Toc382993899)

[Timing requirements 10](#_Toc382993900)

[Switching characteristics 10](#_Toc382993901)

[Operating characteristics 11](#_Toc382993902)

[Analog front-end and in-pixel digital section 12](#_Toc382993903)

[Double column and region numbering 15](#_Toc382993904)

[Priority Encoders and pixel indexing 16](#_Toc382993905)

[Configuration Interface 17](#_Toc382993906)

[JTAG I/O signals 18](#_Toc382993907)

[Instruction 18](#_Toc382993908)

[Address field of the Instruction Register 18](#_Toc382993909)

[Data Registers 18](#_Toc382993910)

[Control Write operation 18](#_Toc382993911)

[Control Read operation 19](#_Toc382993912)

[Description of address space 20](#_Toc382993913)

[Internal registers 21](#_Toc382993914)

[Periphery Control Register 21](#_Toc382993915)

[Region Disable Registers 21](#_Toc382993916)

[STROBE\_B Timing Register 21](#_Toc382993917)

[Column Disable Register (one per region) 21](#_Toc382993918)

[Pixel configuration registers 21](#_Toc382993919)

[Pixel CFG Register 1 22](#_Toc382993920)

[Pixel CFG Register 2 22](#_Toc382993921)

[DACs setting registers 22](#_Toc382993922)

[Current/Voltage Monitoring and Overriding control register 22](#_Toc382993923)

[Status Register (one per region) 23](#_Toc382993924)

[Reset value 23](#_Toc382993925)

[Operation modes 23](#_Toc382993926)

[Self-Test 24](#_Toc382993927)

[Pattern Generator Mode 25](#_Toc382993928)

[Data readout and triggering 25](#_Toc382993929)

[Readout Mode A 25](#_Toc382993930)

[Readout Mode B 26](#_Toc382993931)

[Data Port and Data Format 26](#_Toc382993932)

[Event Data Format 27](#_Toc382993933)

[Region Event Data Format 27](#_Toc382993934)

[Sample data stream 28](#_Toc382993935)

[Known issues 30](#_Toc382993936)

[Overwriting of region readout FIFOs 30](#_Toc382993937)

[READY input ignored at the beginning of data transmission 30](#_Toc382993938)

[Power-on initialization and reset 30](#_Toc382993939)

[Preliminary operations before starting a readout mode 31](#_Toc382993940)

[Test Pulsing 31](#_Toc382993941)

[Analog bias and internal DACs 33](#_Toc382993942)

[Monitoring and Overriding of the DACs 33](#_Toc382993943)

[Minimal set of signals to be connected to operate the chip 37](#_Toc382993944)

[Access the internal registers, memory locations, chip configuration 38](#_Toc382993945)

[Readout of an event frame via JTAG 38](#_Toc382993946)

[Triggering a test pulse and readout of an event frame via JTAG 38](#_Toc382993947)

[Table of chip pads 39](#_Toc382993948)

[Pad naming conventions 41](#_Toc382993949)

[Pad signals 42](#_Toc382993950)

[Pad geometry 43](#_Toc382993951)

[Pads coordinates 44](#_Toc382993952)

# Introduction

The pALPIDEfs chip is a particle detector based on Monolithic Active Pixels Sensor technology. It is implemented in a 180 nm CMOS technology for CMOS Imaging Sensors. A general block diagram of the pALPIDEfs is given in Figure 1. A floorplan view of the chip is given in Figure 2. The chip measures 15.3 mm (Y) by 30 mm (X) and contains a matrix of 512 (Y) × 1024 (X) sensitive pixels. The pixels are 28×28 µm2. A periphery circuit region of 1×30 mm2 is also present. The pixel columns are numbered from 0 to 1023 going from left to right as illustrated in the figure. Pixel rows are numbered from 0 to 511 going from the top to the bottom of the sensitive matrix.

There are four sub-matrices of 512×256 pixels, each matrix being composed by identical pixels. The four flavours of pixels (S1, S2, S2\_DR and S4) are functionally identical; they differ by the size of the charge collection diode and by the way the diode reset is implemented. Each pixel features a low-power front-end with binary (discriminated) output. The front-end is non-linear with a shaping time around 2 µs. The assertion of a STROBE/TRG signal during the response interval following an event of charge release in the pixel causes the latching of the discriminated output into an in-pixel storage cell. The pixels feature built-in test pulse injection circuit triggered by an external signal (PULSE). A digital-only test pulse mode is also available, forcing the writing of a logic one in the in-pixel memory cell.

The hits stored in the pixels are read out by means of Priority Encoder circuits (Figure 3). These provide the address of a pixel with a hit based on a topological priority. In consecutive read cycles the selected pixels are reset and the addresses of subsequent pixels with hits are generated. This continues until all hits at the inputs of the Priority Encoders are read out. The readout of the sensitive matrix to the periphery is zero-suppressed and digital power is consumed only to transfer hit information to the periphery.

The matrix is organized in 32 regions (512×32 pixels), each of them with 16 double columns being read out by 16 Priority Encoder circuits. The hits inside one region are read out sequentially in consecutive readout cycles. The readout of regions is executed in parallel and it is driven by state machines in the region readout blocks. The region readout units also contain multi-event storage SRAM memories and data compression functionality based on clustering by adjacency. The data from the 32 region readout blocks are combined and transmitted off-chip by a top level Chip Readout unit. Hit data are transmitted on a parallel 8-bit output data port using CMOS signalling.

A top-level Control block provides full access to the control and status registers of the chip as well as to the multi-event memories in the region readout blocks. The slow control interface implements a JTAG communication protocol.

All the analog signals required by the front-ends are generated by a set of 11 on-chip DACs. The DACs require only one external low-noise voltage reference (VREF) nominally at the potential of the analog supply. Analog monitoring pads (DACMONV, DACMONI) are available to monitor the outputs of the internal DACs. The same pads can be used to override one of the voltage DACs, one of the current DACs or to override the internal reference current used by all current DACs.

# Block diagram and chip interfaces

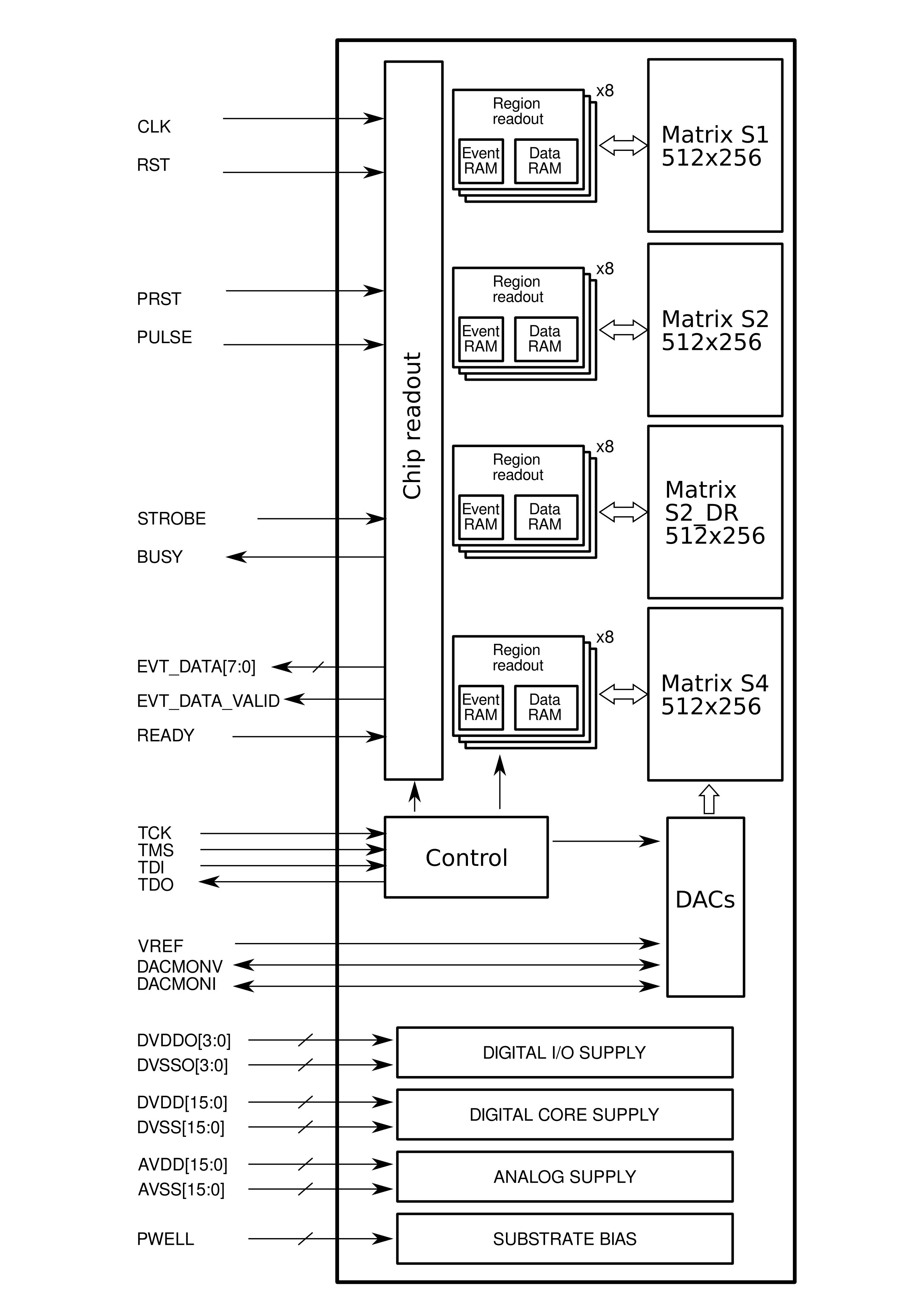


Figure 1 General block diagram of the pALPIDEfs chip

# Floorplan

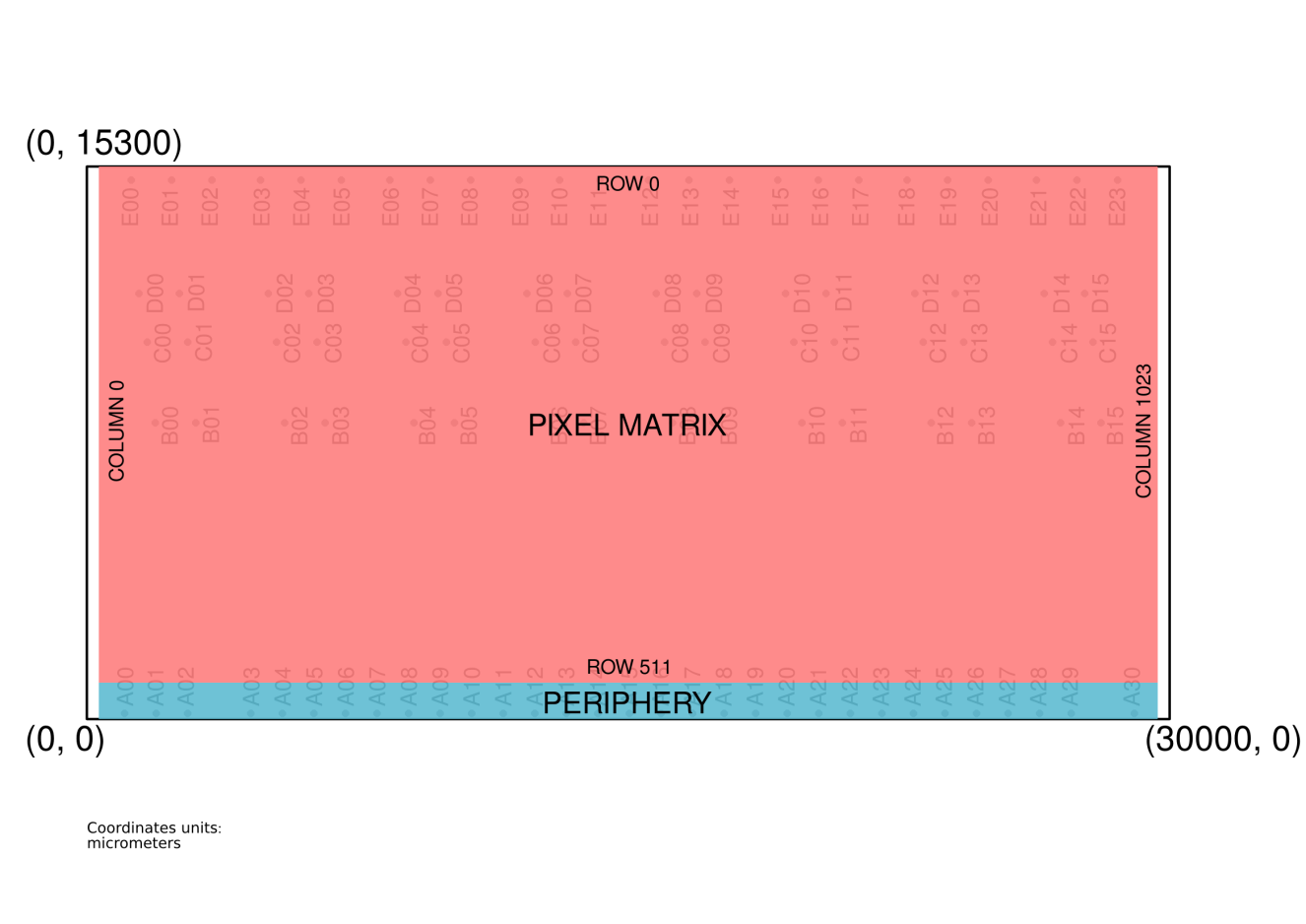


Figure 2: Chip floorplan

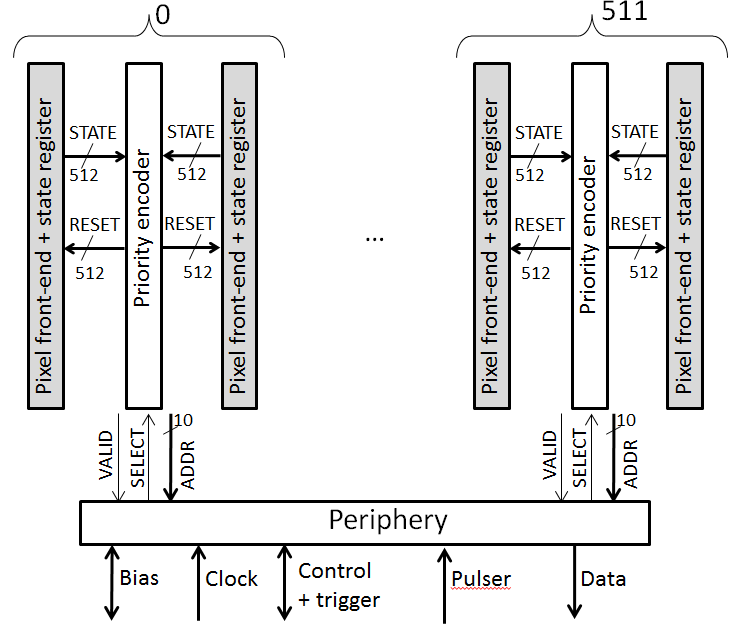


Figure 3 Block diagram of the readout of the sensitive matrix based on Priority Encoders

# Interface signals

|  |  |  |  |
| --- | --- | --- | --- |
| **Net** | **Type** | **Direction** | **Purpose** |
| TCK | DIGITAL | INPUT | Control interface clock |
| TMS | DIGITAL | INPUT | Control interface protocol signal |
| TDI | DIGITAL | INPUT | Control interface data input |
| RST | DIGITAL | INPUT | Global digital reset |
| CLK | DIGITAL | INPUT | Master clock |
| TDO | DIGITAL | OUTPUT | Control interface data output |
| EVT\_DATA\_VALID | DIGITAL, 3-STATE | OUTPUT | Valid flag for data port |
| EVT\_DATA[0] | DIGITAL, 3-STATE | OUTPUT | Data port |
| EVT\_DATA[1] | DIGITAL, 3-STATE | OUTPUT | Data port |
| EVT\_DATA[2] | DIGITAL, 3-STATE | OUTPUT | Data port |
| EVT\_DATA[3] | DIGITAL, 3-STATE | OUTPUT | Data port |
| EVT\_DATA[4] | DIGITAL, 3-STATE | OUTPUT | Data port |
| EVT\_DATA[5] | DIGITAL, 3-STATE | OUTPUT | Data port |
| EVT\_DATA[6] | DIGITAL, 3-STATE | OUTPUT | Data port |
| EVT\_DATA[7] | DIGITAL, 3-STATE | OUTPUT | Data port |
| BUSY | DIGITAL,  OPEN DRAIN | OUTPUT | Busy flag. Asserted: Logic LOW. Deasserted: HIGH IMPEDANCE |
| READY | DIGITAL | INPUT | Data transmission enable and data bus ownership |
| PRST | DIGITAL | INPUT | Pixels state reset pulse |
| STROBE | DIGITAL | INPUT | Enable latching the pixel discriminator states |
| PULSE | DIGITAL | INPUT | Trigger of internal test pulse (analog and digital) |
| DACMONV | ANALOG | OUTPUT / INPUT | Voltage monitoring output / Voltage DACs override input |
| DACMONI | ANALOG | OUTPUT / INPUT | Current monitoring output / Current DACs override input |
| VREF | ANALOG | INPUT | Input reference voltage for DACs |

Table 1 Interface signals

The DIGITAL I/Os are 1.8V CMOS compatible. Table 4, Table 5, Table 6 provide the related characteristics and requirements. All CMOS outputs with exception of BUSY have programmable drive strength.

**CLK: Main clock for all the digital circuits of the chip. The maximum design frequency is 40 MHz. All the operations of the readout circuits can be suspended by stopping the clocks (CLK and TCK) and all IO activity.**

**RST: Global reset for the digital circuits of the chip. The current implementation of the chip does not feature any power-on reset functionality.**

**TCK, TMS, TDI, TDO: JTAG port used for the slow control. In the current implementation the TCK clock shall be derived from the main digital clock (CLK) dividing it by 4. It also has to have a precise phase relationship with CLK: the TCK rising edge must arrive in the 4 ns interval following the CLK rising edge.**

**PRST:** Global signal distributed to all the pixels with the purpose of forcing the reset of all the in-pixel hit storage memory cells. The PRST input is fully asynchronous. It is buffered by a distribution tree and applied to all the pixels in parallel.

**PULSE**: Global signal distributed to all the pixels with the purpose of triggering the injection of test charge in the analog front-end or forcing high the hit storage memory cell of pre-selected pixels (digital pulsing). The PULSE input is fully asynchronous. It is buffered by a distribution tree and applied to all the pixels in parallel. However it is effective only on a set of pre-configured pixels.

**STROBE**: This signal triggers the initiation of an event readout sequence. Depending on the configuration of the readout state machine, it also defines the timing of the internal signal applied simultaneously to all the pixels (STROBE\_B) that enables the latching of the discriminated front-end output in the pixel storage element.

**BUSY:** Flag asserted after a STROBE pulse is received until the readout of the hits from the pixel matrix to the memory blocks in the periphery is completed. The BUSY output can be in one of two states: actively driven low or high impedance. The signalling is therefore active low. An external strong pull-up resistor is required for correct operation. The recommended value of the external resistor is 1 kOhm for a load of about 30 pF. The risetime of the deassertion edge entirely depends on the external load and pull-up resistor.

**EVT\_DATA\_VALID: Flag used to validate the octet on the EVT\_DATA[7:0] port.**

**EVT\_DATA[7:0]: Data readout port.** The data port pins EVT\_DATA[7:0] and EVT\_DATA\_VALID are tri-state and they are not continuously driven by the chip. A weak (>=33 kOhm) pull-down or pull-up resistor is recommended at least for the EVT\_DATA\_VALID net that is used to validate the remaining ones. Weak pull-down or pull-ups are suggested for the data wires to avoid leaving the input pins of the target device floating.

**READY:** input signal for throttling the transmission of data on the output port. When READY is asserted, provided that at least one of the EVT\_DATAPORT\_OEN1, EVT\_DATAPORT\_OEN2 configuration bits is set to 1, the EVT\_DATA[7:0] bus and EVT\_DATA\_VALID are actively driven by the chip. In the current implementation, it is required that the READY input signal is continuously kept asserted during a whole readout sequence, starting asserting it before the STROBE pulse and eventually de-asserting if after completion of the event readout. The READY input can safely be kept continuously asserted.

**DACMONV**: Analog pin with dual purpose. It can be used to monitor each of the voltages generated by the on-chip voltage DACs. It can also be used to override the internal voltage DACs. The overriding is possible for one user-selectable DAC at a given time.

**DACMONI**: Analog pin with triple purpose. It can be used to monitor each of the currents generated by the on-chip current DACs. It can also be used to override the internal current DACs. The overriding is possible for one user-selectable DAC at a given time. It can also be used to override the internal current reference, thus changing the range of all current DACs simultaneously.

**VREF**: A voltage reference is to be applied to the internal DACs through this pin. This is to be connected to the same potential of the AVDD supply voltage. Noise filtering of this reference is recommended. However any series resistance between the power supply and the pad should be lower than 100 Ω to avoid reducing the range of the DACs.

# Supply and ground nets

|  |  |  |
| --- | --- | --- |
| DVDDO | POWER | CMOS I/O drivers power supply |
| DVSSO | GROUND | CMOS I/O drivers ground |
| DVDD | POWER | Digital core power supply |
| DVSS | GROUND | Digital core ground |
| AVDD | POWER | Analog supply |
| AVSS | GROUND | Analog ground |
| PWELL | SUBSTRATE | Substrate bias (nominally SHORTED to AVSS) |

Table 2 Supply and Ground nets

The PWELL substrate bias must be connected. Reverse bias up to -6 V with respect to analog ground (AVSS) is in principle possible. For system studies it is recommended to short the PWELL bias pins to the AVSS ground. It is also recommended to bond the PWELL pads to a stiff ground reference before any other pad is bonded to reduce the risk of ESD damage. All supplies must be connected to the recommended nominal voltages. It is not compulsory to wire all the pads of a given supply net. The pads of each supply or ground net are all internally electrically shorted through the on-chip supply rails. A reduction of supply or ground connections can impair the circuit performance and operating capabilities and also increase the risk of damaging the chip.

# Recommended operating conditions

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  | MIN | TYP | MAX | Unit | Condition |
| AVSS | Analog ground |  | 0 |  | V |  |
| DVSS | Digital core ground |  | 0 |  | V | Connect to DVSSO |
| DVSSO | Digital I/O ground |  | 0 |  | V | Connect to DVSS |
| DVDD | Digital core supply | 1.62 | 1.8 | 1.98 | V | = AVDD |
| DVDDO | Digital I/O supply | 1.62 | 1.8 | 1.98 | V | = DVDD |
| AVDD | Analog supply | 1.62 | 1.8 | 1.98 | V | = DVDD |
| PWELL | Substrate bias |  | 0 | 0 | V | Connect to AVSS |
| VREF | DAC reference |  | AVDD | AVDD | V |  |
| VI | Input voltage | 0 |  | DVDDO | V |  |
| VIH | High level input voltage | 0.65\*DVDDO |  |  | V |  |
| VIL | Low level input voltage |  |  | 0.35\*DVDDO | V |  |
| IOH | High level output current |  |  | -3.4 | mA | Min drive strength  Vo > DVDDO-0.45 |
| IOH | High level output current |  |  | -7.2 | mA | Mid drive strength  Vo > DVDDO-0.45 |
| IOH | High level output current |  |  | -7.8 | mA | Max drive strength  Vo >DVDDO-0.45 |
| IOL | Low level output current |  |  | 3.4 | mA | Min drive strength  Vo < 0.45 |
| IOL | Low level output current |  |  | 7.2 | mA | Mid drive strength  Vo < 0.45 |
| IOL | Low level output current |  |  | 7.8 | mA | Max drive strength  Vo < 0.45 |
| T | Operating temperature |  | 300 |  | K |  |

Table 3 Recommended operating conditions

# Electrical characteristics

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  | MIN | TYP | MAX | Unit | Condition |
| VOH | High level output voltage | DVDDO-0.45 |  |  | V | Min drive strength,  Io = -3.4 mA |
| VOH | High level output voltage | DVDDO-0.45 |  |  | V | Mid drive strength,  Io = -7.2 mA |
| VOH | High level output voltage | DVDDO-0.45 |  |  | V | Max drive strength,  Io = -7.8 mA |
| VOL | Low level output voltage |  |  | 0.45 | V | Min drive strength,  Io = 3.4 mA |
| VOL | Low level output voltage |  |  | 0.45 | V | Mid drive strength,  Io = 7.2 mA |
| VOL | Low level output voltage |  |  | 0.45 | V | Max drive strength,  Io = 7.8 mA |
| IIL |  |  |  | 7.5 | nA |  |
| IIH |  |  |  | 73 | nA |  |
| CPAD | I/O Pad input capacitance |  | 2 |  | pF |  |

Table 4 Electrical characteristics

# Timing requirements

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  | Applies to | MIN | TYP | MAX | Unit |
| fCLK | Digital clock frequency | CLK |  |  | 40 | MHz |
| fTCK | Control port clock frequency | TCK |  | f(CLK)/4 | 10 | MHz |
| Δφ | Delay from CLK rising edge to TCK rising edge (1) | TCK↑, CLK↑ | 0 |  | 4 | ns |
| tw | Pulse width | RST | 25 |  |  | ns |
| tw | Pulse width | PULSE | 400 |  |  | ns |
| tw | Pulse width | PRST | 400 |  |  | ns |
| tsu | Setup time | TMS, TDI to TCK↑ | 3.5 |  |  | ns |
| tho | Hold time | TMS, TDI from TCK↑ | 2.6 |  |  | ns |
| tsu | Setup time | READY, STROBE to CLK↑ | 9.6 |  |  | ns |
| tho | Hold time | READY, STROBE from CLK↑ | 6.3 |  |  | ns |

Table 5 Timing requirements

The RST input signal is internally re-synchronized to the CLK domain, thus there are no setup-hold timing constraints.

(1) This is requiring that **TCK rising edge must arrive in the 4 ns interval following the CLK rising edge.**

# Switching characteristics

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | From | To | MIN | TYP | MAX | Unit | Condition |
| tpd | Propagation delay | CLK | EVT\_DATA[\*], EVT\_DATA\_VALID | 4 | 7 |  | ns | Max drive, Cload=32 pF |
| tpd | Propagation delay | CLK | EVT\_DATA[\*],  EVT\_DATA\_VALID |  | 9 | 15 | ns | Min drive, Cload=32 pF |
| tpd | Propagation delay | TCK | TDO | 4 | 10 |  | ns | Max drive, Cload=32 pF |
| tpd | Propagation delay | TCK | TDO |  | 12 | 18 | ns | Min drive, Cload=32 pF |
| tpd | Propagation delay | CLK | BUSY assertion  (falling edge) | 3.7 |  | 6.7 | ns | Rpullup 1 kOhm, Cload = 32 pF |
| tpd | Propagation delay | CLK | BUSY deassertion  (rising edge) | 24 |  | 26 | ns | Rpullup 1 kOhm, Cload = 32 pF |

Table 6 Switching characteristics

# Operating characteristics

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  | MIN | TYP | MAX | Unit | Condition |
| IAVDD | Analog current |  | 11.2 |  | mA | Nominal DACs |
| Cdig | Digital core power dissipation capacitance | 1.9 |  |  | nF | Estimate from sim |
| CIO,INT | Output switching power dissipation capacitance | 2.8 |  |  | pF | Estimate from sim |

Table 7 Operating characteristics

The analog power consumption is dominated by IBIAS (refer to the sections on the pixel front-end and DAC block) and it is also influenced by ITHR. Nominally these currents are respectively 20 nA and 0.5 nA per pixel yielding an analog current consumption of about 10.75mA of the whole pixel matrix. About 0.5 mA current is consumed by the peripheral biasing circuitry. The exact value of this depends on whether monitoring circuits are active or not.

The power dissipated in the digital core is dominated by the internal consumption in the memory blocks and by the switching of the clock tree. No low power techniques were adopted (disabling of memories, clock gating) in the current implementation of the pALPIDEfs chip. The PDVDD power can be estimated with the formula:

For nominal values this formula yields at least PDVDD ~= 250 mW, that is <IDVDD>=140 mA for the average current consumed by the digital core.

The power consumption of the I/O supply rail (DVDDO/DVSSO) rail is dominated by the output switching and is directly proportional to the load and to the activity of the outputs. It can be estimated with the formula:

where NSO is the average number of outputs transitioning from 0 to 1 at each clock cycle.

For typical values (NSO = 4, CLOAD = 15 pF, CIO,INT =2.8 pF, V = 1.8 V) this formula yields   
at least PDVDDO ~= 9.2 mW. The corresponding average current drained from the DVDDO supply during the driving of valid data on the output bus would be <IDVDDO> ~= 5.1 mA.

# Analog front-end and in-pixel digital section

Figure 4: Schematic of the pixel analog front-end(s)

The pixel front-end circuit is shown in Figure 4. There are two front-end implementations which differ for the collecting diode (D1) reset circuitry:

* PMOS reset scheme (S1, S2, S4 pixel types). VRESET establishes the reset voltage of the charge collecting node (pix\_in) and IRESET defines the maximum reset current.
* Diode reset scheme (S2\_DR pixel type), the VAUX DAC establishes the reset voltage of the charge collecting node (pix\_in).

When a particle hit is received the front end will increase the potential at the input of transistor M5 (pix\_out), forcing it into conduction. If the current in M5 overcomes IDB, M5 will drive PIX\_OUT\_B low.

The charge threshold of the pixel is defined by ITHR, VCASN and IDB. The effective charge threshold is increased by increasing ITHR or IDB. It is decreased by augmenting VCASN. The active low PIX\_OUT\_B signal is applied to the digital section of the pixel where it is used to set the hit status register.

It is possible to inject a test charge in the input node for test purposes. This is achieved by applying a voltage pulse of controllable amplitude to the VPULSE pin of the Cinj capacitor. This is controlled by the digital section of the pixel.

The digital section of the pixel is illustrated in Figure 5. The corresponding signals are listed in Table 8. The hit information is kept by a Set-Reset latch (STATE\_INT). This bit can be masked and the result is the output to the Priority Encoder (STATE signal). The latch is normally set by the front-end discriminated output PIX\_OUT\_B if STROBE\_B is asserted simultaneously. It can also be set programmatically by the DPULSE signal (digital pulse functionality). The latch is reset either by a PIX\_RESET pulse generated by the Priority Encoder during the readout, either by a global PRST pulse applied to the chip PRST input pin. The latch is sensitive to the falling edge of PIX\_RESET and it is level sensitive with respect to the PRST input.

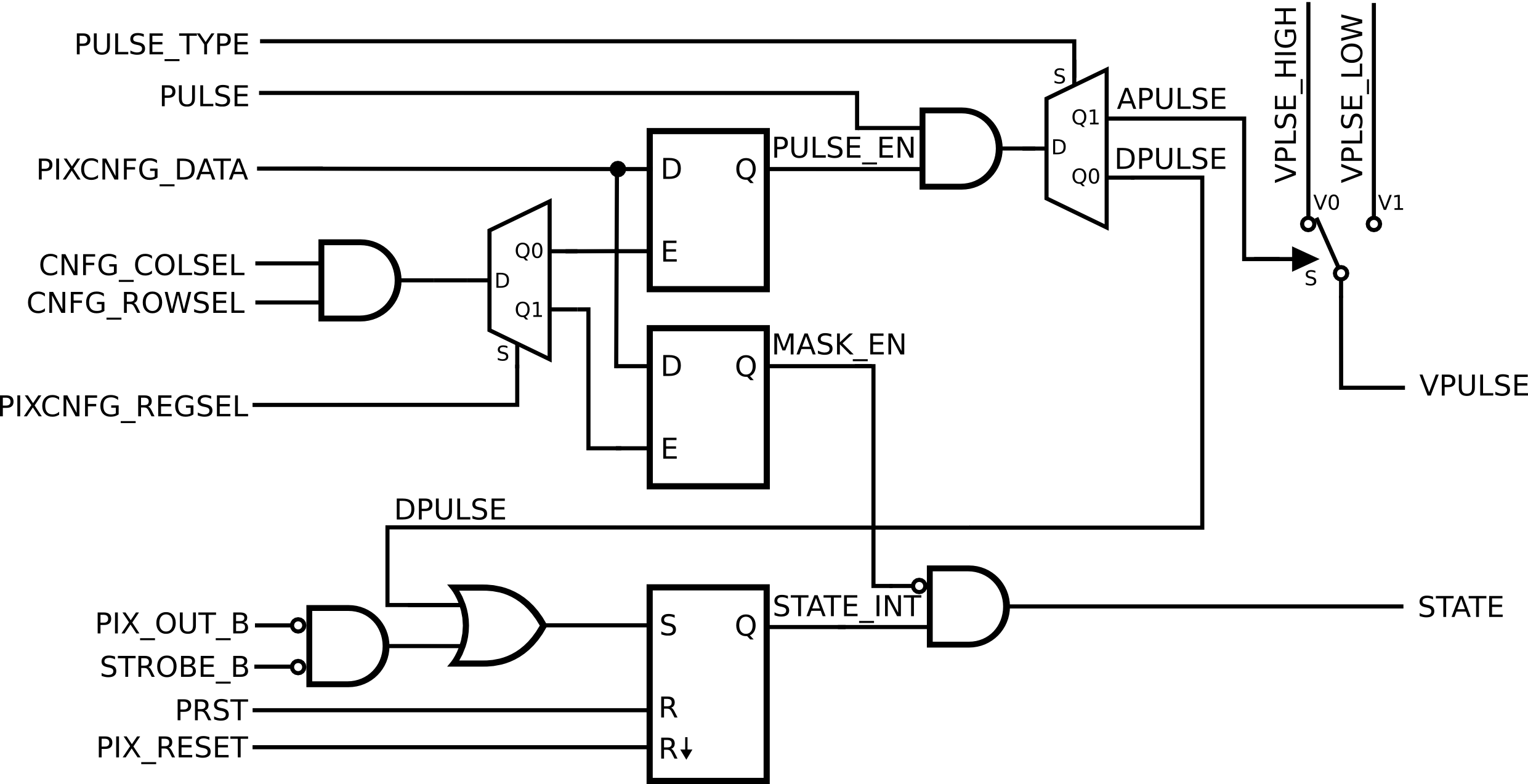


Figure 5: Functional diagram of the pixel logic

The logic provides two programmable functions: masking and pulsing.

When control bit MASK\_EN is set high, the STATE output is forced to 0, effectively masking the pixel otuput to the priority encoder. The low value provides normal functionality.

The PULSE\_EN control bit and the PULSE\_TYPE input (set globally) control the type of pulsing. The testing functionalities are enabled by setting PULSE\_EN=1, disabled otherwise. Digital pulsing is selected by PULSE\_TYPE=0, analog pulsing is activated by PULSE\_TYPE=1. In both cases the global signal PULSE, applied to one of the chip input pins, acts as trigger of the test pulse.

The digital testing consists in forcing to logic high the hit latch (STATE\_INT), bypassing the pixel front-end and the STROBE\_B signal.

The analog testing consists in the injection of test charge in the input node through Cinj (160 aF nominal). The amplitude of the applied voltage pulse is defined by the difference between VPLSE\_HIGH and VPLSE\_LOW, both set in the DAC unit. Notice that the two edges of the pulse provoke the injection of two charge pulses of opposite polarities. The rising edge of PULSE corresponds to the discharge of the collection diode, in a manner equivalent to the passage of a charged particle.

There are two D-latches to store the PULSE\_EN and MASK\_EN configuration bits. Notice that their values after power-on are undefined. Setting of these latches is done by the PIXCNFG\_COLSEL, PIXCNFG\_ROWSEL, PIXCNFG\_REGSEL, PIXCNFG\_DATA lines, all driven by the periphery control circuitry. The addressing of the pixels for configuration is based on the simultaneous selection of a specific row and a specific column. PIXCNFG\_REGSEL determines which of the two latches is to be written. PIXCNFG\_DATA provides the value to be stored in the selected latch. The simultaneous assertion of PIXCNFG\_COLSEL and PIXCNFG\_ROWSEL pixel inputs enables the selected latch. There is no direct way to read back the values in the latches from the control interface.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **Signal** | **Description** | **Logic level** | |
| **0** | **1** |
| INPUT | PULSE\_TYPE | Pulse type selection | Enable DPULSE | Enable APULSE |
| PULSE | CMOS pulse | see DPULSE and APULSE | |
| PIXCNFG\_DATA | Configuration data | D-LATCH data line | |
| PIXCNFG\_COLSEL | Column selection | Disable | Enable |
| PIXCNFG\_ROWSEL | Row selection | Disable | Enable |
| PIXCNFG\_REGSEL | Register selection | Pulse reg. | Mask reg. |
| PIX\_OUT\_B | Pixel front-end output | Active low | |
| STROBE\_B | Strobe window | Active low | |
| PRST | State register reset (global) | Active high | |
| PIX\_RESET | State register reset from priority encoder | Effective on falling edge | |
| VPLSE\_HIGH | Analog pulse high level | Analog | |
| VPLSE\_LOW | Analog pulse low level | Analog | |
| INTERNAL | PULSE\_EN | Pulse enable | Active high | |
| MASK\_EN | State register mask enable | Active high | |
| STATE\_INT | State register data | Active high | |
| APULSE | VPULSE voltage level selection | VPLSE\_HIGH | VPLSE\_LOW |
| DPULSE | Digital Pulse | Hold STATE\_INT | STATE\_INT = 1 |
| OUTPUT | VPULSE | Voltage step for test charge injection into pix\_in net | Qinj = Δ(VPULSE) · Cinj  Cinj = 160 aF | |
| STATE | State register value to priority encoder (if MASK\_EN = 0) | Active high | |

Table 8: Signals of the pixel cell

# Double column and region numbering

Looking at the chip with the digital periphery on the bottom, the leftmost region is region 0 and the rightmost region is region 31 (see Figure 6).

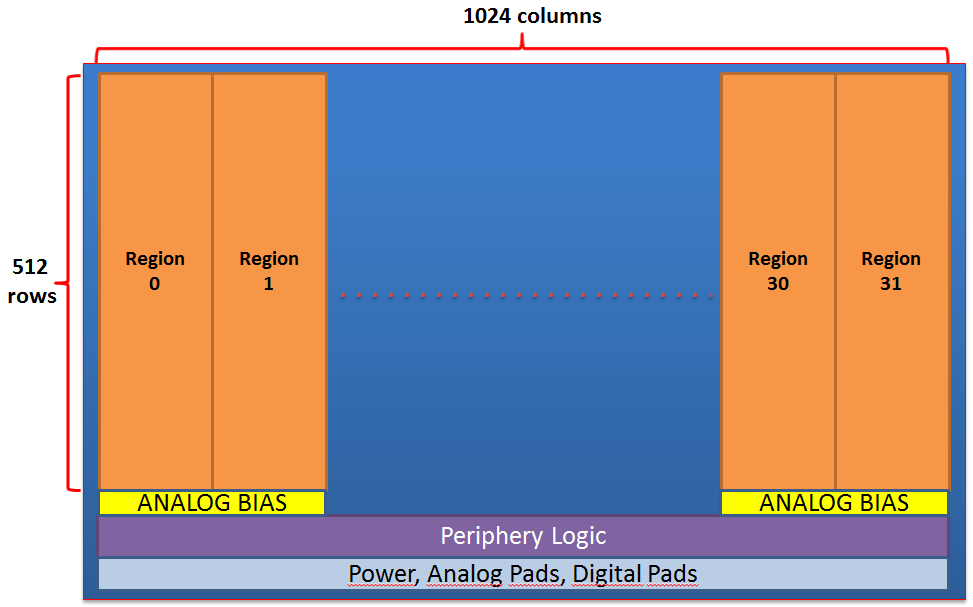


Figure 6: Region numbering

Each region contains 16 double columns. Double column 0 is the leftmost and double column 15 is the rightmost (see Figure 7).

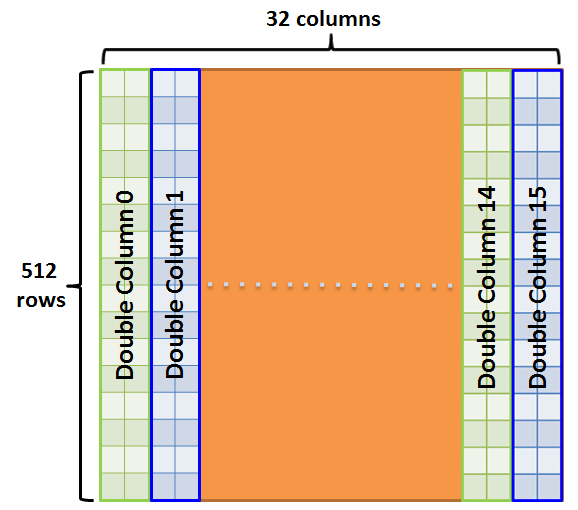


Figure 7: Double column numbering inside of a region

# Priority Encoders and pixel indexing

The matrix of pixels is readout by an array of 512 Priority Encoder blocks as illustrated in Figure 3. The pixels are arranged in double columns and the regions at the middle of each double column are occupied by the Priority Encoders, as illustrated in Figure 8. The indexing of the pixels in the readout data words is defined by the Priority Encoders. The indexing of the pixels en each double column is illustrated in Figure 9.

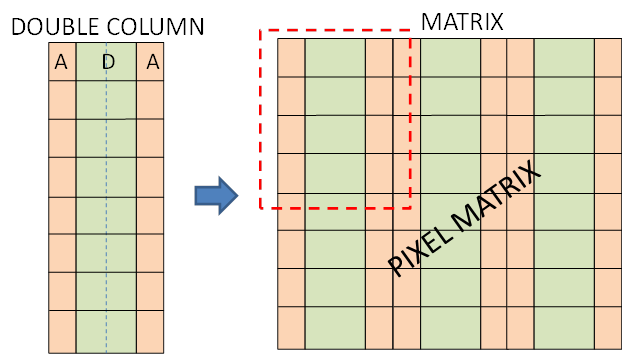


Figure 8: Grouping of pixels in double columns and Priority Encoders

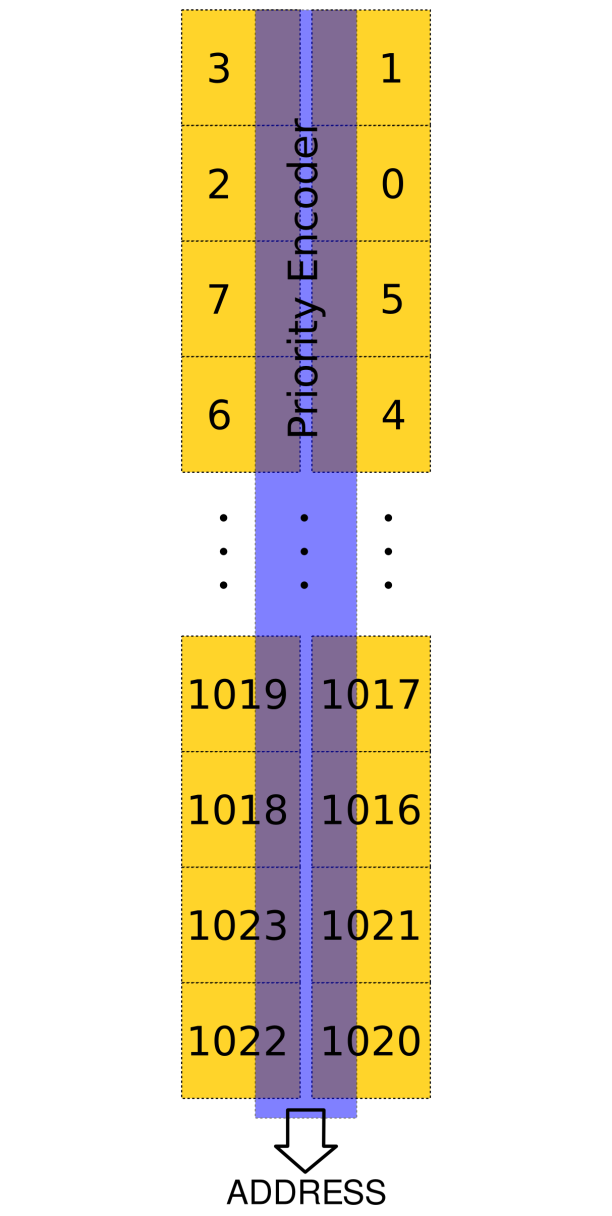


Figure 9: Indexing of pixels inside a double column provided by the Priority Encoders

# Configuration Interface

The configuration interface of the pALPIDEfs chip implements the JTAG communication protocol. The Instruction Register is 18 bit wide. All the chip internal registers and also the word locations of the memory blocks are mapped to JTAG Data Registers selectable via the Instruction Register. The Data Registers appear to the JTAG controller as 16 bit wide. Figure 10 shows the standard JTAG state machine diagram used for reference during the implementation.

A slow control transaction is constituted by two subsequent JTAG scans: one IR scan to set the desired address and access type in the IR and a subsequent DR scan to read/write the data from/into the selected register. All slow control operations therefore require the shifting of 34 bits in two shift sequences (IR scan and DR scan). For both type of JTAG transactions (Instruction Register Scan and Data Register Scan), the ordering of the bits in the serial lines (TDI, TDO) is MSB first and LSB last.

**In the current implementation of pALPIDEfs, the JTAG clock domain and the internal clock domain must be synchronous. The JTAG clock TCK shall be derived dividing by 4 the pALPIDEfs main clock (CLK).**

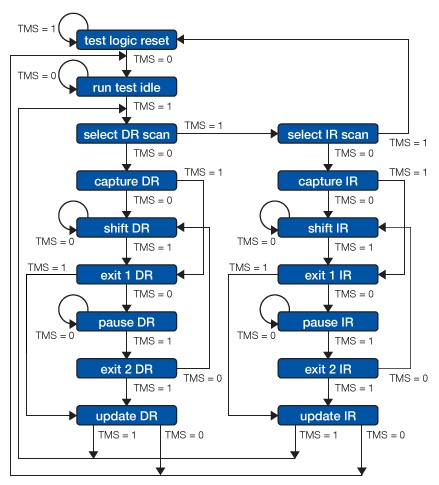


Figure 10: JTAG controller state machine diagram

## JTAG I/O signals

|  |  |  |
| --- | --- | --- |
| **NAME** | **TYPE** | **DESCRIPTION** |
| TCK | Input | Clock signal (one fourth of CLK frequency) |
| TMS | Input | Test Mode Select (Control signal for the TAP state machine) |
| TDI | Input | Test Data Input (Serial data input) |
| TDO | Output | Test Data Output (Serial data output) |

## Instruction

The instruction is 18 bit wide, with MSB sent first and LSB last.

|  |  |
| --- | --- |
| **BIT** | **DESCRIPTION** |
| 17 | RESERVED. **Must be 0** |
| 16 | Read/Write(0 Write – 1 Read) |
| 15:0 | ADDRESS (Reg/Mem location address) |

## Address field of the Instruction Register

|  |  |
| --- | --- |
| **BIT** | **DESCRIPTION** |
| 7:0 | SUB\_ADDR[8]. Address of location inside the memory or register in group |
| 10:8 | BASE\_ADDR[3]. Address of selected memory or register group (0-7) |
| 15:11 | RGN\_ADDR[5]. Address of selected region (0-31) |

## Data Registers

The data registers all appear as 16 bit wide, with MSB sent first and LSB last.

## Control Write operation

A control write operation requires the shifting of 34 bits, 18 bit for setting the Instruction Register and 16 bit for setting the selected Data Register. The first bit to be shifted in the IR is reserved and must be 0. The second bit is 0 for a write operation; the next 16 bits shifted in the IR are the location address. During the subsequent DR scan, the 16 bit word to be written is shifted in (MSB first).

Figure 11 shows an example of a JTAG write operation on a destination register. JTAG\_instruction and JTAG\_datain represent respectively the instruction and the data that have to be serially shifted inside of the chip so that the operation can be executed successfully. By properly driving the TMS signal the JTAG SM executes a complete IR scan during which the 18 bit instruction is shifted in the chip through the TDI input (MSB first). Once the instruction is completely shifted, the destination register (which in the example is the control register) is then selected addressed and can be written (or read depending on the value of the 2nd MSB of the instruction, see next paragraph). Since the 2nd MSB of the instruction is low in the example, the destination register is selected for writing. The write data are shifted in during a subsequent DR scan driven by the TMS signal. The TMS signal is then kept high to bring the JTAG SM to the “Test Logic Reset” state.

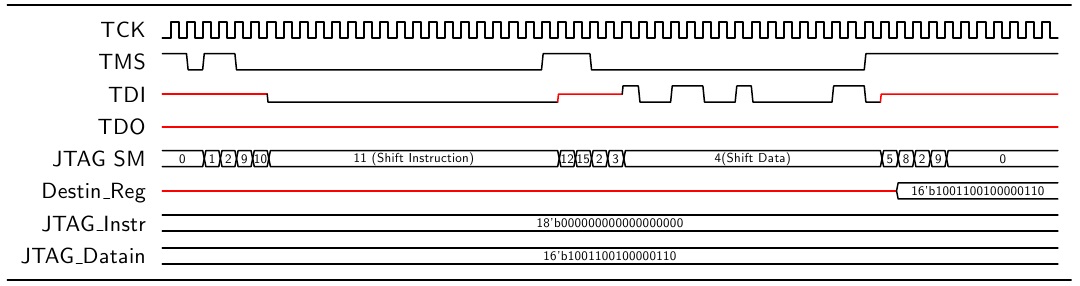


Figure 11: Timing diagram of a JTAG write operation. The destination register can be either a register or a memory location. Red lines are "don't care" (X) values

## Control Read operation

A control read operation requires the shifting of 34 bits, 18 bit for setting the Instruction Register and 16 bit for reading the selected Data Register. The operation requires the setting of the 18 bits of the Instruction Register with the desired address by an IR scan transaction. The MSB of the IR is reserved and must be 0; the second MSB bit is 1 for a Control Read operation; in this way the internal registers are not updated at the end of the subsequent DR scan transaction. The next 16 bits shifted in the IR are the address of the register (MSB first).

The requested data are then shifted out by the TDO port during the subsequent DR scan of 16 bits. These are the data read from the selected register or memory location (MSB first). The bits applied to the TDI input during the DR scan are ignored. If an unassigned address is selected for reading, the word 0xFFFF will be shifted out.

Figure 12 shows an example of a JTAG read operation. In this example the 2nd MSB of the instruction is high in order to enable the reading of the target register. Once the instruction is shifted inside of the chip during the IR scan, the TMS is driven to reach the DR scan states in which the content of the register previously selected is shifted outside the chip through the TDO output with the MSB going out first.

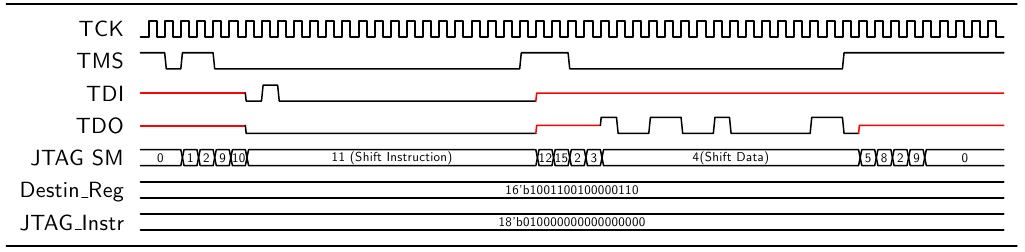


Figure 12: Timing diagram of a JTAG read operation. The destination register can be either a register or a memory location. Red lines represent don’t care (X) values

## Description of address space

|  |  |  |  |
| --- | --- | --- | --- |
| **RGN\_ADDR** | **BASE\_ADDR** | **SUB\_ADDR** | **SELECTION** |
| DON’T CARE | 0 | 0 | Periphery Control Register |
| NC | 0 | 1 | Region Disable Register: regions from 15 down to 0 |
| NC | 0 | 2 | Region Disable Register: regions from 31 down to 16 |
| NC | 0 | 3 | STROBE\_B Timing Register |
| 0-31 | 1 | 0-15 | Memory location of the event length FIFO for selected region |
| 0-31 | 2 | 0-255 | Memory location of data FIFO for selected region |
| 0-31 | 3 | 0 | Column Disable Register for selected region |
| NC | 4 | NC | RESERVED |
| NC | 5 | 0 | Pixel CFG register 1 |
| NC | 5 | 1 | Pixel CFG register 2 |
| NC | 6 | 0 | VRESET[15:8]; VAUX [7:0]. DACs setting registers. |
| NC | 6 | 1 | VCASP[15:8]; VCASN[7:0]. DACs setting registers. |
| NC | 6 | 2 | VPULSEH[15:8]; VPULSEL[7:0] DACs setting registers |
| NC | 6 | 3 | IAUX2[15:8]; IRESET[7:0]. DACs setting registers |
| NC | 6 | 4 | IDB[15:8]; IBIAS[7:0]. DACs setting registers |
| NC | 6 | 5 | UNUSED[15:8]; ITHR[7:0] DAC setting register |
| NC | 6 | 6 | Current/Voltage monitoring and overriding control register |
| 0-31 | 7 | NC | Status register |

## Internal registers

### Periphery Control Register

|  |  |
| --- | --- |
| **BIT** | **DESCRIPTION** |
| 1:0 | Chip Mode. 0 Configuration Mode, 1 Readout Mode A(STROBE\_B always asserted), 2 Readout Mode B (STROBE\_B asserted after trigger), 3 Pattern Generator Mode |
| 2 | Clustering Enabled (1) / Disabled (0) |
| 3 | Start Self Test (Only if Chip Mode is 0). Reset automatically after 1 clock cycle. |
| 4 | Strobe of pixel configuration, enable row selection. Automatically self-resetting after 16 clock cycles. |
| 5 | EVT\_DATA\_PORT\_OEN1 |
| 6 | EVT\_DATA\_PORT\_OEN2 |
| 7 | RESERVED |
| 15:8 | Matrix Readout Start Delay. Delay time between STROBE\_B deassertion and beginning of the readout of Priority Encoders (number of CLK clock cycles. Applies to Readout Mode A and Readout Mode B) |

Bit 4 Strobe of pixel configuration has the purpose to activate the access to the in-pixel configuration latches enabling temporarily the propagation of the Row Selection signals to the pixel matrix.

### Region Disable Registers

Two 16 bit registers used to disable the readout of specific regions. When a bit is set to 1, the corresponding region is disabled.

### STROBE\_B Timing Register

|  |  |
| --- | --- |
| **BIT** | **DESCRIPTION** |
| 15:0 | Readout Mode A: delay between end of matrix readout and the automatic re-assertion of STROBE\_B (number of CLK clock cycles).  Readout Mode B: duration of the STROBE\_B pulse applied to the matrix after the trigger arrival (number of CLK clock cycles). |

### Column Disable Register (one per region)

A 16 bit register used to disable the readout of a double column of the selected region. When a bit is set the corresponding column is disabled.

### Pixel configuration registers

In each pixel there are 2 configurable registers: the Mask register and the Pulse Enable register (refer to the section on the digital circuits in the pixels). These registers can be addressed and written by using the 2 following periphery registers and bit 4 of the “Periphery Control Register”. The transmission to the matrix of the row selection signal is gated by bit 4 of the “Periphery Control Register”. This is meant to be set to one after the Pixel CFG Register 1 and Pixel CFG Register 2 have been appropriately written thus enabling the propagation of the row enable signals to the matrix for a duration of 16 clock cycles.

### Pixel CFG Register 1

|  |  |
| --- | --- |
| **BIT** | **DESCRIPTION** |
| 8:0 | Pixel row select address. Selects the row of pixels needs to be addressed, i.e. for which row the CFG\_ROWSEL line will be asserted. |
| 9 | Sets all rows. If set to one the row address field [8:0] is ignored and all rows are enabled simultaneously for configuration. |
| 10 | PIXCNFG\_REGSEL. Selection of the in-pixel register to be addressed: ‘0’ for the Pulse Enable register, ‘1’ for the Mask register. |
| 11 | PIXCNFG\_DATA. Data to be written in the target register |
| 15:12 | Not used |

### Pixel CFG Register 2

|  |  |
| --- | --- |
| **BIT** | **DESCRIPTION** |
| 9:0 | Pixel column select address. Selects which column of pixels needs to be addressed, i.e. for which column the CFG\_COLSEL line is asserted. |
| 10 | All Pixel columns selected. If set to one the column address field [9:0] is ignored and all columns are enabled simultaneously for configuration. |
| 11 | PULSE\_TYPE. Controls the type of test pulse functionality enabled in the pixel circuits: ‘0’ for digital pulsing, ‘1’ for analog pulsing. Applied simultaneously to the whole matrix. |
| 15:12 | Not used |

### DACs setting registers

For each of the DACs, there is an 8-bit setting field. Pairs of these 8-bit registers are combined into 16-bit registers addressable in a single read-write transaction.

### Current/Voltage Monitoring and Overriding control register

|  |  |
| --- | --- |
| **BIT** | **DESCRIPTION** |
| 2:0 | Voltage DAC selection field. Contains a code selecting the voltage DAC to be monitored or overridden by the DACMONV pad |
| 5:3 | Current DAC selection field. Contains a code selecting the current DAC to be monitored or overridden by the DACMONV pad |
| 6 | SWCNTL\_DACMONI. Configures the DAC block to enable the overriding of the selected current DAC. ‘0’ for monitoring, ‘1’ for Overriding. |
| 7 | SWCNTL\_DACMONV. Configures the DAC block to enable the overriding of the selected voltage DAC. ‘0’ for monitoring, ‘1’ for Overriding. |
| 15:8 | Not Used |

The following table gives the correspondence between the value in the [2:0] field of the register and the selected voltage DAC.

|  |  |
| --- | --- |
| **Binary coded value** | **DESCRIPTION** |
| 0 | OFF. No DAC selected. |
| 1 | SWCNTL\_VAUX |
| 2 | SWCNTL\_VCASN |
| 3 | SWCNTL\_VCASP |
| 4 | SWCNTL\_VPLSE\_HIGH |
| 5 | SWCNTL\_VPLSE\_LOW |
| 6 | SWCNTL\_VRESET |
| 7 | OFF. No DAC selected. |

The following table gives the correspondence between the value in the [5:3] field of the register and the selected current DAC.

|  |  |
| --- | --- |
| **Binary coded value** | **DESCRIPTION** |
| 0 | OFF. No DAC selected. |
| 1 | SWCNTL\_IRESET |
| 2 | SWCNTL\_IAUX2 |
| 3 | SWCNTL\_IBIAS |
| 4 | SWCNTL\_IDB |
| 5 | SWCNTL\_IREF. This allows overriding the internal current reference used by all current DACs. |
| 6 | SWCNTL\_ITHR |
| 7 | OFF. No DAC selected. |

### Status Register (one per region)

|  |  |
| --- | --- |
| **FIELD** | **DESCRIPTION** |
| 0 | Region Pixel Self-Test result. |
| 1 | Region Memory Self-Test result. |
| 2 | Asserted if all columns of the region are disabled. Read only. |
| 5:3 | Region Readout SM State. Read only. |
| 7:6 | Region Memory Self-Test SM State. Read only. |
| 11:8 | Periphery Readout SM State. Read only. Independent of the selected region. |
| 15:12 | Not used |

### Reset value

The reset value (after a RST pulse) of all the periphery registers is binary 0, all bits set to zero.

# Operation modes

The chip can be operated in 3 major modes according to the values of the Chip Mode field of the main chip Control Register:

1. Configuration Mode (Chip Mode field = "00")  
   In this mode it is possible to:

* Read or Write each register or memory location through the JTAG port.
* Perform a Self-Test of the Chip. This operation also requires the "Start Self-Test" field in the control register to be set to high. For more details see the Self-Test dedicated Section.

1. Readout mode

In this mode the chip performs the readout of the matrix each time an external trigger pulse is received through the STROBE pad.

There are 2 readout modes:

* Readout Mode A (Chip Mode field = "01")
* Readout Mode B (Chip Mode Field = "10")

For more details on readout modes see the Readout and Triggering section.

1. Pattern Generator mode (Chip Mode field = "11").   
   In this mode the chip sends out a data pattern through the event data port.

In readout and pattern generator modes it is still possible to read and write the registers via the JTAG interface. On the other hand, JTAG access to the memory locations of the Region Readout SRAM blocks (event memory and data memory) is disabled.

In readout mode, it is advisable to act only on the following registers:

* Periphery Control Register
* Pixel CFG register 1
* Pixel CFG register 2
* VAUX (0-7), VRESET (8-15) register
* VCASN (0-7), VCASP (8-15) register
* VPULSEL (0-7), VPULSEH (8-15) register
* IRESET (0-7), IAUX2 (8-15) register
* IBIAS (0-7), IDB (8-15) register
* ITHR register
* Current/Voltage Monitor register
* Status register

# Self-Test

The Self-Test is an automatic test mode that can be run to quickly identify faults inside the chip. During self-test it is not possible to use the JTAG port. The maximum time duration of the self-test operation is 544 clock cycles (13.6 μs at 40 MHz).

During self-test 2 operations are automatically performed by the chip:

1. Check if there are stuck-at-one pixels
2. Check if there are non-functional bits in the SRAM blocks of the region readout blocks.

**Check for stuck-at-one pixels**

A readout sequence of the Priority Encoders is executed to find if there are pixels whose state registers are stuck-at-one and cannot be reset. This test is performed in parallel for the 32 regions. The result of the test performed in a region is written into its status register, in the field “Region Pixel Self-Test result”. If the self-test identifies at least one faulty pixel in a region the Pixel Status bit of the status register of that region is set.

**Search for faulty memory locations in the chip periphery**

A sequence of write-read accesses to the SRAM blocks of the Region Readout units is executed to find if there are faulty bits in the SRAM blocks. This test is executed in parallel for the regions and if at least one malfunctioning bit is found in any location, the bit “Region Memory Self-Test result” of the regions status register is set.

The flags with the result of the tests can be read via the JTAG interface once the Self-Test sequences are completed.

# Pattern Generator Mode

When the Pattern Generator mode is activated the top level readout scans in sequence the 32 data memories of the regions reading through all their locations (from region 0 to region 31 and from word 0 up to 255), pushing the data on the output data port byte-by-byte. The least significant byte of each 16-bit word is always sent first. This produces a repeated pattern of 32×256×2 bytes. Notice that this pattern is programmable by writing directly to the region data memories. This is achievable operating the chip in Configuration Mode before enabling the Pattern Generator mode.

# Data readout and triggering

The chip can be operated in 2 different readout modes called mode A and mode B in the following. In both modes the chip performs the readout of the pixel matrix each time a pulse is received on the STROBE pad. This signal is registered at the input and it influences the behavior of the Top Level State Machine.

An internal signal STROBE\_B (active low) is driven by the State Machine in different ways depending on the readout mode. The STROBE\_B signal is the one applied to the pixels controlling the latching of the discriminated front-end outputs in the in-pixel state latches. The STROBE input influences either the time of de-assertion (mode A) either the timing of the assertion of STROBE\_B (mode B).

## Readout Mode A

In Readout Mode A (Figure 13) the STROBE\_B signal is kept asserted until the arrival of an external STROBE pulse. After this event it is de-asserted, the pixels stop latching the discriminator outputs and the readout of the matrix begins. The time interval between the deassertion of STROBE\_B and the start of the readout is programmable (see Periphery Control register, field Matrix Readout Start Delay). Once the matrix readout is complete the STROBE\_B is automatically re-asserted until another STROBE pulse is received. The time interval which goes from the end of the readout to the reassertion of the STROBE\_B signal is also programmable (refer to STROBE\_B Timing Register). The transmission of data off-chip begins immediately after completion of the transfer of data from the matrix to the SRAM memory blocks in the periphery.

In this mode, the STROBE pulse effectively operates as a start of readout and the pixels integrate all discriminated events during the periods of assertion of STROBE\_B.

The BUSY output is asserted after receiving the STROBE pulse and it is de-asserted simultaneously with the reassertion of the internal STROBE\_B signal.

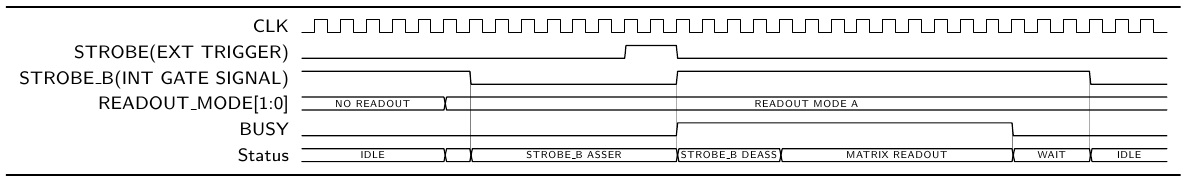


Figure 13: Readout mode A sample waveforms (BUSY is illustrated here active-high. The BUSY pad is active low).

## Readout Mode B

In Readout Mode B (Figure 14), upon the arrival of a pulse on STROBE the periphery of the chip asserts the internal STROBE\_B signal. The width of STROBE\_B is programmable (refer to STROBE\_B Timing Register). The matrix is then read out through the Priority Encoders and the data are transferred to the memories in the periphery. The time interval between the deassertion of the STROBE\_B signal and the start of the readout is programmable (see Periphery Control register, field Matrix Readout Start Delay). After the matrix readout phase, the chip is ready to receive another STROBE pulse. The transmission of data off-chip begins immediately after completion of the transfer of data from the matrix to the SRAM memory blocks.

In this mode, the STROBE pulse effectively controls the timing of the STROBE\_B signal and also initiates a readout sequence. The pixels latch the events above threshold during the interval of assertion of STROBE\_B.

The BUSY output is asserted after receiving the STROBE pulse and it is de-asserted upon completion of the transfer of data from the matrix to the SRAM memory blocks.

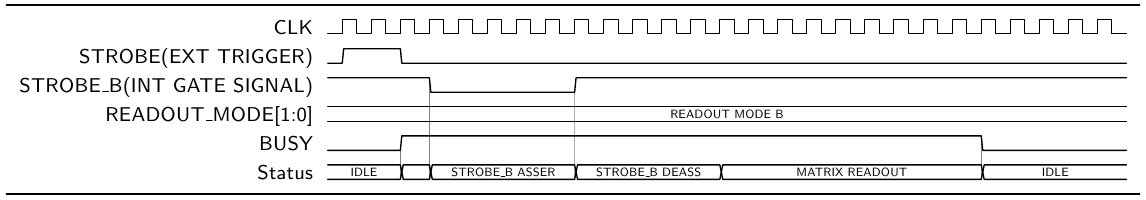


Figure 14: Readout mode B sample waveforms (BUSY is illustrated here active-high. The BUSY pad is active low)

# Data Port and Data Format

The event data port is the main readout port composed of the following signals:

• EVT DATA[7:0]

• EVT DATA VALID

• READY

The EVT\_DATA[7:0] is an 8-bit output bus through which the event data is sent out by the chip. While the chip is transmitting data through the EVT\_DATA bus the EVT\_DATA\_VALID output signal is kept high by the chip. This allows an external readout system to know when any useful data is put on the EVT\_DATA bus.

**READY** is an input signal for throttling the transmission of data on the output port. When READY is asserted, provided that at least one of the EVT\_DATAPORT\_OEN1, EVT\_DATAPORT\_OEN2 bits are set to 1, the EVT\_DATA[7:0] bus and EVT\_DATA\_VALID are actively driven by the chip and are not in high-impedance.

## Event Data Format

Since the chip is functionally divided into 32 identical regions, the data format follows the same structure. For each event the chip sends out first the data which corresponds to the leftmost region (region 0) while the data which corresponds to the rightmost region (region 31) is sent at the end of each event data transmission. Data read in an event that come from the same region are called region event data. Figure 15 shows a simplified data transfer of the chip through the event data port. The maximum operating frequency of CLK is 40 MHz, which means a maximum supported bandwidth of 320 Mbits/s (40 MB/s).

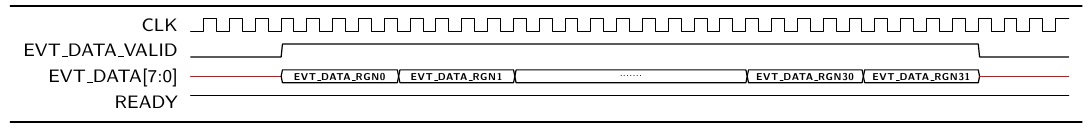


Figure 15: Simplified wave diagram of data transmission through the event data port

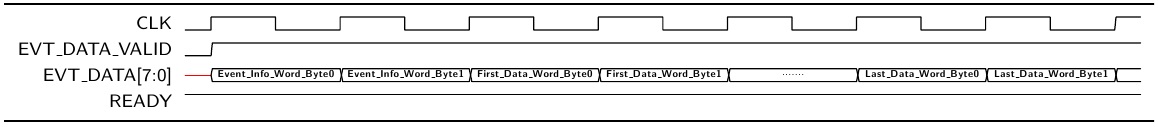
The event data is formatted into 16-bit words. Since the event data bus is 8-bit wide, each of these words is divided in 2 bytes sent sequentially. The least significant byte of each 16-bit word is always sent first (Figure 16). The transmission starts with the event info word. After the event info word is sent out, the transmission of the pixel data starts, following the same scheme for each data word. Once the last data word of one region is sent out, the chip starts to transmit the data of the next region following the same scheme (event info word and then data words).

Figure 16: Expanded view of the data transmission of the first (leftmost) region of the chip through the event data port

## Region Event Data Format

Data from each region are constituted of a first header word (Region Event Info Word) followed by a variable number of Data Words.

1. **Region Event Info Word**

**15 11 10 8 7 0**

|  |  |  |
| --- | --- | --- |
| REGION NUMBER (Bits 4:0) | Not Used (Bits 2:0) | REGION EVENT LENGTH (Bits 7:0) |

The event info word is always transmitted by each region even if the number of datawords is zero in a given event. This header contains 2 fields:

• **RGN NUMBER** - Bits 15:11. It represents the source (region) of the region event data according to Figure 6.

• **REGION EVENT LENGTH** - Bits 7:0. It is the number of Data Words transmitted subsequently in the region event data (excluded the Region Event Info Word).

The field of bits [10:8] is not used and they are always set to zero.

1. **Data Word**

15 14 13 10 9 0

|  |  |  |
| --- | --- | --- |
| CLUSTER SIZE (Bits 1:0) | DOUBLE COLUMN ADDR (Bits 3:0) | PIXEL ADDR (Bits 9:0) |

The Data Words contain 3 fields:

• **DOUBLE COLUMN ADDRESS** - Bits 13:10 contain the binary coded index of the double column containing the hit pixel according to Figure 7.

• **PIXEL ADDR** - Bits 9:0 contain the binary coded index of the pixel inside the double column according to the coding of Figure 9.

• **CLUSTER SIZE** - Bits 15:14.

* **Clustering disabled**: always set to 0 by the chip
* **Clustering enabled**: number of consecutive hit pixels in a double column which follow the first hit pixel identified by the **PIXEL ADDRESS**. For single pixel sets this field is binary 0, for two consecutive pixels is 1, for three consecutive pixels is 2, for four consecutive pixels is 3.

## Sample data stream

In the following example it is assumed that the frame contains one single fired pixel, pixel number 511 of column number 7 of region number 15.

The data format consists of 16-bit words as described in the previous sections. The sequence of output words is the following:

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| x0000 | x0800 | x1000 | x1800 | x2000 | x2800 | x3000 | x3800 | x4000 | x4800 | x5000 |
| x5800 | x6000 | x6800 | x7000 | x7801 | **x1DFF** | x8000 | x8800 | x9000 | x9800 | xA000 |
| xA800 | xB000 | xB800 | xC000 | xC800 | xD000 | xD800 | xE000 | xE800 | xF000 | xF800 |

Each empty region sends only an header containing the region number and the number of datawords which is zero:

|  |  |  |
| --- | --- | --- |
| Region number [15:11] | Not used [10:8] | Region Event Length[7:0] |
| 5'b00001 (region numer = 1) | 3'b000 | 8'b00000000 (num of dw = 0) |

The fired pixel dataword (**x1DFF**) has the following format:

|  |  |  |
| --- | --- | --- |
| Cluster size [15:14] | Double column [13:10] | Pixel Address [9:0] |
| 2'b00 (cluster size = 0) | 4'b0111 (Double column = 7) | 10'b0111111111 (Pixel address = 511) |

The LSB (least significant BYTE) of the 16 bit words is always sent first on the 8 bit port. This leads to the following stream of bytes sent out through the event data port (in order of transmission), still assuming that pixel number 511 of the column number 7 of region 15 was fired:

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 00 | 00 | 00 | 08 | 00 | 10 | 00 | 18 | 00 | 20 | 00 | 28 | 00 | 30 | 00 | 38 | 00 | 40 | 00 | 48 | 00 | 50 |
| 00 | 58 | 00 | 60 | 00 | 68 | 00 | 70 | 01 | 78 | FF | 1D | 00 | 80 | 00 | 88 | 00 | 90 | 00 | 98 | 00 | A0 |
| 00 | A8 | 00 | B0 | 00 | B8 | 00 | C0 | 00 | C8 | 00 | D0 | 00 | D8 | 00 | E0 | 00 | E8 | 00 | F0 | 00 | F8 |

# Known issues

## Overwriting of region readout FIFOs

The FIFO memories that receive the hit data during the matrix readout are not protected for overwrite once they get full. The data FIFOs are 256 words deep. Therefore up to 256 pixel hits in a region can be safely stored assuming to begin the readout with empty FIFOs. If clustering is enabled, the limits become 256 clusters per region. However, assuming that the chip is operated in single event mode, i.e. that the data of a frame are fully readout before issuing the next STROBE, the data should remain consistent. This is true also in case of a highly occupied frame causing overflow during the writing into the FIFOs. The data are overwritten but the pointers and the counters also wrap-around. The expected outcome is that the chip would transmit out the last N modulo 256 hits (or clusters) that are readout from each region during the readout of the matrix by the Priority Encoders. It is also noticed that masking all but 256 pixels in a region is another mean to overcome the potential issues with high occupancy frames.

## READY input ignored at the beginning of data transmission

If READY is de-asserted at the start of an event data transmission sequence, the first byte of the stream is sent to the output port but the drivers are disabled because of READY low. The first byte is therefore lost. This contains the length of the data of the first region. The reconstruction of the data stream becomes cumbersome. This is due to a bug in the top level readout state machine: the READY input is not sampled in the idle state. However the bug affects the transmission of the first byte only. The SM reacts correctly to the READY input during the subsequent transmission phases until the completion of the event data sequence. This is the reason for recommending that the READY signal is asserted before sending a STROBE pulse to the chip and kept (continuously) asserted during the event data transmission.

# Power-on initialization and reset

After power-on, the chip must be reset and initialized.

1. All the registers and State Machines of the periphery shall be forced into the reset state: assert the RST signal. The reset value of all the periphery registers, including the DAC setting registers is binary 0, all bits set to zero.
2. Set the DACs to required values: write the appropriate binary codes into the eleven 8-bit fields of the DAC setting registers
3. Initialize to a known value (reset) the in-pixel MASK\_EN registers:
   1. Select all rows, select MASK\_EN and reset PIXCNFG\_DATA: write hex value x0600 into Pixel CFG Register 1
   2. Select all columns: write hex value x0400 into Pixel CFG Register 2
   3. Execute the pixel configuration transaction: set bit 4 of the Periphery Control Register to binary 1
4. Initialize to a known value (reset) the in-pixel PULSE\_EN registers:
   1. Select all rows, select PULSE\_EN and reset PIXCNFG\_DATA: write hex value x0200 into Pixel CFG Register 1
   2. Select all columns: write hex value x0400 into Pixel CFG Register 2
   3. Execute the pixel configuration transaction: set to 1 bit 4 of the Periphery Control Register
5. Reset the STATE registers in the pixels: assert the PRST input signal

# Preliminary operations before starting a readout mode

After reset, the chip automatically enters in configuration mode. In this mode it is not possible to read the pixel matrix while registers and SRAM memories can be accessed via the JTAG interface. To enter the readout modes it is necessary to set the control register, field Chip Mode, via the JTAG interface. Before doing that, it might be needed to perform one or more of the following operations:

* Set field [15:8] Matrix Readout Start Delay of the Periphery Control Register. This field controls the delay from the deassertion of STROBE\_B and the beginning of the matrix readout. (applies to Readout Mode A and Readout Mode B)
* Set STROBE\_B Timing Register. In Readout Mode A this establishes the delay between the completion of the matrix readout and the automatic re-assertion of the internally driven STROBE\_B signal. In Readout Mode B this establishes the duration of the STROBE\_B pulse, asserted on arrival of the external trigger (STROBE input).

• Enable the output drivers. The data port is driven by adjustable strength buffers, which are by default disabled. These outputs must be enabled before the readout. To enable these buffers it is necessary to set the EVT\_DATAPORT\_OEN1 and/or the EVT\_DATAPORT\_OEN2 bits in the Periphery Control Register to 1. Setting only the OEN1 will result in the minimum drive strength of the output signals, setting only OEN2 will enable drive strength three times bigger than the minimum, setting both OEN1 and OEN2 will result in the maximum strength.

• Enable/Disable the data compression by clustering. The data compression algorithm that reduces the data throughput of the chip can be enabled setting bit 2 of the Periphery Control register.

• Enable/Disable regions. The readout of one or more regions can be disabled. This can be done by setting the bits of the two Region Disable Registers.

• Enable/Disable double columns inside of regions. It is possible to disable the readout of individual Priority Encoders by acting on the column disable registers of each region.

• Mask single pixels in the matrix. It is possible to address and mask single pixels before the readout. For details on the procedure, see the previous section on the initialization and execute the operations to set to binary 1 the MASK\_EN registers of the pixels to be masked.

# Test Pulsing

It is possible to test a set of pixels with built-in analog test pulse injection functionality. It is also possible to force the output of a set of pixels to one programmatically (digital test pulse). Refer to the section on the pixel circuits for more details.

The PULSE\_EN registers of the selected pixels shall be set to binary one using the mechanism provided by the Pixel CFG Register 1, Pixel CFG Register 2 and the bit 4 of the Periphery Control Register. This is similar to the procedure to reset the PULSE\_EN registers. However the PIXCNFG\_DATA shall be set to one and only selected pixels shall be configured.

The bit PULSE\_TYPE of Pixel CFG Register 2 configures globally (for all the pixels) the activation of the analog test pulse injection instead of the digital test pulse functionality.

A Readout Mode shall be activated (Readout Mode B requires controlled timing between the signal applied to the PULSE pad and the signal applied to the STROBE pad. For Readout Mode A the timing is less critical since the pixels operate in integrating mode).

Trigger the test pulse by driving a pulse on the PULSE input. Then apply a pulse to the STROBE input to latch the response of the front-end circuits and initiate the readout of the matrix.

# Analog bias and internal DACs

The pALPIDEfs chip has eleven internal DACs: six 8-bit voltage DACs and five 8-bit current DACs. These DACs are used to set the voltage and current biases required by the pixel front-end circuits. Table 9 provides an overview of the specifications of the DACs.

The DAC block has three operation modes:

1. Normal – the outputs of all DACs are connected directly to the pixel matrix.
2. Monitor - it is possible to select a voltage DAC and monitor its output on the DACMONV pad. It is also possible to select a current DAC and monitor its output on the DACMONI pad.
3. Override - it is possible to override the output of one selected voltage DAC by the DACMONV pad. It is possible to override the output of one selected current DAC by the DACMONI pad. It is also possible to override the internally generated IREF current that defines the LSB value of the current DACs.

The voltage DACs are based on a 256 stages resistive divider connected between the VREF pad and AVSS. Each resistor has a nominal value of 40 Ω, for a total resistance of 10.2 kΩ. This allows to generate voltage levels between AVSS and VREF∙(256-1)/256 with 8 bit resolution. The values of the voltage DAC setting registers are decoded and used to control arrays of analog switches connected between the 256 nodes of the resistor divider and the output pins of the DACs. The VCASN and VCASP outputs are directly applied to the matrix without any amplification or scaling. The VRESET, VPLSE\_LOW and VPLSE\_HIGH and VAUX outputs are buffered with unit gain followers. This causes an offset of about 370 mV and saturation for codes above about 200 for these DACs.

The nominal voltage to apply to the VREF pad is 1.8 V (AVDD). Any external additional resistance between the VREF source and the pad decreases the maximum voltage reachable by the DACs. A low series resistance (< 100 Ω) should be guaranteed between the source and the pad. At the nominal bias value (VREF = 1.8 V) the current sunk by the VREF pad is ≈ 180 µA.

The current DACs are implemented by repeating 256 times the same building unit that is a current source generating the current corresponding to the LSB. This is 1/256 of IREF, an internally generated reference current. IREF is nominally 10.24 uA, the LSB value is nominally 40 nA. The values of the current DACs setting registers are decoded and used to control the analog switches connecting the LSB sources in parallel into the output node of each DAC. The outputs of the current DACs are then scaled to appropriate levels before being applied to the matrix. The scaling factors are given in Table 10.

## Monitoring and Overriding of the DACs

It is possible to monitor the output of a selected voltage DAC using the DACMONV pad. The DACMONV pin should be monitored with a high input impedance circuit (Rin > 1 MΩ). Only one voltage can be monitored at a given time.

It is possible to monitor the output of a selected current DAC using the DACMONI pad loaded with a shunt resistor to AVSS. The recommended shunt resistance is 5 kΩ. Only one current can be monitored at a given time. The current on the shunt resistor is equal to ten times the output current of the selected DAC, upstream the scaling towards the pixels.

It is possible to override a selected voltage DAC using the DACMONV pad. Once the functionality is activated a voltage between 0 and VREF needs to be applied to the DACMONV pad. This will feature high input impedance. The voltage applied to DACMONV goes directly to the pixel matrix.

It is possible to override a selected current DAC using the DACMONI pad. Once the functionality is activated a current needs to be sourced from DACMONI as illustrated in Figure 17. This current is divided by 10 internally and this replaces the output of the DAC before the internal scaling towards the pixel matrix. The range of interest for the external overriding current is 0 to 200 µA, covering almost twice the internal nominal range.

Finally the internal IREF current constituting the reference for all the current DACs can be overridden. In this case the current sourced by the DACMONI pad is divided by 11 before being used by the internal DACs.

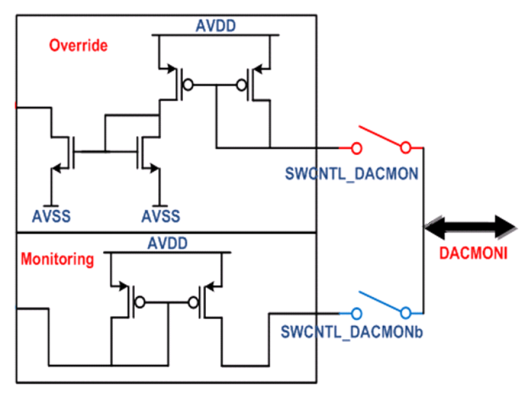
The configuration of the DAC block for monitoring or overriding and the selection of the DACs are done by the dedicated “Current/Voltage Monitoring and Overriding control register” and the values to be set are detailed in Table 11, Table 12, Table 13 and Table 14.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **Range**  **(As seen by the pixels)** | | **Nominal setting** | **Nominal Value** |
| IBIAS | 0 nA | 80 nA | 64 | 20 nA |
| ITHR | 0 nA | 2.56 nA | 51 | 0.5 nA |
| IDB | 0 nA | 40 nA | 64 | 10 nA |
| IRESET | 0.7 pA | 26 pA | 50 | 5 pA |
| IAUX2 | Not used | | | |
| VCASP | 0 V | 1.8 V | 86 | 0.60 V |
| VCASN | 0 V | 1.8 V | 57 | 0.40 V |
| VRESET | 0.37 V | 1.8 V | 117 | 1.20 V |
| VPLSE\_LOW | 0.37 V | 1.8 V | 0 | 0.38 V |
| VPLSE\_HIGH | 0.37 V | 1.8 V | 255 | 1.80 V |
| VAUX | 0.37 V | 1.8 V | 117 | 1.20 V |

Table 9: DACs specifications overview

|  |  |  |
| --- | --- | --- |
| DAC | Scaling from DAC to Matrix | Scaling from DACMONI to Matrix |
| IBIAS | 1:128 | 1:1280 |
| ITHR | 1:4096 | 1:40960 |
| IDB | 1:256 | 1:2560 |
| IRESET | ~ 1:4.105 | ~ 1:4.106 |

Table 10: Scaling factors for the Current DACs



- Overriding reduction current mirror =

10 : 1 for bias currents

11 : 1 for IREF

- Monitoring amplification current mirror = 1 : 10

0 to 20 A

Monitor or override a current in the 0 to 200 µA range

PAD



1 : 10

1 : 10

AVSS

Figure 17: Current DACs monitoring and overriding scheme

|  |  |  |
| --- | --- | --- |
| **Input** | | **Operation** |
| SWCNTL\_Vxxx | 0 | To matrix (normal operation) |
| 1 | To DACMONV |
| SWCNTL\_DACMONV  *Common signal for all voltage DACs* | 0 | Monitoring |
| 1 | Overriding |

Table 11: Voltage DAC operating settings

|  |  |  |
| --- | --- | --- |
| **Input** | | **Operation** |
| SWCNTL\_Ixxx | 0 | To matrix (normal operation) |
| 1 | To DACMONI |
| SWCNTL\_DACMONI  *Common signal for all current DACs* | 0 | Monitoring |
| 1 | Overriding |

Table 12: Current DAC operating settings

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Voltage DAC operation | SWCNTL\_DACMONV | SWCNTL\_VCASP | SWCNTL\_VCASN | SWCNTL\_VRESET | SWCNTL\_VPLSE\_LOW | SWCNTL\_VPLSE\_HIGH | SWCNTL\_VAUX |
| No monitoring & no overriding | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| No monitoring & no overriding | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Monitoring of VCASP | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| Overriding of VCASP | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| Monitoring of VCASN | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| Overriding of VCASN | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| Monitoring of VRESET | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| Overriding of VRESET | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| Monitoring of VPLSE\_LOW | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Overriding of VPLSE\_LOW | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| Monitoring of VPLSE\_HIGH | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Overriding of VPLSE\_HIGH | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| Monitoring of VAUX | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Overriding of VAUX | 1 | 0 | 0 | 0 | 0 | 0 | 1 |

Table 13: Detailed configuration settings for the voltage DACs

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Current DACs operation | SWCNTL\_DACMONI | SWCNTL\_IREF | SWCNTL\_IBIAS | SWCNTL\_ITHR | SWCNTL\_IDB | SWCNTL\_IRESET | SWCNTL\_IAUX2 |
| No monitoring & no overriding | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| No monitoring & no overriding | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Monitoring of internal IREF (DO NOT USE THIS) | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| Overriding of internal IREF | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| Monitoring of IBIAS | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| Overriding of IBIAS | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
| Monitoring of ITHR | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| To matrix using internal IREF with overriding for ITHR | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| Monitoring of IDB | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Overriding of IDB | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| Monitoring of IRESET | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Overriding of IRESET | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| Monitoring of IAUX2 (Not used internally) | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Overriding of IAUX2 (Not used internally) | 1 | 0 | 0 | 0 | 0 | 0 | 1 |

Table 14: Detailed configuration settings for the current DACs

# Minimal set of signals to be connected to operate the chip

This section identifies the ports that must be connected in all cases and the ports that in special scenarios might not be connected, renouncing to have access to the complete set of chip functionalities.

**ALL** supplies **must** be connected: **DVDDO, DVSSO, DVDD, DVSS, AVDD, AVSS**. Notice that it is not compulsory to wire all the pads of a given supply net. The power supply pads of a given net are all internally electrically shorted to the on-chip supply rails. However a reduction of supply connections can and probably will impair the circuit performance and operating capabilities. The risk of damaging the chip is also increased.

The **PWELL** substrate bias **must** be connected. Reverse bias up to -6 V with respect to analog ground (AVSS) is in principle possible. For system studies it is recommended to short the PWELL bias pins to the AVSS ground. It is also recommended to bond the PWELL pads to a stiff ground reference before any other pad is bonded to reduce the risk of ESD damage.

The **VREF** input pin **must** be connected. Shorting this analog reference pin to AVDD supply is recommended.

**DACMONV**, **DACMONI** are optional analog monitoring signals.   
They can be left unconnected in testing scenarios.

**RST, CLK, TCK, TDI** and **TMS** are signals that **must be connected** to initialize, configure and run the chip.  
**TDO** is a signal that **must be connected** to achieve read/write access to the registers or memory locations of the chip.

**STROBE** and **PRST** are signals **required** to readout event data via the JTAG control interface.  
These are INPUT CMOS pins without internal pull-up or pull-down. They shall not be left floating. Direct connection to DVSSO is suggested if their functionality is not used.

**PULSE** is a signal required for triggering the internal test pulse injection circuits (analog and digital).  
This is an INPUT pin. It shall not be left floating. Direct connection to DVSSO is recommended if not used.

**BUSY** is an output signal flagging the status of the readout circuitry.   
It is an output that can be left unconnected in special testing scenarios when this can be ignored.

**EVT\_DATA[7:0], EVT\_DATA\_VALID** are signals for the default data readout functionality.   
These are outputs that can be left unconnected in special testing scenarios, renouncing to the full output bandwidth and eventually accessing the event data stored in the internal memories via the control interface.

**READY** is an input signal **meant** for throttling the transmission of data on the output port. When READY is asserted, the EVT\_DATA[7:0] bus and EVT\_DATA\_VALID are not in high-impedance and are driven by the chip.

## Access the internal registers, memory locations, chip configuration

Required signals: RST, CLK, TCK, TMS, TDI, TDO. All other inputs tied to appropriate logic value as detailed above.

## Readout of an event frame via JTAG

Required signals: RST, CLK, TCK, TMS, TDI, TDO, STROBE, PRST. All other inputs tied to appropriate logic value as detailed in the previous section.

Procedure:

* reset the chip with RST signal (memory pointers must be set to zero)
* configure the registers of the chip (JTAG)
* set/reset the in-pixel memory elements (PRST/JTAG)
* start readout mode (JTAG)
* trigger (STROBE)
* stop readout mode (JTAG)
* read event length memory and data memory in each region (JTAG)

## Triggering a test pulse and readout of an event frame via JTAG

Required signals: RST, CLK, TCK, TMS, TDI, TDO, STROBE, PRST, PULSE. All other inputs tied to appropriate logic value as detailed above.

The same procedure of the previous section applies, pulsing must be done after the start of the readout mode (readout mode A, internal STROBE\_B always asserted):

* reset the chip with RST signal (memory pointers must be set to zero)
* configure the registers of the chip (JTAG)
* set/reset the in-pixel memory elements (PRST/JTAG)
* start readout mode (JTAG)
* Trigger test pulse (PULSE)
* Trigger readout (STROBE)
* stop readout mode (JTAG)
* read event length memory and data memory in each region (JTAG)

# Table of chip pads

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Pad index** | **Net** | **Type** | **Direction** | **Purpose** |
|  |  |  |  |  |
| A00 | TCK | DIGITAL | INPUT | Control interface clock |
| A01 | TMS | DIGITAL | INPUT | Control interface protocol signal |
| A02 | TDI | DIGITAL | INPUT | Control interface data input |
| A03 | RST | DIGITAL | INPUT | Global digital reset |
| A04 | CLK | DIGITAL | INPUT | Master clock |
| A05 | DVDDO | POWER |  | CMOS I/O drivers power rail (1.8 V) |
| A06 | DVSSO | GROUND |  | CMOS I/O drivers ground rail (0 V) |
| A07 | TDO | DIGITAL | OUTPUT | Control interface data output |
| A08 | EVT\_DATA\_VALID | DIGITAL | OUTPUT | Valid data flag for data port |
| A09 | EVT\_DATA[0] | DIGITAL | OUTPUT | Data port |
| A10 | DVDDO | POWER |  | CMOS I/O drivers power rail (1.8 V) |
| A11 | DVSSO | GROUND |  | CMOS I/O drivers ground rail (0 V) |
| A12 | EVT\_DATA[1] | DIGITAL | OUTPUT | Data port |
| A13 | EVT\_DATA[2] | DIGITAL | OUTPUT | Data port |
| A14 | EVT\_DATA[3] | DIGITAL | OUTPUT | Data port |
| A15 | EVT\_DATA[4] | DIGITAL | OUTPUT | Data port |
| A16 | DVDDO | POWER |  | CMOS I/O drivers power rail (1.8 V) |
| A17 | DVSSO | GROUND |  | CMOS I/O drivers ground rail (0 V) |
| A18 | EVT\_DATA[5] | DIGITAL | OUTPUT | Data port |
| A19 | EVT\_DATA[6] | DIGITAL | OUTPUT | Data port |
| A20 | EVT\_DATA[7] | DIGITAL | OUTPUT | Data port |
| A21 | BUSY | DIGITAL | OUTPUT | Busy flag. Asserted: low. Deasserted: high impedance |
| A22 | DVDDO | POWER |  | CMOS I/O drivers power rail (1.8 V) |
| A23 | DVSSO | GROUND |  | CMOS I/O drivers ground rail (0 V) |
| A24 | READY | DIGITAL | INPUT | Data transmission enable and data bus ownership |
| A25 | PRST | DIGITAL | INPUT | Pixels state reset pulse |
| A26 | STROBE | DIGITAL | INPUT | Enable latching the pixel discriminator states |
| A27 | PULSE | DIGITAL | INPUT | Internal test pulse trigger (analog and digital) |
| A28 | DACMONV | ANALOG | OUTPUT | Voltage monitoring output |
| A29 | DACMONI | ANALOG | OUTPUT | Voltage monitoring output |
| A30 | VREF | ANALOG | INPUT | Input reference voltage for DACs |
|  |  |  |  |  |
|  |  |  |  |  |
| B00 | DVSS | GROUND |  | Digital core ground rail (0 V) |
| B01 | DVDD | POWER |  | Digital core power rail (1.8 V) |
| B02 | DVSS | GROUND |  | Digital core ground rail (0 V) |
| B03 | DVDD | POWER |  | Digital core power rail (1.8 V) |
| B04 | DVSS | GROUND |  | Digital core ground rail (0 V) |
| B05 | DVDD | POWER |  | Digital core power rail (1.8 V) |
| B06 | DVSS | GROUND |  | Digital core ground rail (0 V) |
| B07 | DVDD | POWER |  | Digital core power rail (1.8 V) |
| B08 | DVSS | GROUND |  | Digital core ground rail (0 V) |
| B09 | DVDD | POWER |  | Digital core power rail (1.8 V) |
| B10 | DVSS | GROUND |  | Digital core ground rail (0 V) |
| B11 | DVDD | POWER |  | Digital core power rail (1.8 V) |
| B12 | DVSS | GROUND |  | Digital core ground rail (0 V) |
| B13 | DVDD | POWER |  | Digital core power rail (1.8 V) |
| B14 | DVSS | GROUND |  | Digital core ground rail (0 V) |
| B15 | DVDD | POWER |  | Digital core power rail (1.8 V) |
|  |  |  |  |  |
| C00 | DVSS | GROUND |  | Digital core ground rail (0 V) |
| C01 | DVDD | POWER |  | Digital core power rail (1.8 V) |
| C02 | DVSS | GROUND |  | Digital core ground rail (0 V) |
| C03 | DVDD | POWER |  | Digital core power rail (1.8 V) |
| C04 | DVSS | GROUND |  | Digital core ground rail (0 V) |
| C05 | DVDD | POWER |  | Digital core power rail (1.8 V) |
| C06 | DVSS | GROUND |  | Digital core ground rail (0 V) |
| C07 | DVDD | POWER |  | Digital core power rail (1.8 V) |
| C08 | DVSS | GROUND |  | Digital core ground rail (0 V) |
| C09 | DVDD | POWER |  | Digital core power rail (1.8 V) |
| C10 | DVSS | GROUND |  | Digital core ground rail (0 V) |
| C11 | DVDD | POWER |  | Digital core power rail (1.8 V) |
| C12 | DVSS | GROUND |  | Digital core ground rail (0 V) |
| C13 | DVDD | POWER |  | Digital core power rail (1.8 V) |
| C14 | DVSS | GROUND |  | Digital core ground rail (0 V) |
| C15 | DVDD | POWER |  | Digital core power rail (1.8 V) |
|  |  |  |  |  |
|  |  |  |  |  |
| D00 | AVSS | GROUND |  | Analog ground rail (0 V) |
| D01 | AVDD | POWER |  | Analog power rail (1.8 V) |
| D02 | AVSS | GROUND |  | Analog ground rail (0 V) |
| D03 | AVDD | POWER |  | Analog power rail (1.8 V) |
| D04 | AVSS | GROUND |  | Analog ground rail (0 V) |
| D05 | AVDD | POWER |  | Analog power rail (1.8 V) |
| D06 | AVSS | GROUND |  | Analog ground rail (0 V) |
| D07 | AVDD | POWER |  | Analog power rail (1.8 V) |
| D08 | AVSS | GROUND |  | Analog ground rail (0 V) |
| D09 | AVDD | POWER |  | Analog power rail (1.8 V) |
| D10 | AVSS | GROUND |  | Analog ground rail (0 V) |
| D11 | AVDD | POWER |  | Analog power rail (1.8 V) |
| D12 | AVSS | GROUND |  | Analog ground rail (0 V) |
| D13 | AVDD | POWER |  | Analog power rail (1.8 V) |
| D14 | AVSS | GROUND |  | Analog ground rail (0 V) |
| D15 | AVDD | POWER |  | Analog power rail (1.8 V) |
|  |  |  |  |  |
|  |  |  |  |  |
| E00 | AVSS | GROUND |  | Analog ground rail (0 V) |
| E01 | AVDD | POWER |  | Analog power rail (1.8 V) |
| E02 | PWELL | SUBSTRATE |  | Substrate bias rail (nominally shorted to AVSS) |
| E03 | AVSS | GROUND |  | Analog ground rail (0 V) |
| E04 | AVDD | POWER |  | Analog power rail (1.8 V) |
| E05 | PWELL | SUBSTRATE |  | Substrate bias rail (nominally shorted to AVSS) |
| E06 | AVSS | GROUND |  | Analog ground rail (0 V) |
| E07 | AVDD | POWER |  | Analog power rail (1.8 V) |
| E08 | PWELL | SUBSTRATE |  | Substrate bias rail (nominally shorted to AVSS) |
| E09 | AVSS | GROUND |  | Analog ground rail (0 V) |
| E10 | AVDD | POWER |  | Analog power rail (1.8 V) |
| E11 | PWELL | SUBSTRATE |  | Substrate bias rail (nominally shorted to AVSS) |
| E12 | AVSS | GROUND |  | Analog ground rail (0 V) |
| E13 | AVDD | POWER |  | Analog power rail (1.8 V) |
| E14 | PWELL | SUBSTRATE |  | Substrate bias rail (nominally shorted to AVSS) |
| E15 | AVSS | GROUND |  | Analog ground rail (0 V) |
| E16 | AVDD | POWER |  | Analog power rail (1.8 V) |
| E17 | PWELL | SUBSTRATE |  | Substrate bias rail (nominally shorted to AVSS) |
| E18 | AVSS | GROUND |  | Analog ground rail (0 V) |
| E19 | AVDD | POWER |  | Analog power rail (1.8 V) |
| E20 | PWELL | SUBSTRATE |  | Substrate bias rail (nominally shorted to AVSS) |
| E21 | AVSS | GROUND |  | Analog ground rail (0 V) |
| E22 | AVDD | POWER |  | Analog power rail (1.8 V) |
| E23 | PWELL | SUBSTRATE |  | Substrate bias rail (nominally shorted to AVSS) |

# Pad naming conventions

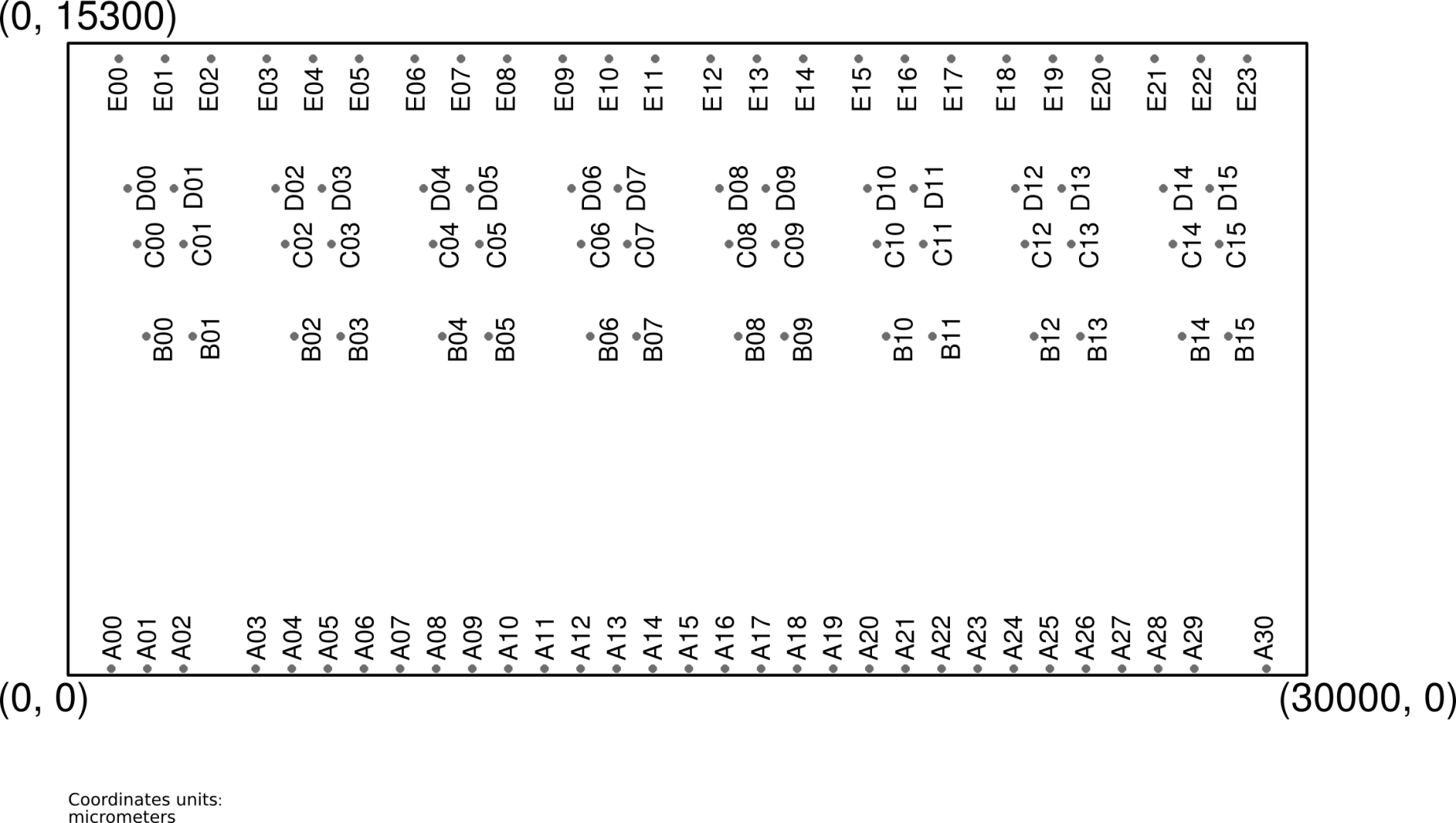


Figure 18: Pad naming convention

# Pad signals

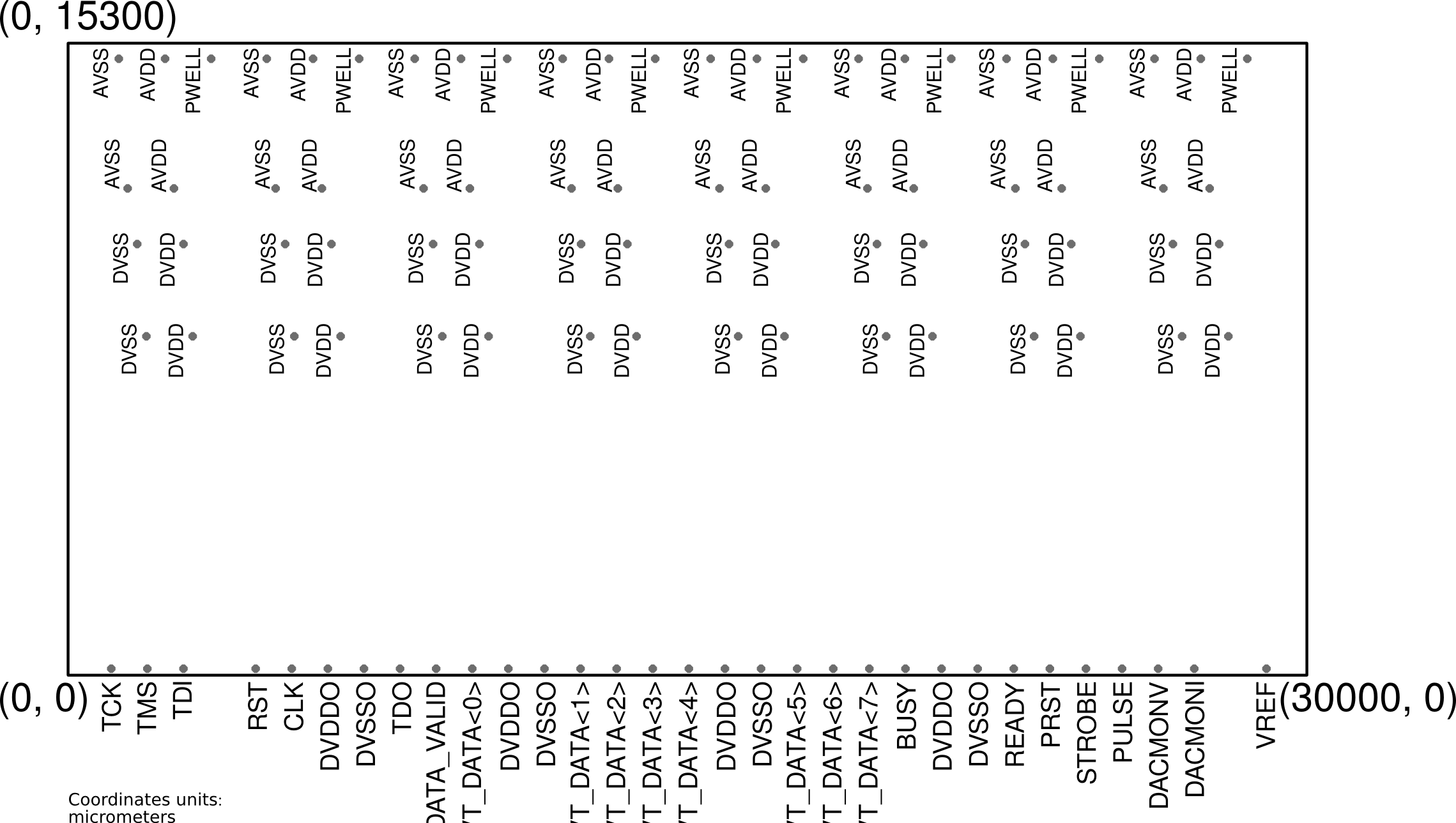


Figure 19: Pad signals

# Pad geometry

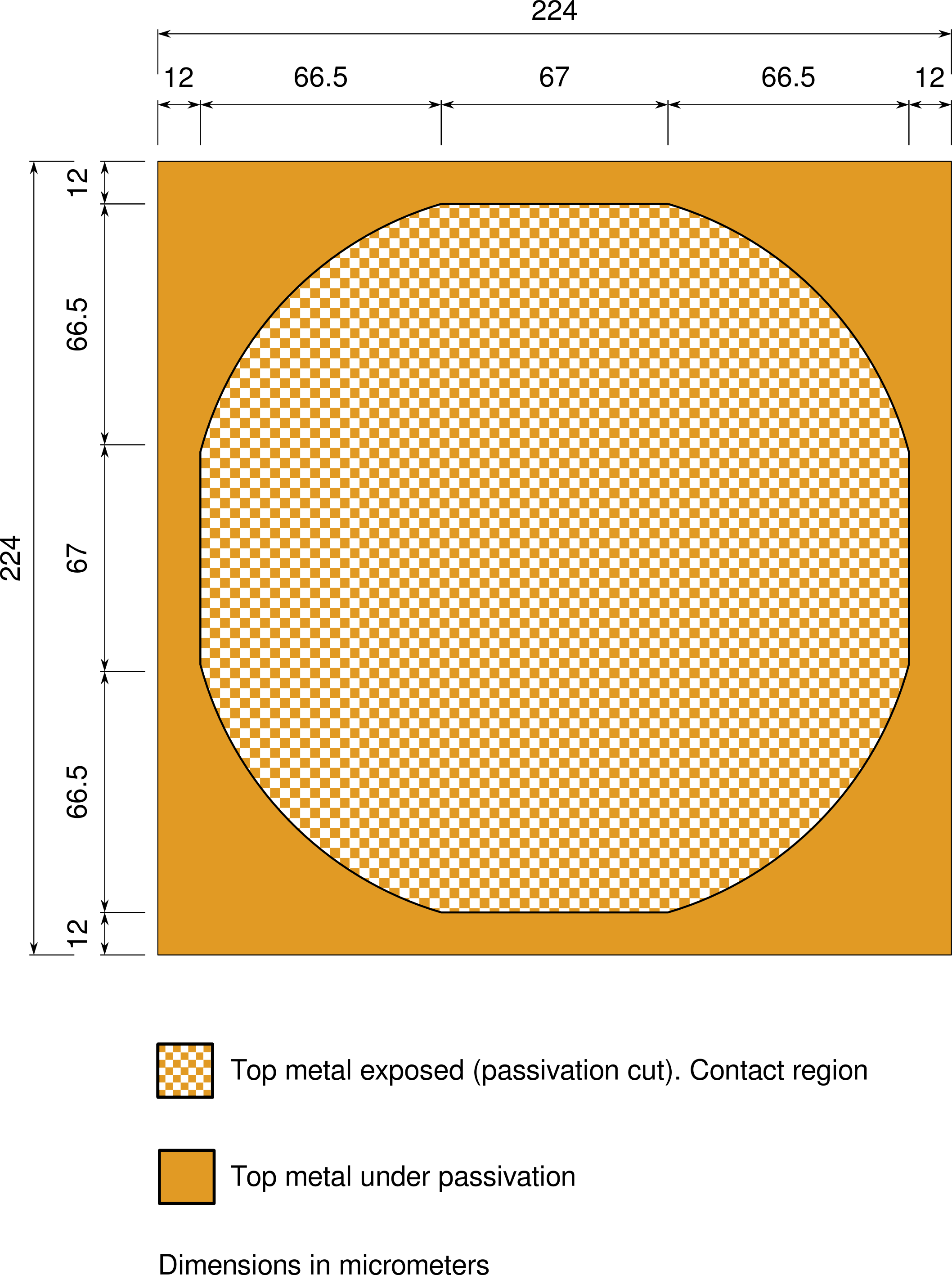


Figure 20: Geometry of a pad

# Pads coordinates

Lower Left vertex coordinates: (xll, yll)

Upper Right vertex coordinates: (xur, yur)

Centre point coordinates: (x\_cntr, y\_cntr)

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Pad index** | **Net** | **xll [um]** | **yll [um]** | **xur [um]** | **yur [um]** | **x\_cntr [um]** | **y\_cntr [um]** |
|  |  |  |  |  |  |  |  |
| A00 | TCK | 933 | 42.4 | 1157 | 266.4 | 1045 | 154.4 |
| A01 | TMS | 1807 | 42.4 | 2031 | 266.4 | 1919 | 154.4 |
| A02 | TDI | 2681 | 42.4 | 2905 | 266.4 | 2793 | 154.4 |
| A03 | RST | 4429 | 42.4 | 4653 | 266.4 | 4541 | 154.4 |
| A04 | CLK | 5303 | 42.4 | 5527 | 266.4 | 5415 | 154.4 |
| A05 | DVDDO | 6177 | 42.4 | 6401 | 266.4 | 6289 | 154.4 |
| A06 | DVSSO | 7051 | 42.4 | 7275 | 266.4 | 7163 | 154.4 |
| A07 | TDO | 7925 | 42.4 | 8149 | 266.4 | 8037 | 154.4 |
| A08 | EVT\_DATA\_VALID | 8799 | 42.4 | 9023 | 266.4 | 8911 | 154.4 |
| A09 | EVT\_DATA[0] | 9673 | 42.4 | 9897 | 266.4 | 9785 | 154.4 |
| A10 | DVDDO | 10547 | 42.4 | 10771 | 266.4 | 10659 | 154.4 |
| A11 | DVSSO | 11421 | 42.4 | 11645 | 266.4 | 11533 | 154.4 |
| A12 | EVT\_DATA[1] | 12295 | 42.4 | 12519 | 266.4 | 12407 | 154.4 |
| A13 | EVT\_DATA[2] | 13169 | 42.4 | 13393 | 266.4 | 13281 | 154.4 |
| A14 | EVT\_DATA[3] | 14043 | 42.4 | 14267 | 266.4 | 14155 | 154.4 |
| A15 | EVT\_DATA[4] | 14917 | 42.4 | 15141 | 266.4 | 15029 | 154.4 |
| A16 | DVDDO | 15791 | 42.4 | 16015 | 266.4 | 15903 | 154.4 |
| A17 | DVSSO | 16665 | 42.4 | 16889 | 266.4 | 16777 | 154.4 |
| A18 | EVT\_DATA[5] | 17539 | 42.4 | 17763 | 266.4 | 17651 | 154.4 |
| A19 | EVT\_DATA[6] | 18413 | 42.4 | 18637 | 266.4 | 18525 | 154.4 |
| A20 | EVT\_DATA[7] | 19287 | 42.4 | 19511 | 266.4 | 19399 | 154.4 |
| A21 | BUSY | 20161 | 42.4 | 20385 | 266.4 | 20273 | 154.4 |
| A22 | DVDDO | 21035 | 42.4 | 21259 | 266.4 | 21147 | 154.4 |
| A23 | DVSSO | 21909 | 42.4 | 22133 | 266.4 | 22021 | 154.4 |
| A24 | READY | 22783 | 42.4 | 23007 | 266.4 | 22895 | 154.4 |
| A25 | PRST | 23657 | 42.4 | 23881 | 266.4 | 23769 | 154.4 |
| A26 | STROBE | 24531 | 42.4 | 24755 | 266.4 | 24643 | 154.4 |
| A27 | PULSE | 25405 | 42.4 | 25629 | 266.4 | 25517 | 154.4 |
| A28 | DACMONV | 26279 | 42.4 | 26503 | 266.4 | 26391 | 154.4 |
| A29 | DACMONI | 27153 | 42.4 | 27377 | 266.4 | 27265 | 154.4 |
| A30 | VREF | 28901 | 42.4 | 29125 | 266.4 | 29013 | 154.4 |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
| B00 | DVSS | 1784 | 8089.6 | 2008 | 8313.6 | 1896 | 8201.6 |
| B01 | DVDD | 2904 | 8089.6 | 3128 | 8313.6 | 3016 | 8201.6 |
| B02 | DVSS | 5368 | 8089.6 | 5592 | 8313.6 | 5480 | 8201.6 |
| B03 | DVDD | 6488 | 8089.6 | 6712 | 8313.6 | 6600 | 8201.6 |
| B04 | DVSS | 8952 | 8089.6 | 9176 | 8313.6 | 9064 | 8201.6 |
| B05 | DVDD | 10072 | 8089.6 | 10296 | 8313.6 | 10184 | 8201.6 |
| B06 | DVSS | 12536 | 8089.6 | 12760 | 8313.6 | 12648 | 8201.6 |
| B07 | DVDD | 13656 | 8089.6 | 13880 | 8313.6 | 13768 | 8201.6 |
| B08 | DVSS | 16120 | 8089.6 | 16344 | 8313.6 | 16232 | 8201.6 |
| B09 | DVDD | 17240 | 8089.6 | 17464 | 8313.6 | 17352 | 8201.6 |
| B10 | DVSS | 19704 | 8089.6 | 19928 | 8313.6 | 19816 | 8201.6 |
| B11 | DVDD | 20824 | 8089.6 | 21048 | 8313.6 | 20936 | 8201.6 |
| B12 | DVSS | 23288 | 8089.6 | 23512 | 8313.6 | 23400 | 8201.6 |
| B13 | DVDD | 24408 | 8089.6 | 24632 | 8313.6 | 24520 | 8201.6 |
| B14 | DVSS | 26872 | 8089.6 | 27096 | 8313.6 | 26984 | 8201.6 |
| B15 | DVDD | 27992 | 8089.6 | 28216 | 8313.6 | 28104 | 8201.6 |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
| C00 | DVSS | 1560 | 10329.6 | 1784 | 10553.6 | 1672 | 10441.6 |
| C01 | DVDD | 2680 | 10329.6 | 2904 | 10553.6 | 2792 | 10441.6 |
| C02 | DVSS | 5144 | 10329.6 | 5368 | 10553.6 | 5256 | 10441.6 |
| C03 | DVDD | 6264 | 10329.6 | 6488 | 10553.6 | 6376 | 10441.6 |
| C04 | DVSS | 8728 | 10329.6 | 8952 | 10553.6 | 8840 | 10441.6 |
| C05 | DVDD | 9848 | 10329.6 | 10072 | 10553.6 | 9960 | 10441.6 |
| C06 | DVSS | 12312 | 10329.6 | 12536 | 10553.6 | 12424 | 10441.6 |
| C07 | DVDD | 13432 | 10329.6 | 13656 | 10553.6 | 13544 | 10441.6 |
| C08 | DVSS | 15896 | 10329.6 | 16120 | 10553.6 | 16008 | 10441.6 |
| C09 | DVDD | 17016 | 10329.6 | 17240 | 10553.6 | 17128 | 10441.6 |
| C10 | DVSS | 19480 | 10329.6 | 19704 | 10553.6 | 19592 | 10441.6 |
| C11 | DVDD | 20600 | 10329.6 | 20824 | 10553.6 | 20712 | 10441.6 |
| C12 | DVSS | 23064 | 10329.6 | 23288 | 10553.6 | 23176 | 10441.6 |
| C13 | DVDD | 24184 | 10329.6 | 24408 | 10553.6 | 24296 | 10441.6 |
| C14 | DVSS | 26648 | 10329.6 | 26872 | 10553.6 | 26760 | 10441.6 |
| C15 | DVDD | 27768 | 10329.6 | 27992 | 10553.6 | 27880 | 10441.6 |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
| D00 | AVSS | 1336 | 11673.6 | 1560 | 11897.6 | 1448 | 11785.6 |
| D01 | AVDD | 2456 | 11673.6 | 2680 | 11897.6 | 2568 | 11785.6 |
| D02 | AVSS | 4920 | 11673.6 | 5144 | 11897.6 | 5032 | 11785.6 |
| D03 | AVDD | 6040 | 11673.6 | 6264 | 11897.6 | 6152 | 11785.6 |
| D04 | AVSS | 8504 | 11673.6 | 8728 | 11897.6 | 8616 | 11785.6 |
| D05 | AVDD | 9624 | 11673.6 | 9848 | 11897.6 | 9736 | 11785.6 |
| D06 | AVSS | 12088 | 11673.6 | 12312 | 11897.6 | 12200 | 11785.6 |
| D07 | AVDD | 13208 | 11673.6 | 13432 | 11897.6 | 13320 | 11785.6 |
| D08 | AVSS | 15672 | 11673.6 | 15896 | 11897.6 | 15784 | 11785.6 |
| D09 | AVDD | 16792 | 11673.6 | 17016 | 11897.6 | 16904 | 11785.6 |
| D10 | AVSS | 19256 | 11673.6 | 19480 | 11897.6 | 19368 | 11785.6 |
| D11 | AVDD | 20376 | 11673.6 | 20600 | 11897.6 | 20488 | 11785.6 |
| D12 | AVSS | 22840 | 11673.6 | 23064 | 11897.6 | 22952 | 11785.6 |
| D13 | AVDD | 23960 | 11673.6 | 24184 | 11897.6 | 24072 | 11785.6 |
| D14 | AVSS | 26424 | 11673.6 | 26648 | 11897.6 | 26536 | 11785.6 |
| D15 | AVDD | 27544 | 11673.6 | 27768 | 11897.6 | 27656 | 11785.6 |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
| E00 | AVSS | 1112 | 14809.6 | 1336 | 15033.6 | 1224 | 14921.6 |
| E01 | AVDD | 2232 | 14809.6 | 2456 | 15033.6 | 2344 | 14921.6 |
| E02 | PWELL | 3352 | 14809.6 | 3576 | 15033.6 | 3464 | 14921.6 |
| E03 | AVSS | 4696 | 14809.6 | 4920 | 15033.6 | 4808 | 14921.6 |
| E04 | AVDD | 5816 | 14809.6 | 6040 | 15033.6 | 5928 | 14921.6 |
| E05 | PWELL | 6936 | 14809.6 | 7160 | 15033.6 | 7048 | 14921.6 |
| E06 | AVSS | 8280 | 14809.6 | 8504 | 15033.6 | 8392 | 14921.6 |
| E07 | AVDD | 9400 | 14809.6 | 9624 | 15033.6 | 9512 | 14921.6 |
| E08 | PWELL | 10520 | 14809.6 | 10744 | 15033.6 | 10632 | 14921.6 |
| E09 | AVSS | 11864 | 14809.6 | 12088 | 15033.6 | 11976 | 14921.6 |
| E10 | AVDD | 12984 | 14809.6 | 13208 | 15033.6 | 13096 | 14921.6 |
| E11 | PWELL | 14104 | 14809.6 | 14328 | 15033.6 | 14216 | 14921.6 |
| E12 | AVSS | 15448 | 14809.6 | 15672 | 15033.6 | 15560 | 14921.6 |
| E13 | AVDD | 16568 | 14809.6 | 16792 | 15033.6 | 16680 | 14921.6 |
| E14 | PWELL | 17688 | 14809.6 | 17912 | 15033.6 | 17800 | 14921.6 |
| E15 | AVSS | 19032 | 14809.6 | 19256 | 15033.6 | 19144 | 14921.6 |
| E16 | AVDD | 20152 | 14809.6 | 20376 | 15033.6 | 20264 | 14921.6 |
| E17 | PWELL | 21272 | 14809.6 | 21496 | 15033.6 | 21384 | 14921.6 |
| E18 | AVSS | 22616 | 14809.6 | 22840 | 15033.6 | 22728 | 14921.6 |
| E19 | AVDD | 23736 | 14809.6 | 23960 | 15033.6 | 23848 | 14921.6 |
| E20 | PWELL | 24856 | 14809.6 | 25080 | 15033.6 | 24968 | 14921.6 |
| E21 | AVSS | 26200 | 14809.6 | 26424 | 15033.6 | 26312 | 14921.6 |
| E22 | AVDD | 27320 | 14809.6 | 27544 | 15033.6 | 27432 | 14921.6 |
| E23 | PWELL | 28440 | 14809.6 | 28664 | 15033.6 | 28552 | 14921.6 |