ALPIDE-3 Operations Manual - DRAFT

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1 Introduction

The ALPIDE-3 is one of several chips implemented in the context of the microelectronics R&D process, towards the design of a final ALPIDE chip that will target all the requirements of the for the ALICE ITS Upgrade. The ALPIDE-3 chip is a third step on a path intended to address system aspects related to the integration of a large scale (3×1.5 cm^2) MAPS chip and to the physical and electrical interconnection of such a chip on flex printed circuits. With respect to its immediate predecessors (pALPIDEfs and pALPIDE-2), the ALPIDE-3 targets meeting most of the requirements for the ALICE ITS Upgrade. The ALPIDE-3 sensitive matrix is composed of eight variants of pixels, for continuing optimization of the pixel analog circuits.

The purpose of this document is to collect most technical information about the ALPIDE-3 chip and enable integration of test systems, evaluation boards and module prototypes based on it.

The ALPIDE-3 chip is a particle detector based on Monolithic Active Pixels Sensor technology. It is implemented in a 180 nm CMOS technology for Imaging Sensors. The chip measures 15 mm (Y) by 30 mm (X) and contains a matrix of 512 $\times$1024 (Y$\times$X) sensitive pixels. The pixels are 29.24 μm $\times$ 26.88 μm X$\times$Y). A periphery circuit region of 1.2×30 mm^2 including the readout and control functionalities is present. It is assumed that the chip is observed from the circuits side and oriented such that the periphery is the bottom. The pixel columns are numbered from 0 to 1023 going from left to right. Pixel rows are numbered from 0 to 511 going from the matrix top side to the bottom one.

There are eight sub-matrices of 512$\times$128 pixels, each one being composed by identical pixels. The eight flavors of pixels are functionally identical from the readout perspective. They differ for specific parameters of the charge collection diode and of the analog front-end circuits. Each pixel variant features an ultra-low power, non-linear front-ent with shaping and discriminated output. The pixel sensor and front-end are always active. The front-end acts as a delay line: upon a particle hit, it generates a pulse with a duration of a few microseconds. A threshold is applied to form a binary pulse. A hit is latched into one of the three in-pixel memory cells if a STROBE signal is applied to the corresponding cell while the aforementioned binary pulse is asserted. The assertion of STROBE signals to the pixels during the response interval following an event of charge release in the sensing diode causes the latching of the discriminated output into one of three storage cells in the digital section of the pixel. The pixels feature a built-in test pulse injection circuit triggerable on command. A digital-only test pulse mode is also available, forcing the writing of a logic one in the selected in-pixel memory cell. The STROBE signals are generated at the periphery and applied simultaneously to all pixels. The logic generating the STROBE signal is configurable according to different operating modes and the duration of the STROBE signals is also programmable. The generation of STROBE signals is typically triggered by an externally applied trigger command.

The hits stored in the pixels multi-event buffers are read out by means of Priority Encoder circuits. These provide the address of a pixel with a stored hit based on a hardwired topological priority. During one hit transfer cycle a pixel with a hit is selected, its address generated and transmitted to the periphery and finally the in-pixel memory element is reset. This cycle is repeated until all hits at the inputs of the Priority Encoder are read out. The readout of the sensitive matrix to the periphery is therefore zero-suppressed and hit-driven. Time and energy are consumed proportionally to the number of hits at the inputs of the Priority Encoder.

The raedout of the matrix is organized in 32 regions (512×32 pixels), each of them with 16 double columns being read out by 16 Priority Encoder circuits. The hits inside one region are read out sequentially in consecutive readout cycles.

The processes of readout of the 32 regions are executed in parallel. They are driven by state machines in the Region Readout Unit blocks. The Region Readout Units also contain multi-event storage memories and data compression functionality based on clustering by adjacency. The data from the 32 region readout blocks are assembled and formatted by a chip level Top Readout Unit.

Hit data can be transmitted on two different data interfaces according to one of three alternative operating modes envisaged for the Upgraded ALICE ITS: *Inner Barrel Module chip*, *Outer Barrel Module Master*,*Outer Barrel Module Slave*. A 1.2 Gb/s serial port (HSDATA) with differential signalling is intended to be the primary data readout interface for the Inner Barrel Module chips. The same interface is intended to be used for the transmission of data off-detector by the Outer Barrel Module Master chips. These also collect the data of a set of neighboring Outer Barrel Module Slave chips and forward their data off-detector on a common differential link.

A parallel output data port using CMOS signaling is also present. It enables the implementation of the data exchange between the Outer Barrel Module Slave chips and the corresponding Master. All the functionalities related to the Outer Barrel Module bus arbitration, data encoding, data transmission are implemented by a dedicated Data Management Unit.

A top-level Control Management Unit block provides full access to the control and status registers of the chip as well as to the multi-event memories in the Region Readout Units. Control commands are supported by the control interface. The slow control is implemented onto a differential, serial, half-duplex link specifically designed for the Upgraded ITS (DCNTRL). A secondary single-ended control port (CNTRL) is dedicated to the forwarding of control transactions between the Outer Barrel Module Master chips and the Outer Barrel Module Slaves.

All the analog signals required by the front-ends are generated by a set of on-chip DACs. Analog monitoring pads (DACMONV, DACMONI) are available to monitor the outputs of the internal DACs. The DACMONV pad can be used to override any of the voltage DACs. The DACMONI pad can be used to override any of the current DACs or to override the internal reference current used by the current DACs.

2 ALPIDE-3 data sheet

This chapter shall contain summarized technical information about the chip, interfaces, pin functions, die geometry, pads geometry, electrical characteristics, timing requirements, switching characteristics.

2.1 Block diagram and pinout

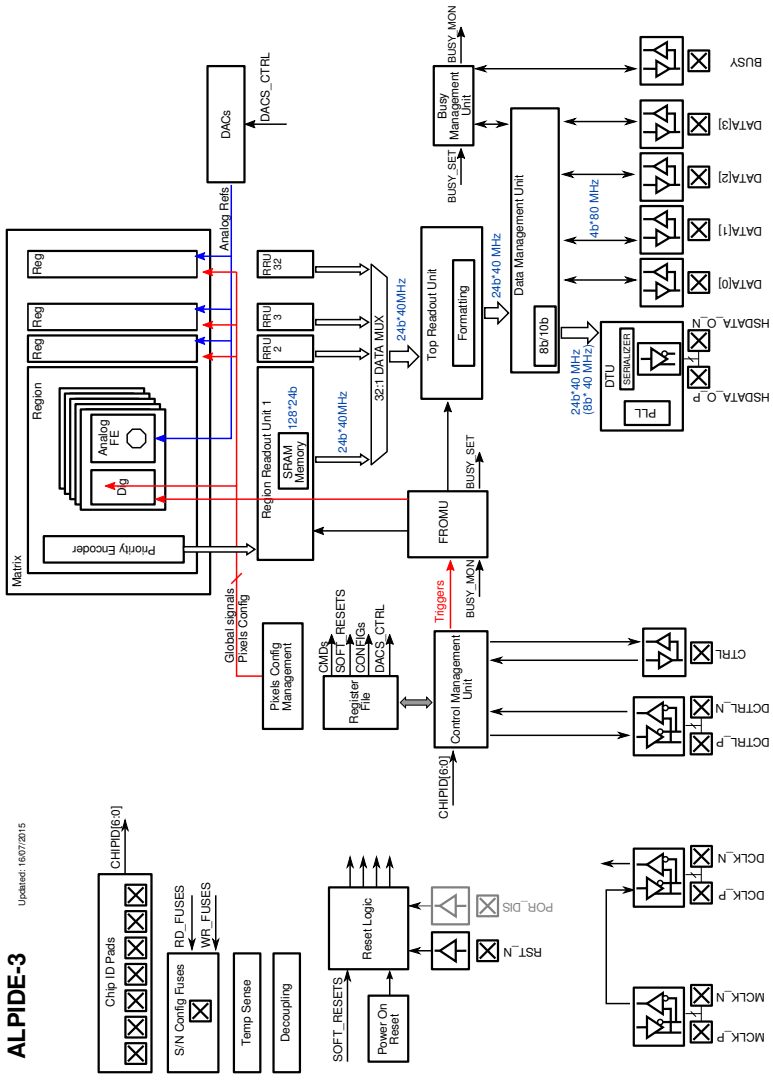


Figure 2.1: ALPIDE-3 chip block diagram.

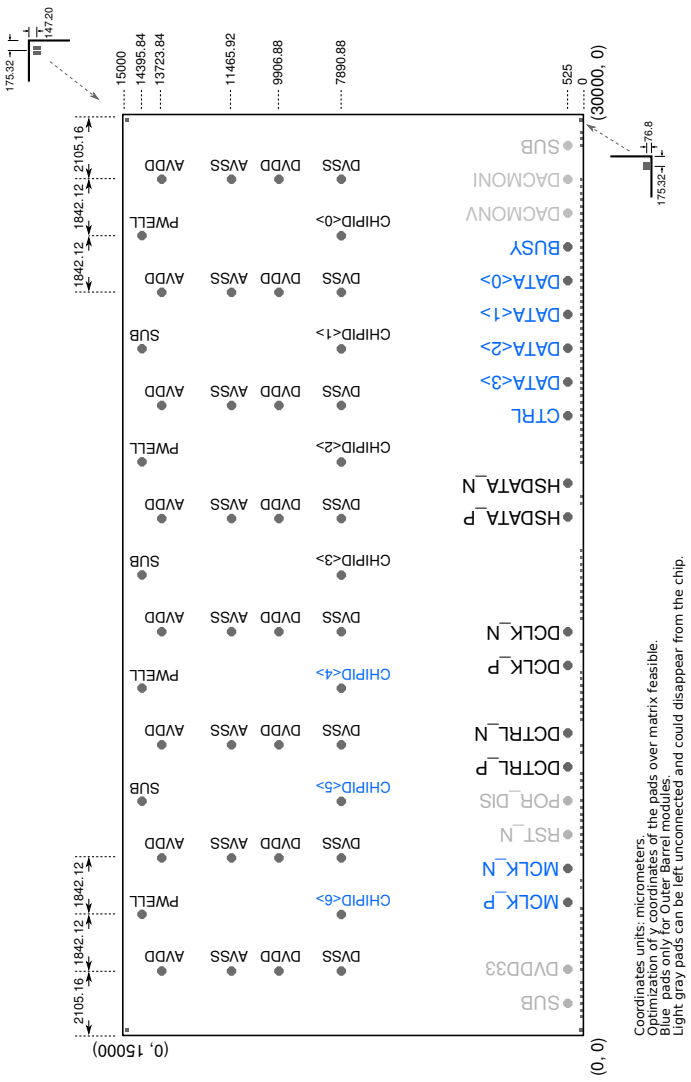


Figure 2.2: ALPIDE-3 pinout.

2.2 List of features

2.3 Interface signals

The main functional I/Os of the ALPIDE-3 chip are listed in Table 2.1. Figure 2.2 shows the locations of the pads.

The CMOS I/Os are 1.8 V compatible. Two types of CMOS I/O pad cells are used in ALPIDE-3: one has an internal pull-up resistor and one an internal pull-down resistor. The internal resistors are always connected to the pad. The driving strengths of the two cells are equal and fixed. The pad cells are tri-state capable and their drivers can be turned off and placed in a high-impedance mode depending on configuration and conditions.

The MCLK, DCTRL ans DCLK differential ports are implemented with a custom designed differential transceiver cell. This has been designed with reference to standard TIA/EIA-899 Electrical Characteristics of Multipoint-Low-Voltage Differential Signaling (M-LVDS)[1]. However the differential ports are not standard compliant in particular with respect to the acceptable range of the common signal.

Tables 2.3, Table 2.4 and Table 2.5 summarize the recommended DC operating conditions and the electrical characteristics of the various interfaces.

The analog monitoring ports provide access to internal nodes through a series resistor.

Table 2.1: ALPIDE-3 interface signals.

Signal	Type	Direction	Purpose
MCLK_P	Differential (MLVDS)	INPUT	Forwarded clock input
MCLK_N	Differential (MLVDS)	INPUT	Forwarded clock input
RST_N	CMOS, internal pull-up	INPUT	Global chip reset
POR_DIS_N	CMOS, internal pull-up	INPUT	Power On Reset Disable
DCTRL_P	Differential (MLVDS)	BIDIR	Differential Control port
DCTRL_N	Differential (MLVDS)	BIDIR	Differential Control port
DCLK_P	Differential (MLVDS)	BIDIR	Main clock input and clock forwarding output
DCLK_N	Differential (MLVDS)	BIDIR	Main clock input and clock forwarding output
HSDATA_P	Differential (LVDS)	OUTPUT	Serial Data Output
HSDATA_N	Differential (LVDS)	OUTPUT	Serial Data Output
CTRL	CMOS, internal pull-up	BIDIR	Control port (OB local bus)
DATA[7]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
DATA[6]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
DATA[5]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
DATA[4]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
DATA[3]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
DATA[2]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
DATA[1]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
DATA[0]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
BUSY	CMOS, internal pull-up	BIDIR	Busy flag
DACMONV	ANALOG	OUTPUT	Current Monitoring Output
DACMONI	ANALOG	OUTPUT	Voltage Monitoring Output
CHIPID[6]	CMOS, internal pull-down	INPUT	Topological chip address
CHIPID[5]	CMOS, internal pull-down	INPUT	Topological chip address

[1] See Texas Instrument Application Report SLLA108A

CHIPID[4]	CMOS, internal pull-down	INPUT	Topological chip address
CHIPID[3]	CMOS, internal pull-down	INPUT	Topological chip address
CHIPID[2]	CMOS, internal pull-down	INPUT	Topological chip address
CHIPID[1]	CMOS, internal pull-down	INPUT	Topological chip address
CHIPID[0]	CMOS, internal pull-down	INPUT	Topological chip address

MCLK_P, MCLK_N: Clock forwarding input port, used to implement the clock distribution in the Outer Barrel Module application scenario. This is a receiving only port, the driver behind it being disabled in all scenarios. The receiver is enabled when the chip is configured as Outer Barrel Module Master and the signal applied to this port is then forwarded to the DCLK_P, DCLK_N port. A chip configured as Inner Chip or Outer Barrel slave chip keeps the receiver on this port disabled.

RST_N: Global active-low reset signal. The ALPIDE-3 chip includes a power-on-reset circuit. The chip can also be reset by commands issued by the control interface. This port can be left unconnected in applications not needing a dedicated reset pin.

POR_DIS_N: Disabling of the power-on-reset circuit, active low. Driving low this input masks the output of the internal power-on reset circuitry. If the internal power-on-reset is used this pin can be left unconnected since it is internally pulled-up.

DCTRL_P, DCTRL_N: Differential bidirectional control port. Intended to implement the half-duplex control bus segments between the Inner Barrel chips or the Outer Barrel Module Master chips and the off detector electronics. The DCTRL port is unused by a chip configured as Outer Barrel Module Slave Chip.

DCLK_P, DCLK_N: Main clock input and forwarded clock output. Nominal clock frequency is 40 MHz. This is the chip clock source regardless of the operating mode and configuration scenario. In all configurations the receiver circuit at this port provides the clock to the chip core. A chip configured as Outer Barrel Module Master has an active driver on this port and forwards on it the signal received on the MCLK_P, MCLK_N port.

HSDATA_P, HSDATA_N: Differential data output port. This port is used for the high speed serial transmission of data between chips and the off-detector electronics. It is used by chips configured as Inner Barrel Chip or Outer Barrel Module Master. Signaling rate on this port is 1.2 Gb/s in the Inner Barrel Chip configuration and 400 Mb/s in the Outer Barrel Module Master configuration. The serial stream is (by default) 8b/10b encoded.

CTRL: Single ended, bidirectional control port. Intended to implement the half-duplex local control bus segments between the Outer Barrel Module Master chip and the associated slaves. These chips shall have their CTRL ports directly connected by a single shared wire. The CTRL port is unused by a chip configured as Inner Chip.

DATA[7:0]: CMOS bidirectional data port. Intended to implement a shared parallel data bus between the Outer Barrel Module Slave chips and the associated Master. By default, the 4 lowermost lines of this port operate in Double Data Rate mode, with bits launched or sampled at both clock edges and one complete byte transfer completed at every clock cycle. Thus the uppermost 4 bits can be left unconnected and the bus can be implemented using 4 parallel wires shared by the chips. Optionally, the chips can be configured to revert to Single Data Rate signaling also on the lowermost 4 bits. In this case one byte is launched or sampled at every rising edge of the clock. This operating mode can be used for readout of chips through a 8 bit Single Data Rate parallel bus.

BUSY: Single ended port. It is intended to implement the communication of the BUSY state between the Outer Barrel Module Slaves and the associated Master chip by wiring in parallel all

their BUSY ports. This port is not used when the chip operates as an ITS Inner Barrel chip. This port can be in one of two states: actively driven low or high impedance, thus emulating an open-drain topology. The signaling is active low. The pad provides weak internal pull-up. An external strong pull-up resistor might be required to speed-up the rise-time of the de-assertion (rising) edge depending on the total capacitance of the line and the number of chips connected to it. The sampling of the input on this port is equipped with a sychronizer to guarantee reliable operation.

DACMONV: Analog pin with dual purpose. It can be used to monitor each of the voltages generated by the on-chip voltage DACs. It can also be used to override the internal voltage DACs. The overriding is possible for one user-selectable DAC at a given time.

DACMONI: Analog pin with triple purpose. It can be used to monitor each of the currents generated by the on-chip current DACs. It can also be used to override the internal current DACs. The overriding is possible for one user-selectable DAC at a given time. It can also be used to override the internal current reference, thus changing the range of all current DACs simultaneously.

CHIPID[6:0]: Chip topological address and mode selection. This port is intended to assign a binary coded address to each chip depending on its position on the ALICE ITS Modules. The address is used in the transactions via the control interface. The address value also selects if the chip behaves as a Inner Barrel Chip, an Outer Barrel Module Master chip or an Outer Barrel Module Slave chip. This pads have been designed to be directly wired to digital supply in order to set a binary '1' on a given line. Leaving one unconnected effectively sets to '0' the corresponding bit line due to the internal pull-down.

2.4 Supply, ground and bias nets

Table 2.2: ALPIDE-3 supply, ground and bias nets.

Net	Type	Purpose
AVDD	SUPPLY	Analog domain supply
AVSS	GROUND	Analog domain ground
DVDD	SUPPLY	Digital domain supply
DVSS	GROUND	Digital domain ground
DVDD33	SUPPLY	Fuses programming supply
PWELL	SUBSTRATE	Substrate bias
SUB	SUBSTRATE	Substrate bias

AVDD, AVSS: Supply and ground rails of the analog domain. This includes the pixel front-end circuits and the analog biasing circuit.

DVDD, DVSS: Supply and ground rails of the digital domain. This includes the in-pixel configuration registers, the matrix readout circuits (AERD), the peripheral readout circuits and the chip input and output cells.

DVDD33: Supply for the programming of the write-once on chip fuses.

PWELL: bias of the p-type wells in the pixel matrix region.

SUB: bias to the contacts to the substrate in the seal ring and in the periphery region.

All supply and ground nets must be connected to the recommended voltages. The pads of each supply or ground net are internally electrically connected by the on-chip supply and ground meshes. Therefore it is not mandatory to wire all the pads of a given supply or ground net.

However, a reduction of the number of connected supply or ground pads can have detrimental effects on the circuit performance and operating capabilities or increase the risk of damaging the chip.

The PWELL and SUB bias nets cannot be left floating and must be strongly connected to appropriate bias voltages. The source impedance of the supply to these nets shall be kept as small as possible to limit the probability of latch-up.

The pads of the PWELL net are internally connected as well as those of the SUB net, therefore it is not mandatory to wire all the pads of a given net. The PWELL and SUB nets are weakly connected through the die substrate conductance.

The purpose of the PWELL and SUB substrate biasing nets is to enable the increase of the reverse bias voltage on the charge collecting diodes. This is obtained by applying to these nets a negative voltage with respect to analog ground (AVSS).

For system studies not requiring optimal sensor performance it is recommended to short both the PWELL and SUB pads to the AVSS ground (0 V with respect to AVSS). It is also recommended to bond the PWELL and SUB pads to a grounding conductor before any other pad is bonded, to reduce the risk of ESD damage.

2.5 Recommended operating conditions

Table 2.3: Recommended operating conditions.

		MIN	TYP	MAX	Unit	Condition
AVSS	Analog ground		0		V	
AVDD	Analog supply	1.62	1.8	1.98	V	
DVSS	Digital core ground		0		V	
DVDD	Digital core supply	1.62	1.8	1.98	V	
PWELL	Substrate bias		0	0	V	Shorted to AVSS
SUB	Substrate bias		0	0	V	Shorted to AVSS
V_I	Voltage at any CMOS input	0		DVDD	V	
V_{IL}	Low level digital input voltage			0.33*DVDD	V	
V_{IH}	High level digital input voltage	0.66*DVDD			V	
I_{OL}	Low level digital output current			13.7	mA	Vo <0.45
$\|I_{OH}\|$	High level digital output current			13.6	mA	Vo >DVDD-0.45
V_P or V_N	Voltage at any differential bus terminal	0		DVDD	V	
$\|V_{ID}\|$	Magnitude of differential input voltage	50		DVDD	mV	
R_L	Differential load resistance	40	50	60	Ω	
T	Operating temperature	-25	25	85	℃	

2.6 Electrical characteristics

Table 2.4: CMOS IOs electrical characteristics over recommended operating conditions unless otherwise noted.

		MIN	TYP	MAX	Unit	Condition
V_{OH}	High level output voltage	DVDD-0.45			V	Io >-13.6 mA

V_{OL}	Low level output voltage		0.45	V	Io <13.7 mA
$\|I_{IL}\|$		44.4	62	μA	Pads with pull-up
I_{IH}		0.87	3.8	nA	Pads with pull-up
$\|I_{IL}\|$		3.3	11.5	nA	Pads with pull-down
I_{IH}		44.4	62	μA	Pads with pull-down
R_{Pullup}	Internal pull-up	40.6		kΩ	Pads with pull-up
R_{Pullup}	Internal pull-down	40.6		kΩ	Pads with pull-down
C_{PAD}	Input capacitance	0.98		pF	Inputs with A type pad only
C_{PAD}	Input capacitance	4.5		pF	Inputs with A and B type pads

Table 2.5: Electrical characteristics of MCLK, DCTRL and DCLK differential ports over recommended operating conditions unless otherwise noted.

		MIN	TYP	MAX	Unit	Condition
C_P or C_N	Input capacitance			3	pF	V_I, other pin at 1.1 V, driver disabled
C_{PN}	Differential input capacitance				pF	V_{ID} =, V_{IC} =, driver disabled
I_{OZ}	High-impedance state output current	-45		102	μA	Driver disabled
Driver related characteristics						
		MIN	TYP	MAX	Unit	Condition
$\|V_{OD}\|$	Output differential signal magnitude	80		480	mV	
$\|I_{OD}\|$	Output differential current magnitude	2		8	mA	
$V_{OS(SS)}$	Steady-state output common signal	980		1210	mV	
$\Delta V_{OS(SS)}$	Change in steady-state output common signal between logic states	-20		+20	mV	
$V_{OS(PP)}$	Peak-to-peak output common signal			75	mV	
Receiver related characteristics						
		MIN	TYP	MAX	Unit	Condition
V_{IC}	Input common signal	DVSS+25	1.1	DVDD-25	mV	
V_{IT+}	Positive-going differential input voltage threshold			50	mV	
V_{IT-}	Negative-going differential input voltage threshold	-50			mV	

2.7 Timing requirements

2.8 Switching characteristics

2.9 Pad tables and geometrical data

A floorplan view with the name of the signals at the pads used for the connection to the ALICE ITS FPCs is given in Figure 2.2. The pad naming convention and the layout of the die with the position of the pads are illustrated in Figure 2.3.

Table 2.6 lists all the pads and interface nets of the chip. Table 2.7 gives the x and y coordinates of the *center* points of the chip pads.

Two types of pads with differing geometries are employed in the ALPIDE-3 chip.

Type A pads are used for the pads in the pad ring along the chip south edge (from A00 to A100). All interface nets are available in this pad ring. Type A pads are standard size and intended to support wire bonding, probe testing or other applications. Figure 2.4 details the geometry of the opening of type A pads. The opening in the passivation layer of type A pads is square and 88 μm wide.

Type B are large pads over logic used above the periphery and the sensitive matrix of the chip (B00-B20, C00-C14, D00-D07, E00-E07, F00-F07, G00-G06). These pads enable the connection to Flexibel Printed Circuits by laser soldering. The nets available through pads of type B are also found in the ring of pads of type A (A00-A100). Figure 2.5 details the geometry of the opening of pads of type B. The opening in the passivation layer of type B pads has rounded edges and it is 290 μm wide.

Table 2.6: ALPIDE-3 pads and interface nets.

Pad Id	Net	Type	Direction	Purpose
A00	PWELL	SUBSTRATE		Substrate bias, matrix
A01	AVSS	GROUND		Analog ground
A02	SUB	SUBSTRATE		Substrate bias, periphery
A03	AVDD	SUPPLY		Analog supply
A04	DVSS	GROUND		Digital ground
A05	DVDD	SUPPLY		Digital supply
A06	DVDD33	SUPPLY		Fuses programming supply
A07	AVSS	GROUND		Analog ground
A08	AVDD	SUPPLY		Analog supply
A09	DVSS	GROUND		Digital ground
A10	DVDD	SUPPLY		Digital supply
A11	SCI	CMOS	NA	Future use
A12	AVSS	GROUND		Analog ground
A13	AVDD	SUPPLY		Analog supply
A14	CHIPID[6]	CMOS, pull-down	INPUT	Topological chip address
A15	DVSS	GROUND		Digital ground
A16	MCLK_P	MLVDS	INPUT	Forwarded clock input
A17	MCLK_N	MLVDS	INPUT	Forwarded clock input
A18	DVDD	SUPPLY		Digital supply
A19	PWELL	SUBSTRATE		Substrate bias, matrix
A20	RESERVE_0	CMOS	NA	Future use
A21	RST_N	CMOS, pull-up	INPUT	Global chip reset
A22	RESERVE_2	CMOS	NA	Future use
A23	DVSS	GROUND		Digital ground
A24	DVDD	SUPPLY		Digital supply
A25	CHIPID[5]	CMOS, pull-down	INPUT	Topological chip address
A26	POR_DIS_N	CMOS, pull-up	INPUT	Power On Reset Disable
A27	AVSS	GROUND		Analog ground
A28	AVDD	SUPPLY		Analog supply
A29	DVSS	GROUND		Digital ground
A30	DCTRL_P	MLVDS	BIDIR	Differential Control port
A31	DCTRL_N	MLVDS	BIDIR	Differential Control port
A32	DVDD	SUPPLY		Digital supply
A33	SUB	SUBSTRATE		Substrate bias, periphery
A34	AVSS	GROUND		Analog ground
A35	AVDD	SUPPLY		Analog supply

A36	SCO	CMOS	NA	Future use
A37	CHIPID[4]	CMOS, pull-down	INPUT	Topological chip address
A38	DVSS	GROUND		Digital ground
A39	DVDD	SUPPLY		Digital supply
A40	DCLK_P	MLVDS	BIDIR	Clock input. Clock forwarding output
A41	DCLK_N	MLVDS	BIDIR	Clock input. Clock forwarding output
A42	PWELL	SUBSTRATE		Substrate bias, matrix
A43	DVSS	GROUND		Digital ground
A44	DVDD	SUPPLY		Digital supply
A45	SCE	CMOS	NA	Future use
A46	AVSS	GROUND		Analog ground
A47	AVDD	SUPPLY		Analog supply
A48	CHIPID[3]	CMOS, pull-down	INPUT	Topological chip address
A49	RESERVE_1	CMOS	NA	Future use
A50	SUB	SUBSTRATE		Substrate bias, periphery
A51	DVSS	GROUND		Digital ground
A52	DVDD	SUPPLY		Digital supply
A53	HSDATA_P	LVDS	OUTPUT	Serial data output
A54	HSDATA_N	LVDS	OUTPUT	Serial data output
A55	CHIPID[2]	CMOS, pull-down	INPUT	Topological chip address
A56	DVSS	GROUND		Digital ground
A57	DVDD	SUPPLY		Digital supply
A58	AVSS	GROUND		Analog ground
A59	AVDD	SUPPLY		Analog supply
A60	DVSS	GROUND		Digital ground
A61	DVDD	SUPPLY		Digital supply
A62	CTRL	CMOS, pull-up	BIDIR	Control port (OB)
A63	DVSS	GROUND		Digital ground
A64	DVDD	SUPPLY		Digital supply
A65	DVSS	GROUND		Digital ground
A66	DVDD	SUPPLY		Digital supply
A67	DATA[3]	CMOS, pull-up	BIDIR	Data port
A68	DATA[7]	CMOS, pull-up	BIDIR	Data port
A69	DVSS	GROUND		Digital ground
A70	DVDD	SUPPLY		Digital supply
A71	CHIPID[1]	CMOS, pull-down	INPUT	Topological chip address
A72	DATA[2]	CMOS, pull-up	BIDIR	Data port
A73	DATA[6]	CMOS, pull-up	BIDIR	Data port
A74	DVSS	GROUND		Digital ground
A75	DVDD	SUPPLY		Digital supply
A76	DVSS	GROUND		Digital ground
A77	DATA[1]	CMOS, pull-up	BIDIR	Data port
A78	DATA[5]	CMOS, pull-up	BIDIR	Data port
A79	DVDD	SUPPLY		Digital supply
A80	AVSS	GROUND		Analog ground
A81	AVDD	SUPPLY		Analog supply
A82	DATA[0]	CMOS, pull-up	BIDIR	Data port
A83	DATA[4]	CMOS, pull-up	BIDIR	Data port
A84	SUB	SUBSTRATE		Substrate bias, periphery
A85	DVSS	GROUND		Digital ground
A86	DVDD	SUPPLY		Digital supply
A87	BUSY	CMOS, pull-up	BIDIR	Busy flag
A88	CHIPID[0]	CMOS, pull-down	INPUT	Topological chip address
A89	DVSS	GROUND		Digital ground
A90	DVDD	SUPPLY		Digital supply
A91	PWELL	SUBSTRATE		Substrate bias, matrix

A92	DACMONV	ANALOG		Voltage monitoring and overriding
A93	AVSS	GROUND		Analog ground
A94	AVDD	SUPPLY		Analog supply
A95	SUB	SUBSTRATE		Substrate bias, periphery
A96	PWELL	SUBSTRATE		Substrate bias, matrix
A97	DACMONI	ANALOG		Current monitoring and overriding
A98	SUB	SUBSTRATE		Substrate bias, periphery
A99	AVSS	GROUND		Analog ground
A100	AVDD	SUPPLY		Analog supply
B00	SUB	SUBSTRATE		Substrate bias, periphery
B01	DVDD33	SUPPLY		Fuses programming supply
B02	MCLK_P	MLVDS	INPUT	Forwarded clock input
B03	MCLK_N	MLVDS	INPUT	Forwarded clock input
B04	RST_N	CMOS, pull-up	INPUT	Global chip reset
B05	POR_DIS_N	CMOS, pull-up	INPUT	Power On Reset Disable
B06	DCTRL_P	MLVDS	BIDIR	Differential Control port
B07	DCTRL_N	MLVDS	BIDIR	Differential Control port
B08	DCLK_P	MLVDS	BIDIR	Main clock input. Clock forward output
B09	DCLK_N	MLVDS	BIDIR	Main clock input. CLock forward output
B10	HSDATA_P	LVDS	OUTPUT	Serial data output
B11	HSDATA_N	LVDS	OUTPUT	Serial data output
B12	CTRL	CMOS, pull-up	BIDIR	Control port (OB)
B13	DATA[3]	CMOS, pull-up	BIDIR	Data port (OB local bus)
B14	DATA[2]	CMOS, pull-up	BIDIR	Data port (OB local bus)
B15	DATA[1]	CMOS, pull-up	BIDIR	Data port (OB local bus)
B16	DATA[0]	CMOS, pull-up	BIDIR	Data port (OB local bus)
B17	BUSY	CMOS, pull-up	BIDIR	Busy flag
B18	DACMONV	ANALOG		Voltage monitoring and overriding
B19	DACMONI	ANALOG		Current monitoring and overriding
B20	SUB	SUBSTRATE		Substrate bias, periphery
C00	DVSS	GROUND		Digital ground
C01	CHIPID[6]	CMOS, pull-down	INPUT	Topological chip address
C02	DVSS	GROUND		Digital ground
C03	CHIPID[5]	CMOS, pull-down	INPUT	Topological chip address
C04	DVSS	GROUND		Digital ground
C05	CHIPID[4]	CMOS, pull-down	INPUT	Topological chip address
C06	DVSS	GROUND		Digital ground
C07	CHIPID[3]	CMOS, pull-down	INPUT	Topological chip address
C08	DVSS	GROUND		Digital ground
C09	CHIPID[2]	CMOS, pull-down	INPUT	Topological chip address
C10	DVSS	GROUND		Digital ground
C11	CHIPID[1]	CMOS, pull-down	INPUT	Topological chip address
C12	DVSS	GROUND		Digital ground
C13	CHIPID[0]	CMOS, pull-down	INPUT	Topological chip address
C14	DVSS	GROUND		Digital ground
D00	DVDD	SUPPLY		Digital supply
D01	DVDD	SUPPLY		Digital supply
D02	DVDD	SUPPLY		Digital supply
D03	DVDD	SUPPLY		Digital supply
D04	DVDD	SUPPLY		Digital supply
D05	DVDD	SUPPLY		Digital supply
D06	DVDD	SUPPLY		Digital supply
D07	DVDD	SUPPLY		Digital supply

E00	AVSS	GROUND	Analog ground
E01	AVSS	GROUND	Analog ground
E02	AVSS	GROUND	Analog ground
E03	AVSS	GROUND	Analog ground
E04	AVSS	GROUND	Analog ground
E05	AVSS	GROUND	Analog ground
E06	AVSS	GROUND	Analog ground
E07	AVSS	GROUND	Analog ground
F00	AVDD	SUPPLY	Analog supply
F01	AVDD	SUPPLY	Analog supply
F02	AVDD	SUPPLY	Analog supply
F03	AVDD	SUPPLY	Analog supply
F04	AVDD	SUPPLY	Analog supply
F05	AVDD	SUPPLY	Analog supply
F06	AVDD	SUPPLY	Analog supply
F07	AVDD	SUPPLY	Analog supply
G00	PWELL	SUBSTRATE	Substrate bias, matrix
G01	SUB	SUBSTRATE	Substrate bias, periphery
G02	PWELL	SUBSTRATE	Substrate bias, matrix
G03	SUB	SUBSTRATE	Substrate bias, periphery
G04	PWELL	SUBSTRATE	Substrate bias, matrix
G05	SUB	SUBSTRATE	Substrate bias, periphery
G06	PWELL	SUBSTRATE	Substrate bias, matrix

Table 2.7: Coordinates of the center points of the pads.

Pad Id	Net	Pad Geometry	x [μm]	y [μm]
A00	PWELL	A	607.62	66.8
A01	AVSS	A	827.62	66.8
A02	SUB	A	1047.62	66.8
A03	AVDD	A	1267.62	66.8
A04	DVSS	A	1487.62	66.8
A05	DVDD	A	1707.62	66.8
A06	DVDD33	A	2147.62	66.8
A07	AVSS	A	2367.62	66.8
A08	AVDD	A	2587.62	66.8
A09	DVSS	A	2807.62	66.8
A10	DVDD	A	3027.62	66.8
A11	SCI	A	3247.62	66.8
A12	AVSS	A	3467.62	66.8
A13	AVDD	A	3687.62	66.8
A14	CHIPID[6]	A	3907.62	66.8
A15	DVSS	A	4127.62	66.8
A16	MCLK_P	A	4828.125	66.8
A17	MCLK_N	A	5048.125	66.8
A18	DVDD	A	5887.62	66.8
A19	PWELL	A	6107.62	66.8
A20	RESERVE_0	A	6327.62	66.8
A21	RST_N	A	6547.62	66.8
A22	RESERVE_2	A	6767.62	66.8
A23	DVSS	A	6987.62	66.8
A24	DVDD	A	7207.62	66.8
A25	CHIPID[5]	A	7427.62	66.8

A26	POR_DIS	A	7647.62	66.8
A27	AVSS	A	8087.62	66.8
A28	AVDD	A	8307.62	66.8
A29	DVSS	A	8527.62	66.8
A30	DCTRL_P	A	9228.125	66.8
A31	DCTRL_N	A	9448.125	66.8
A32	DVDD	A	10287.62	66.8
A33	SUB	A	10507.62	66.8
A34	AVSS	A	10727.62	66.8
A35	AVDD	A	10947.62	66.8
A36	SCO	A	11167.62	66.8
A37	CHIPID[4]	A	11387.62	66.8
A38	DVSS	A	11607.62	66.8
A39	DVDD	A	11827.62	66.8
A40	DCLK_P	A	12528.125	66.8
A41	DCLK_N	A	12748.125	66.8
A42	PWELL	A	13587.62	66.8
A43	DVSS	A	13807.62	66.8
A44	DVDD	A	14027.62	66.8
A45	SCE	A	14247.62	66.8
A46	AVSS	A	14467.62	66.8
A47	AVDD	A	14687.62	66.8
A48	CHIPID[3]	A	14907.62	66.8
A49	RESERVE_1	A	15127.62	66.8
A50	SUB	A	15347.62	66.8
A51	DVSS	A	15567.62	66.8
A52	DVDD	A	15787.62	66.8
A53	HSDATA_O_P	A	17344.275	66.8
A54	HSDATA_O_N	A	17564.275	66.8
A55	CHIPID[2]	A	18647.62	66.8
A56	DVSS	A	18867.62	66.8
A57	DVDD	A	19087.62	66.8
A58	AVSS	A	19307.62	66.8
A59	AVDD	A	19527.62	66.8
A60	DVSS	A	19747.62	66.8
A61	DVDD	A	19967.62	66.8
A62	CTRL	A	20187.62	66.8
A63	DVSS	A	20407.62	66.8
A64	DVDD	A	20627.62	66.8
A65	DVSS	A	20847.62	66.8
A66	DVDD	A	21067.62	66.8
A67	DATA[3]	A	21287.62	66.8
A68	DATA[7]	A	21507.62	66.8
A69	DVSS	A	21727.62	66.8
A70	DVDD	A	21947.62	66.8
A71	CHIPID[1]	A	22167.62	66.8
A72	DATA[2]	A	22387.62	66.8
A73	DATA[6]	A	22607.62	66.8
A74	DVSS	A	22827.62	66.8
A75	DVDD	A	23047.62	66.8
A76	DVSS	A	23267.62	66.8
A77	DATA[1]	A	23487.62	66.8
A78	DATA[5]	A	23707.62	66.8
A79	DVDD	A	23927.62	66.8
A80	AVSS	A	24147.62	66.8
A81	AVDD	A	24367.62	66.8

A82	DATA[0]	A	24587.62	66.8
A83	DATA[4]	A	24807.62	66.8
A84	SUB	A	25027.62	66.8
A85	DVSS	A	25247.62	66.8
A86	DVDD	A	25467.62	66.8
A87	BUSY	A	25687.62	66.8
A88	CHIPID[0]	A	25907.62	66.8
A89	DVSS	A	26127.62	66.8
A90	DVDD	A	26347.62	66.8
A91	PWELL	A	26567.62	66.8
A92	DACMONV	A	26787.62	66.8
A93	AVSS	A	27007.62	66.8
A94	AVDD	A	27227.62	66.8
A95	SUB	A	27447.62	66.8
A96	PWELL	A	27667.62	66.8
A97	DACMONI	A	27887.62	66.8
A98	SUB	A	28987.62	66.8
A99	AVSS	A	29207.62	66.8
A100	AVDD	A	29427.62	66.8
B00	SUB	B	1057.62	525
B01	DVDD33	B	2157.62	525
B02	MCLK_P	B	4357.62	525
B03	MCLK_N	B	5457.62	525
B04	RST_N	B	6557.62	525
B05	POR_DIS	B	7657.62	525
B06	DCTRL_P	B	8757.62	525
B07	DCTRL_N	B	9857.62	525
B08	DCLK_P	B	12057.62	525
B09	DCLK_N	B	13157.62	525
B10	HSDATA_P	B	16897.62	525
B11	HSDATA_N	B	17997.62	525
B12	CTRL	B	20197.62	525
B13	DATA[3]	B	21297.62	525
B14	DATA[2]	B	22397.62	525
B15	DATA[1]	B	23497.62	525
B16	DATA[0]	B	24597.62	525
B17	BUSY	B	25697.62	525
B18	DACMONV	B	26797.62	525
B19	DACMONI	B	27897.62	525
B20	SUB	B	28997.62	525
C00	DVSS	B	2105.16	7890.88
C01	CHIPID[6]	B	3947.28	7890.88
C02	DVSS	B	5789.40	7890.88
C03	CHIPID[5]	B	7631.52	7890.88
C04	DVSS	B	9473.64	7890.88
C05	CHIPID[4]	B	11315.76	7890.88
C06	DVSS	B	13157.88	7890.88
C07	CHIPID[3]	B	15000.00	7890.88
C08	DVSS	B	16842.12	7890.88
C09	CHIPID[2]	B	18684.24	7890.88
C10	DVSS	B	20526.36	7890.88
C11	CHIPID[1]	B	22368.48	7890.88
C12	DVSS	B	24210.60	7890.88
C13	CHIPID[0]	B	26052.72	7890.88

C14	DVSS	B	27894.84	7890.88
D00	DVDD	B	2105.16	9906.88
D01	DVDD	B	5789.40	9906.88
D02	DVDD	B	9473.64	9906.88
D03	DVDD	B	13157.88	9906.88
D04	DVDD	B	16842.12	9906.88
D05	DVDD	B	20526.36	9906.88
D06	DVDD	B	24210.6	9906.88
D07	DVDD	B	27894.84	9906.88
E00	AVSS	B	2105.16	11465.92
E01	AVSS	B	5789.40	11465.92
E02	AVSS	B	9473.64	11465.92
E03	AVSS	B	13157.88	11465.92
E04	AVSS	B	16842.12	11465.92
E05	AVSS	B	20526.36	11465.92
E06	AVSS	B	24210.6	11465.92
E07	AVSS	B	27894.84	11465.92
F00	AVDD	B	2105.16	13723.84
F01	AVDD	B	5789.40	13723.84
F02	AVDD	B	9473.64	13723.84
F03	AVDD	B	13157.88	13723.84
F04	AVDD	B	16842.12	13723.84
F05	AVDD	B	20526.36	13723.84
F06	AVDD	B	24210.6	13723.84
F07	AVDD	B	27894.84	13723.84
G00	PWELL	B	3947.28	14395.84
G01	SUB	B	7631.52	14395.84
G02	PWELL	B	11315.76	14395.84
G03	SUB	B	15000.00	14395.84
G04	PWELL	B	18684.24	14395.84
G05	SUB	B	22368.48	14395.84
G06	PWELL	B	26052.72	14395.84

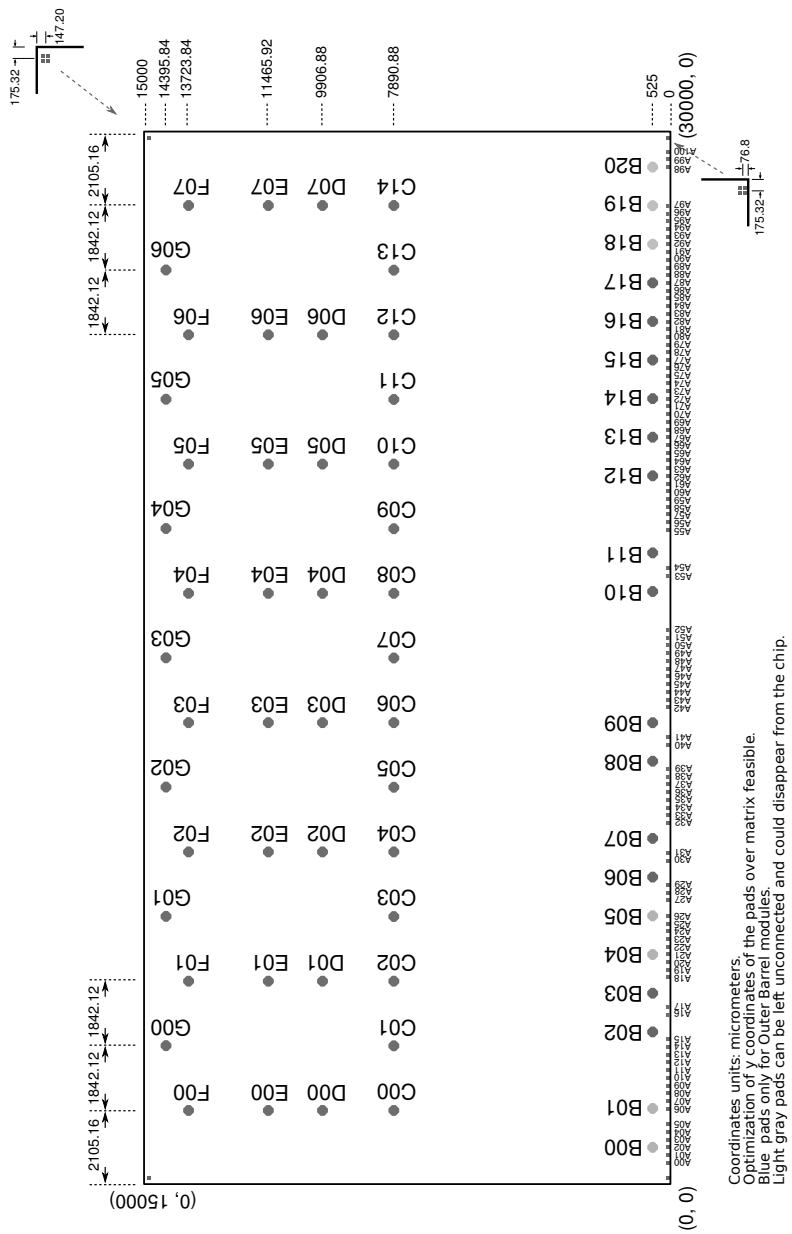


Figure 2.3: ALPIDE-3 pad naming convention.

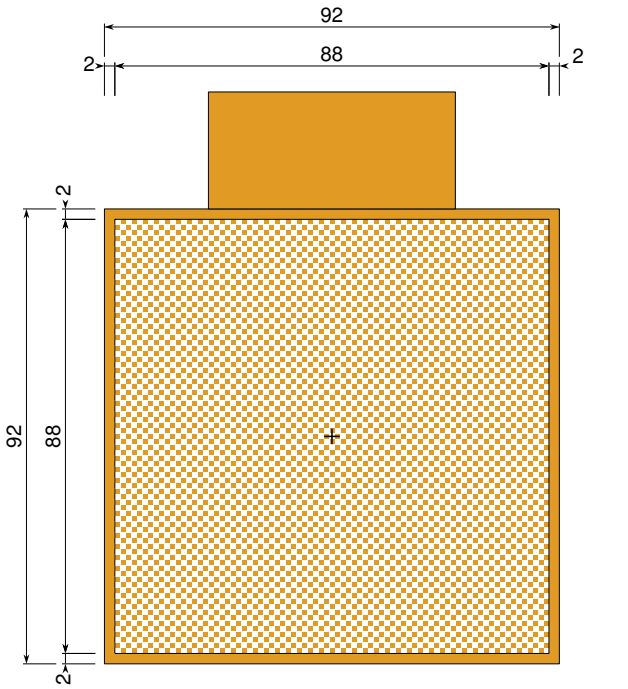


Figure 2.4: Geometry of type A pad.

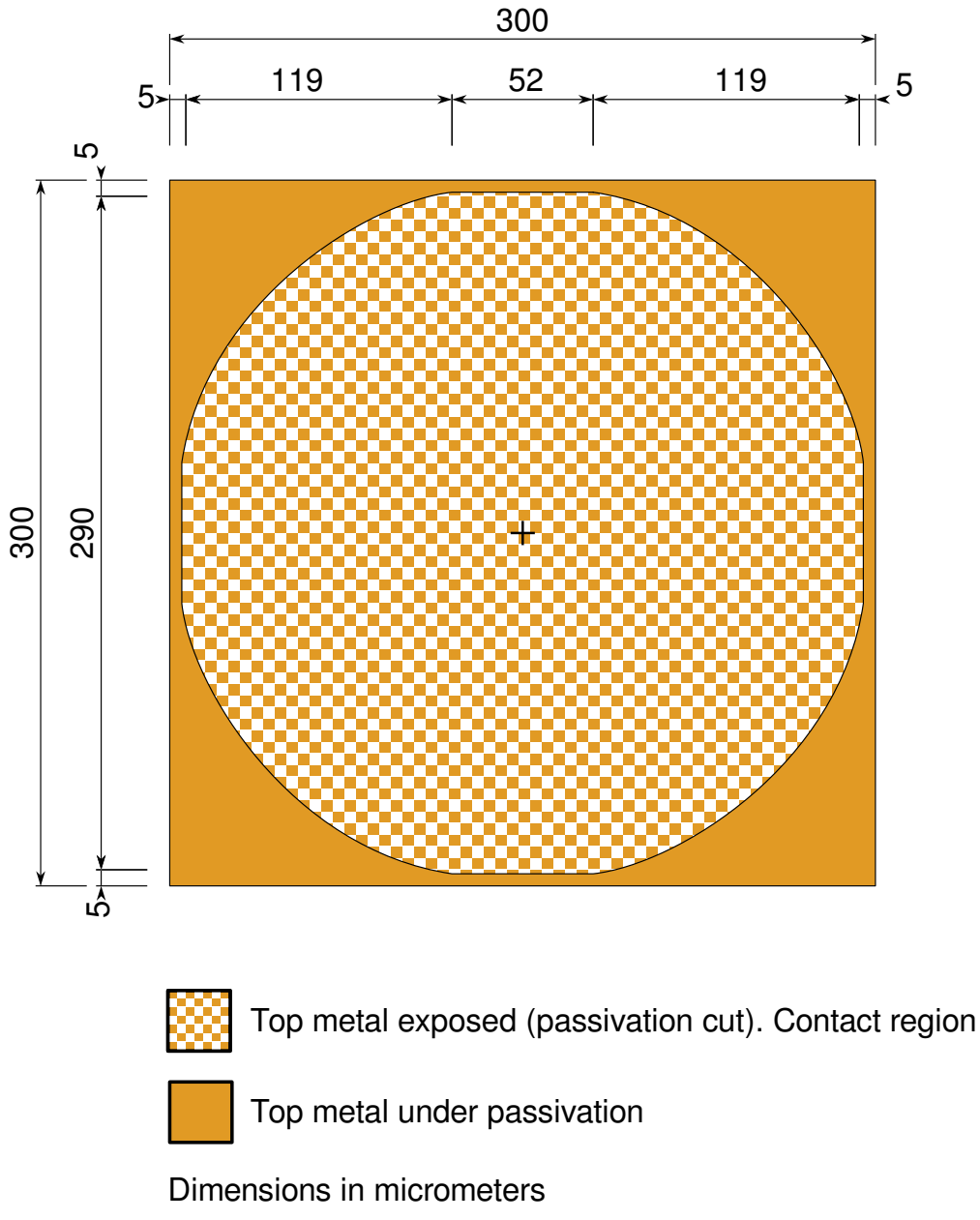


Figure 2.5: Geometry of type B pad.

3 User manual

This chapter shall outline the operation of the chip as far as the users of the chip are interested. Programming options, control options, operating mode, data formats should be summarized.

3.1 Control interface and protocol

3.1.1 Chip identification and geographical address allocation

The chip can operate in three different roles in the ALICE ITS Upgrade application: Inner Barrel Chip, Outer Barrel Module Master and Outer Barrel Module Slave. The selection of the operating mode is based on the input applied to the **CHIPID[6:0]** chip port. This port selects the operating mode and also provides an address to the chip for the slow control transactions. The pads of this port shall be tied to digital supply (DVDD) to set the corresponding bit to 1. The pads have internal pull-down resistors. Leaving them unconnected is equivalent to shorting them to digital ground (DVSS) thus establishing a value of 0 for the corresponding bit.

The three bits **CHIPID[6:4]** constitute a **Module Identifier** field. The remaining bits **CHIPID[3:0]** act as identifiers of the position and role inside a module. The reference specification for the allocation of the values of CHIPID to the chips on the modules is illustrated in Fig. 3.1 and Fig. 3.2.

The *Module Identifier* field shall be **all zeros** for Inner Barrel chips. Chips with the three bits CHIPID[6:4] all set to zero identify and configure themselves as Inner Barrel Chips. The remaining bits **CHIPID[3:0]** shall be a position dependent binary identifier and can have any of the values from 0 up to 14 (binary *b1110*). The binary code *b1111* **shall not be used** for CHIPID[3:0], since it is reserved for broadcast addressing.

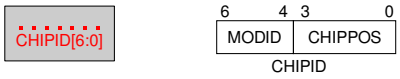
The *Module Identifier* field shall contain at least one non-zero bit to configure the chip to operate in one of the Outer Barrel roles, i.e. CHIPID[6:4] *must not* be *b000*. CHIPID[6:4] is intended to be a module index, a unique value for all the fourteen chips of a specific module on a half-stave. CHIPID[6:4] can be one of *b001*, *b010*, *b011*, *b100* for modules on Middle Layers staves. CHIPID[6:4] can be one of *b001*, *b010*, *b011*, *b100*, *b101*, *b110*,*b111* for modules on Outer Layers staves. The four bits **CHIPID[3:0]** are also meant to specify the geographical position of the chip on the Outer Barrel Module and its role. There are two rows of seven chips on an Outer Barrel Module. Bit CHIPID[3] identifies in which of the two rows the chip is located. The remaining three bits **CHIPID[2:0]** select the operating mode of Outer Barrel Master if they are all set to zero, *b000*. Otherwise the chip behaves as an Outer Barrel Slave. Bits CHIPID[2:0] **must not be** binary *b111*, since this is reserved for broadcast addressing.

3.1.2 Control interfaces

The slow control interface serve two purposes:

1. provide write and read access to internal registers, commands, configuration and memories
2. distribute trigger commands or broadcast synchronous signals

The pALPIDE-3 chip has two ports to implement the slow control functionalities: a differential DCNTRL port and a single-ended CNTRL port. The port that is actually functional depends on the operating scenario. In Inner Barrel Chip role only the differential DCNTRL port is used.



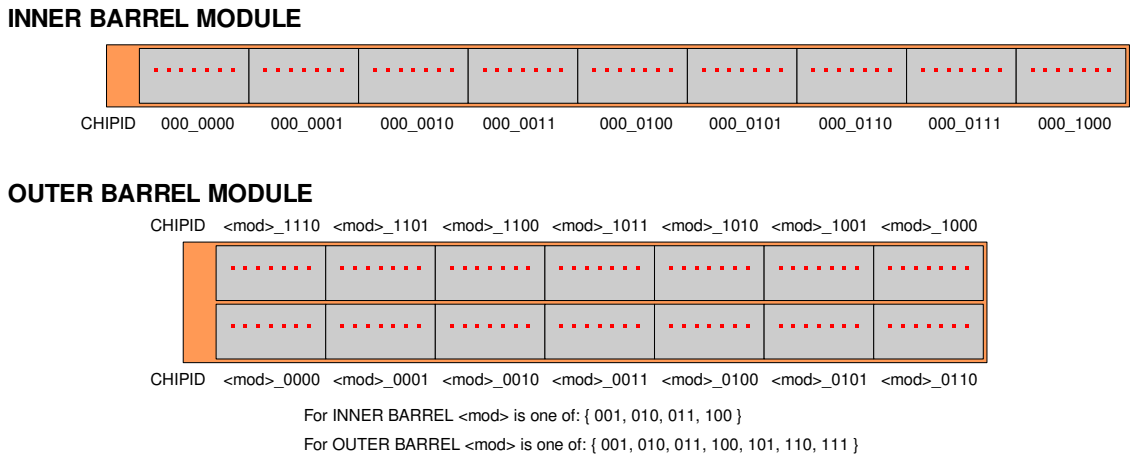


Figure 3.1: Illustration of chip identification and geographical address allocation. Default assignments of CHIPID values on one Inner Barrel Module and on a generic Outer Barrel Module.

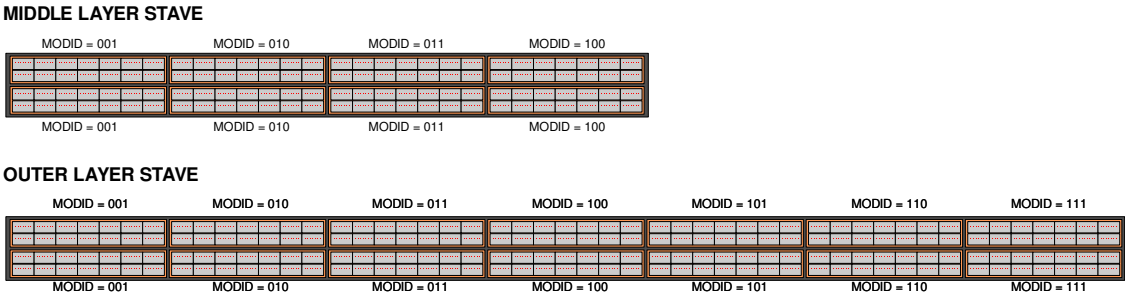


Figure 3.2: Illustration of chip identification and geographical address allocation. Default assignments of Module Identifier fields for the Middle Layer Stave and Outer Layer Stave.

In Outer Barrel Module Master role both ports are operated. In Outer Barrel Module Slave role only the single ended CNTRL port is used. The slow control interface and the ports have been designed to implement a hierarchical control bus topology with multi-point connections of chips on the same electrical line.

The nine (9) chips on an Inner Barrel module are directly connected to a shared control differential line using the DCNTRL port. The Inner Barrel control bus is entirely based on differential signaling and it has multipoint topology.

On Outer Barrel Staves, the control bus is implemented with a hierarchical structure. Every Module Master chip is connected with other Master chips on the same half-stave by a differential shared bus with multi-point topology. The differential line crosses the module boundaries and can connect 4 (Middle Layer Stave) or 7 (Outer Layer Stave) Module Master chips on the row of chips located on the same row along the z axis. Each Outer Barrel Module Master chip acts as a slow control *hub* and relays the control transactions to six Outer Barrel Module Slave chips that are connected in a multi-point shared line topology with the Master. The bus segment local to the Outer Barrel Module operates with single-ended signaling.

Inner Barrel modules and Outer Barrel modules present to the off-detector hardware fully equivalent control interfaces, physically appearing as a bi-directional differential port. The control interface supports bi-directional, half-duplex data exchanges. The signaling on the control buses is serial and synchronous with the system clock (nominal 40.08 MHz, LHC clock) that is distributed through a hierarchical clock tree. The slow control *transactions* are governed by the off-detector hardware initiating all type of messaging on the control bus. All chips continuosly sample the incoming serial control stream and decode the transactions on the bus.

3.1.3 Control transactions format

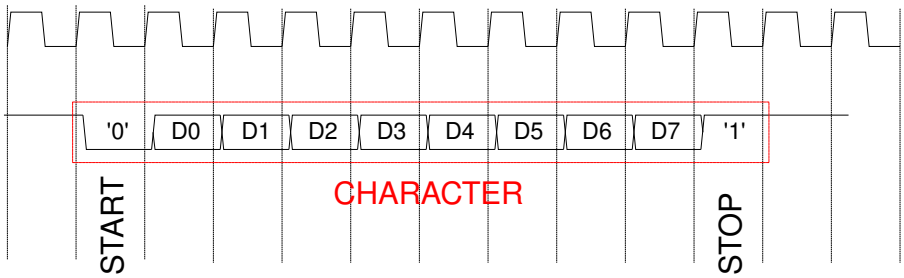


Figure 3.3: Format of a single character exchanged on the control bus.

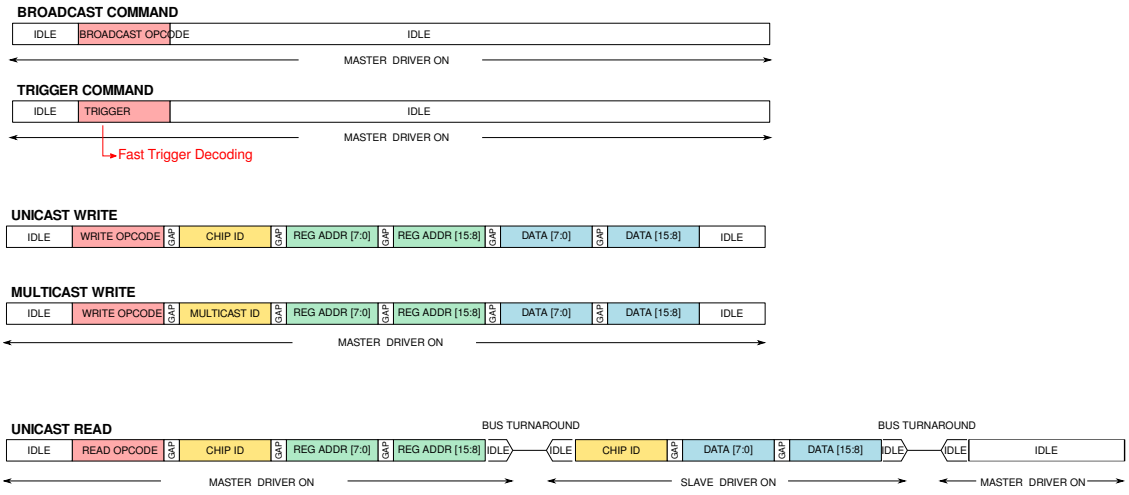


Figure 3.4: Format of valid transactions on the control bus.

Opcode	Hex value	Purpose
TRIGGER	8'hB1	Trigger command
TRIGGER	8'h55	Trigger command
TRIGGER	8'hC9	Trigger command
TRIGGER	8'h2D	Trigger command
GRST	8'hD2	Chip global reset
PRST	8'hE4	Pixel matrix reset
PULSE	8'h78	Pixel matrix pulse
BCRST	8'h36	Bunch Counter reset
RORST	8'h63	Readout (RRU/TRU/DMU) reset
WROP	8'h9C	Start Unicast or Multicast Write
RDOP	8'h4E	Start Unicast Read

Table 3.1: Valid opcodes of control transactions

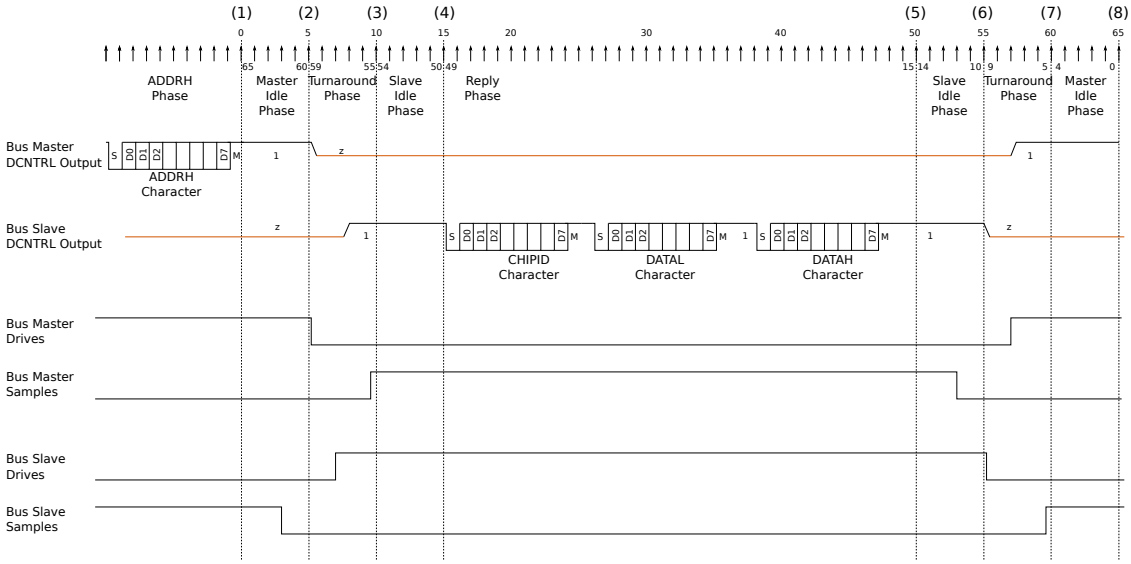


Figure 3.5: Timing diagram of the reply phase of a Read transaction including turnaroud phases.

3.2 Control registers and addressing space

The pALPIDE-3 control interface provides access to the chip internal registers and data path memories. The write and read transactions via the control interface have 16 bit wide address field and 16 bit wide data payload.

3.2.1 Addressing space

The register address is internally treated as composed of three sub-fields:

- Region selector **RGN_ADDR[4:0]** = ADDRESS[15:11]
- Register or memory group selector **BASE_ADDR[2:0]** = ADDRESS[10:8]
- Register offset **SUB_ADDR[7:0]** = ADDRESS[7:0].

The registers and physical memory locations are mapped to the addressing space according to the scheme described in Table 3.2. The fields qualified *not considered* are equivalent for the address decoding. Most registers are in fact accessible at multiple addresses. A read access to an unused address returns decimal value 255 (hexadecimal FFFF) while a write access has no effects.

Several addresses point to registers or physical memory locations that are less than 16 bit wide. In these cases the physical bits are accessible as *least significant* bits of the transaction data field. The unused most significant bits are read as constant binary 0s.

Table 3.2: pALPIDE-3 registers and memory addressing.

Address[15 : 0]			Mode	Reset	Register or memory
RGN_ADDR [4 : 0]	BASE_ADDR [2 : 0]	SUB_ADDR [7 : 0]			

NC	0	0	R/W	h0000	Command Register.
NC	0	1	R/W	h0020	Periphery Control register
NC	0	2	R/W	h0000	Region Disable Register 1
NC	0	3	R/W	h0000	Region Disable Register 2
NC	0	4	R/W	h0010	FROMU Configuration Register 1
NC	0	5	R/W	h0000	FROMU Configuration Register 2
NC	0	6	R/W	h0000	FROMU Pulsing Register1
NC	0	7	R/W	h0000	FROMU Pulsing Register 2
NC	0	8	R	-	FROMU Status Register 1
NC	0	9	R	-	FROMU Status register 2
NC	0	10	R/W	h0AAA	DAC settings for DCLK/MCLK I/O buffers
NC	0	11	R/W	h00AA	DAC settings for CMU I/O buffers
NC	0	12	R/W	h008F	CMU and DMU Configuration Register
NC	0	13	R	-	CMU Errors Counter
NC	0	14	R/W	h008D	DTU Configuration Register
NC	0	15	R/W	h0088	DTU DACs Register
NC	0	16	R	-	DTU PLL Lock Register 1
NC	0	17	R/W	h0000	DTU PLL Lock Register 2
NC	0	18	R/W	h0000	DTU Test Register 1
NC	0	19	R/W	h0000	DTU Test Register 2
NC	0	20	R/W	h0000	DTU Test Register 3
NC	0	21	R/W	h0008	BUSY min width
NC	0	22	R/W	h0000	Fuses Write LSBs
NC	0	23	R/W	h0000	Fuses Write MSBs
NC	0	24	R	-	Fuses Read LSBs
NC	0	25	R	-	Fuses Read MSBs
NC	0	26	R	-	Temperature Sensor
0-31	1	0-127	R/W	-	RRU MEB LSBs.
0-31	2	0-127	R/W	-	RRU MEB MSBs
0-31	3	0	R/W	h0000	Double Column Disable Register
NC	4	0	R	-	DMU and TRU State
NC	5	0	R/W	h0000	Pixel CFG Register 1
NC	5	1	R/W	h0000	Pixel CFG Register 2
NC	5	2	R/W	h0000	Pixel CFG Register 3 (Special Behaviour)
NC	6	0	R/W	h0400	Analog Monitor and Override Register
NC	6	1	R/W	h0075	VRESETP
NC	6	2	R/W	h0000	VRESETD
NC	6	3	R/W	h0056	VCASP
NC	6	4	R/W	h0039	VCASN
NC	6	5	R/W	h00FF	VPULSEH
NC	6	6	R/W	h0000	VPULSEL
NC	6	7	R/W	h0040	VCASN2
NC	6	8	R/W	h0000	VCLIP
NC	6	9	R/W	h0000	VTEMP
NC	6	10	R/W	h0000	IAUX2
NC	6	11	R/W	h0032	IRESET
NC	6	12	R/W	h0040	IDB

NC	6	13	R/W	h0040	IBIAS
NC	6	14	R/W	h0033	ITHR
NC	6	15	R/W	h0000	Buffer Bypass Register
0-31	7	0	R	-	Region Readout Status Register

3.2.2 Description of internal registers

Commands register

The commands register is a special register allowing the execution of internal operations or sequences. Writing of specific codes to these register generates internal pulses. The valid and recognised codes are listed in table 3.2.2.

Opcode	Hex value	Purpose
GRST	16'h00D2	Chip global reset
PRST	16'h00E4	Pixel matrix **RESET**
PULSE	16'h0078	Pixel matrix **PULSE**
BCRST	16'h0036	Bunch Counter reset
RORST	16'h0063	Readout (RRU/TRU/DMU) reset
WROP	16'h009C	Start Unicast or Multicast Write
RDOP	16'h004E	Start Unicast Read
CMU CLEAR ERR	16'hFF00	Clear CMU error flags

Table 3.3: Command codes recognised by the command register

It is not a coincidence that the valid opcodes of broadcast command transactions (3.1.3) coincide with valid commands. The byte code of *BROADCAST COMMAND* control transactions or the byte code of *TRIGGER COMMAND* transactions are always written to the command register (padding the most significant byte with zeros). Therefore, the *BROADCAST COMMAND* control transactions are effectively shortcuts for a broadcast write transaction to the command register of all receiving chips. Notice however that the command *CMU CLEAR ERR* is accessible only by a normal write transaction and there is no shortcut for it. This reflects on the command code having the most significant byte differing from binary zero.

The *TRIGGER COMMANDs* are an exception to the mechanism described before. These are decoded directly in the CMU during deserialization, not in the command register. This is done to minimize the latency of decoding trigger commands. However the *TRIGGER* opcode is still written to the command register on a valid *TRIGGER COMMAND* transaction and a read back from the command register after the transmission of a trigger command will return the trigger opcode value.

Periphery Control Register

Bits	Purpose
1:0	Chip Mode selector
2	Clustering enable
3	Start Memory Self Test
4	Unused
5	Matrix Readout Speed
6	Force Busy
7	Force Busy Value
15:8	Not used

Table 3.4: Periphery Control Register Field Description

- **Chip Mode Selector** – 0: Configuration Mode (default), 1: Readout Triggered Mode, 2: Readout Continuous Mode.
- **Clustering Enable** – 0: Clustering disabled, 1: Clustering enabled (default)
- **Start Memory Self Test** – Bit will auto reset, memory status is written on bit 1 of Region Readout Status Register.
- **Matrix Readout Speed** – 0: 10MHz, 1: 20MHz (default).
- **Force Busy** – 0: disabled (default), 1: BUSY line is forced to the value specified in Force Busy Value bit.
- **Force Busy Value** – Logical value forced in the BUSY line when Force Busy is asserted.

Region Disable Register 1

A 16–bit register used to disable the readout of specific regions. When a bit is set to 1, the corresponding region is disabled. The LSB corresponds to Region 0 and MSB to Region 15.

Region Disable Register 2

A 16–bit register used to disable the readout of specific regions. When a bit is set to 1, the corresponding region is disabled. The LSB corresponds to Region 16 and MSB to Region 31.

FROMU Configuration Register 1

Bits	Purpose
2:0	Pixel MEB Mask
3	Internal **STROBE** generation
4	Enable **BUSY** Monitoring
5	Test Pulse Mode
6	Enable Test **STROBE**
7	Not used
12:8	SM states (read only)
15:13	Not used

Table 3.5: FROMU Configuration Register 1 Register Field Description

- **Pixel MEB Mask** – 1: disable given event buffer (default 000 to enable all meb slices). Setting bit 0 masks Matrix Slice 1, bit 1 masks Slice 1 and bit 2 masks Slice 3. **Masking all slices is ignored and equivalent to enabling all.**
- **Internal Strobe Generation** – 0: disabled, 1: enable generation of a repetitive strobe pulse in continuous mode.
- **Enable Busy Monitoring** – 0: disabled, 1: FROMU will monitor external BUSY line, and reject triggers when BUSY is asserted (default).
- **Test Pulse Mode** – 0: digital pulse to pixels (default), 1: set analog pulse as a test pulse
- **SM states** – State machine bits

FROMU Configuration Register 2

Set the duration of the**STROBE** signal from 25ns to 1638.4us (step 25ns).

FROMU Pulsing Register 1

Set the delay from the test **PULSE** to the **STROBE** signal from 0 to 1638.4us (step 25ns).

FROMU Pulsing Register 2

Set the test **PULSE** duration from 0 to 1638.4us (step 25ns).

FROMU Status Register 1

Current value of the **STROBE** counter.

FROMU Status Register 2

Bits	Purpose
11:0	Bunch Counter
13:12	Event Counter
15:14	Not used

Table 3.6: FROMU Status Register 2 Field Description

- **Bunch Counter** – Internal FROMU counter to be synchronised to LHC Bunch Crossing Counter via a BCRST.
- **Event Counter** – 2 least significative bits of the internal event counter.

DAC settings for MLVDS I/O buffers

The **DCLK**, **MCLK** and **DCTRL** differential ports are implemented with two instances of the same pseudo-MLVDS transceiver block. The transceiver block has tunable currents for the receiver and for the driver circuits. The following two registers control the currents of the MLVDS circuits:

DAC settings for DCLK and MCLK I/O buffers

Bits	Purpose	Value at reset
3:0	DCLK Receiver current	hA
7:4	DCLK Driver current	hA
11:8	MCLK Receiver current	hA
15:12	Not used	

Table 3.7: CLK buffer DAC Settings Register Field Description

DAC settings for CMU I/O buffers

Bits	Purpose	Value at reset
3:0	DCTRL receiver current	hA
7:4	DCTRL driver current	hA
15:8	Not used	

Table 3.8: CMU Buffer DAC Settings Register Field Description

CMU and DMU configuration register

This register is used to configure the Control Management Unit (CMU) and Data Management Unit (DMU) modules.

Bits	Purpose
3:0	Previous Chip ID
4	XOff
5	Initial Token
6	Disable Manchester encoding
7	Enable Double Data Rate
15:8	Not used

Table 3.9: CMU and CMU Config Register Field Description

- **Previous Chip ID** – Value of the chip Index of the chip accessing the OB Module local bus just before the chip on which the register resides (default hF)
- **XOff** - 0: DMU Enabled (default), 1: DMU disabled, data sending is paused.
- **Initial Token** – Must be set to 1 to the chip that has the token by default (normally should be the MASTER chip of the module)
- **Disable Manchester Encoding** – 0: CMU Manchester Encoding enabled (default), 1: Encoding disabled
- **Enable Double Data Rate** – 0: Disable DDR on Local Bus, 1: Enable DDR on Local Bus (default)

CMU Errors Counter Register

Bits	Purpose
3:0	Deserializer error counter
7:4	Time-out error counter
11:8	Unknown OPCODE error counter

Table 3.10: CMU Errors Counter Register Field Description

The CMU has three 4 bit wide counters of control protocol error conditions. This is a read only register to retrieve the values of the counters and to detect control protocol violation errors. Under normal conditions these counters should remain at zero. These counters can be reset by a dedicated command written to the command register.

The deserializer errors are of two types. A *framing error* is induced by the incoming serial stream if the stop bit is not received at the expected cycle after the start bit. An *overrun error* is induced by a missing acknowledge of the retrieval of a deserialized character from the output port.

DTU Configuration Register

Bits	Purpose
1:0	PLL VCO Delay Stages control
2	PLL Bandwitdth control
3	PLL off signal
7:4	Serializer Phase
8	PLL Reset
11:9	Not used
12	Load Enable Status (Read Only)
15:13	Not used

Table 3.11: DTU Configuration Register Field Description

- **PLL VCO Delay Stages control** – these two bits control the number of delay stages used in the VCO. *b00*: VCO with 3 stages (slow case). *b01*: VCO with 4 stages (typical case). *b11*: VCO with 5 stages (fast case).
- **PLL bandwidth control** – *b0* selects a wide bandwith response, *b1* selects a narrow bandwidth response.
- **PLL off signal** – *b1* shuts down the PLL.
- **Serializer Phase** – control of the timing of the parallel load of data into the shift registers of the serializer.
- **PLL Reset** – Asynchronous reset of the PLL.
- **Load Enable Status** – read only monitor of the enable input of the DTU Serializer generated by the DTU logic.

DTU DACs Register

Bits	Purpose	Value at reset
3:0	PLL Charge Pump current setting	8
7:4	High Speed Line Driver current setting	8
11:8	Pre-emphasis driver current setting	0
15:12	Not used	

Table 3.12: DTU DACs Register Field Description

DTU PLL Lock Register 1

This read only register gives access to output signals and flags of PLL related logic.

Bits	Purpose
7:0	Lock Counter
8	Lock Flag
9	Lock Status
15:10	Not used

Table 3.13: DTU PLL Lock Register 1 Field Description

- **Lock Counter** – Internal counter incremented every time the PLL monitoring state machine enters the *PLL LOCKED* state.
- **Lock Flag** – Direct access to the unfiltered PLL Lock flag.
- **Lock Status** – Asserted while the PLL monitoring state machine is in the *PLL LOCKED* state. This signal is the result of a moving average of the PLL Lock Flag executed by the PLL monitoring state machine.

DTU PLL Lock Register 2

This register provides control of the behavior of the PLL monitoring state machine.

Bits	Purpose
7:0	Lock Wait Cycles
15:8	Unlock Wait Cycles

Table 3.14: DTU PLL Lock Register 2 Fields Description

- **Lock Wait Cycles** – The PLL monitoring state machine enters the *PLL LOCKED* state after sampling a continuous assertion of the PLL Lock flag for a number of clock cycles set with this register.
- **Unlock Wait Cycles** – The PLL monitoring state machine enters the *PLL UNLOCKED* state after sampling the PLL Lock flag continuosly deasserted for a number of clock cycles set with this register.

DTU Test Register 1

This register provides access to the built-in DTU test facilities.

Bits	Purpose
0	Test Enable
1	Internal Pattern Enable
2	Prbs Enable
3	Bypass 8b10b
5:4	BDIN8b10b0
7:6	BDIN8b10b1
9:8	BDIN8b10b2
10	K0
11	K1
12	K2
13	Force Load Enable High
14	Force Load Enable Low
15	Not used

Table 3.15: DTU Test Register 1 Field Description

- **Test Enable** – Activates the DTU test mode. When this bit is set, the parallel data bus to the encoder and then to the DTU is driven by the test logic and effectively disconnected from the chip Data Management Unit.
- **Internal Pattern Enable** – Selects between constant test patterns or test patterns generated by an internal pattern generator.
- **Prbs Enable** – Selects the type of pattern of the internal pattern generator; *b0* bynary up-counter, *b1* pseudo-random bit pattern.
- **Bypass 8b10b** – Forces bypassing the 8b10b encoding stage. The parallel data (either from the DMU either from the test logic) are applied directly to the DTU Serializer parallel inputs when this signal is asserted. Note: this is effective independently from the enabling of the test mode.
- **BDIN8b10b0** – Padding bits for the DIN0 Test Code, used in configurations when the 8b10b encoder is bypassed and the internal pattern generator is not used.
- **BDIN8b10b1** – Padding bits for the DIN1 Test Code, used in configurations when the 8b10b encoder is bypassed and the internal pattern generator is not used.
- **BDIN8b10b2** – Padding bits for the DIN2 Test Code, used in configurations when the 8b10b encoder is bypassed and the internal pattern generator is not used.
- **K0** – Direct drive of the K-code selection bit of lane 0 of the 8b10b encoder. Useful in test configurations with the encoder enabled and test patterns applied to the encoder inputs.
- **K1** – Direct drive of the K-code selection bit of lane 1 of the 8b10b encoder. Useful in test configurations with the encoder enabled and test patterns applied to the encoder inputs.
- **K2** – Direct drive of the K-code selection bit of lane 2 of the 8b10b encoder. Useful in test configurations with the encoder enabled and test patterns applied to the encoder inputs.
- **Force Load Enable High** – Forces to logic high the Load Enable input of the Serializer. This overrides the normal behavior consisting of having the Load Enable equal to the Locked Status of the PLL monitoring state machine. This control is always effective, independently of the enabling of the DTU test logic (bit 0).
- **Force Load Enable Low** – Forces to logic low (resetting level) the Load Enable input of the Serializer. This overrides the normal behavior consisting of having the Load Enable

equal to the Locked Status of the PLL monitoring state machine. This control is always effective, independently of the enabling of the DTU test logic (bit 0) and has priority over the Force Load Enable High control bit. When the DTU Serializer receives a low level on the Load Enable input it remains in a reset condition and its two shift registers keep constant values. When this bit is set the high speed output consists of a replica of the PLL output clock propagated through the Serializer and the DTU Driver input multiplexer.

DTU Test Register 2

Bits	Purpose
7:0	DIN0 Test Code
15:8	DIN1 Test Code

Table 3.16: DTU Test Register 2 Field Description

- **DIN0** – Constant programmable test code applied to the lane 0 (bits 7:0) of the encoder when Test Mode is selected and the internal pattern generator is disabled.
- **DIN1** – Constant programmable test code applied to the lane 1 (bits 15:8) of the encoder when Test Mode is selected and the internal pattern generator is disabled.

DTU Test Register 3

Bits	Purpose
7:0	DIN2 Test Code
15:8	Not used

Table 3.17: DTU Test Register 3 Field Description

- **DIN2** – Constant programmable test code applied to the lane 2 (bits 23:16) of the encoder when Test Mode is selected and the internal pattern generator is disabled.

BUSY Minimum Width

Bits 4:0 set the minimum length of the **BUSY** signal, in step of 25ns.

Fuses Write register

This 24 bit register spans two addresses since it is 24 bits wide. It is used to set the input code to the Fuses block during the Fuses programming. This is the value that is to be irreversibly stored in the fuses with the fuses write operation.

Fuses Read register

This read only 24 bit register spans two addresses since it is 24 bits wide. It is used to read the output of the Fuses block. After programming, this is the value that is irreversibly stored in the fuses.

Temperature sensor register

This is a single bit read only register to retrieve the value of the output of an analog comparator. The comparator inputs are a temperature dependent voltage and the voltage output of the **VAUX** DAC. In order to measure the die temperature, a scan of the VAUX DAC is to be made through the control interface while retrieving the value of the temperature bit. The VAUX value at which the bit toggles is an indirect measurement of the temperature.

Notice: during the scan of the DAC searching for the toggling point, it is expected that glitches on the Front-End analog bias DACs are generated. It is recommended to avoid executing a temperature finding scan during readout sequences.

RRU Memory random access

The RRU FIFO can be accessed as RAM when the chip is in Configuration Mode. To correctly write a memory location, LSBs bits 15:0 must be first written (Note that *SUB_ADDR* is not considered when writing), and subsequently the MSBs bits 23:16

RRU MEB LSBs

On a write operation, the 16 bit data is stored in a temporary register which will be written to the RAM location when the MSBs are written. A read operation would retreive bit 15:0 of the selected RAM memory location.

RRU MEB MSBs

Bits	Purpose
7:0	RRU MEB MSBs
15:8	Not used

Table 3.18: RRU MEB MSBs Register Field Description

- **RRU MEB MSBs** – 8 most significant bits of the memory data

Double Column Disable Registers

Set of 32 registers used to disable the readout of a double column in a specific region. When a bit is set the readout of the corresponding double column (Priority Encoder) is disabled.

DMU and TRU State

Bits	Purpose
2:0	TRU SM State
5:3	DMU SM State
6	Busy Mismatch Error
7	Busy FIFO Full Error
15:8	Not used

Table 3.19: DMU and TRU State Register Field Description

- **TRU SM State** – TRU State Machine bits
- **DMU SM State** – DMU State Machine bits
- **Busy Mismatch Error** – set if the DMU logic sees a BUSY ON/OFF opcode in the Local Bus which does not match the content of his internal FIFO. Reset on RORST command
- **Busy FIFO Full Error** – set if the DMU Busy FIFO becomes full. Reset on RORST command

Pixel configuration registers

In each pixel there are 2 writable registers: the Mask register and the Pulse Enable register (refer to the section on the digital circuits in the pixels). These registers can be addressed and written by using Pixel CFG Register 1, Pixel CFG Register 2. The transmission to the matrix of the row and column selection signal is gated by bit 0 of the Pixel CFG Register 3 (MatrixLatchEN). This is intended to be set to 1 after the Pixel CFG Register 1 and Pixel CFG Register 2 have been appropriately written, enabling the propagation of the row and column signals to the matrix as long as the bit remains asserted.

Pixel CFG Register 1

Bits	Purpose
8:0	Pixel row selector
9	Sets all rows
10	PIXCNFG_REGSEL
11	PIXCNFG_DATA
15:12	Not used

Table 3.20: Pixel CFG Register 1 Field Description

- **Pixel Row Selector** – Value of a single row to be selected
- **Set All Rows** – Set to 1 to select all rows
- **PIXCNFG_REGSEL** – Selection of the in-pixel register to be addressed: 0: for the Pulse Enable register, 1: for the Mask register
- **PIXCNFG_DATA** – Bit to be written in the target register

Pixel CFG Register 2

Bits	Purpose
9:0	Pixel column selector
10	Sets all columns
15:11	Not used

Table 3.21: Pixel CFG Register 2 Field Description

- **Pixel Column Selector** – Value of a single column to be selected
- **Set All Columns** – Set to 1 to select all column

Pixel CFG Register 3

Setting the bit 0 to 1 will enable the propagation of the row and column signals to the matrix. When bit is set, a subsequent write to this register will reset the bit and disable the row and column selection, regardless of the value being written. Therefore, the user should be aware that if that register is written to twice in a row will result in a final value of '0' regardless of the last attempted write value.

Analog monitor and override settings register

This register is used to control the monitoring and overriding of the internal DACs using the DACMONV and DACMONI pins.

Bits	Purpose
3:0	Voltage DAC selection
6:4	Current DAC selection
7	SWCNTL_DACMONI
8	SWCNTL_DACMONV
10:9	IRef Buffer current
15:11	Not Used

Table 3.22: Analog Monitor and Override Register Field Description

- **Voltage DAC Selection** – Voltage selected to DACMONV pin as per values in Table 3.23
- **Current DAC Selection** – Current selected to DACMONI pin as per values in Table 3.24
- **SWCNTL_DACMONI** – Configures the DAC block to enable the overriding of the selected voltage DAC. 0: for monitoring, 1: for overriding
- **SWCNTL_DACMONV** – Configures the DAC block to enable the overriding of the selected current DAC. 0: for monitoring, 1: for overriding
- **IREF Buffer Current** – IRef buffer current as per values in Table 3.25

Value	Selected voltage
0	VCASN
1	VCASP
2	VPULSEH
3	VPULSEL
4	VRESETP
5	VRESETD
6	VCASN2
7	VCLIP
8	VTEMP

Table 3.23: DACMONV Voltage Selection Field Description

Value	Selected current
0	IRESET
1	IAUX2
2	IBIAS
3	IDB
4	IREF
5	ITHR
6	IREFBuffer

Table 3.24: DACMONI Current Selection Field Description

Value	Current
0	0,25uA
1	0,74uA
2	1,00uA (default)
3	1,25uA

Table 3.25: IREF Buffer Current Settings Field Description

DACs setting registers

For each of the DACs, there is an 8-bit setting field. The default values for each of those are indicated in Table 3.2.

Buffer Bypass Register

A value of 1 in the corresponding bit will bypass the buffer cell for that particular voltage or current.

Bit	Purpose
0	VCASN
1	VCASN2
2	VCASP
3	VCLIP
4	IRESET
5	IBIAS
6	ITHR
7	IDB
15:8	Not Used

Table 3.26: Buffer Bypass Field Description

Reagion Readout Status Register

Bit	Purpose
0	Pixel Status
1	Memory Status
2	All Columns Disabled
4:3	Readout SM state
6:5	FIFO Self Test SM state
15:7	Not Used

Table 3.27: Region Readout Status Register Field Description

- **Pixel Status** – Set to 1 when a faulty pixel is detected during readout
- **Memory Status** – Set to 1 when a faulty memory location is detected during Memory Self Test
- **All Columns Disabled** – Set to 1 when all columns in the region are disabled
- **Readout SM State** - State Machine bits
- **FIFO Self Test SM State** - State Machine bits

3.3 Triggering and Framing

Pixels in the pALPIDE-3 Matrix have 3 in pixel hit data storage elements. These implement a three-stages memory buffer for hit data and enable the storage of a up to 2 additional hit frames while the readout of a given frame to the periphery is progressing.

The recording of the pixel discriminator outputs in the storage registers is controlled by three global signals (STROBE_B[2:0]) distributed from the periphery to all pixels. The outputs of the state registers in the pixels can be selectively connected to the inputs of the Priority Encoders. This is governed by three global signals (MEMSEL_B[2:0]) and only one bank of registers can be selected at any time for readout. The STROBE_B and MEMSEL_B signals act as write and read pointers to the matrix event buffers. The orderly generation of the STROBE_B signals in response to trigger commands and the updating of the MEMSEL_B signals on completion of frame readout is the main functionality of the FROMU module.

The assertion of the STROBE ad MEMSEL signals to the matrix buffers is sequenced such that a circular buffer is effectively implemented. By design, only one of the three STROBE signals or one of the three MEMSEL signals can be asserted at any time.

3.3.1 Operation

Readout Modes

There are two readout modes (see Chip Mode Selector Field, Section 3.2.2) - *Triggered* and *Continuous*.

In **triggered** mode, the assertion of the STROBE to the available matrix buffer and the scheduling of the frame readout are initiated by TRIGGER commands. The chip asserts the BUSY output once all matrix storage buffers are occupied with hit data. The BUSY is deasserted on completion of the matrix buffer readout to the periphery memories. In case a trigger command is received while BUSY is asserted, the FROMU will not generate the STROBE to the matrix, but an empty event packet with the BUSY VIOLATION flag set in its trailer is generated and put in the read out pipeline. The duration of the internal STROBE signal is programmable. Trigger commands received during the interval of assertion of the internal STROBE are ignored. The user shall ensure that the time between consecutive trigger commands (time between start bits of the control transactions) is longer than the programmed STROBE duration to prevent missed trigger commands.

In **continuous** mode the FROMU handles the signals to the matrix buffers in a different manner. The purpose of this mode is to support strobing and reading out frames at a constant (but programmable) rate, integrating all hit events occurring during a framing interval. The duration of the STROBE pulse constrains the minimum repetition period of the readout. In *continuous mode*, if there is only one available matrix event buffer, an incoming trigger forces a reset (*flush*) of the buffer that is currently being read out. This is achieved by asserting FLUSH global signals to the selected matrix memory slice and it forces a completion of the frame readout. One memory location in the pixels is freed for the subsequent trigger, at the price of loss of hit data. The activation of this mechanism and the occurrence of data loss is reported by a flag in the CHIP TRAILER (refer to 3.4.1).

The continuous mode can be used both with external triggers and with an internal sequencer. With external triggers, the operation resembles the one in trigger mode, but the handling of the BUSY assertion and of the FLUSH mechanism are different as described above. It is left to the user to provide periodical trigger commands and to set the STROBE duration accordingly. The recommended configuration consists of providing **triggers with a periodicity equal to the STROBE duration plus 1 additional clock period**. The internal generation of triggers can be enabled by bit 3 of *FROMU Configuration Register 1*. With this feature enabled, on completion of a STROBE assertion interval, the internal sequencer sends a new internal trigger to the FROMU (after a gap of one clock cycle). However the internal sequencer must be started with a single initial trigger command to the chip. This is to enable the synchronization of framing intervals across multiple chips for applications with multiple chips.

STROBE Window Duration

The duration of the STROBE signals applied to the pixels can be programmed using FROMU Configuration Register 2 (ref. to Table 3.2). A minimum duration of 2 CLK cycles (50 ns) is recommended for this setting.

Memory Bank Masking

The FROMU provides the functionality to mask any of the Matrix memory slices to prevent their usage for hit data storage. This setting affects the order of assertions of STROBE and MEMSEL signals. The remaining active memory buffers are still accessed in a rotating fashion. This function is accessed by the Pixel MEB Mask Field of FROMU Configuration Register 1 (see Table 3.2).

BUSY Monitoring and Assertion

Regardless of the chip function (IB or OB), a device will itself assert the BUSY, be it the shared BUSY line on an OB or via a direct transmission of the BUSY_ON word in the case of IB, for one of a few reasons:

- There are no more available Matrix Memory Slices
- The Frame Start Fifo is full

If a device is BUSY and in TRIGGERED mode, it would reply with a CHIP HEADER and a CHIP TRAILER with the corresponding flags asserted and NOT with a CHIP EMPTY FRAME. If a device is in CONTINUOUS mode, there is only one empty matrix slice and a STROBE window is generated, the frame presently being read out will be interrupted by FLUSH-ing that slice and the corresponding flags in the CHIP TRAILER set accordingly.

The BUSY behaviour is slightly different for an OB. If the Enable Busy Monitoring Field of the FROMU Config Register 1 is set, which is the recommended setting, a trigger received by a non-busy device will be ignored if the shared BUSY line is still asserted.

The TRIGGERED mode has been verified more extensively and it is recommended that the chip is utilised with that in mind.

3.3.2 Triggering and Waveform Diagrams

The propagation delay between the assertion of the first bit in a TRIGGER command and the assertion of the STROBE window can be seen in Figure 3.6. Note that shown is the behaviour in an OB with *PAD_MCLK_P* being the main clock signal received by the master chip and *clk* being the clock signal inside the digital_top abstraction following the delays in the differential clock receiver.

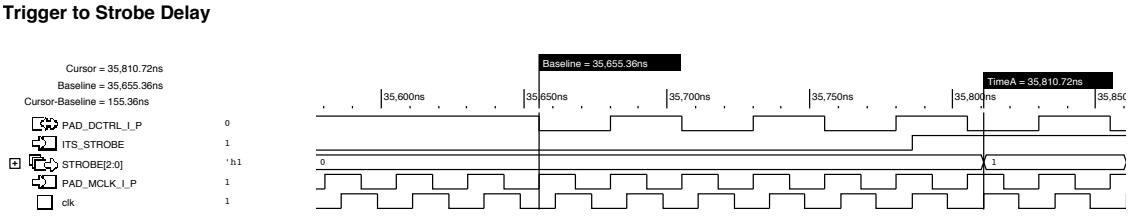


Figure 3.6: TRIGGER to STROBE delay assertion on an OB module chip

3.4 Data readout

The pALPIDE-3 has two means of data transmission - a serial transmission port (PAD_HSDATA_O_P / PAD_HSDATA_O_N) and a parallel data port (PAD_DATA[7:0]). Both of these utilise the same

Data Word	Lenght (Bits)	Value (binary)
IDLE	8	1111_1111
COMMA	8	1011_1100
CHIP HEADER	16	1010<chip_id[3:0]><frame_start_data[7:0]>
CHIP TRAILER	16	1011<readout_flags[3:0]><reserved[7:0]>
CHIP EMPTY FRAME	24	1110<chip_id[3:0]><frame_start_data[7:0] ><reserved[7:0]>
REGION HEADER	8	110<region_id[4:0]>
DATA SHORT	16	01<data_field[13:0]>
DATA LONG	24	00<data_field[13:0]>_0_ <hit_map[6:0]>
BUSY ON	8	1111_0001
BUSY OFF	8	1111_0000

Table 3.28: Data Format adopted in pALPIDE-3.

byte-oriented data format. The two ports are intended to implement the data interfaces on the ITS Modules as described in the Appendices B and C.

The serial port implements a clock synchronous transmission based on the 600 MHz clock produced by the internal PLL. Data is 8b/10b encoded with the LSB launched first. Further, a bit is sent on every clock edge. It is important for stream interpretation purposes to note that data is loaded for transmission 30 bits at a time - 3 characters of 10 bit encoded bytes.

In the case of an Inner Barrel device, the 600 MHz clock signal is used directly to produce a DDR stream at 1.2 Gbps. Outer Barrel devices still use the same clock but send every bit 3 times thus producing an effective 400 Mbps DDR serial stream. The data protocol utilised is independent of the chip type and is described in Section 3.4.1.

The parallel data port, also referred to as the local bus, is main clock synchronous (40 MHz) and has two modes of operation. In the default mode, the full byte is transmitted over pads DATA[3:0] using Double Data Rate transmission. Each byte is sent in two consecutive nibbles with the most significant nibble (bits 7–4) first. Nibbles are launched on both rising and falling edges of the chip clock.

The chip can be optionally configured to utilize Single Data Rate transmission on the full bus DATA[7:0], with a byte being launched at every clock rising edge (see CMU and DMU config register description) .

The uppermost DATA[7:4] bits are always clocked on a positive clock edge i.e. they always operate in Single Data Rate mode.

There is no data encoding on the local bus and the protocol described in Section 3.4.1 is used directly. A sample local bus stream utilising DDR transmission and the corresponding serial transmission can be seen in Figure 3.7.

3.4.1 Data format

Table 3.28 lists the valid Data Words. The valid words are identified by predefined prefix bit strings.

COMMA Control symbol for the 8b/10b encoding to be transmitted only on the serial port. Standard K28.5 words with running disparity are utilised. Thus, the encoded COMMA value of 8'hBC is either 10'b001111_1010 or 10'b110000_0101 depending on the running disparity. The

COMMA transmission can be used for clock recovery and synchronisation to the data stream. The COMMA word can be observed in the following scenarios:

- When there is no readout in progress and the chip is completely idle.
- When there is a readout in progress but the chip hasn't had enough time to process data and/or pack it. This would typically happen:
  1. following a CHIP HEADER on an IB before the readout and processing has been completed.
  2. in the first frame payload on an OB before the chip has had a chance to pack data for maximum transmission efficiency.

IDLE Also referred to as NOP for historical reasons, the IDLE codeword can be observed in two different scenarios :

- In an OB, on the local bus when it is compeletly undriven i.e. there is no readout in progress
- In an OB, IDLEs are stripped from the data stream except for turnover byte when the virtual token is passed over (see Section 3.4.3)
- In an IB, when a word as defined in Table 3.28 is less than 3 bytes, that word is padded with IDLE words to bring the total to 3. For example, that means 2 × IDLE word padding for a REGION HEADER and a single IDLE for a DATA SHORT.

CHIP HEADER Symbol transmitted at the beginning of each data frame. Bits CHIPID[3:0], which are sent as the least significant nibble of the first CHIP HEADER byte, identify the geographical location of a given chip on a ITS module. Additionally, the second byte of the CHIP HEADER word contains bits [7:0] of the 9 bit Frame Start Data information. That data field has the following composition :

frame_start_data[7:0] = <BUNCH_COUNTER_FOR_FRAME[8:3]><STROBE_COUNTER[1:0]>

where BUNCH_COUNTER_FOR_FRAME is an internal 40 MHz running counter meant to be synchronised to the LHC Bunch Crossing Counter via the BCRST instruction (Table 3.1.3) and STROBE_COUNTER is an internal counter incremented every time the internal a STROBE pulse is propagated to the Matrix.

CHIP TRAILER Byte transmitted at the end of each data frame.

Data composition of the variable field <readout_flags[3:0]> can be structered in one of two ways:

- In the case of a busy signal violation (TRIGGER sent while BUSY is still asserted and we are operating in TRIGGERED mode):

$$< readout\_flags[3:0] >= \{< is\_busy\_violation >< 3'b000 >\}$$

- When there is no busy violation or we are operating in CONTINUOUS mode :

$$< readout\_flags[3:0] >= \{< 1'b0 >< FLUSHED\_INCOMPLETE > < FATAL >< BUSY\_TRANSITION >\}$$

The flags outlined above are generated as follows:

- IS_BUSY_VIOLATION – when the BUSY has been asserted and a new TRIGGER is received whilst in TRIGGERED mode.
- FATAL – when the Frame Start Fifo is full (depth 16) and another a new TRIGGER is sent. Only observed in CONTINUOUS Mode.
- FLUSHED_INCOMPLETE – in Continuous Readout Mode only, when a MEB slice was flushed in order to ensure that the MATRIX always has a free memory bank for storing new events. Only observed in CONTINUOUS Mode.
- BUSY_TRANSITION – when the BUSY has been set during the readout of the frame in question. Only observed in CONTINUOUS Mode.

Finally, the reserved[7:0] field was incorporated in the data format in order to simplify the token exchange logic on the OB. This field is set to be an IDLE byte.

CHIP EMPTY FRAME Word transmitted at the beginning of an empty data frame. This conserves a byte of bandwidth as opposed to sending a CHIP HEADER followed by a CHIP TRAILER. Bits CHIPID[3:0], which are sent as the least significant nibble of the first CHIP EMPTY FRAME byte, identify the geographical location of a given chip on a ITS module. Additionally, the second byte of the CHIP HEADER word contains bits [7:0] of the 9 bit Frame Start Data information (see CHIP HEADER for a detailed description of data encapsulation). Finally, the reserved[7:0] field was incorporated in the data format in order to simplify the token exchange logic on the OB. This field is set to be an IDLE byte.

REGION HEADER Chip data frames are made of 32 region data frames. Each region data frame is initiated with this word. The variable part *region_id[4:0]* is the index of the region. Region data frames are sent sequentially in ascending order. The region header is only sent for regions with data content.

DATA SHORT Pixel hit data information container. This word is used to transmit pixel hit position information. Is is used for single pixel hits when clustering is enabled or for all pixel hits when clustering is disabled. The variable field in the DATA SHORT word has the following structure:

data_field[13:0] = <encoder_id[3:0]><addr[9:0]>

where *encoder_id* is the index of the priority encoder inside a region and *addr* is the pixel hit index generated by the priority encoder.

DATA LONG Pixel hit data information container. This word is used to transmit cluster information. It is generated only when clustering is enabled. The variable field in the DATA LONG word has the following structure:

¡ data_field[13:0]><hit_map[7:0]]>= <encoder_id[3:0]><addr[9:0]><hit_map[6:0]>

where *encoder_id* is the index of the priority encoder inside a region, *addr* is the pixel hit index generated by the priority encoder for the first hit in a cluster and *hit_map[6:0]* contains the cluster

shape information in the form of a bit map. A bit in the hit_map is set for any active pixel among the 7 immediately after (based on PE pixel addreses) the one indicated by the addr[9:0] field. The LSB of hit map corresponds to first subsequent pixel and bit 6 to the 7th. Therefore, a DATA LONG can transmit a maximum of 8 pixels at once.

BUSY ON Code word transmitted on assertion of the BUSY status. Transmitted on both the serial link and on the parallel bus. See Section 3.4.3 for further notes on the BUSY signaling mechanism.

BUSY OFF Code word transmitted on the serial port on de-assertion of the BUSY status. Transmitted on both the serial link and on the parallel bus.

3.4.2 Data format rules

- Data words are transmitted byte by byte, most significant byte first.
- IDLE, BUSY_ON and BUSY_OFF words can be arbitrarily inserted betweeen other code words.
- Words that are 16 or 24 bits (DATA SHORT, DATA LONG, CHIP HEADER, CHIP EMPTY FRAME) cannot be split by a IDLE or a BUSY.
- The BUSY words are transmitted as soon as possible without violating data integrity.

3.4.3 Local Data Bus Sharing Mechanism

The OB Slave chips send their data to the OB Master using a shared Local Data Bus implemented using the PAD_DATA parallel port. Only one chip at a time gets the right to write to the Local Bus. The chip with the token is allowed to enable the drivers onto the DATA ports. The DATA I/Os are equipped with internal pull-ups and the inactive state of the Local Bus is **xFF** (IDLE code word). This is described in further detail in Appendix C.

The OB Module chip continously sample the bus and write to it in turn. Time division multiplexing of the write access to the bus is governed by a *virtual token* exchange mechanism. The token is effectively constituted by the CHIP TRAILER data word of a Chip Data Frame and by the CHIP EMPTY FRAME in case of an empty frame. The chips monitor the Local Bus waiting for the previous chip in the sequence to complete the transmission of its own data frame. Once a chip, be it Master or Slave, obtains the right to write onto the bus, it transmits one complete Chip Data Frame and releases the bus.

Following a reset, the token is assigned to the chip that has the initial_token field set to 1 (see CMU and DMU Config Register). It is the user's responsibility to ensure that only one chip in a module has this bit set to 1 to ensure that the local bus is not driven by two devices.

The token passing order is established through the Previous Chip ID field (see CMU and DMU Config Register) of each chip. It is the user's responsibility that the full loop integrity is ensured i.e. that the chip with the initial_token field set to 1 has its Previous Chip ID pointing to the last device in the sequence.

It is possible to bypass selected chips (both Master and Slaves) in the readout sequence. Should the Master device be bypassed, it continues to monitor the local bus and transmit data via the serial link.

Should there be no pending frames, the bus is left undriven. In this case the bus is maintained to the idle state (IDLE code) by the pull-ups.

3.4.4 Sample Data Streams

Outlined in Figure 3.7 are two sample data streams that would be observed on the Serial and Local Bus respectively for an identical frame. The Master samples the local bus irrespective of which device is driving it and transmits the data on the serial link.

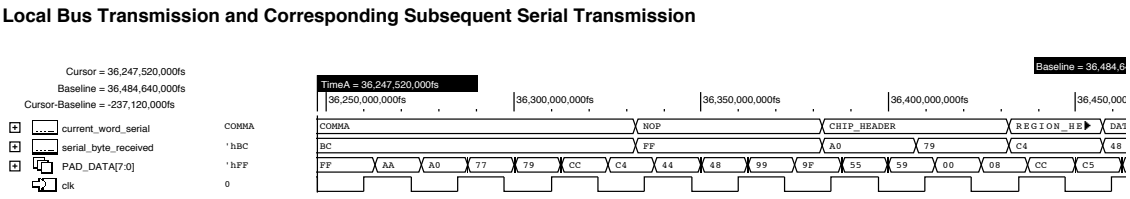


Figure 3.7: A Sample Data Stream on the Local Bus in DDR Mode and the Corresponding Transmission on the Serial Bus

3.4.5 Busy Signaling Mechanism

The OB Slave chips and the OB Master chips share a wire connected to their BUSY pins. This realizes a wired-or signalling of the busy condition of the chips.

The chip that has the virtual token (see Local Data Bus Sharing Mechanism) transmits the BUSY flag unless it would break a data transmission rule (see Data Format Rules). If the token is passed before the BUSY has been sent, the new chip assumes the responsibility of sending it.

Since the BUSY words are part of the regular data stream on the local bus, they are transmitted on the serial link with minimal delay.

The BUSY is asserted for a minimum duration as indicated by the BUSY Minimum Width Register (see Busy Minimum Width Register Description). By the default, this is set to 8 CLK cycles.

3.5 Configuring pixels. Masking and pulsing.

The in-pixel logic in the pALPIDE-3 includes the functionality to temporarily force a pixel's output to a predefined value via an external command on the control interface (PULSE). This functionality is closely interleaved with the latching logic.

Every pixel has a MASK_EN and PULSE_EN latch within it. The change in pixel behaviour depending on the value of those latches is described in Section INSERT REF TO THANUs section. This section describes the setting of those values from the control interface and the recommended procedure to do so.

In order to configure a pixel one must first set the values of the **Pixel CFG Register 1** and **Pixel CFG Register 2**.

- The Pixel CFG Register 1 acts as a row selector. The spare bits within the register are also used to select whether to write to PULSE_EN or MASK_EN and what value to write to the selected field. Please see Table 3.20 for further details.

- The Pixel CFG Register 2 acts as a column selector. Please see Table 3.21 for further details.

The settings are then propagated by writing 1'b1 to **Pixel CFG Register 3**. Note that the Pixel CFG Register 3 is self-resetting on the next register write. Therefore, it is recommended that '0' is written to it immediately after writing a '1' to ensure consistency.

The procedure for writing to specific pixel selections are outlined below:

- Writing to a single pixel – The user must ensure that the *Set All Rows* and *Set All Columns* fields of the Pixel CFG Register 1 and 2 are set to '0'. The single pixel is then selected by setting the appropriate column and row number to the *Pixel column selector* and the *Pixel Row selector* fields. Further, the user selects to write to PULSE_EN by setting the *PIXCNFG_REGSEL* bit to '1' and to MASK_EN by setting it to '0'. The data it writes to the selected latch is given by the *PIXCNFG_DATA* bit. Finally, the user must write 1'b1 to Pixel CFG Register 3 to enable the propagation of the settings to the Matrix. It is recommended that this is immediately followed by writing 1'b0 to the same register.
- Writing to a column – If one wants to write a full column, there is a slight tweak in the procedure. The *Set All Rows* bit is set to '1' while *Set All Columns* is maintained at '0' and the column in question selected via the *Pixel column selector*. The *Pixel Row selector* field is then irrelevant. The remainder of the configuration procedure is unchanged.
- Writing to a row – Similarly, if one writes to a row, all columns must be selected along with the appropriate row only. The remainder of the configuration procedure is unchanged.
- Writing to all pixels – Selecting all pixels, mostly done for initialisation purposes, is done by setting both *Set All Rows* and *Set All Columns* bits to '1'. The column and row selectors are then irrelevant and one can set either all PULSE_EN or all MASK_EN latches in the Matrix.

It is recommended that all PULSE_EN and MASK_EN latches are intialised to '0' via writes to all pixels in the chip's configuration.

Pulsing the configured pixels is discussed in Section 3.6.

3.6 Analog test pulse injection and pixel digital testing.

The pALPIDE-3 chip has two ways of forcing the output of the pixel to be high - analog and digital pulsing.

- The positive edge of an analog pulse, APULSE, injects charge to simiulate a particle hitting the pixel. Therefore, there is a delay matching the shaping time of the front end discriminator (see Section 4.1.1) before the pixel output changes to high.
- The digital pulse, DPULSE, allows for a way of circumventing the analog front end discriminator output and still latching a '1' into the memory of the pixel.

Note that both options require that STROBE_B for the given element is asserted in order to latch the output to be stored. The pixel behaviour is described in detail in Section 4.1.1. This section describes the means of generating the APULSE and DPULSE signals for testing purposes and any additional associated features.

3.6.1 Test Pulse Selection, Timing and Generation

Both DPULSE and APULSE are generated by the FROMU following the reception of a PULSE command (see Table 3.1.3 and Table 3.2.2). The selection between the two is made via the setting

of the *Test Pulse Mode* bit within the **FROMU Configuration Register 1** (see Table 3.5) If it is set to '0', a PULSE command will generate DPULSE. Altenatively, if it is set to '1', an APULSE will be generated.

The duration of the APULSE/DPULSE is set by the value written to the **FROMU Pulsing Register 2**. This 16-bit register and a step of 25 ns give a maximum duration of 1638.4 μs.

The propagation delay between the assertion of the first bit of the PULSE command on the control interface (PAD_DCTRL_I_P) and the assertion of the DPULSE as seen by the Matrix (DPULSE) can be seen in Figure 3.8. Note that the delay is identical in the case of an APULSE. This delay works out as 19 clock cycles, 10 of which make up the length of the control command opcode.

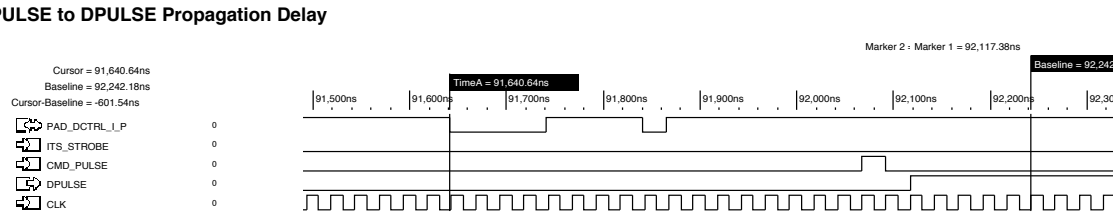


Figure 3.8: Delay between the assertion of the first bit of the PULSE command and the assertion of the DPULSE as seen by the Matrix. Post-PULSE automated STROBE window assertion along with the relevant programmable input delay.

3.6.2 Extra Non-Essential Features

In order to facilitate testing a number of non-essential features have been added. Firstly, it is possible to set the chip up to generate an automatic STROBE window after a PULSE (be it a DPULSE or an APULSE). This functionality is enabled via the setting of the *Enable Test STROBE* bit in the **FROMU CFG Register 2**. The duration of that STROBE assertion is as set by the **FROMU CFG Register 2**. The delay between the positive edge on the test pulse in question and the automated STROBE assertion is set via the **FROMU Pulsing Register 1**. This functionality can also be observed in Figure 3.8.

3.7 Chip initialization

This section outlines sample procedures to initialise the chip and prepare it for data taking. It is assumed that the control interface(s) are operational and well-configured. It is recommended that an initial **global reset** is applied to the chip in order to load all configuration registers with recommended default values.

3.7.1 Configuration and start-up of the Data Transmission Unit

The following procedure configures and starts up the high speed data transmission port. This is to be executed for Inner Barrel Chips or Outer Barrel Master chips in the ITS Upgrade application.

Writes to **DTU Configuration Register** and **DTU DACs Register**:

1. Set the PLL VCO stages and bandwidth configuration fields to desired values. Nominal design value are 4 stages and narrow bandwidth and should provide adequate behavior. However tuning of these settings might be needed depending on the incoming clock jitter and operating conditions.

2. Set the *PLL charge pump current* control to valid value. The nominal design value of 4'b1000 is intended to provide adequate behavior.
3. Set the *Line Driver current* and *Pre-emphasis Driver* current controls to values optimized for the line characteristics.
4. Clear *PLL off signal* bit to **start the PLL up**.
5. Force a **reset of the PLL**. This is done by **first setting and then clearing the PLL reset bit** with two subsequent transactions, leaving all the other bits of the DTU Configuration Register unchanged.

3.7.2 Configuration of in-pixel logic

Even if the user does not intend to use the Test Pulse functionality, it is recommended that the PULSE_EN and MASK_EN latches in every pixel are initialised. This is done via the following procedure: In order to initialise MASK_EN to '0' :

1. Write to **Pixel CFG Register 1**
   - *Pixel Row Selector* field is redundant - can be left all '0'.
   - Set *Set All Rows* field to '1'.
   - Set *PIXCNFG_REGSEL* field to '1' to select MASK_EN.
   - Set *PIXCNFG_DATA* to '0'.
2. Write to **Pixel CFG Register 2**
   - *Pixel Column Selector* field is redundant - can be left all '0'.
   - Set *Set All Columns* field to '1'.
3. Write to **Pixel CFG Register 3** the value 1'b1.
4. Write to **Pixel CFG Register 3** the value 1'b0.

In order to initialise all PULSE_EN latches to '0' the procedure outlined above is repeated with the *PIXCNFG_REGSEL* bit flipped to '0'.

3.7.3 Setting up of readout

Setting CMU and DMU Configuration Register in the Outer Barrel scenario

This register should be written to individually for every register in an OB.

- Set the *Previous Chip ID* field as required. Every chip monitors the parallel bus. Upon detecting in a CHIP HEADER the ID value programmed, the chip waits for the previous one to transmit the CHIP TRAILER word and thus yield the token.
- Bit 4 is unused.
- Set the *Initial Token* as required to specify the chip in question is the first in the readout chain. Care should be taken to ensure that only one chip in an module has this bit set to '1'.

Setting CMU and DMU Configuration Register in the Inner Barrel scenario

- The *Previous Chip ID* field is redundant - can be set to the default value of 4'b1111. Note that is a sanity check as 4'b1111 is not a legal CHIP ID.
- Bit 4 is unused.
- The *Initial Token* field is redundant - can be set to '0'.

Setting FROMU Configuration Registers and enabling readout mode

Items outlined below apply to both IB and OB configuration. It is recommended that a MULTICAST to target all chips in a module is used to ensure consistency.

1. Write to **FROMU Configuration Register 1**
   - Set *Pixel MEB Mask* field as required. Mask LSB to mask Matrix Memory Slice 0.
   - Set *Internal STROBE generation* field if repetitive auto-generate STROBEs in CONTINUOUS mode is a desired. An initial TRIGGER will then be required to start the strobing, but following that no further TRIGGERS should be sent if this feature is utilised.
   - RECOMMENDED : Set *Enable BUSY Monitoring* to '1'.
   - Set *Test Pulse Mode* field as required - '0' for DPULSE and '1' for APULSE.
   - Set *Enable Test STROBE* field as required - '1' to auto-generate STROBE windows following a PULSE. Note that if this feature is to be used the user must also set the **FROMU Pulsing Register 1** and **FROMU Pulsing Register 2**. Further, if the feature is to be used, once a PULSE is sent, any TRIGGERs sent while the PULSE is still active will be ignored. This duration will depend on the **FROMU Configuration Register 2**.
   - Leave remaining bits as '0' - they are either Not used or read-only.
2. Write to **FROMU Configuration Register 2**
   - Set STROBE duration as required (25 ns step).
3. If PULSE is to be used the user should also program the **FROMU Pulsing Register 1** and **FROMU Pulsing Register 2**.
4. Write to **Periphery Control Register**. This should be the last register write before TRIGGER/PULSE commands start being sent as it would put the chip in a readout mode:
   - Set *Chip Mode selector* field as required - 2'b01 for TRIGGERED and 2'b10 for CONTINUOUS.
   - Set *Clustering enable* field as required - '1' is the recommended value.
   - Set *Start Memory Self Test* and *XOff* to '0'.
   - Set *Matrix Readout Speed* as required - '1' is the default (20 kHz). Setting '0' would imply readout at 10 kHz.
   - Set *Force Busy* and *Force Busy Value* as required.
   - Note that it is recommended that *Force Busy*, *Force Busy Value* and *Xoff* fields would typically be modified while in readout so the values for the remaining fields should be stored.

3.8 Programming and reading of fuses.

The polysilicon fuses block interfaces with the rest of the chip through two registers, the fuses write and fuses read registers(see Table 3.2). Since there are 24 fuses, each of the aforementioned registers span two addresses. The fuses read register is read only and reflects the state of the fuses, equal to '0' prior to burning, and equal to '1' if the fuse has been burnt. The fuses write register is used to selectively and permanently burn the poly fuses. This is done by applying 3.3 V to the DVDD33 pad and writing the desired code into the fuses write register and maintaining the state in the fuses write register for a minimum 5 microseconds. During the write operation the read register reflects the code from the beginning of the write operation, even before the fuse is fully burnt. It is recommended to only write into the fuses write register with the intention to burn the fuses; writing into this register should be avoided when the 3.3 V is not applied.

4 Principles of Operation

This chapter shall describe with enough detail the operation of the chip and the structure and design of all the internal circuits. This targets the internal users that have to test the chip or build support systems.

4.1 Pixel circuits. Analog Front-End and Digital Pixel.

4.1.1 Analog Front-End

The ALPIDE-3 matrix is divided in 8 sectors of 512 × 128 pixels. Each region thus comprises 4 regions. The sectors are numbered from left to right on the chip. Each sector implements a different front-end flavour as reported in Table 4.2. A comprehensive scheme for the pixel front-end circuit including all possible variations is shown in Figure 4.1.

Sector	M3, M5, M6, M8	VCASN2 (M9)	Clipping M6 gate	M1 bulk	Reset	Spacing
0	optimized size	Yes	diode conn.	AVDD	Diode	2 μm
1	optimized size	No	diode conn.	AVDD	Diode	2 μm
2	as in pALPIDE-1/2	No	diode conn.	AVDD	Diode	2 μm
3	optimized size	Yes	VCLIP	AVDD	Diode	2 μm
4	optimized size	Yes	VCLIP	Source	Diode	2 μm
5	optimized size	Yes	VCLIP	Source	Diode	3 μm
6	as in pALPIDE-1/2	No	diode conn.	AVDD	PMOS	2 μm
7	optimized size	Yes	VCLIP	AVDD	PMOS	2 μm

Table 4.2: ALPIDE-3 sectors

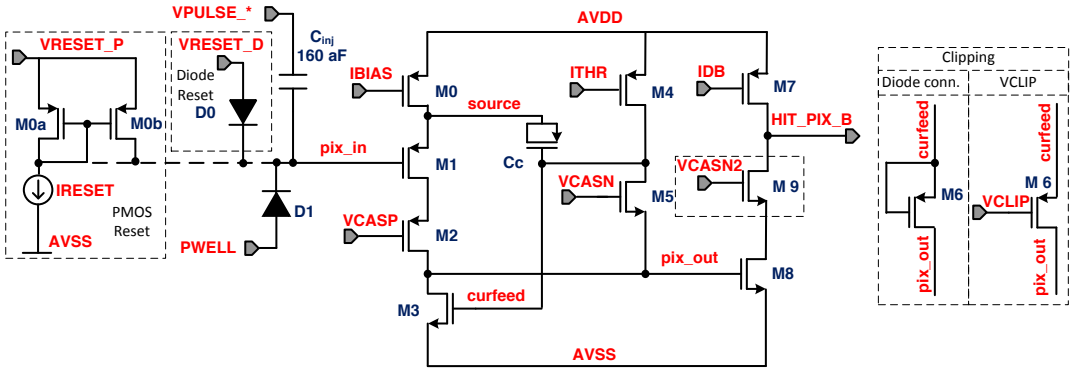


Figure 4.1: ALPIDE-3 Front-end(s) comprehensive scheme

There are two implementations of the collecting diode (D1) reset circuitry. In the PMOS reset scheme, VRESETP establishes the reset voltage of the charge collecting node (pix_in) and IRESET defines the maximum reset current. In the Diode reset scheme, the VRESETD establishes the reset voltage of the charge collecting node (pix_in). For the PMOS reset the potential on pix_in

will typically be close to VRESET_P, if IRESET is set to a value larger than the pixel leakage current. For the DIODE reset some more significant voltage drop, depending on the magnitude of sensor leakage, will be present. When a particle hit is received, the front end will increase the potential at the input of transistor M5 (pix_out), forcing it into conduction. If the current in M5 overcomes IDB, M5 will drive PIX_OUT_B low. The charge threshold of the pixel is defined by ITHR, VCASN and IDB. The effective charge threshold is increased by increasing ITHR or IDB. It is decreased by augmenting VCASN. The active low PIX_OUT_B signal is applied to the digital section of the pixel where it is used to set the hit status register. It is possible to inject a test charge in the input node for test purposes. This is achieved by applying a voltage pulse of controllable amplitude to the VPULSE pin of the C_{inj} capacitor. This is controlled by the digital section of the pixel.

The front-end circuits in ALPIDE-3 are based on the pALPIDE-1/2 front-end circuit with step by step modifications in order to trace the effects on performance. Sectors 2 and 6 implement the same architecture as in ALPIDE-1 and ALPIDE-2, with larger current bias transistors (M0, M4, M7). This change is intended for the reduction of the pixel-to-pixel variation of IBIAS, ITHR and IDB reference currents. Sector 2 implements the diode reset scheme, sector 6 implements the PMOS reset scheme. Sector 1 optimizes the M3, M5, M6, M8 transistors size with the aim a of further reduction of the pixel-to-pixel mismatch. Sector 0 adds transistor M9 (VCASN2), in order to reduce the equivalent Miller capacitance on pix_out. Sectors 3 and 7 have the possibility to tune the pulse duration acting on the clipping transistor gate (M6): it is decreased by augmenting VCASN. Sector 3 implements diode reset and sector 7 implements PMOS reset. Sector input transistor bulk is connected to its source instead of being connected to AVDD. This configuration is expected to increase the front-end gain by 18 %. In all sectors the collection n-well has octagonal shape with 2 μm diameter. All sectors, except sector 5, have 2 μm collection n-well to p-well spacing. Sector 5 has the same circuit of sector 4, with n-well to p-well spacing of 3 μm.

4.1.2 Digital Pixel

The digital section of the pixel is illustrated in Figure 4.2. The corresponding signals are listed in Table 4.3. The pixel features three State Registers. Each State Register is a Set-Reset Latch that can keep the hit information. The State Register is normally set by the front-end discriminated output PIX_OUT_B if the corresponding STROBE_B<2:0> is asserted simultaneously. It can also be set programmatically by the DPULSE signal (digital pulse functionality) if the corresponding STROBE_B<2:0> is asserted simultaneously. The State Register can be selected for read/reset by asserting the corresponding MEMSEL_B<2:0> bit. The selected State Register is reset either by a PIX_RESET pulse generated by the Priority Encoder during the readout, either by a global FLUSH_B signal. The State Register is sensitive to the falling edge of PIX_RESET and it is level sensitive with respect to the FLUSH_B input. The selected State Register output bit can be masked and the result is the output to the Priority Encoder (STATE signal). If no State Register is selected STATE is 0.

The logic provides two programmable functions: masking and pulsing. When control bit MASK_EN is set high, the STATE output is forced to 0, effectively masking the pixel otuput to the priority encoder. The low value provides normal functionality. The testing functionalities are enabled by setting PULSE_EN=1, disabled otherwise. DPULSE assertion allows for the pixel digital pulsing. This consists in forcing to logic high the hit latch (STATE_INT), bypassing the pixel front-end signal. This can be done asserting DPULSE. The analog testing consists in the injection of test charge in the input node through Cinj (160 aF nominal). The amplitude of the applied voltage pulse is defined by the difference between VPLSE_HIGH and VPLSE_LOW, both set in the DAC unit. Notice that the two edges of the pulse provoke the injection of two charge pulses of opposite polarities. The rising edge of APULSE corresponds to the discharge of the collection diode, in a manner equivalent to the passage of a charged particle. There are two

D-latches to store the PULSE_EN and MASK_EN configuration bits. Notice that their values after power-on are undefined. Setting of these latches is done by the PIXCNFG_COLSEL, PIXCNFG_ROWREGPSEL, PIXCNFG_ROWREGMSEL, PIXCNFG_DATA lines, all driven by the periphery control circuitry. The addressing of the pixels for configuration is based on the simultaneous selection of a specific row and a specific column. The simultaneous assertion of PIXCNFG_COLSEL and PIXCNFG_ROWREGMSEL pixel inputs selects the mask latch. The simultaneous assertion of PIXCNFG_COLSEL and PIXCNFG_ROWREGPSEL pixel inputs selects the pulse latch. PIXCNFG_DATA provides the value to be stored in the selected latch. There is no direct way to read back the values in the latches from the control interface.

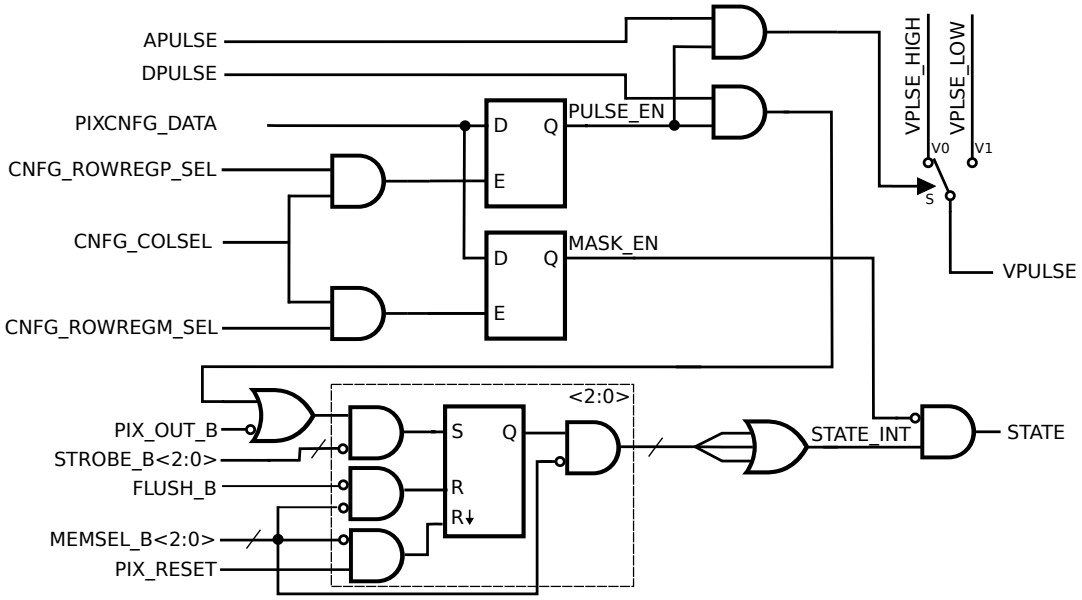


Figure 4.2: Functional diagram of the pixel logic

4.2 Priority Encoders and pixel indexing.

Looking at the chip with the digital periphery on the bottom, the leftmost region is region 0 and the rightmost region is region 31 (see Figure 4.3).

Each region contains 16 double columns. Double column 0 is the leftmost and double column 15 is the rightmost (see Figure 4.4).

The matrix of pixels is readout by an array of 512 Priority Encoder blocks. The pixels are arranged in double columns and the regions at the middle of each double column are occupied by the Priority Encoders. The indexing of the pixels in the readout data words is defined by the Priority Encoders. The indexing of the pixels in each double column is illustrated in Figure 4.5.

4.3 Analog bias and internal DACs

The pALPIDEfs chip has eleven internal DACs: six 8-bit voltage DACs and five 8-bit current DACs. These DACs are used to set the voltage and current biases required by the pixel front-end circuits. Table provides an overview of the specifications of the DACs. The DAC block has three operation modes:

	Signal	Description	Logic level
	APULSE	VPULSE voltage level selection if PULSE_EN = 1	Positive edge charge injection
	DPULSE	Digital Pulse if PULSE_EN = 1	Active high
	PIXCNFG_DATA	Configuration data	D-LATCH data line
	PIXCNFG_COLSEL	Column selection	Active high
	PIXCNFG_ROWREGPSEL	Row and Pulse reg. selection	Active high
	PIXCNFG_ROWREGMSEL	Row and Mask reg. selection	Active high
	PIX_OUT_B	Pixel front-end output	Active low
	STROBE_B<2:0>	Enable State register for hit acquisition	Active low
	MEMSEL_B<2:0>	Select State register for read and reset	Active low
	FLUSH_B	General reset of the selected the state register(s)	Active high
	PIX_RESET	Priority encoder reset of the selected register	Effective on falling edge
	VPLSE_HIGH	Analog pulse high level	Analog
	VPLSE_LOW	Analog pulse low level	Analog
	MASK_EN	State register mask enable	Active high
	STATE_INT	State register data	Active high
	VPULSE	Voltage step for test charge injection into pix_in net	$Q_{inj} = \Delta(\text{VPULSE}) \cdot 160$ aF
	STATE	State register value to priority encoder (if MASK_EN = 0)	Active high

Table 4.3: Signals of the pixel cell

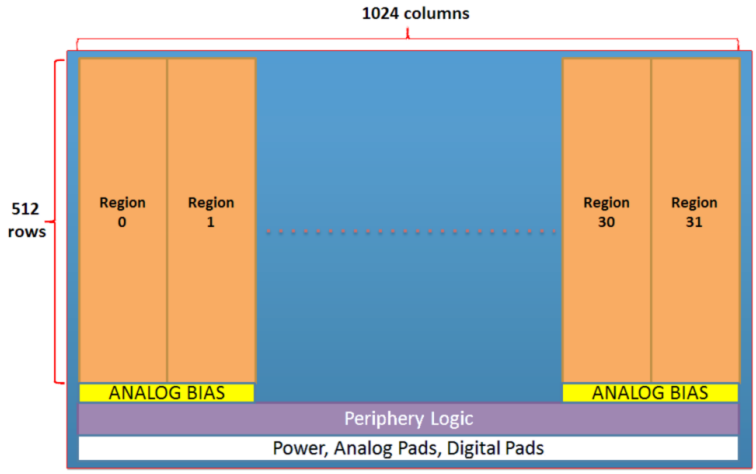


Figure 4.3: Region numbering

1. Normal - the outputs of all DACs are connected directly to the pixel matrix.
2. Monitor - it is possible to select a voltage DAC and monitor its output on the DACMONV pad. It is also possible to select a current DAC and monitor its output on the DACMONI pad.
3. Override - it is possible to override the output of one selected voltage DAC by the DACMONV pad. It is possible to override the output of one selected current DAC by the

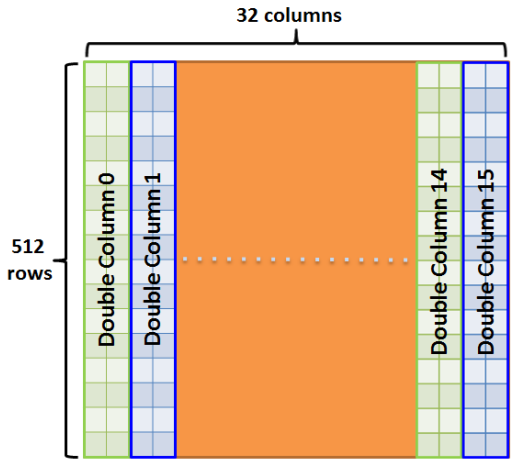


Figure 4.4: Double column numbering inside of a region

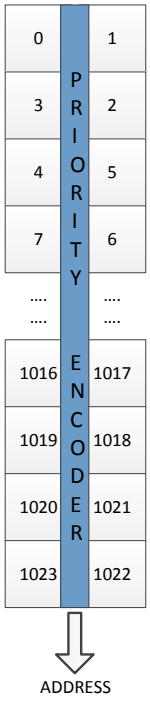


Figure 4.5: Indexing of pixels inside a double column provided by the Priority Encoders

DACMONI pad. It is also possible to override the internally generated IREF current that defines the LSB value of the current DACs.

The voltage DACs are based on a 256 stages resistive divider connected between the VREF pad and AVSS. Each resistor has a nominal value of 40 Ω, for a total resistance of 10.2 kΩ. This allows to generate voltage levels between AVSS and VREF (256-1)/256 with 8 bit resolution. The values

of the voltage DAC setting registers are decoded and used to control arrays of analog switches connected between the 256 nodes of the resistor divider and the output pins of the DACs. The VCASN and VCASP outputs are directly applied to the matrix without any amplification or scaling. The VRESET, VPLSE_LOW and VPLSE_HIGH and VAUX outputs are buffered with unit gain followers. This causes an offset of about 370 mV and saturation for codes above about 200 for these DACs. The nominal voltage to apply to the VREF pad is 1.8 V (AVDD). Any external additional resistance between the VREF source and the pad decreases the maximum voltage reachable by the DACs. A low series resistance ($< 100\ \Omega$) should be guaranteed between the source and the pad. At the nominal bias value (VREF = 1.8 V) the current sunk by the VREF pad is $\approx 180\ \mu$A. The current DACs are implemented by repeating 256 times the same building unit that is a current source generating the current corresponding to the LSB. This is 1/256 of IREF, an internally generated reference current. IREF is nominally 10.24 μA, the LSB value is nominally 40 nA. The values of the current DACs setting registers are decoded and used to control the analog switches connecting the LSB sources in parallel into the output node of each DAC. The outputs of the current DACs are then scaled to appropriate levels before being applied to the matrix. The scaling factors are given in Table . Monitoring and Overriding of the DACs It is possible to monitor the output of a selected voltage DAC using the DACMONV pad. The DACMONV pin should be monitored with a high input impedance circuit (Rin $>$ 1 MΩ). Only one voltage can be monitored at a given time. It is possible to monitor the output of a selected current DAC using the DACMONI pad loaded with a shunt resistor to AVSS. The recommended shunt resistance is 5 kΩ. Only one current can be monitored at a given time. The current on the shunt resistor is equal to ten times the output current of the selected DAC, upstream the scaling towards the pixels. It is possible to override a selected voltage DAC using the DACMONV pad. Once the functionality is activated a voltage between 0 and VREF needs to be applied to the DACMONV pad. This will feature high input impedance. The voltage applied to DACMONV goes directly to the pixel matrix. It is possible to override a selected current DAC using the DACMONI pad. Once the functionality is activated a current needs to be sourced from DACMONI as illustrated in Figure . This current is divided by 10 internally and this replaces the output of the DAC before the internal scaling towards the pixel matrix. The range of interest for the external overriding current is 0 to 200 μA, covering almost twice the internal nominal range. Finally the internal IREF current constituting the reference for all the current DACs can be overridden. In this case the current sourced by the DACMONI pad is divided by 11 before being used by the internal DACs. The configuration of the DAC block for monitoring or overriding and the selection of the DACs are done by the dedicated Current/Voltage Monitoring and

4.4 Details on the readout and framing circuits.

This shall contain all the technical documentation material we shared with the design, namely the block diagrams, state machine diagrams, illustrations, wave timing diagrams from simulations and similar.

Appendices

Appendix A Application note. Chip and modules clocking schemes.

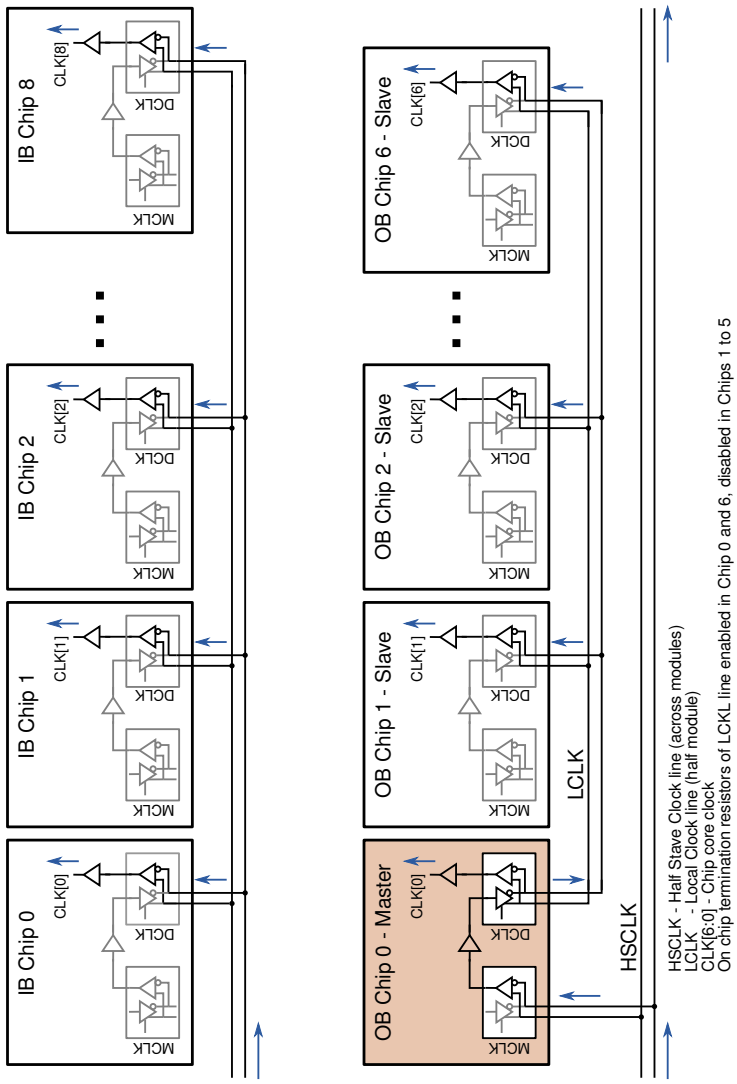


Figure A.1: Illustration of the clock distribution scheme for the ITS Inner Barrel and Outer Barrel Modules.

Appendix B Application note. ALICE ITS Inner Barrel Modules

The following text (this appendix) was copied over from the pALPIDE-2 datasheet draft. This is for the convenience of having text snippets and templates. Requires sistematic revision to become valid for ALPIDE-3 and its structure can be revised.

Remarks

- Inner Barrel Module prototypes include 9 chips
- The 9 chips receive from the off detector electronics a global clock signal on the shared differential line DCLK.
- The DCLK lines connects in a multi-drop configuration the DCLK_P, DCLK_N terminal pairs. Double termination of the line on transmitter and far end sides is required.
- An unavoidable skew of the internal clocks related to the propagation delays on the line is to be expected.
- The nominal clock frequency for the Inner Barrel module prototypes is **40 MHz**.
- A DCTRL differential line connects in a multi-point configuration the DCTRL_P, DCTRL_N terminals with a differential transceiver on the off-detector side. Double terminations of the line shall be provided at both extremities.
- Signaling on the DCTRL bus is half-duplex and synchronous to the clock. Topological symmetry between the DCTRL line and the DCLK line ensures that the sampling of the DCTRL bus by the chips can be achieved and maintained with correct timing.
- The off-detector electronics shall be capable to transmit serially on the DCTRL bus with a bit period twice (or at least equal) to the clock period.
- The off-detector electronics shall be capable to disable its line driver during the responding periods in which one chip on the line activates its own driver.
- Chips respond on DCTRL according to a pre-defined protocol (ref. datasheet).
- Chips responses on DCTRL are clock synchronous serial transmissions.
- The DCTRL signal sampled at the off-detector electronic side will present a changing phase with respect to the transmitted clock, depending on the distance of the transmitting chip down along the line. Over the 30 cm length of IB Module prototypes this is expected to be irrelevant. Means of appropriate re-timing could be foreseen on the off-detector electronics.
- Chips send their data off-detector by point-to-point uni-directional differential signaling (DATAPORT).
- Serial transmission on DATAPORT has a bit period equal to half clock period. One bit is transmitted at every clock edge (Double Data Rate). With nominal 40 MHz clock this is a serial stream at 80 Mbps.

- The signal sampled on the data links at the off-detector electronic side will present a changing phase with respect to the reference clock depending on the length of the line between the transmitting chip and the receiver. Over the 30 cm length of IB Module prototypes this is expected to be irrelevant. Means of appropriate re-timing should be foreseen on the off-detector electronics.
- An idling character is transmitted continuously when no payload data are being sent. This enables the off-detector electronics to byte-align the deserialized bit stream.

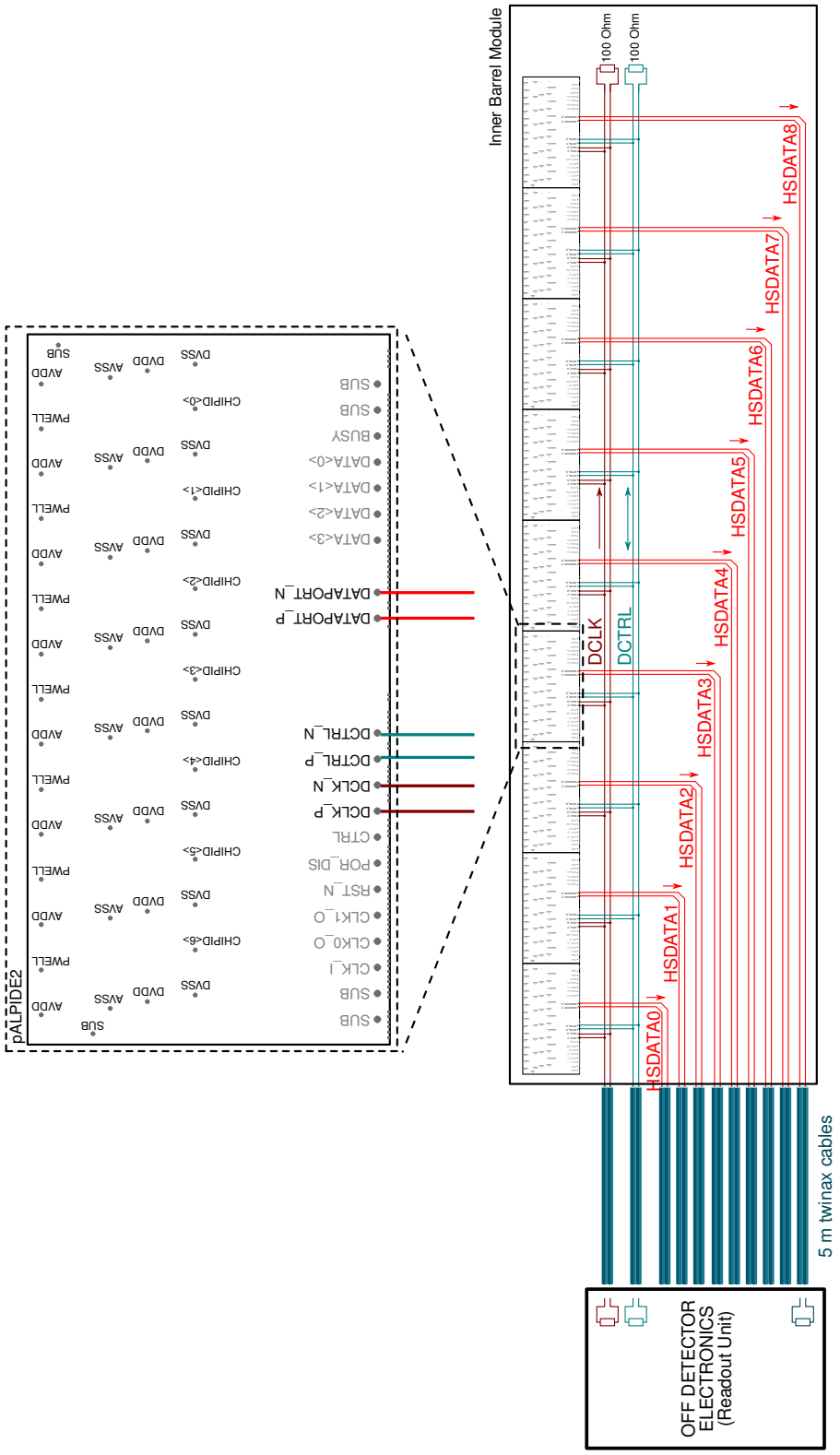


Figure B.1: Schematic diagram of the electrical interconnections between the ALICE ITS Upgrade Inner Barrel module and the off-detector electronics.

Appendix C Application note. ALICE ITS Outer Barrel Modules

The following text (this appendix) was copied over from the pALPIDE-2 datasheet draft. This is for the convenience of having text snippets and templates. Requires sistematic revision to become valid for ALPIDE-3 and its structure can be revised.

- Outer Barrel Module prototypes include 14 chips in two sets of 7 (seven). Each subset includes one Outer Barrel Module Master and six associated Outer Barrel Module Slaves.
- The OB Module Master chips receive from the off detector electronics a global clock signal on a shared differential line DCLK.
- 7 (or 4) Master chips share one DCLK line routed along 7 (or 4) modules constituting one Outer (Middle) Layer half stave.
- The DCLK lines connects in a multi-drop configuration the DCLK_P, DCLK_N terminal pairs of the OB Module Master chips. Double termination of the line on transmitter and far end sides is required.
- An unavoidable skew of the internal clocks related to the propagation delays on the line is to be expected.
- The nominal clock frequency for the Outer Barrel module prototypes is **20 MHz**.
- A DCTRL differential line connects in a multi-point configuration the DCTRL_P, DCTRL_N terminals of the OB Master chips with a differential transceiver on the off-detector side. Double terminations of the line shall be provided at both extremities.
- Signaling on the DCTRL bus is half-duplex and synchronous to the clock. Topological symmetry between the DCTRL line and the DCLK line ensures that the sampling of the DCTRL bus by the OB Master chips can be achieved and maintained with correct timing.
- The off-detector electronics shall be capable to transmit serially on the DCTRL bus with a bit period twice (or at least equal) to the clock period.
- The off-detector electronics shall be capable to disable its line driver during the responding periods in which one of the OB Master chips on the line activates its own driver.
- Chips respond on DCTRL according to a pre-defined protocol (ref. datasheet).
- Chips responses on DCTRL are clock synchronous serial transmissions.
- The DCTRL signal sampled at the off-detector electronic side will present a changing phase with respect to the transmitted clock, depending on the distance of the transmitting chip down along the line. Means of appropriate re-timing should be foreseen on the off-detector electronics.
- OB Module Master chips transmit data from themselves and the associated six OB Module Slaves by point-to-point uni-directional differential signaling using DATAPORT.
- Serial transmission on DATAPORT has a bit period equal to half clock period. One bit is transmitted at every clock edge (Double Data Rate). With nominal 20 MHz clock this is a serial stream at 40 Mbps.

- The signal sampled on the Data links at the off-detector electronic side will present a changing phase with respect to the reference clock, depending on the length of the line between the transmitting chip and the receiver. Means of appropriate re-timing should be foreseen on the off-detector electronics.
- An idling character is transmitted continuously when no payload data are being sent. This enables the off-detector electronics to byte-align the deserialized bit stream.
- The data exchange between the OB Module Slave chips and the OB Module Master is realized on a OB Module Local Data Bus.
- The OB Module Local Data Bus is a shared parallel bus realized interconnecting the DATA port of the chips.
- The 4 lowermost lines of the DATA port operate in Double Data Rate mode, with bits launched or sampled at both clock edges and one complete byte transfer at every clock cycle. The uppermost 4 bits can be left unconnected and the OB Local Data Bus bus can be implemented using 4 wires shared by the chips. Optionally, the chips can be configured to revert to Single Data Rate signaling on the DATA[3:0] IOs and in this case 8 wires would be needed.
- The OB Module chips drive in turn the Local Data Bus. Write right to the bus is granted by default to the OB Master chip. The slave chips sample the data on the Local Bus monitoring the Chip Data Frame transmitted on it by the other chips. On detection of the completion of a frame by a pre-specified chip in the set, a given slave acquires the right to access the bus and transmit onto it a complete Chip Data Frame. At the end of one frame the chip disables the Local Bus Drivers and enters a waiting state for a new time access slot.
- The ordered sequence of chip identifiers governing the write access to the Local Data Bus is programmable by means of a dedicated register.

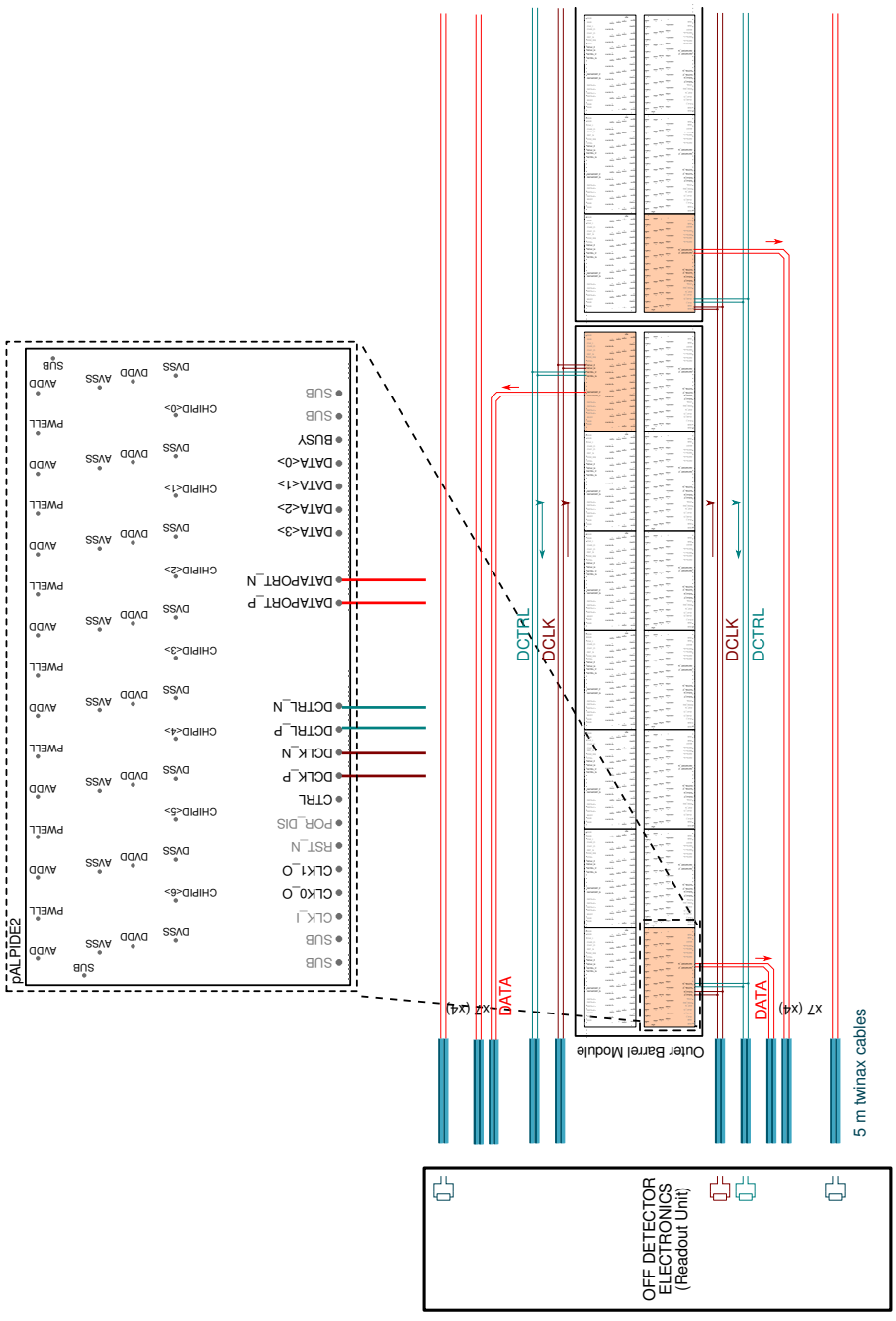


Figure C.1: Schematic diagram of the electrical interconnections between ALICE ITS Upgrade Outer Barrel modules and off-detector electronics.