ALPIDE Operations Manual

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1 Introduction

The ALPIDE chip is a CMOS Monolithic Active Pixel Sensor developed for the Upgrade of the Inner Tracking System of the ALICE experiment at the CERN Large Hadron Collider.

The ALPIDE chip measures 15 mm (Y) by 30 mm (X) and contains a matrix of 512 ×1024 (Y×X) sensitive pixels. The pixels are 29.24 μm × 26.88 μm X×Y). A periphery circuit region of 1.2×30 mm^2 including the readout and control functionalities is present. It is assumed that the chip is observed from the circuits side and oriented such that the periphery is the bottom. The pixel columns are numbered from 0 to 1023 going from left to right. Pixel rows are numbered from 0 to 511 going from the matrix top side to the bottom one.

Each pixel features an ultra-low power, non-linear front-ent with shaping and discriminated output. The pixel sensor and front-end are always active. The front-end acts as a delay line: upon a particle hit, it generates a pulse with a duration of a few microseconds. A threshold is applied to form a binary pulse. A hit is latched into one of the three in-pixel memory cells if a STROBE signal is applied to the corresponding cell while the aforementioned binary pulse is asserted. The assertion of STROBE signals to the pixels during the response interval following an event of charge release in the sensing diode causes the latching of the discriminated output into one of three storage cells in the digital section of the pixel. The pixels feature a built-in test pulse injection circuit triggerable on command. A digital-only test pulse mode is also available, forcing the writing of a logic one in the selected in-pixel memory cell. The STROBE signals are generated at the periphery and applied simultaneously to all pixels. The logic generating the STROBE signal is configurable according to different operating modes and the duration of the STROBE signals is also programmable. The generation of STROBE signals is typically triggered by an externally applied trigger command.

The hits stored in the pixels multi-event buffers are read out by means of Priority Encoder circuits. These provide the address of a pixel with a stored hit based on a hardwired topological priority. During one hit transfer cycle a pixel with a hit is selected, its address generated and transmitted to the periphery and finally the in-pixel memory element is reset. This cycle is repeated until all hits at the inputs of the Priority Encoder are read out. The readout of the sensitive matrix to the periphery is therefore zero-suppressed and hit-driven. Time and energy are consumed proportionally to the number of hits at the inputs of the Priority Encoder.

The raedout of the matrix is organized in 32 regions (512×32 pixels), each of them with 16 double columns being read out by 16 Priority Encoder circuits. The hits inside one region are read out sequentially in consecutive readout cycles.

The processes of readout of the 32 regions are executed in parallel. They are driven by state machines in the Region Readout Unit blocks. The Region Readout Units also contain multi-event storage memories and data compression functionality based on clustering by adjacency. The data from the 32 region readout blocks are assembled and formatted by a chip level Top Readout Unit.

Hit data can be transmitted on two different data interfaces according to one of three alternative operating modes envisaged for the Upgraded ALICE ITS: *Inner Barrel Module chip*, *Outer Barrel Module Master*,*Outer Barrel Module Slave*. A 1.2 Gb/s serial port (HSDATA) with differential signalling is intended to be the primary data readout interface for the Inner Barrel Module chips. This port can optionally operate at reduced bit rates (600 Mb/s or 400 Mb/s).

The same interface is intended to be used for the transmission of data off-detector by the Outer Barrel Module Master chips, using a bit rate of 400 Mb/s. These also collect the data

of a set of neighboring Outer Barrel Module Slave chips and forward their data off-detector on a common differential link.

A parallel output data port using CMOS signaling is also present. It enables the implementation of the data exchange between the Outer Barrel Module Slave chips and the corresponding Master. All the functionalities related to the Outer Barrel Module bus arbitration, data encoding, data transmission are implemented by a dedicated Data Management Unit.

A top-level Control Management Unit block provides full access to the control and status registers of the chip as well as to the multi-event memories in the Region Readout Units. Control commands are supported by the control interface. The slow control is implemented onto a differential, serial, half-duplex link specifically designed for the Upgraded ITS (DCNTRL). A secondary single-ended control port (CNTRL) is dedicated to the forwarding of control transactions between the Outer Barrel Module Master chips and the Outer Barrel Module Slaves.

All the analog signals required by the front-ends are generated by a set of on-chip DACs. Analog monitoring pads (DACMONV, DACMONI) are available to monitor the outputs of the internal DACs. The DACMONV pad can be used to override any of the voltage DACs. The DACMONI pad can be used to override any of the current DACs or to override the internal reference current used by the current DACs.

2 ALPIDE data sheet

This chapter shall contain summarized technical information about the chip, interfaces, pin functions, die geometry, pads geometry, electrical characteristics, timing requirements, switching characteristics.

2.1 Block diagrams and pinout

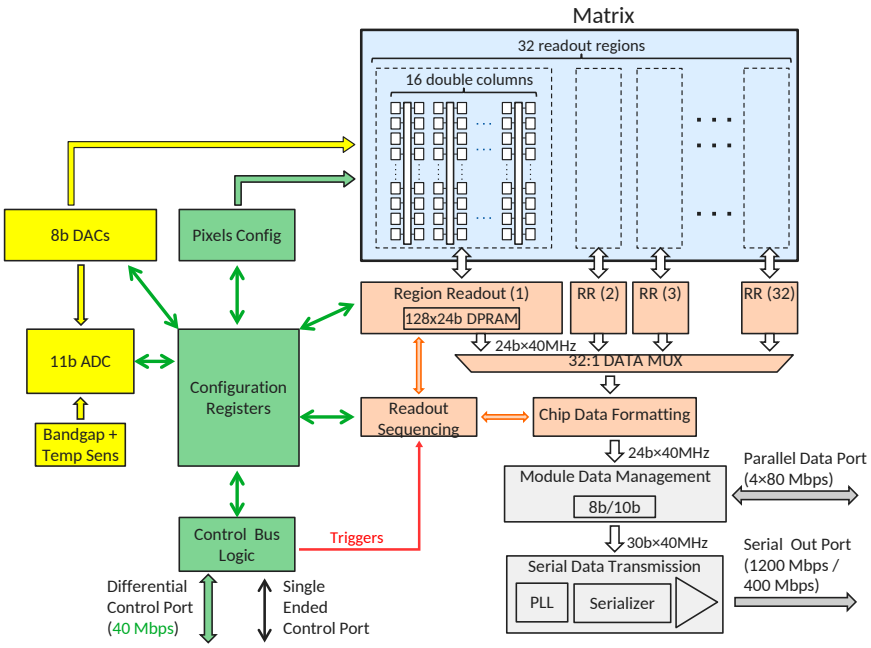

Figure 2.1: ALPIDE chip block diagram.

2.2 Interface signals

The main functional I/Os of the ALPIDE chip are listed in Table 2.1. Figure 2.3 shows the locations of the pads.

The CMOS I/Os are 1.8 V compatible. Two types of CMOS I/O pad cells are used in ALPIDE: one has an internal pull-up resistor and one an internal pull-down resistor. The internal resistors are always connected to the pad. The driving strengths of the two cells are equal and fixed. The pad cells are tri-state capable and their drivers can be turned off and placed in a high-impedance mode depending on configuration and conditions.

The MCLK, DCTRL ans DCLK differential ports are implemented with a custom designed differential transceiver cell. This has been designed with reference to standard TIA/EIA-899 Electrical Characteristics of Multipoint-Low-Voltage Differential Signaling (M-LVDS)[1], however the differential ports are not standard compliant in particular with respect to the acceptable range of the input common voltage.

Tables 2.3, Table 2.4 and Table 2.5 summarize the recommended DC operating conditions and the electrical characteristics of the various interfaces.

[1] See Texas Instrument Application Report SLLA108A

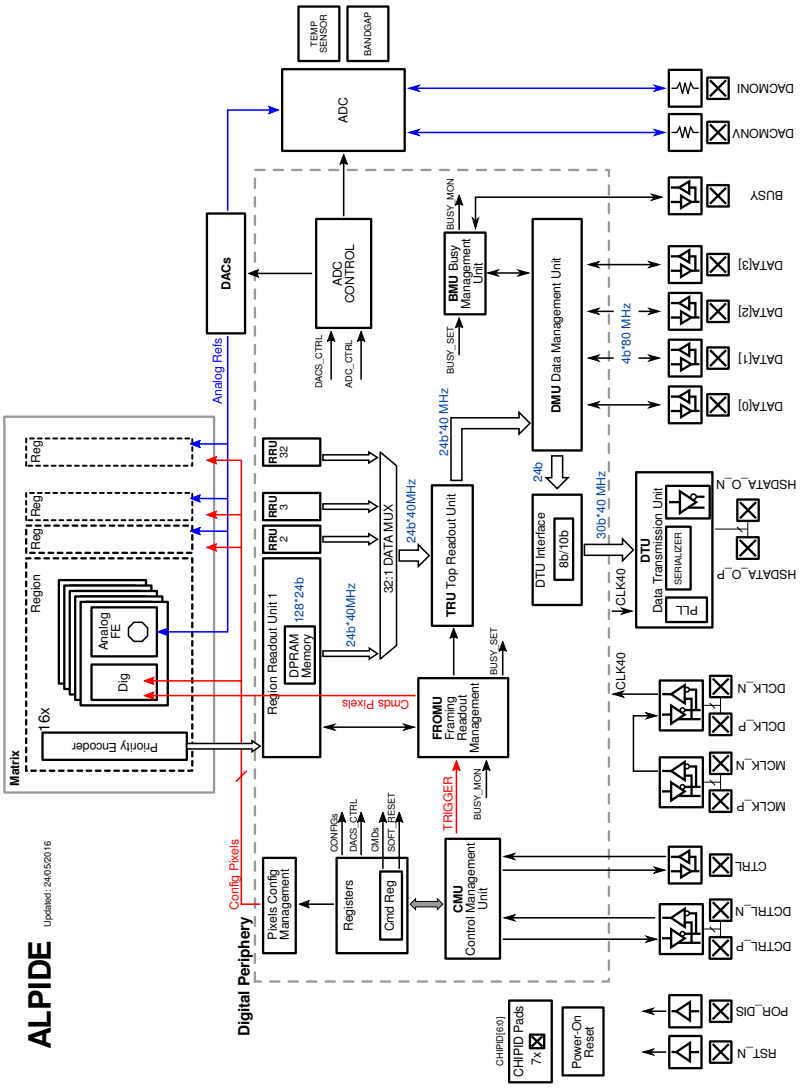

Figure 2.2: ALPIDE chip block diagram with modules and hard-blocks.

The analog monitoring ports provide access to internal nodes through a series resistor.

Table 2.1: ALPIDE interface signals.

Signal	Type	Direction	Purpose
MCLK_P	Differential (MLVDS)	INPUT	Forwarded clock input
MCLK_N	Differential (MLVDS)	INPUT	Forwarded clock input
RST_N	CMOS, internal pull-up	INPUT	Global chip reset
POR_DIS_N	CMOS, internal pull-up	INPUT	Power On Reset Disable
DCTRL_P	Differential (MLVDS)	BIDIR	Differential Control port
DCTRL_N	Differential (MLVDS)	BIDIR	Differential Control port
DCLK_P	Differential (MLVDS)	BIDIR	Main clock input and clock forwarding output
DCLK_N	Differential (MLVDS)	BIDIR	Main clock input and clock forwarding output
HSDATA_P	Differential (LVDS)	OUTPUT	Serial Data Output
HSDATA_N	Differential (LVDS)	OUTPUT	Serial Data Output

CTRL	CMOS, internal pull-up	BIDIR	Control port (OB local bus)
DATA[7]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
DATA[6]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
DATA[5]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
DATA[4]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
DATA[3]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
DATA[2]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
DATA[1]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
DATA[0]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
BUSY	CMOS, internal pull-up	BIDIR	Busy flag
DACMONV	ANALOG	OUTPUT	Voltage Monitoring Output
DACMONI	ANALOG	OUTPUT	Current Monitoring Output
CHIPID[6]	CMOS, internal pull-down	INPUT	Topological chip address
CHIPID[5]	CMOS, internal pull-down	INPUT	Topological chip address
CHIPID[4]	CMOS, internal pull-down	INPUT	Topological chip address
CHIPID[3]	CMOS, internal pull-down	INPUT	Topological chip address
CHIPID[2]	CMOS, internal pull-down	INPUT	Topological chip address
CHIPID[1]	CMOS, internal pull-down	INPUT	Topological chip address
CHIPID[0]	CMOS, internal pull-down	INPUT	Topological chip address

MCLK_P, MCLK_N: Clock forwarding input port, used to implement the clock distribution in the Outer Barrel Module application scenario. This is a receiving only port, the driver behind it being disabled in all scenarios. The receiver is enabled when the chip is configured as Outer Barrel Module Master and the signal applied to this port is then forwarded to the DCLK_P, DCLK_N port. A chip configured as Inner Chip or Outer Barrel slave chip keeps the receiver on this port disabled (refer to appendix A).

RST_N: Global active-low reset signal. This port can be left unconnected in applications not needing a dedicated reset pin. The ALPIDE chip includes a power-on-reset circuit. The chip can also be reset by commands issued by the control interface.

POR_DIS_N: Disabling of the power-on-reset circuit, active low. Driving low this input masks the output of the internal power-on reset circuitry. If the internal power-on-reset is used this pin can be left unconnected since it is internally pulled-up.

DCTRL_P, DCTRL_N: Differential bidirectional control port. Intended to implement the half-duplex control bus segments between the Inner Barrel chips or the Outer Barrel Module Master chips and the off detector electronics. The DCTRL port is unused by a chip configured as Outer Barrel Module Slave Chip.

DCLK_P, DCLK_N: Main clock input and forwarded clock output. Nominal clock frequency is 40 MHz. This is the chip clock source regardless of the operating mode and configuration scenario. In all configurations the receiver circuit at this port provides the clock to the chip core. A chip configured as Outer Barrel Module Master has an active driver on this port and forwards on it the signal received on the MCLK_P, MCLK_N port. This port is also equipped with an on-chip termination resistor (100 Ω) that is enabled depending on the signals applied to the CHIPID configuration port. Additional details can be found in appendix A.

HSDATA_P, HSDATA_N: Differential data output port. This port is used for the high speed serial transmission of data between chips and the off-detector electronics. It is used by chips configured as Inner Barrel Chip or Outer Barrel Module Master. The signaling rate on this port is programmable in the Inner Barrel Chip operating mode, choosing between 1.2 Gb/s (default) or 600 Mb/s or 400 Mb/s. The signaling rate is 400 Mb/s in the Outer Barrel Module Master configuration. The serial stream is (by default) 8b/10b encoded.

CTRL: Single ended, bidirectional control port. Intended to implement the half-duplex local control bus segments between the Outer Barrel Module Master chip and the associated slaves.

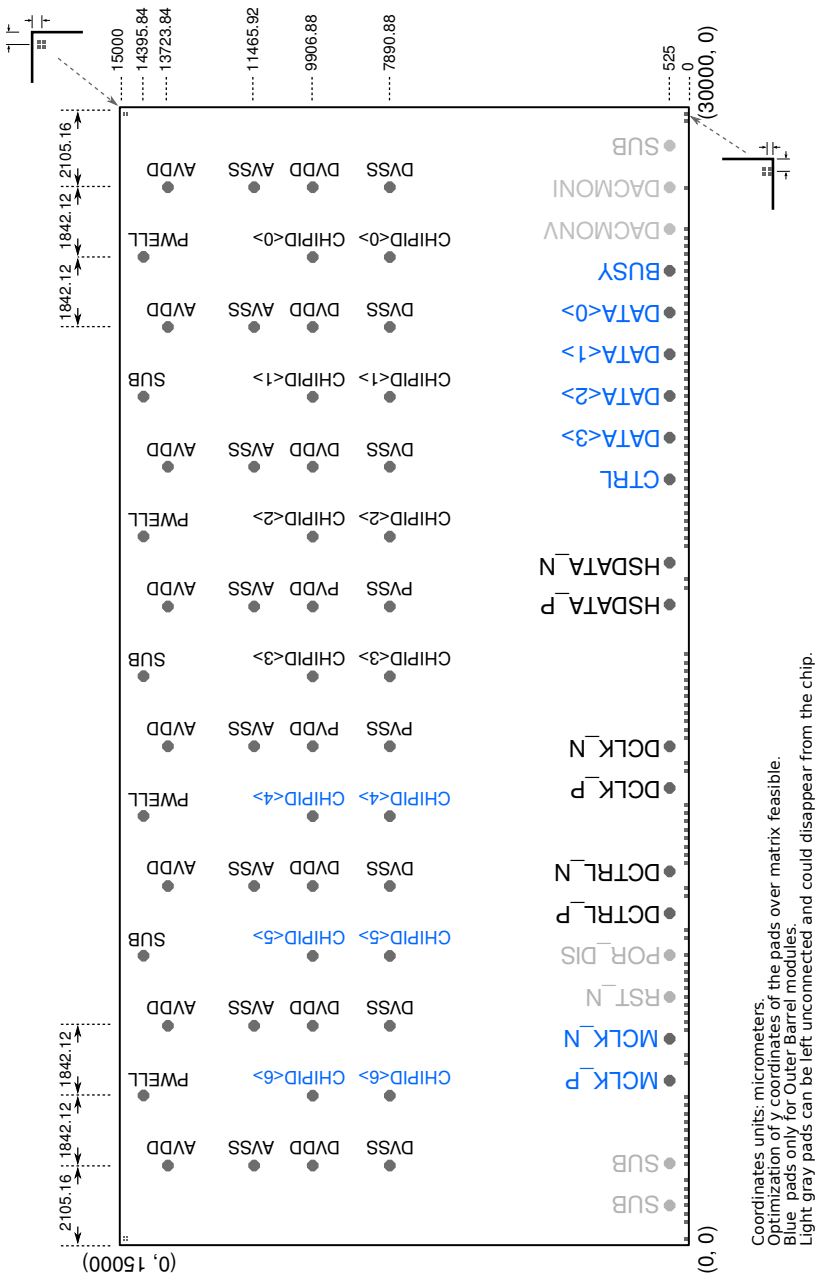

Figure 2.3: Pinout of the ALPIDE chip.

These chips shall have their CTRL ports directly connected by a single shared wire. The CTRL port is unused by a chip configured as Inner Chip.

DATA[7:0]: CMOS bidirectional data port. Intended to implement a shared parallel data bus between the Outer Barrel Module Slave chips and the associated Master. By default, the 4 lowermost lines of this port operate in Double Data Rate mode, with bits launched or sampled at both clock edges and one complete byte transfer completed at every clock cycle. Thus the uppermost 4 bits can be left unconnected and the bus can be implemented using 4 parallel wires shared by the chips. Optionally, the chips can be configured to revert to Single Data Rate signaling also on the lowermost 4 bits. In this case one byte is launched or sampled at every rising edge of the clock. This operating mode can be used for readout of chips through a 8 bit Single Data Rate parallel bus.

BUSY: Single ended port. It is intended to implement the communication of the BUSY state between the Outer Barrel Module Slaves and the associated Master chip by wiring in parallel all their BUSY ports. This port is not used when the chip operates as an ITS Inner Barrel chip. This port can be in one of two states: actively driven low or high impedance, thus emulating an open-drain topology. The signaling is active low. The pad provides weak internal pull-up. An external strong pull-up resistor might be required to speed-up the rise-time of the de-assertion (rising) edge depending on the total capacitance of the line and the number of chips connected to it. The sampling of the input on this port is equipped with a sychronizer to guarantee reliable operation.

DACMONV: Analog pin with dual functionality. It can be used to monitor each of the voltages generated by the on-chip voltage DACs. It can also be used to override the internal voltage DACs. The overriding is possible for one user-selectable DAC at a given time.

DACMONI: Analog pin with triple functionality. (a) Monitoring of the currents generated by the on-chip current DACs. (b) Override of the internal current DACs. The overriding is possible for one user-selectable DAC at a given time. (c) Override of the chip internal current reference, thus changing the range of all current DACs simultaneously.

CHIPID[6:0]: Chip topological address and mode selection. This port is intended to assign a binary coded address to each chip depending on its position on the ALICE ITS Modules. The address is used in the transactions via the control interface. The address value also selects if the chip behaves as a Inner Barrel Chip, an Outer Barrel Module Master chip or an Outer Barrel Module Slave chip. This pads have been designed to be directly wired to digital supply in order to set a binary '1' on a given line. Leaving one unconnected effectively sets to '0' the corresponding bit line due to the internal pull-down.

2.3 Supply, ground and bias nets

Table 2.2: ALPIDE supply, ground and bias nets.

Net	Type	Purpose
AVDD	SUPPLY	Analog domain supply
AVSS	GROUND	Analog domain ground
DVDD	SUPPLY	Digital domain supply
DVSS	GROUND	Digital domain ground
PVDD	SUPPLY	DTU PLL supply
PVSS	GROUND	DTU PLL ground
PWELL	SUBSTRATE	Substrate bias
SUB	SUBSTRATE	Substrate bias

AVDD, AVSS: Supply and ground rails of the analog domain. This includes the pixel front-end circuits and the analog biasing circuit.

DVDD, DVSS: Supply and ground rails of the digital domain. This includes the in-pixel

configuration registers, the matrix readout circuits, the peripheral readout circuits and the chip input and output buffers and transceivers.

PDVDD, PDVSS: Supply and ground rails dedicated to the Phase Locked Loop of the Data Transmission Unit.

PWELL: bias of the p-type wells in the pixel matrix region.

SUB: bias to the contacts to the substrate in the seal ring and in the periphery region.

All supply and ground nets must be connected to the recommended voltages. The pads of each supply or ground net are internally electrically connected by the on-chip supply and ground meshes. Therefore it is not mandatory to wire all the pads of a given supply or ground net. However, a reduction of the number of connected supply or ground pads can have detrimental effects on the circuit performance and operating capabilities or increase the risk of damaging the chip.

The PWELL and SUB bias nets cannot be left floating and must be strongly connected to appropriate bias voltages. The source impedance of the supply to these nets shall be kept as small as possible to limit the probability of latch-up.

The pads of the PWELL net are internally connected as well as those of the SUB net, therefore it is not mandatory to wire all the pads of a given net. The PWELL and SUB nets are weakly connected through the die substrate conductance.

The purpose of the PWELL and SUB substrate biasing nets is to enable the increase of the reverse bias voltage on the charge collecting diodes. This is obtained by applying to these nets a negative voltage with respect to analog ground (AVSS).

For system studies not requiring optimal sensor performance it is recommended to short both the PWELL and SUB pads to the AVSS ground (0 V with respect to AVSS). It is also recommended to bond the PWELL and SUB pads to a grounding conductor before any other pad is bonded, to mitigate the risk of ESD damage.

2.4 Recommended operating conditions

Table 2.3: Recommended operating conditions.

		MIN	TYP	MAX	Unit	Condition
AVSS	Analog ground		0		V	
AVDD	Analog supply	1.62	1.8	1.98	V	
DVSS	Digital core ground		0		V	
DVDD	Digital core supply	1.62	1.8	1.98	V	
PWELL	Substrate bias		0	0	V	Shorted to AVSS
SUB	Substrate bias		0	0	V	Shorted to AVSS
V_I	Voltage at any CMOS input	0		DVDD	V	
V_{IL}	Low level digital input voltage			0.33*DVDD	V	
V_{IH}	High level digital input voltage	0.66*DVDD			V	
I_{OL}	Low level digital output current			13.7	mA	Vo <0.45
$\|I_{OH}\|$	High level digital output current			13.6	mA	Vo >DVDD-0.45
V_P or V_N	Voltage at any differential bus terminal	0		DVDD	V	
$\|V_{ID}\|$	Magnitude of differential input voltage	50		DVDD	mV	
R_L	Differential load resistance	40	50	60	Ω	
T	Operating temperature	-25	25	85	℃	

2.5 Electrical characteristics

Table 2.4: CMOS IOs electrical characteristics over recommended operating conditions unless otherwise noted.

		MIN	TYP	MAX	Unit	Condition
V_{OH}	High level output voltage	DVDD-0.45			V	Io >-13.6 mA
V_{OL}	Low level output voltage			0.45	V	Io <13.7 mA
$\|I_{IL}\|$			44.4	62	μA	Pads with pull-up
I_{IH}			0.87	3.8	nA	Pads with pull-up
$\|I_{IL}\|$			3.3	11.5	nA	Pads with pull-down
I_{IH}			44.4	62	μA	Pads with pull-down
R_{Pullup}	Internal pull-up		40.6		kΩ	Pads with pull-up
R_{Pullup}	Internal pull-down		40.6		kΩ	Pads with pull-down
C_{PAD}	Input capacitance		0.98		pF	Inputs with A type pad only
C_{PAD}	Input capacitance		4.5		pF	Inputs with A and B type pads

Table 2.5: Electrical characteristics of MCLK, DCTRL and DCLK differential ports over recommended operating conditions unless otherwise noted.

		MIN	TYP	MAX	Unit	Condition
C_P or C_N	Input capacitance			3	pF	V_I, other pin at 1.1 V, driver disabled
C_{PN}	Differential input capacitance				pF	V_{ID} =, V_{IC} =, driver disabled
I_{OZ}	High-impedance state output current	-45		102	μA	Driver disabled
Driver related characteristics						
		MIN	TYP	MAX	Unit	Condition
$\|V_{OD}\|$	Output differential signal magnitude	80		480	mV	
$\|I_{OD}\|$	Output differential current magnitude	2		8	mA	
$V_{OS(SS)}$	Steady-state output common signal	980		1210	mV	
$\Delta V_{OS(SS)}$	Change in steady-state output common signal between logic states	-20		+20	mV	
$V_{OS(PP)}$	Peak-to-peak output common signal			75	mV	
Receiver related characteristics						
		MIN	TYP	MAX	Unit	Condition
V_{IC}	Input common signal	DVSS+25	1.1	DVDD-25	mV	
V_{IT+}	Positive-going differential input voltage threshold			50	mV	
V_{IT-}	Negative-going differential input voltage threshold	-50			mV	

2.6 Pad tables, geometrical data, alignment markers

A floorplan view with the name of the signals at the pads used for the connection to the ALICE ITS FPCs is given in Figure 2.3. The pad naming convention and the layout of the die with the position of the pads are illustrated in Figure 2.4.

Table 2.6 lists all the pads and interface nets of the chip. Table 2.7 gives the x and y coordinates of the *center* points of the chip pads.

Two types of pads with differing geometries are employed in the ALPIDE chip.

Type A pads are used for the pads in the pad ring along the chip south edge (from A00 to A94). All interface nets are available in this pad ring. Type A pads are standard size and intended to support wire bonding, probe testing or other applications. Figure 2.5 details the geometry of the opening of type A pads. The opening in the passivation layer of type A pads is square and 88 μm wide.

Type B are large pads over logic used above the periphery and the sensitive matrix of the chip (B00-B20, C00-C14, D00-D14, E00-E07, F00-F07, G00-G06). These pads enable the connection to Flexibel Printed Circuits. The nets accessible through pads of type B are also found in the ring of pads of type A. Figure 2.6 details the geometry of the opening of pads of type B. The opening in the passivation layer of type B pads has rounded edges and it is 290 μm wide.

The chip includes four structures located close to the four corners of the die to facilitate geometrical alignment procedures, as shown in Figure 2.4 for the markers on the top-right and bottom-right corners. The coordinates of the central point of the alignment markers are listed in table 2.8.

Table 2.6: ALPIDE pads and interface nets.

Pad Id	Net	Type	Direction	Purpose
A00	PWELL	SUBSTRATE		Substrate bias, Matrix
A01	AVSS	GROUND		Analog ground
A02	SUB	SUBSTRATE		Substrate bias, periphery
A03	AVDD	SUPPLY		Analog supply
A04	DVSS	GROUND		Digital ground
A05	DVDD	SUPPLY		Digital supply
A06	SUB	SUBSTRATE		Substrate bias, periphery
A07	AVSS	GROUND		Analog ground
A08	AVDD	SUPPLY		Analog supply
A09	DVSS	GROUND		Digital ground
A10	DVDD	SUPPLY		Digital supply
A11	SCI	CMOS		Unused
A12	AVSS	GROUND		Analog ground
A13	AVDD	SUPPLY		Analog supply
A14	CHIPID[6]	CMOS, pull-down	INPUT	Topological chip address
A15	MCLK_P	MLVDS	INPUT	Forwarded clock input
A16	MCLK_N	MLVDS	INPUT	Forwarded clock input
A17	DVSS	GROUND		Digital ground
A18	DVDD	SUPPLY		Digital supply
A19	PWELL	SUBSTRATE		Substrate bias, Matrix
A20	RESERVE_0	CMOS		Unused
A21	RST_N	CMOS, pull-up	INPUT	Global Hard Reset
A22	RESERVE_2	CMOS		Unused
A23	DVSS	GROUND		Digital ground
A24	DVDD	SUPPLY		Digital supply
A25	CHIPID[5]	CMOS, pull-down	INPUT	Topological chip address
A26	POR_DIS_N	CMOS, pull-up	INPUT	Disable Power-On Reset
A27	AVSS	GROUND		Analog ground
A28	AVDD	SUPPLY		Analog supply
A29	DCTRL_P	MLVDS	BIDIR	Differential Control port
A30	DCTRL_N	MLVDS	BIDIR	Differential Control port
A31	DVSS	GROUND		Digital ground
A32	DVDD	SUPPLY		Digital supply
A33	SUB	SUBSTRATE		Substrate bias, periphery
A34	AVSS	GROUND		Analog ground

A35	AVDD	SUPPLY		Analog supply
A36	SCO	CMOS		Unused
A37	CHIPID[4]	CMOS, pull-down	INPUT	Topological chip address
A38	DVSS	GROUND		Digital ground
A39	DCLK_P	MLVDS	BIDIR	Clock input. Clock forwarding output
A40	DCLK_N	MLVDS	BIDIR	Clock input. Clock forwarding output
A41	DVDD	SUPPLY		Digital supply
A42	PWELL	SUBSTRATE		Substrate bias, Matrix
A43	DVSS	GROUND		Digital ground
A44	DVDD	SUPPLY		Digital supply
A45	AVSS	GROUND		Analog ground
A46	AVDD	SUPPLY		Analog supply
A47	CHIPID[3]	CMOS, pull-down	INPUT	Topological chip address
A48	PVSS	GROUND		PLL ground
A49	PVDD	SUPPLY		PLL supply
A50	PVSS	GROUND		PLL ground
A51	PVDD	SUPPLY		PLL supply
A52	HSDATA_P	LVDS	OUTPUT	Serial Data Port
A53	HSDATA_N	LVDS	OUTPUT	Serial Data Port
A54	DVDD	SUPPLY		Digital supply
A55	CHIPID[2]	CMOS, pull-down	INPUT	Topological chip address
A56	DVSS	GROUND		Digital ground
A57	SCE	CMOS		Unused
A58	AVSS	GROUND		Analog ground
A59	AVDD	SUPPLY		Analog supply
A60	DVSS	GROUND		Digital ground
A61	DVDD	SUPPLY		Digital supply
A62	CTRL	CMOS, pull-up	BIDIR	Control Port (OB)
A63	DVSS	GROUND		Digital ground
A64	DVDD	SUPPLY		Digital supply
A65	DVSS	GROUND		Digital ground
A66	DVDD	SUPPLY		Digital supply
A67	DATA[3]	CMOS, pull-up	BIDIR	Data port
A68	DATA[7]	CMOS, pull-up	BIDIR	Data port
A69	DVSS	GROUND		Digital ground
A70	DVDD	SUPPLY		Digital supply
A71	CHIPID[1]	CMOS, pull-down	INPUT	Topological chip address
A72	DATA[2]	CMOS, pull-up	BIDIR	Data port
A73	DATA[6]	CMOS, pull-up	BIDIR	Data port
A74	DVSS	GROUND		Digital ground
A75	DVDD	SUPPLY		Digital supply
A76	DVSS	GROUND		Digital ground
A77	DATA[1]	CMOS, pull-up	BIDIR	Data port
A78	DATA[5]	CMOS, pull-up	BIDIR	Data port
A79	DVDD	SUPPLY		Digital supply
A80	AVSS	GROUND		Analog ground
A81	AVDD	SUPPLY		Analog supply
A82	DATA[0]	CMOS, pull-up	BIDIR	Data port
A83	DATA[4]	CMOS, pull-up	BIDIR	Data port
A84	SUB	SUBSTRATE		Substrate bias, periphery
A85	DVSS	GROUND		Digital ground
A86	DVDD	SUPPLY		Digital supply
A87	BUSY	CMOS, pull-up	BIDIR	Busy Flag
A88	CHIPID[0]	CMOS, pull-down	INPUT	Topological chip address
A89	AVSS	GROUND		Analog ground
A90	AVDD	SUPPLY		Analog supply
A91	PWELL	SUBSTRATE		Substrate bias, Matrix
A92	DACMONV	ANALOG		Voltage monitoring and overriding
A93	DACMONI	ANALOG		Current monitoring and overriding
A94	SUB	SUBSTRATE		Substrate bias, periphery

B00	SUB	SUBSTRATE		Substrate bias, periphery
B01	SUB	SUBSTRATE		Substrate bias, periphery
B02	MCLK_P	MLVDS	INPUT	Forwarded clock input
B03	MCLK_N	MLVDS	INPUT	Forwarded clock input
B04	RST_N	CMOS, pull-up	INPUT	Global Hard Reset
B05	POR_DIS_N	CMOS, pull-up	INPUT	Disable Power-On Reset
B06	DCTRL_P	MLVDS	BIDIR	Differential Control port
B07	DCTRL_N	MLVDS	BIDIR	Differential Control port
B08	DCLK_P	MLVDS	BIDIR	Clock input. Clock forwarding output
B09	DCLK_N	MLVDS	BIDIR	Clock input. Clock forwarding output
B10	HSDATA_P	LVDS	OUTPUT	Serial Data Port
B11	HSDATA_N	LVDS	OUTPUT	Serial Data Port
B12	CTRL	CMOS, pull-up	BIDIR	Control Port (OB)
B13	DATA[3]	CMOS, pull-up	BIDIR	Data port
B14	DATA[2]	CMOS, pull-up	BIDIR	Data port
B15	DATA[1]	CMOS, pull-up	BIDIR	Data port
B16	DATA[0]	CMOS, pull-up	BIDIR	Data port
B17	BUSY	CMOS, pull-up	BIDIR	Busy Flag
B18	DACMONI	ANALOG		Current monitoring and overriding
B19	DACMONV	ANALOG		Voltage monitoring and overriding
B20	SUB	SUBSTRATE		Substrate bias, periphery
C00	DVSS	GROUND		Digital ground
C01	CHIPID[6]	CMOS, pull-down	INPUT	Topological chip address
C02	DVSS	GROUND		Digital ground
C03	CHIPID[5]	CMOS, pull-down	INPUT	Topological chip address
C04	DVSS	GROUND		Digital ground
C05	CHIPID[4]	CMOS, pull-down	INPUT	Topological chip address
C06	PVSS	GROUND		PLL ground
C07	CHIPID[3]	CMOS, pull-down	INPUT	Topological chip address
C08	PVSS	GROUND		PLL ground
C09	CHIPID[2]	CMOS, pull-down	INPUT	Topological chip address
C10	DVSS	GROUND		Digital ground
C11	CHIPID[1]	CMOS, pull-down	INPUT	Topological chip address
C12	DVSS	GROUND		Digital ground
C13	CHIPID[0]	CMOS, pull-down	INPUT	Topological chip address
C14	DVSS	GROUND		Digital ground
D00	DVDD	SUPPLY		Digital supply
D01	CHIPID[6]	CMOS, pull-down	INPUT	Topological chip address
D02	DVDD	SUPPLY		Digital supply
D03	CHIPID[5]	CMOS, pull-down	INPUT	Topological chip address
D04	DVDD	SUPPLY		Digital supply
D05	CHIPID[4]	CMOS, pull-down	INPUT	Topological chip address
D06	PVDD	SUPPLY		PLL supply
D07	CHIPID[3]	CMOS, pull-down	INPUT	Topological chip address
D08	PVDD	SUPPLY		PLL supply
D09	CHIPID[2]	CMOS, pull-down	INPUT	Topological chip address
D10	DVDD	SUPPLY		Digital supply
D11	CHIPID[1]	CMOS, pull-down	INPUT	Topological chip address
D12	DVDD	SUPPLY		Digital supply
D13	CHIPID[0]	CMOS, pull-down	INPUT	Topological chip address
D14	DVDD	SUPPLY		Digital supply
E00	AVSS	GROUND		Analog ground
E01	AVSS	GROUND		Analog ground
E02	AVSS	GROUND		Analog ground
E03	AVSS	GROUND		Analog ground
E04	AVSS	GROUND		Analog ground
E05	AVSS	GROUND		Analog ground
E06	AVSS	GROUND		Analog ground

E07	AVSS	GROUND	Analog ground
F00	AVDD	SUPPLY	Analog supply
F01	AVDD	SUPPLY	Analog supply
F02	AVDD	SUPPLY	Analog supply
F03	AVDD	SUPPLY	Analog supply
F04	AVDD	SUPPLY	Analog supply
F05	AVDD	SUPPLY	Analog supply
F06	AVDD	SUPPLY	Analog supply
F07	AVDD	SUPPLY	Analog supply
G00	PWELL	SUBSTRATE	Substrate bias, Matrix
G01	SUB	SUBSTRATE	Substrate bias, periphery
G02	PWELL	SUBSTRATE	Substrate bias, Matrix
G03	SUB	SUBSTRATE	Substrate bias, periphery
G04	PWELL	SUBSTRATE	Substrate bias, Matrix
G05	SUB	SUBSTRATE	Substrate bias, periphery
G06	PWELL	SUBSTRATE	Substrate bias, Matrix

Table 2.7: Coordinates of the center points of the pads.

Pad Id	Net	Pad Geometry	x [μm]	y [μm]
A00	PWELL	A	607.62	66.8
A01	AVSS	A	827.62	66.8
A02	SUB	A	1047.62	66.8
A03	AVDD	A	1267.62	66.8
A04	DVSS	A	1487.62	66.8
A05	DVDD	A	1707.62	66.8
A06	SUB	A	2147.62	66.8
A07	AVSS	A	2367.62	66.8
A08	AVDD	A	2587.62	66.8
A09	DVSS	A	2807.62	66.8
A10	DVDD	A	3027.62	66.8
A11	SCI	A	3247.62	66.8
A12	AVSS	A	3467.62	66.8
A13	AVDD	A	3687.62	66.8
A14	CHIPID[6]	A	3907.62	66.8
A15	MCLK_P	A	4797.62	62.755
A16	MCLK_N	A	5017.62	62.755
A17	DVSS	A	5667.62	66.8
A18	DVDD	A	5887.62	66.8
A19	PWELL	A	6107.62	66.8
A20	RESERVE_0	A	6327.62	66.8
A21	RST_N	A	6547.62	66.8
A22	RESERVE_2	A	6767.62	66.8
A23	DVSS	A	6987.62	66.8
A24	DVDD	A	7207.62	66.8
A25	CHIPID[5]	A	7427.62	66.8
A26	POR_DIS_N	A	7647.62	66.8
A27	AVSS	A	8087.62	66.8
A28	AVDD	A	8307.62	66.8
A29	DCTRL_P	A	9197.62	62.755
A30	DCTRL_N	A	9417.62	62.755
A31	DVSS	A	10067.62	66.8
A32	DVDD	A	10287.62	66.8
A33	SUB	A	10507.62	66.8
A34	AVSS	A	10727.62	66.8
A35	AVDD	A	10947.62	66.8
A36	SCO	A	11167.62	66.8
A37	CHIPID[4]	A	11387.62	66.8

A38	DVSS	A	11607.62	66.8
A39	DCLK_P	A	12497.62	62.755
A40	DCLK_N	A	12717.62	62.755
A41	DVDD	A	13367.62	66.8
A42	PWELL	A	13587.62	66.8
A43	DVSS	A	13807.62	66.8
A44	DVDD	A	14027.62	66.8
A45	AVSS	A	14247.62	66.8
A46	AVDD	A	14467.62	66.8
A47	CHIPID[3]	A	14687.62	66.8
A48	PVSS	A	14907.62	66.8
A49	PVDD	A	15127.62	66.8
A50	PVSS	A	15347.62	66.8
A51	PVDD	A	15567.62	66.8
A52	HSDATA_P	A	17325.355	61.82
A53	HSDATA_N	A	17545.355	61.82
A54	DVDD	A	18427.62	66.8
A55	CHIPID[2]	A	18647.62	66.8
A56	DVSS	A	18867.62	66.8
A57	SCE	A	19087.62	66.8
A58	AVSS	A	19307.62	66.8
A59	AVDD	A	19527.62	66.8
A60	DVSS	A	19747.62	66.8
A61	DVDD	A	19967.62	66.8
A62	CTRL	A	20187.62	66.8
A63	DVSS	A	20407.62	66.8
A64	DVDD	A	20627.62	66.8
A65	DVSS	A	20847.62	66.8
A66	DVDD	A	21067.62	66.8
A67	DATA[3]	A	21287.62	66.8
A68	DATA[7]	A	21507.62	66.8
A69	DVSS	A	21727.62	66.8
A70	DVDD	A	21947.62	66.8
A71	CHIPID[1]	A	22167.62	66.8
A72	DATA[2]	A	22387.62	66.8
A73	DATA[6]	A	22607.62	66.8
A74	DVSS	A	22827.62	66.8
A75	DVDD	A	23047.62	66.8
A76	DVSS	A	23267.62	66.8
A77	DATA[1]	A	23487.62	66.8
A78	DATA[5]	A	23707.62	66.8
A79	DVDD	A	23927.62	66.8
A80	AVSS	A	24147.62	66.8
A81	AVDD	A	24367.62	66.8
A82	DATA[0]	A	24587.62	66.8
A83	DATA[4]	A	24807.62	66.8
A84	SUB	A	25027.62	66.8
A85	DVSS	A	25247.62	66.8
A86	DVDD	A	25467.62	66.8
A87	BUSY	A	25687.62	66.8
A88	CHIPID[0]	A	25907.62	66.8
A89	AVSS	A	26127.62	66.8
A90	AVDD	A	26347.62	66.8
A91	PWELL	A	26567.62	66.8
A92	DACMONV	A	26797.62	66.8
A93	DACMONI	A	27897.62	66.8
A94	SUB	A	29627.62	66.8
B00	SUB	B	1057.62	525
B01	SUB	B	2157.62	525
B02	MCLK_P	B	4357.62	525

B03	MCLK_N	B	5457.62	525
B04	RST_N	B	6557.62	525
B05	POR_DIS_N	B	7657.62	525
B06	DCTRL_P	B	8757.62	525
B07	DCTRL_N	B	9857.62	525
B08	DCLK_P	B	12057.62	525
B09	DCLK_N	B	13157.62	525
B10	HSDATA_P	B	16897.62	525
B11	HSDATA_N	B	17997.62	525
B12	CTRL	B	20197.62	525
B13	DATA[3]	B	21297.62	525
B14	DATA[2]	B	22397.62	525
B15	DATA[1]	B	23497.62	525
B16	DATA[0]	B	24597.62	525
B17	BUSY	B	25697.62	525
B18	DACMONI	B	26797.62	525
B19	DACMONV	B	27897.62	525
B20	SUB	B	28997.62	525
C00	DVSS	B	2105.16	7890.88
C01	CHIPID[6]	B	3947.28	7890.88
C02	DVSS	B	5789.4	7890.88
C03	CHIPID[5]	B	7631.52	7890.88
C04	DVSS	B	9473.64	7890.88
C05	CHIPID[4]	B	11315.76	7890.88
C06	PVSS	B	13157.88	7890.88
C07	CHIPID[3]	B	15000	7890.88
C08	PVSS	B	16842.12	7890.88
C09	CHIPID[2]	B	18684.24	7890.88
C10	DVSS	B	20526.36	7890.88
C11	CHIPID[1]	B	22368.48	7890.88
C12	DVSS	B	24210.6	7890.88
C13	CHIPID[0]	B	26052.72	7890.88
C14	DVSS	B	27894.84	7890.88
D00	DVDD	B	2105.16	9906.88
D01	CHIPID[6]	B	3947.28	9906.88
D02	DVDD	B	5789.4	9906.88
D03	CHIPID[5]	B	7631.52	9906.88
D04	DVDD	B	9473.64	9906.88
D05	CHIPID[4]	B	11315.76	9906.88
D06	PVDD	B	13157.88	9906.88
D07	CHIPID[3]	B	15000	9906.88
D08	PVDD	B	16842.12	9906.88
D09	CHIPID[2]	B	18684.24	9906.88
D10	DVDD	B	20526.36	9906.88
D11	CHIPID[1]	B	22368.48	9906.88
D12	DVDD	B	24210.6	9906.88
D13	CHIPID[0]	B	26052.72	9906.88
D14	DVDD	B	27894.84	9906.88
E00	AVSS	B	2105.16	11465.92
E01	AVSS	B	5789.4	11465.92
E02	AVSS	B	9473.64	11465.92
E03	AVSS	B	13157.88	11465.92
E04	AVSS	B	16842.12	11465.92
E05	AVSS	B	20526.36	11465.92
E06	AVSS	B	24210.6	11465.92
E07	AVSS	B	27894.84	11465.92
F00	AVDD	B	2105.16	13723.84

F01	AVDD	B	5789.4	13723.84
F02	AVDD	B	9473.64	13723.84
F03	AVDD	B	13157.88	13723.84
F04	AVDD	B	16842.12	13723.84
F05	AVDD	B	20526.36	13723.84
F06	AVDD	B	24210.6	13723.84
F07	AVDD	B	27894.84	13723.84
G00	PWELL	B	3947.28	14395.84
G01	SUB	B	7631.52	14395.84
G02	PWELL	B	11315.76	14395.84
G03	SUB	B	15000	14395.84
G04	PWELL	B	18684.24	14395.84
G05	SUB	B	22368.48	14395.84
G06	PWELL	B	26052.72	14395.84

Table 2.8: Coordinates of the center points of the alignment markers.

Marker	Location	x [μm]	y [μm]
AM-TL	Top Left	175.32	14852.8
AM-TR	Top Right	29824.68	14852.8
AM-BL	Bottom Left	175.32	76.8
AM-BR	Bottom Right	29824.68	76.8

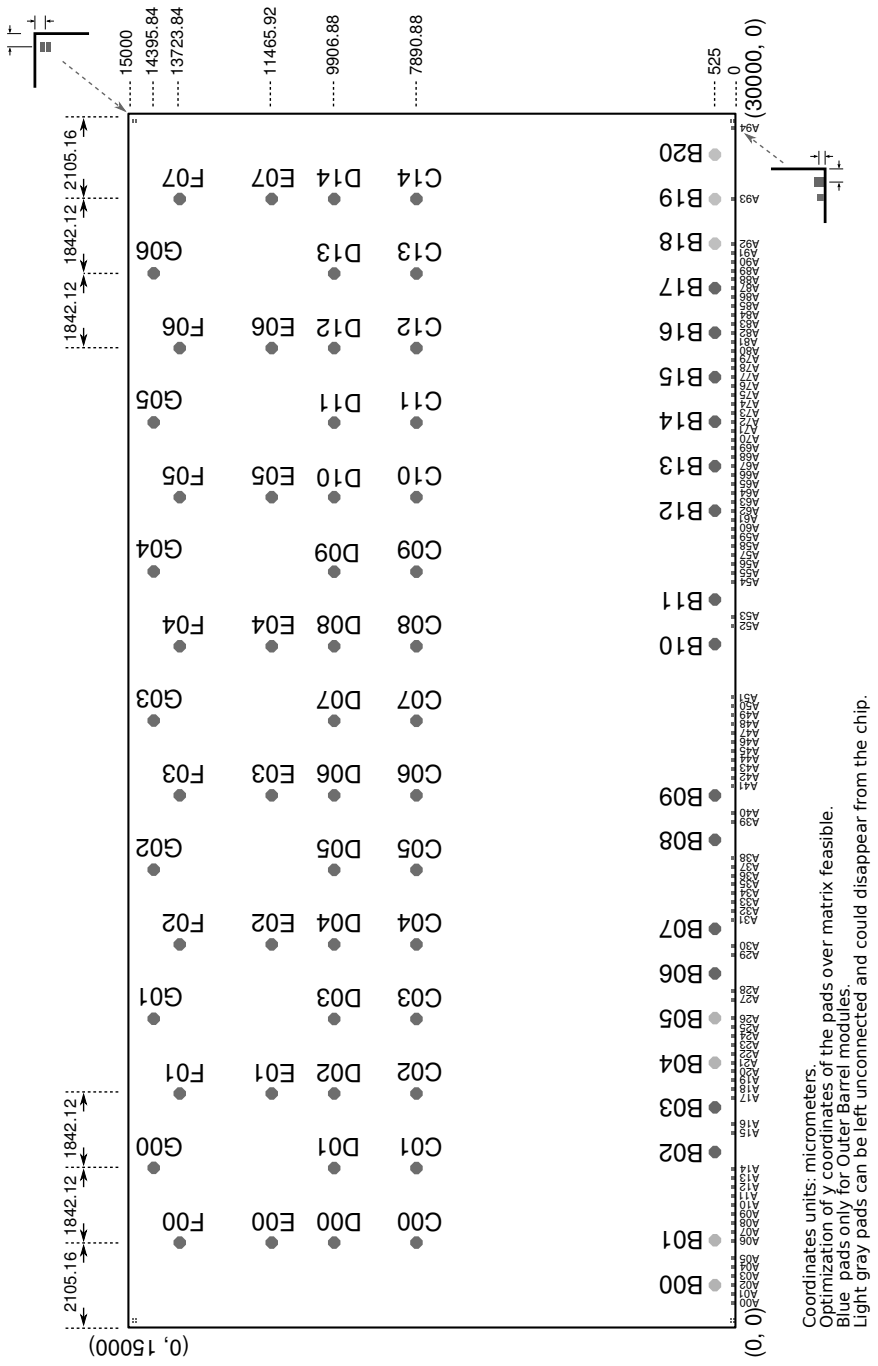

Figure 2.4: ALPIDE pad naming convention.

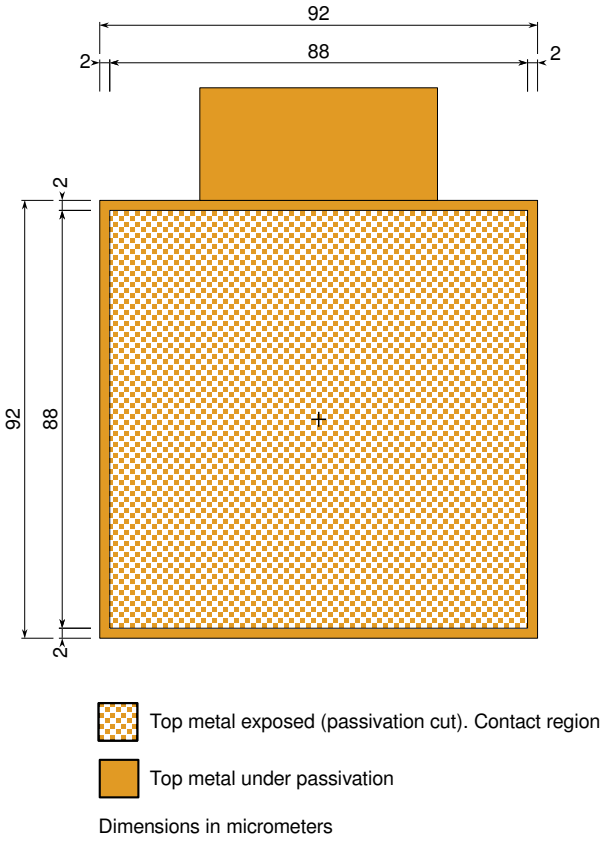

Figure 2.5: Geometry of type A pad.

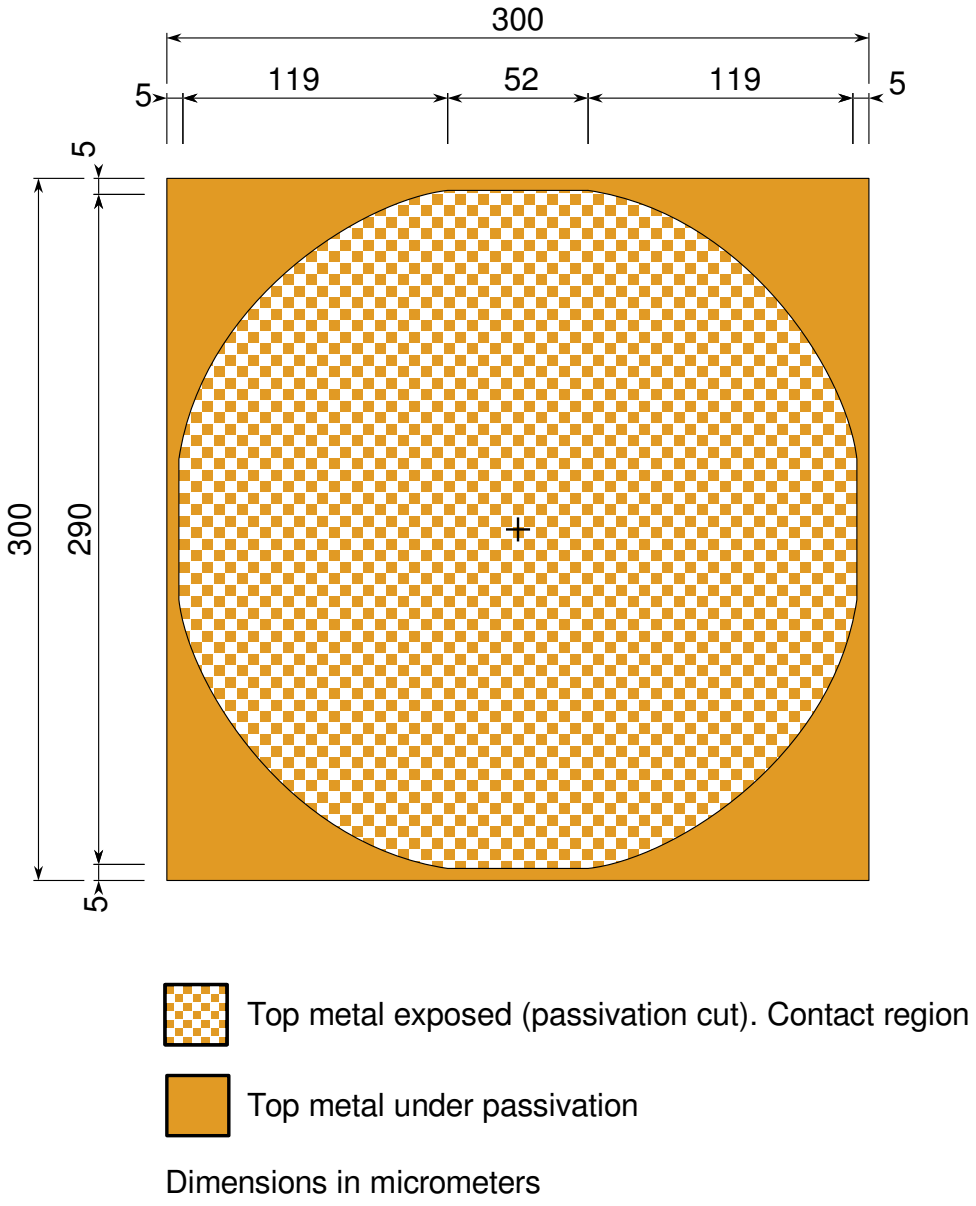

Figure 2.6: Geometry of type B pad.

3 User manual

This chapter shall outline the operation of the chip as far as the users of the chip are interested. Programming options, control options, operating mode, data formats should be summarized.

Employ present tense, terse and brief factual statements. Do NOT use narrative style; no stylish prose; no remarks or comments; preferably NO historical remarks

Skeleton of User Guide sections to be reviewed or written

- Address space, registers and purposes (Davide)
- Triggering readout, FROMU modes (Svet)
- Data formats, readout (Svet)
- Pixel pulsing and masking configuration procedures (Svet, Davide)
- Digital and analog pulsing commands (Svet, Davide)
- Chip initialization procedure, quick-start guide (Svet, Davide)
- DTU Logic test features, user guide (Gianluca)
- Setting and monitoring of DACs (Revision by Thanu)
- User guide for the ADC, including temp sens (Christophe, Fabrice)
- Shadow registers diagnostic feature, user guide (Davide)

Folder structure: set of .tex files, top level file is *ALPIDE-operations-manual.tex*. All others included from top-level.

ILLUSTRATIONS: all illustrations and figures should be inserted in pdf format. Code templates for illustrations already available in the .tex sources. All illustrations shal originate from a vector graphics original file.

GENERATION OF PDF: the source files of this manual shall compile with *pdflatex*, command syntax: pdflatex ALPIDE-operations-manual.tex

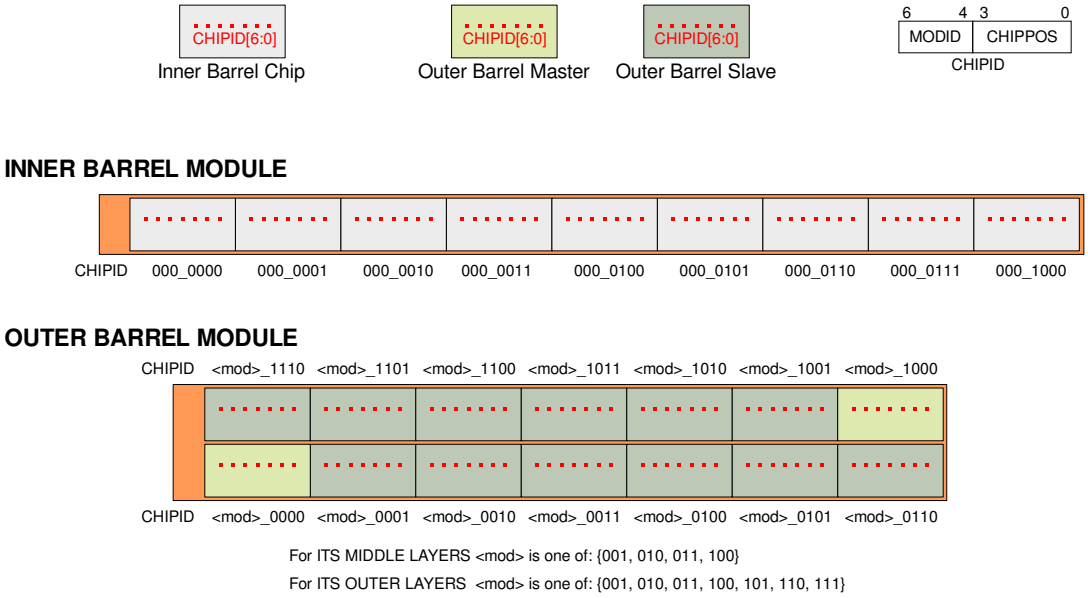

Figure 3.1: Illustration of chip identification and geographical address allocation. Default assignments of CHIPID values on one Inner Barrel Module and on a generic Outer Barrel Module.

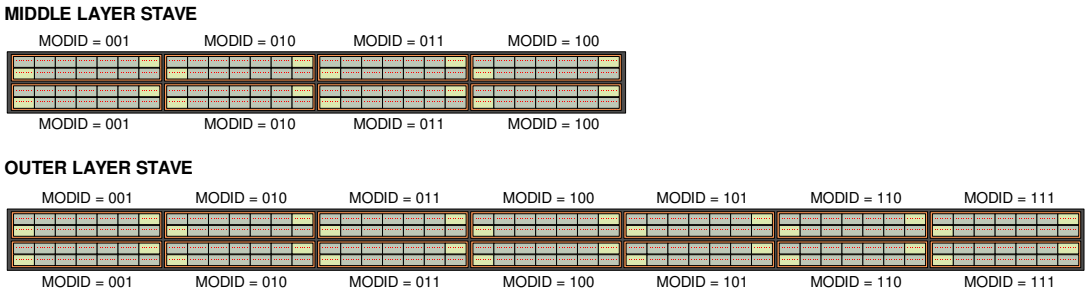

Figure 3.2: Illustration of chip identification and geographical address allocation. Default assignments of Module Identifier fields for the Middle Layer Stave and Outer Layer Stave.

3.1 Control interface and protocol

3.1.1 Chip identification and geographical address allocation

The chip can operate in three different roles in the ALICE ITS Upgrade application: Inner Barrel Chip, Outer Barrel Module Master and Outer Barrel Module Slave. The selection of the operating mode is based on the input applied to the **CHIPID[6:0]** chip port. This port selects the operating mode and also provides an address to the chip for the slow control transactions. The pads of this port shall be tied to digital supply (DVDD) to set the corresponding bit to 1. The pads have internal pull-down resistors. Leaving them unconnected is equivalent to shorting them to digital ground (DVSS) thus establishing a value of 0 for the corresponding bit.

The three bits **CHIPID[6:4]** constitute a **Module Identifier** field. The remaining bits **CHIPID[3:0]** act as identifiers of the position and role inside a module. The reference specification for the allocation of the values of CHIPID to the chips on the modules is illustrated in Fig. 3.1 and Fig. 3.2.

The *Module Identifier* field shall be **all zeros** for Inner Barrel chips. Chips with the three bits CHIPID[6:4] all set to zero identify and configure themselves as Inner Barrel Chips. The

remaining bits **CHIPID[3:0]** shall be a position dependent binary identifier and can have any of the values from 0 up to 14 (binary *b1110*). The binary code *b1111* **shall not be used** for CHIPID[3:0], since it is reserved for broadcast addressing.

The *Module Identifier* field shall contain at least one non-zero bit to configure the chip to operate in one of the Outer Barrel roles, i.e. CHIPID[6:4] *must not* be *b000*. CHIPID[6:4] is intended to be a module index, a unique value for all the fourteen chips of a specific module on a half-stave. CHIPID[6:4] can be one of *b001*, *b010*, *b011*, *b100* for modules on Middle Layers staves. CHIPID[6:4] can be one of *b001*, *b010*, *b011*, *b100*, *b101*, *b110*,*b111* for modules on Outer Layers staves. The four bits **CHIPID[3:0]** are also meant to specify the geographical position of the chip on the Outer Barrel Module and its role. There are two rows of seven chips on an Outer Barrel Module. Bit CHIPID[3] identifies in which of the two rows the chip is located. The remaining three bits **CHIPID[2:0]** select the operating mode of Outer Barrel Master if they are all set to zero, *b000*. Otherwise the chip behaves as an Outer Barrel Slave. Bits CHIPID[2:0] **must not be** binary *b111*, since this is reserved for broadcast addressing.

3.1.2 Control interfaces

The slow control interface serve two purposes:

1. provide write and read access to internal registers, commands, configuration and memories
2. distribute trigger commands or broadcast synchronous signals

The ALPIDE chip has two ports to implement the slow control functionalities: a differential DCTRL port and a single-ended CTRL port. The port that is actually functional depends on the operating scenario. In Inner Barrel Chip role only the differential DCTRL port is used. In Outer Barrel Module Master role both ports are operated. In Outer Barrel Module Slave role only the single ended CTRL port is used. The slow control interface and the ports have been designed to implement a hierarchical control bus topology with multi-point connections of chips on the same electrical line. The reader can refer to appendices B and C for further details and illustrations on the items of this section.

The nine (9) chips on an Inner Barrel module are directly connected to a shared control differential line using the DCTRL port. The Inner Barrel control bus is entirely based on differential signaling and it has multipoint topology.

On Outer Barrel Staves, the control bus is implemented with a hierarchical structure. Every Module Master chip is connected with other Master chips on the same half-stave by a differential shared bus with multi-point topology. The differential line crosses the module boundaries and can connect 4 (Middle Layer Stave) or 7 (Outer Layer Stave) Module Master chips on the row of chips located on the same row along the z axis. Each Outer Barrel Module Master chip acts as a slow control *hub* and relays the control transactions to six Outer Barrel Module Slave chips that are connected in a multi-point shared line topology with the Master. The bus segment local to the Outer Barrel Module operates with single-ended signaling.

Inner Barrel modules and Outer Barrel modules present to the off-detector hardware fully equivalent control interfaces, physically appearing as a bi-directional differential port. The control interface supports *bi-directional, half-duplex* data exchanges. The signaling on the control buses is serial and synchronous with the system clock (nominal 40.08 MHz, LHC clock) that is distributed through a hierarchical clock tree. The slow control *transactions* are governed by the off-detector hardware initiating all type of messaging on the control bus. All chips have clocks derived from the same system clock and continuosly sample the incoming serial control stream, decoding the transactions on the bus. The deserialization and the decoding of the control messages are executed at corresponding clock edges in all chips.

The ALPIDE control interface has been designed with support of DC balanced signaling on the DCTRL port for applications that require or can benefit of AC coupling of the DCTRL line. This is obtained using Manchester encoding for the serial characters transmitted by the

chips, following the IEEE8 802.3 convention for the bi-phase symbols. The transmission of control replyies on th DCTRL line using Manchester coding is enabled by deafult (post reset value) but can be disabled in the chip configuration space. The off-detector electronics can also signal using Manchester encoding, this being transparent to on-chip circuits. The chips sample the control bus on the clock rising edges, therefore it is the electrical value seen on the bus at those sampling edges that is used by the logic of the chip control module.

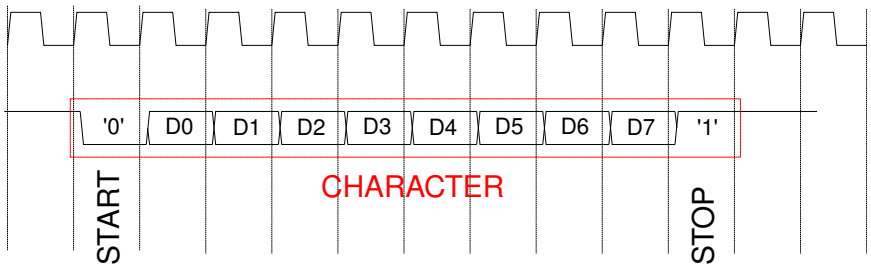

Figure 3.3: Format of a single character exchanged on the control bus.

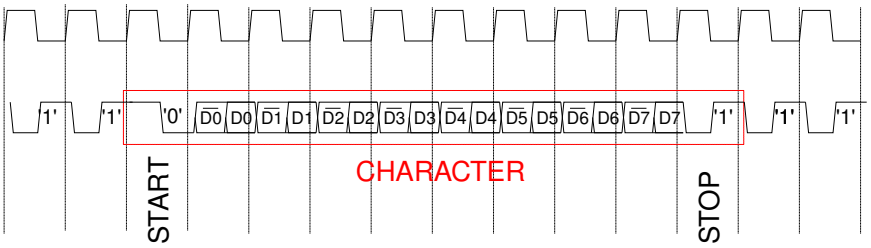

Figure 3.4: Format of a single character exchanged on the DCTRL bus with Manchester coding enabled (default).

3.1.3 Control transactions format

The transactions on the Control Bus are constituted of sequences of 10-bit wide *characters*. A character (Fig. 3.3) corresponds to the exchange of a single byte and it is made by a leading start bit (logic 0), 8-bit wide arbitrary payload and a trailing stop bit (logic 1). The serial transmission convention is Less Significant Bit first. Fig. 3.4 illustrates the transmission of reply characters on the DCTRL line when Manchester signaling is enabled (default setting).

The idle state of the physical lines between the characters is logic 1. Bus idle gaps are allowed between characters transmitted by the bus master. The minimum length of the idle gap between characters is 0 clock cycles (start bit immediately follows end bit of previous characters), the maximum length is 42 cycles.

The valid control transactions begin with pre-defined **OPCODE** characters, listed in Table 3.1.3. There is a Hamming distance of 4 bits between any two opcodes. This is meant to prevent the internal execution of transactions in case of bit errors on the transmission. There are broadcast type opcodes, to which all chips react executing an internal action. Specific opcodes are reserved for the triggering. These are similar to broadcast opcodes but the internal decoding latency is reduced. Longer write and read transactions are prefix with dedicated opcodes.

There are five types of valid transactions, as illustrated in Fig. 3.5:

- **BROADCAST COMMAND**: a single 10-bit character message (one of GRST, PRST, PULSE, BCRST, RORST); all chips react (e.g. Resets)

- **TRIGGER COMMAND**: a single character message (TRIGGER opcode), all chips react. The decoding of the trigger commands is internally executed at the deserializing stage to minimize trigger latency.

- **UNICAST WRITE**: six (6) characters message. A 32b data word is written to an internal register of one specific chip. It begins with a WRITE OPCODE character, followed by a CHIPID character identifying the target chip on the bus. The internal chip address is specified with the subsequent two characters (REG_ADDR) and finally the DATA payload is transferred with the last two characters.

- **MULTICAST WRITE**: six (6) characters message. A 32b data word is written siultaneously to an internal register of a set chips. It has the same format of a UNICAST WRITE with the expection that a MULTICAST ID chip identifier is used for the CHIPID character.

- **READ**: four (4) + three (3) characters message. The first four characters are driven by the bus master to initiate the transaction (READ OPCODE), target the chip (CHIPID) and the chip internal address (REG_ADDR). Then a bus turnaround phase is initiated and the target chip (if present on the bus) transmits a response with its own CHIPID (acknowledge) followed by two DATA characters payload. The response characters are tipycally transmitted one after the other without any idle gap between the stop and start bits of consecutive characters.

The BROADCAST COMMAND transactions are shortcuts for MULTICAST WRITE transactions targeting the chip command register (see also section **??**).

The MULTICAST WRITE transactions are based on reserved values for the chip identification characters. These are identified as **MULTICAST ID** control addresses:

- **GLOBAL BROADCAST** is the binary string **b00001111**. Any chip listening to a write transaction with this byte on the chip identification character reacts and internally executes the write transaction.

- **Outer Barrel MULTICASTs**: binary code {*b0*, modid[2:0], master_id, *b111*}. This enables addressing 7 chips on a specific outer barrel module identified by the 3 bits *modid* and connected to the OB master with CHIPD[3] equal to bit *master_id*.

Opcode	Hex value	Purpose
TRIGGER	8'hB1	Trigger command
TRIGGER	8'h55	Trigger command
TRIGGER	8'hC9	Trigger command
TRIGGER	8'h2D	Trigger command
GRST	8'hD2	Chip global reset
PRST	8'hE4	Pixel matrix reset
PULSE	8'h78	Pixel matrix pulse
BCRST	8'h36	Bunch Counter reset
RORST	8'h63	Readout (RRU/TRU/DMU) reset
WROP	8'h9C	Start Unicast or Multicast Write
RDOP	8'h4E	Start Unicast Read

Table 3.1: Valid opcodes of control transactions

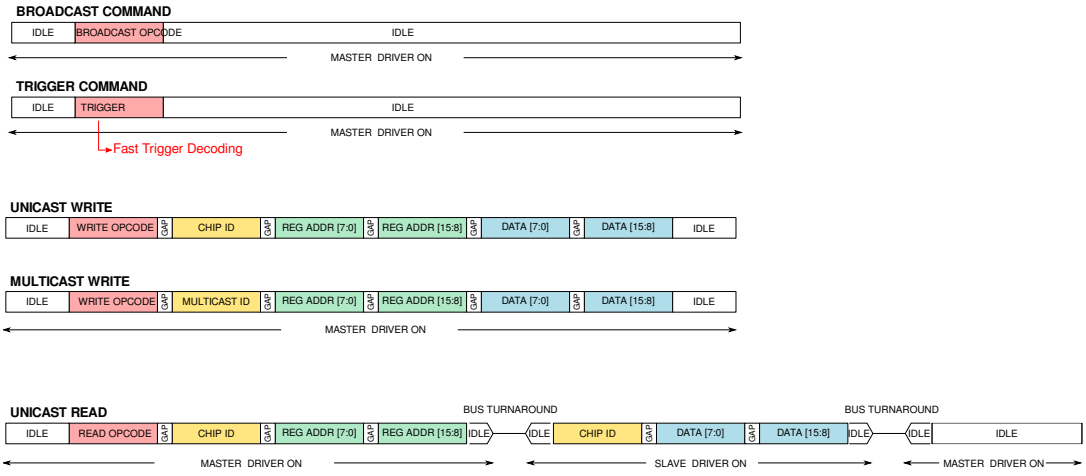

Figure 3.5: Format of valid transactions on the control bus.

3.1.4 Bus turnaround and reply phase of read control transactions

The reply of bus slaves in Read transactions is strictly specified and comply with the timing specification illustrated in Fig. 3.6.

The Bus Master must release the electrical drive of the bus line for a predefined number of clock cycles (50). This interval is used by the addressed chip (if any) to reply with its own CHIPID followed by two consecutive DATA characters. The same specification of bus turnaround timing applies to: (a) the differential bus connecting a Readout Unit and Inner Chips, (b) the differential bus connecting a Readout Unit and OB Masters and (c) the single ended shared bus connecting one Outer Barrel Master chip with its Slave chips.

The bus turnaround and the reply phase can be divided in distinct phases separated by notable clock edges.

1. Clock edge 0, reference clock edge. The bus master completes the transmission of stop (mark) bit of ADDRH character. Beginning of *Master Idle Phase* with duration of 5 (five) clock periods. Purpose: allow bus slaves to complete sampling of the delayed message. Bus slaves stop sampling the line during this phase ignoring the state of the line onwards.

2. 5^{th} clock edge, the bus master disables the line driver. Beginning of the *First Turnaround Phase*: duration 5 cycles. Purpose: allow margin to prevent line contention and a period in which the line electrical state is ignored by both bus masters and bus slaves. The target bus slave shall start actively driving the line (with Idle) during this phase.

3. 10^{th} clock edge, the bus master starts sampling the line at this edge (included). The target shall already be driving actively (with Idle) the line at this time. It is the beginning of the *Slave Idle Phase*: duration 5 cycles. Purpose: allow the line receiver to sense the Idle and signaling phase (if Manchester coding is used by the Target).

4. 15^{th} clock edge, the responding slave shall keep driving idle up to this edge. This edge can be the launching edge of a start bit. Beginning of the *Reply Phase*: duration 35 cycles. The responding slave transmits the three reply characters (min 30 cycles needed) foreseen for the Read Transaction.

5. 50^{th} clock edge, the bus master samples the line for the last edge. End of Reply Phase, beginning of second *Slave Idle Phase*: duration 5 cycles. The responding slave shall drive the line Idle during the Slave Idle Phase. The bus master stops sampling the line during the Slave Idle Phase.

6. 55^{th} clock edge, beginning of the *Second Turnaround Phase*, duration 5 cycles. The responding slave stops driving actively the line after this edge. The bus master starts driving the line actively (with Idle) from during the Second Turnaround phase.
7. 60^{th} clock edge, the bus slaves shall start sampling the line at this edge (included). The line shall be driven Idle by the bus master. Marks the beginning of the *Second Master Idle phase*: duration 5 cycles. The bus master keeps driving Idle during the Second Master Idle phase.
8. 65^{th} clock edge, completion of Read Transaction

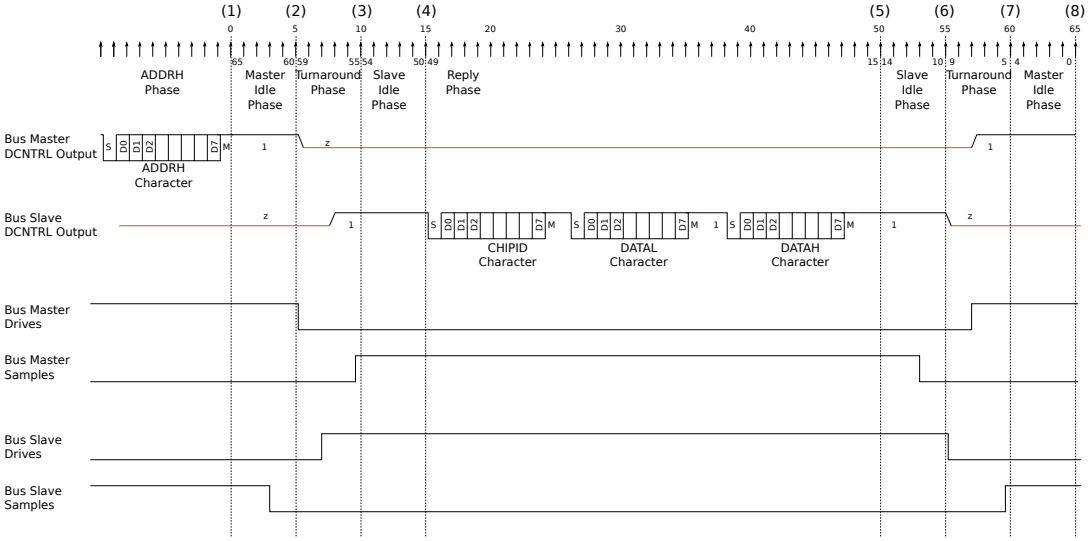

Figure 3.6: Timing diagram of the reply phase of a Read transaction including turnaroud phases. Signaling is represented as seen on the differential line at the output of the bus master (off-detector electronics).

3.2 Data Transmission Unit and Test Logic

To be edited by Gianluca

3.3 Operation of the ADC

To be edited by Fabrice, Christophe

3.4 Usage of shadow registers

To be edited by Davide

4 Principles of Operation

This chapter shall describe with enough detail the operation of the chip and the structure and design of all the internal circuits. This targets the internal users that have to test the chip or build support systems.

Employ present tense, terse and brief factual statements. Do NOT use narrative style; no stylish prose; no remarks or comments; preferably NO historical remarks

Skeleton of itemsto be reviewed or written

- Review Analog section of the pixel (Thanu)
- Review description of digital section (Hung)
- Review Analog Bias, make DAC naming uniform, refer to name of registers (Thanu)

4.1 Pixel circuits. Analog Front-End and Digital Pixel

4.1.1 Analog Front-End

Commented this section on the pixel, needs adaptation for the ALPIDE chip

4.1.2 Digital Pixel

The digital section of the pixel is illustrated in Figure 4.1. The corresponding signals are listed in Table 4.1. The pixel features three State Registers. Each State Register is a Set-Reset Latch that can keep the hit information. The State Register is normally set by the front-end discriminated output PIX_OUT_B if the corresponding STROBE_B<2:0> is asserted simultaneously. It can also be set programmatically by the DPULSE signal (digital pulse functionality) if the corresponding STROBE_B<2:0> is asserted simultaneously. The State Register can be selected for read/reset by asserting the corresponding MEMSEL_B<2:0> bit. The selected State Register is reset either by a PIX_RESET pulse generated by the Priority Encoder during the readout, either by a global FLUSH_B signal. The State Register is sensitive to the falling edge of PIX_RESET and it is level sensitive with respect to the FLUSH_B input. The selected State Register output bit can be masked and the result is the output to the Priority Encoder (STATE signal). If no State Register is selected STATE is 0.

The logic provides two programmable functions: masking and pulsing. When control bit MASK_EN is set high, the STATE output is forced to 0, effectively masking the pixel otuput to the priority encoder. The low value provides normal functionality. The testing functionalities are enabled by setting PULSE_EN=1, disabled otherwise. DPULSE assertion allows for the pixel digital pulsing. This consists in forcing to logic high the hit latch (STATE_INT), bypassing the pixel front-end signal. This can be done asserting DPULSE. The analog testing consists in the injection of test charge in the input node through Cinj (160 aF nominal). The amplitude of the applied voltage pulse is defined by the difference between VPLSE_HIGH and VPLSE_LOW, both set in the DAC unit. Notice that the two edges of the pulse provoke the injection of two charge pulses of opposite polarities. The rising edge of APULSE corresponds to the discharge of the collection diode, in a manner equivalent to the passage of a charged particle. There are two D-latches to store the PULSE_EN and MASK_EN configuration bits. Notice that their values after power-on are undefined. Setting of these latches is done by the PIXCNFG_COLSEL, PIXCNFG_ROWREGPSEL, PIXCNFG_ROWREGMSEL, PIXCNFG_DATA lines, all driven by the periphery control circuitry. The addressing of the pixels for configuration is based on the simultaneous selection of a specific row and a specific

column. The simultaneous assertion of PIXCNFG_COLSEL and PIXCNFG_ROWREGMSEL pixel inputs selects the mask latch. The simultaneous assertion of PIXCNFG_COLSEL and PIXCNFG_ROWREGPSEL pixel inputs selects the pulse latch. PIXCNFG_DATA provides the value to be stored in the selected latch. There is no direct way to read back the values in the latches from the control interface.

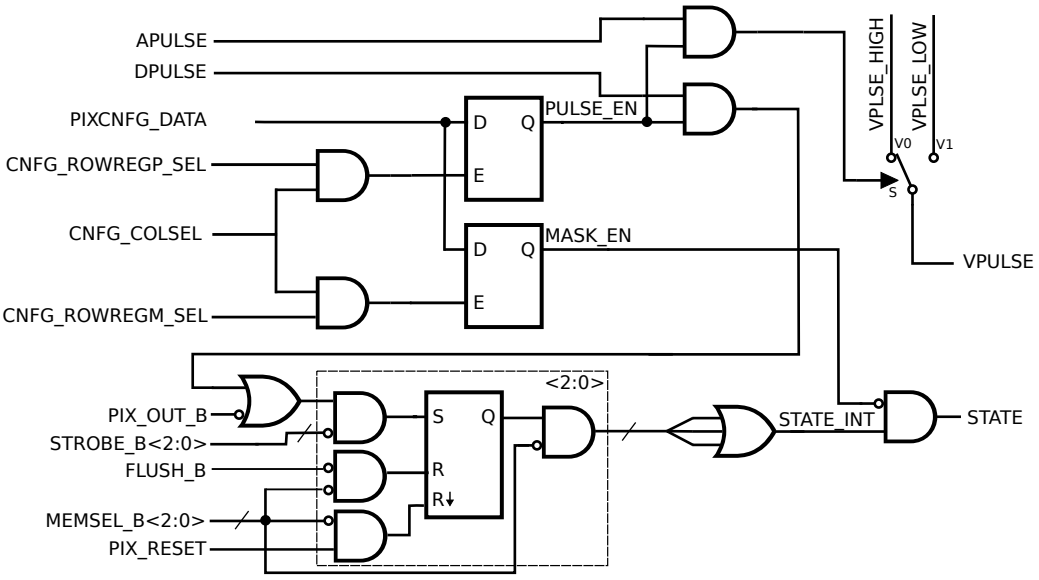

Figure 4.1: Functional diagram of the pixel logic

4.2 Priority Encoders and pixel indexing

Looking at the chip with the digital periphery on the bottom, the leftmost region is region 0 and the rightmost region is region 31 (see Figure 4.2).

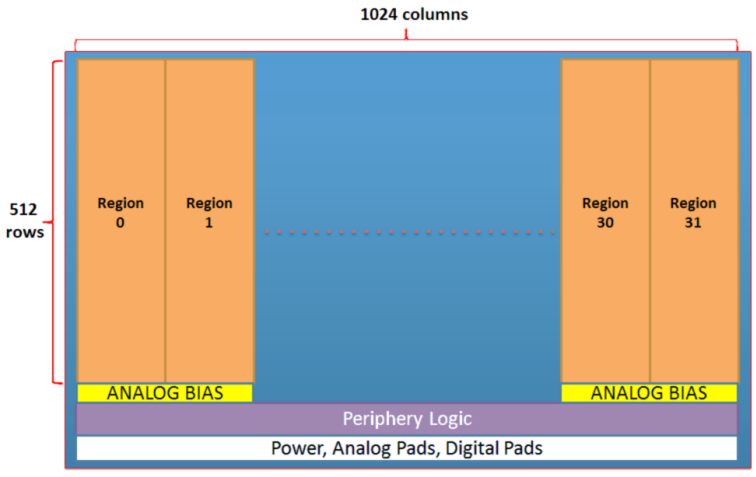

Figure 4.2: Region numbering

Each region contains 16 double columns. Double column 0 is the leftmost and double column 15 is the rightmost (see Figure 4.3).

The matrix of pixels is readout by an array of 512 Priority Encoder blocks. The pixels are arranged in double columns and the regions at the middle of each double column are occupied

	Signal	Description	Logic level
	APULSE	VPULSE voltage level selection if PULSE_EN = 1	Positive edge charge injection
	DPULSE	Digital Pulse if PULSE_EN = 1	Active high
	PIXCNFG_DATA	Configuration data	D-LATCH data line
	PIXCNFG_COLSEL	Column selection	Active high
	PIXCNFG_ROWREGPSEL	Row and Pulse reg. selection	Active high
	PIXCNFG_ROWREGMSEL	Row and Mask reg. selection	Active high
	PIX_OUT_B	Pixel front-end output	Active low
	STROBE_B<2:0>	Enable State register for hit acquisition	Active low
	MEMSEL_B<2:0>	Select State register for read and reset	Active low
	FLUSH_B	General reset of the selected the state register(s)	Active high
	PIX_RESET	Priority encoder reset of the selected register	Effective on falling edge
	VPLSE_HIGH	Analog pulse high level	Analog
	VPLSE_LOW	Analog pulse low level	Analog
	MASK_EN	State register mask enable	Active high
	STATE_INT	State register data	Active high
	VPULSE	Voltage step for test charge injection into pix_in net	$Q_{inj} = \Delta(\text{VPULSE}) \cdot 160$ aF
	STATE	State register value to priority encoder (if MASK_EN = 0)	Active high

Table 4.1: Signals of the pixel cell

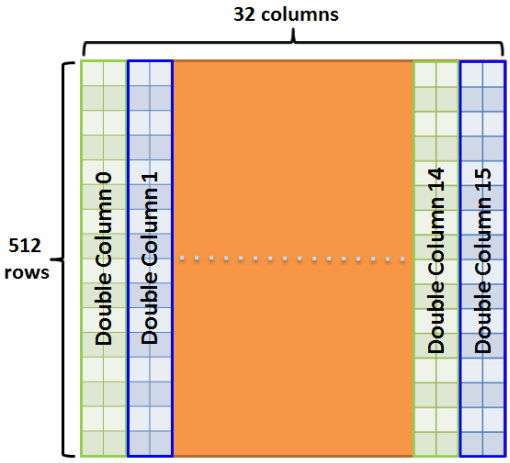

Figure 4.3: Double column numbering inside of a region

by the Priority Encoders. The indexing of the pixels in the readout data words is defined by the Priority Encoders. The indexing of the pixels in each double column is illustrated in Figure 4.4.

4.3 Analog bias and internal DACs

The pALPIDEfs chip has eleven internal DACs: six 8-bit voltage DACs and five 8-bit current DACs. These DACs are used to set the voltage and current biases required by the pixel front-end circuits. Table provides an overview of the specifications of the DACs. The DAC block has three operation modes:

1. Normal - the outputs of all DACs are connected directly to the pixel matrix.

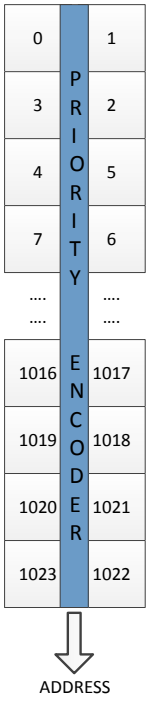

Figure 4.4: Indexing of pixels inside a double column provided by the Priority Encoders

2. Monitor - it is possible to select a voltage DAC and monitor its output on the DACMONV pad. It is also possible to select a current DAC and monitor its output on the DACMONI pad.

3. Override - it is possible to override the output of one selected voltage DAC by the DACMONV pad. It is possible to override the output of one selected current DAC by the DACMONI pad. It is also possible to override the internally generated IREF current that defines the LSB value of the current DACs.

The voltage DACs are based on a 256 stages resistive divider connected between the VREF pad and AVSS. Each resistor has a nominal value of 40 Ω, for a total resistance of 10.2 kΩ. This allows to generate voltage levels between AVSS and VREF (256-1)/256 with 8 bit resolution. The values of the voltage DAC setting registers are decoded and used to control arrays of analog switches connected between the 256 nodes of the resistor divider and the output pins of the DACs. The VCASN and VCASP outputs are directly applied to the matrix without any amplification or scaling. The VRESET, VPLSE_LOW and VPLSE_HIGH and VAUX outputs are buffered with unit gain followers. This causes an offset of about 370 mV and saturation for codes above about 200 for these DACs. The nominal voltage to apply to the VREF pad is 1.8 V (AVDD). Any external additional resistance between the VREF source and the pad decreases the maximum voltage reachable by the DACs. A low series resistance (< 100 Ω) should be guaranteed between the source and the pad. At the nominal bias value (VREF = 1.8 V) the current sunk by the VREF pad is ≈ 180 μA. The current DACs are implemented by repeating 256 times the same building unit that is a current source generating the current corresponding to the LSB. This is 1/256 of IREF, an internally generated reference current. IREF is nominally 10.24 μA, the LSB value is nominally 40 nA. The values of the current DACs setting registers are decoded and used to control the analog switches connecting the LSB sources in parallel into the output node of each DAC. The outputs of the current DACs are then scaled to appropriate levels before being applied to the matrix. The scaling factors

are given in Table . Monitoring and Overriding of the DACs It is possible to monitor the output of a selected voltage DAC using the DACMONV pad. The DACMONV pin should be monitored with a high input impedance circuit (Rin $>$ 1 MΩ). Only one voltage can be monitored at a given time. It is possible to monitor the output of a selected current DAC using the DACMONI pad loaded with a shunt resistor to AVSS. The recommended shunt resistance is 5 kΩ. Only one current can be monitored at a given time. The current on the shunt resistor is equal to ten times the output current of the selected DAC, upstream the scaling towards the pixels. It is possible to override a selected voltage DAC using the DACMONV pad. Once the functionality is activated a voltage between 0 and VREF needs to be applied to the DACMONV pad. This will feature high input impedance. The voltage applied to DACMONV goes directly to the pixel matrix. It is possible to override a selected current DAC using the DACMONI pad. Once the functionality is activated a current needs to be sourced from DACMONI as illustrated in Figure . This current is divided by 10 internally and this replaces the output of the DAC before the internal scaling towards the pixel matrix. The range of interest for the external overriding current is 0 to 200 μA, covering almost twice the internal nominal range. Finally the internal IREF current constituting the reference for all the current DACs can be overridden. In this case the current sourced by the DACMONI pad is divided by 11 before being used by the internal DACs. The configuration of the DAC block for monitoring or overriding and the selection of the DACs are done by the dedicated Current/Voltage Monitoring and

Appendices

Appendix A Application note. Chip and modules clocking schemes

Figure A.1 illustrates the clocking schemes supported by the chip.

The chip has two differential ports dedicated to the clock signals, DCLK and MCLK (section 2.2).

- The *receiver* of the DCLK port is always enabled.
- The internal clock used by the core circuits is always the signal received on the DCLK port.
- In the IB module scenario (left side of the figure), the chips receive the clock from an external circuit driving the multi-drop differential line connected to the DCLK ports.
- When the chip is configured to operate as an Outer Barrel Master (CHIPID[2:0]=3'b000), the *driver* of the DCLK port and the *receiver* of the MCLK port are enabled. The signal received on the MCLK port is internally buffered and forwarded to the driver of the DCLK port. This allows to implement a local regeneration of a clock signal and a local clock bus (LCLK) on a module.
- The line connected to the DCLK port of a chip configured as OB Master shall not be driven by any external circuit. The external clock shall be applied to the MCLK port of an OB Master chip.
- When the chip is configured to operate as an Outer Barrel Master or it is configured as an Outer Barrel Slave with the specific value of the *chipid* field CHIPID[3:0]=4'b0110=d6, an on-chip termination resistor (100 Ω) gets activated on the DCLK port. This is to remove the need of connecting termination resistors on the LCKL local clock bus.
- The *driver* of the MCLK port is never enabled.

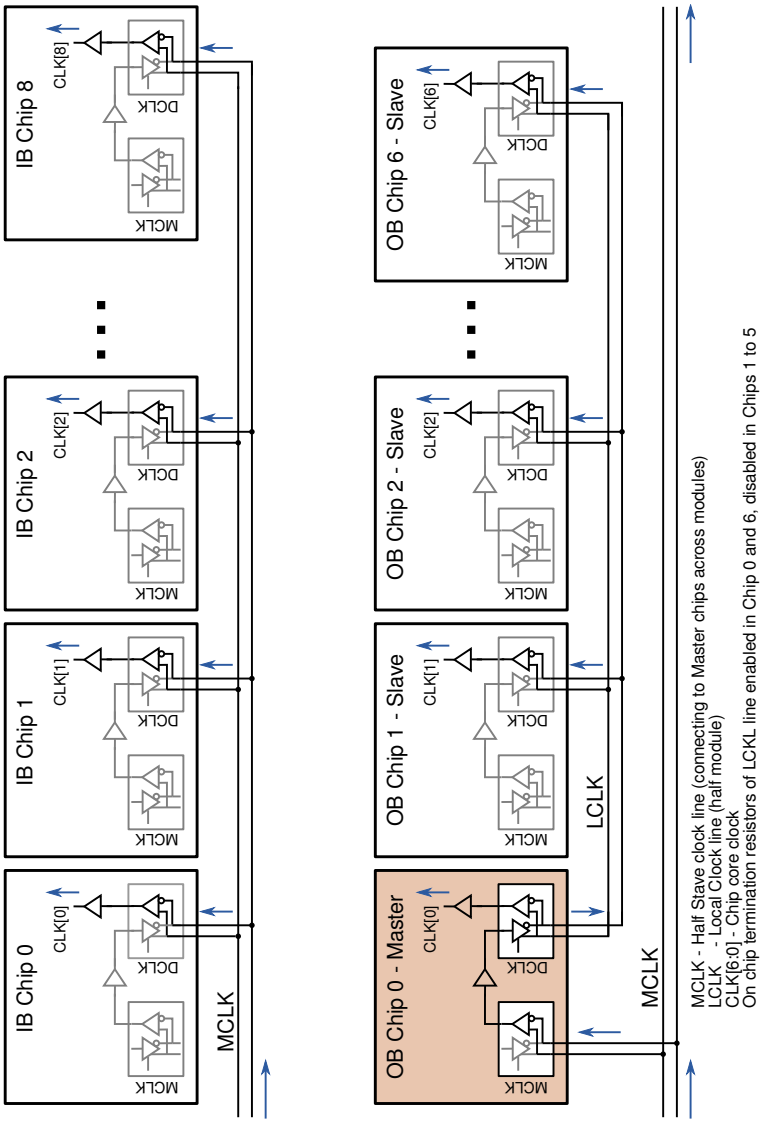

Figure A.1: Illustration of the clock distribution scheme for the ITS Inner Barrel and Outer Barrel Modules.

Appendix B Application note. ALICE ITS Inner Barrel Modules

- Inner Barrel Module include 9 chips
- The 9 chips receive from the off detector electronics a global clock signal on the shared differential line MCLK.
- The MCLK lines connects in a multi-drop configuration the DCLK_P, DCLK_N terminal pairs. Termination of the MCLK line on transmitter side and module far end side is required.
- An unavoidable skew of the internal clocks related to the propagation delays on the line is expected.
- The nominal clock frequency for the Inner Barrel module prototypes is **40.08 MHz** (LHC clock frequency).
- A DCTRL differential line connects in a multi-point configuration the DCTRL_P, DCTRL_N terminals with a differential transceiver (MLVDS) on the off-detector side. Termination resistors shall be provided at both ends of the DCTRL line.
- Signaling on the DCTRL bus is half-duplex and synchronous to the clock. Topological symmetry between the DCTRL line and the MCLK line ensures that the sampling of the DCTRL bus by the chips can be achieved and maintained with correct timing.
- The off-detector electronics shall be capable to transmit serially on the DCTRL bus with a bit period twice (or at least equal) to the clock period.
- The off-detector electronics shall be capable to disable its line driver during the responding periods in which one chip on the line activates its own driver.
- Chips respond on DCTRL according to a pre-defined protocol (section 3.1.3).
- Chips responses on DCTRL are clock synchronous serial transmissions.
- The DCTRL signal sampled at the off-detector electronic side will present a changing phase with respect to the transmitted clock, depending on the distance of the transmitting chip down along the line. Over the 30 cm length of IB Module prototypes this is expected to be negligible. Techniques for appropriate re-timing could be foreseen on the off-detector electronics.
- Chips transmit their data off-detector over point-to-point uni-directional differential links (HSDATA). Signaling on these lines is at 1.2 Gbps by default. Lower rates (600 Mb/s and 400 Mb/s) can be selected optionally.

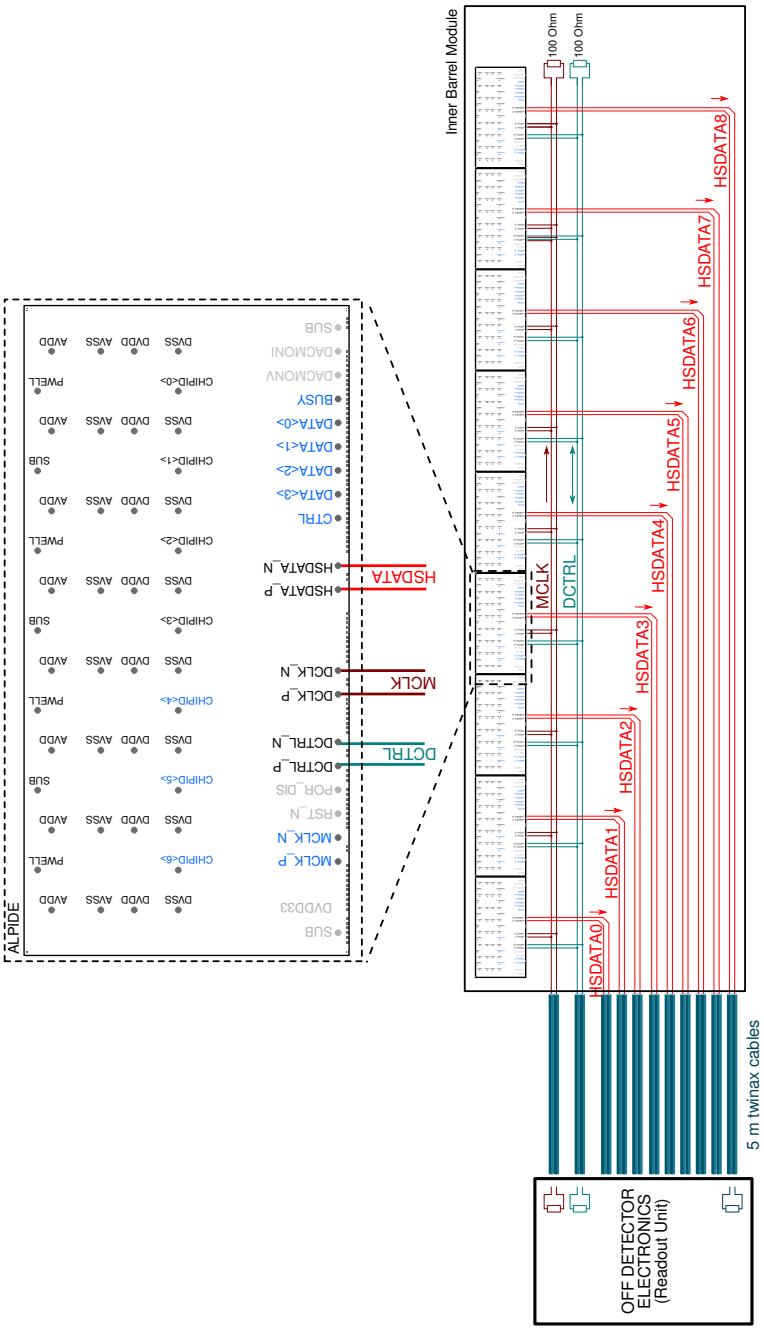

Figure B.1: Schematic diagram of the electrical interconnections between the ALICE ITS Upgrade Inner Barrel module and the off-detector electronics.

Appendix C Application note. ALICE ITS Outer Barrel Modules

- Outer Barrel Module prototypes include 14 chips divided in two sets of 7 (seven). Each subset includes one Outer Barrel Module Master and six associated Outer Barrel Module Slaves.
- The OB Module Master chips receive from the off detector electronics a global clock signal on a shared differential line MCLK.
- 7 (or 4) Master chips share one MCLK line routed along 7 (or 4) modules constituting one Outer (Middle) Layer half stave.
- The MCLK lines connects in a multi-drop configuration the MCLK_P, MCLK_N terminal pairs of the OB Module Master chips. Termination of the MCLK line on transmitter and far end sides is required.
- An unavoidable skew of the chip clocks related to the propagation delays on the line is to be expected.
- The nominal clock frequency for the Outer Barrel module prototypes is **40.08 MHz** (LHC frequency).
- The reference clock is forwarded by the Master chips to the Slave chips using a module local bus (LCLK).
- The reference clock is forwarded by the Master chips to the Slave chips using a module local bus (LCLK).
- The signal received on the MCLK port by the Master chips is replicated (driven) through the driver of the DCLK port.
- All chips receive the clock for the internal circuits through the receivers of the DCLK port.
- The LCLK bus gets terminated by on-chip termination resistors enabled on the DCLK ports of the OB Master chip and of the OB Slave chips with CHIPID[3:0]=6 or CHIPID[3:0]=14.
- A DCTRL differential line connects in a multi-point configuration the DCTRL_P, DCTRL_N terminals of the OB Master chips with a differential transceiver on the off-detector side.
- Proper termination of the line shall be provided at both extremities.
- Signaling on the DCTRL bus is half-duplex and synchronous to the clock. Topological symmetry between the DCTRL line and the MCLK line ensures that the sampling of the DCTRL bus by the OB Master chips can be achieved and maintained with correct timing.
- The off-detector electronics shall be capable to transmit serially on the DCTRL bus with a bit period twice (or at least equal) to the clock period.
- The off-detector electronics shall be capable to disable its line driver during the responding periods in which one of the OB Master chips on the line activates its own driver.
- Chips respond on DCTRL according to a pre-defined protocol (section 3.1.3).

- Chips responses on DCTRL are clock synchronous serial transmissions.
- The DCTRL signal sampled at the off-detector electronic side will present a changing phase with respect to the transmitted clock, depending on the distance of the responding chip down along the line. Means of appropriate re-timing should be foreseen on the off-detector electronics.
- A local control bus (LCLK) is implemented between the OB Master and the OB Slaves using the single ended CTRL ports.
- The OB Master acts as a hub on the control bus, replicating the characters received on the DCTRL port and forwarding from the CTRL to the DCTRL port when one of the associated Slaves is the target of a control read transaction.
- OB Module Master chips transmit their own data and data of the associated six OB Module Slaves on point-to-point uni-directional differential links, using the HSDATA output port.
- Serial transmission on the HSDATA port is at 400 Mbps.
- The signal sampled on the HSDATA links at the off-detector electronic side will present a changing phase with respect to the reference clock, depending on the length of the line between the transmitting chip and the receiver. Means of appropriate re-timing should be foreseen on the off-detector electronics.
- The data exchange between the OB Module Slave chips and the OB Module Master is realized on a OB Module Local DATA Bus.
- The OB Module Local Data Bus is a shared parallel bus realized interconnecting the parallel DATA ports of the chips.
- The 4 lowermost lines of the DATA port operate in Double Data Rate mode, with bits launched or sampled at both clock edges and one complete byte transfer at every clock cycle. The uppermost 4 bits can be left unconnected and the OB Local DATA Bus on the OB moules is implemented using 4 wires shared by the chips.
- Optionally, the chips can be configured with Single Data Rate signaling on the DATA[3:0] IOs and in this case the 8 wires DATA[7:0] would be interconnected across chips. This requires interconnection of the small pads of the chips.
- The OB Module chips drive the Local DATA Bus in turn. Write access to the bus is granted by default to a pre-configured chip. This chip (typically the OB Master) actively drives the DATA bus while idling. The other chips on the bus are configured with the identifier of a preceeding chip in a token exchange chain. All chips sample the data on the Local Bus monitoring the Chip Data Frame transmitted on it by the other chips. On detection of the completion of a frame by the preceeding chip in the chain, a given slave is granted the right to access the bus and transmit onto it a complete Chip Data Frame. At the end of one Chip Data Frame the chip disables the Local Bus Drivers and enters a waiting state for a new time access slot.
- The ordered sequence of chip identifiers governing the write access to the Local DATA Bus and the chip having access to the bus by default are programmable by means of dedicated configuration registers.

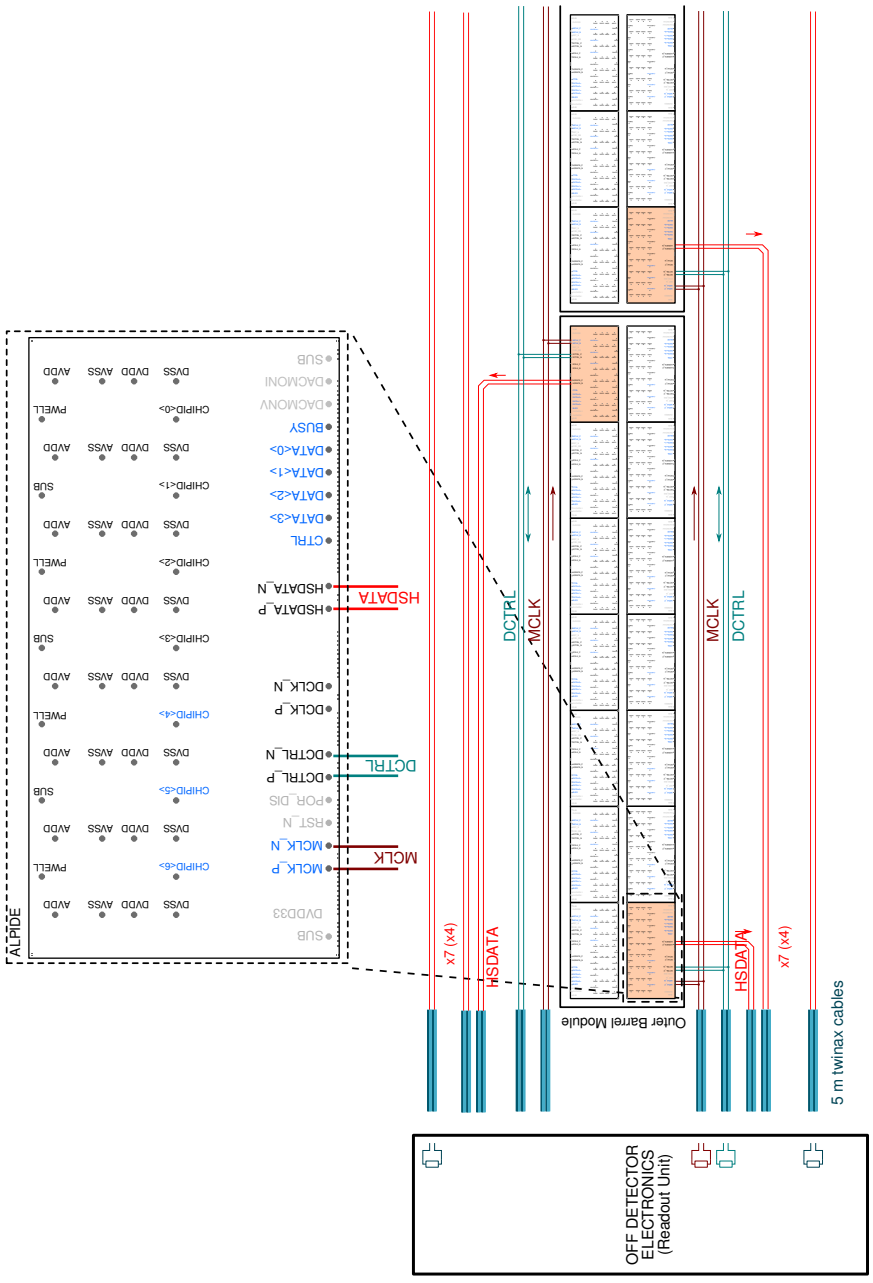

Figure C.1: Schematic diagram of the electrical interconnections between ALICE ITS Upgrade Outer Barrel modules and off-detector electronics.

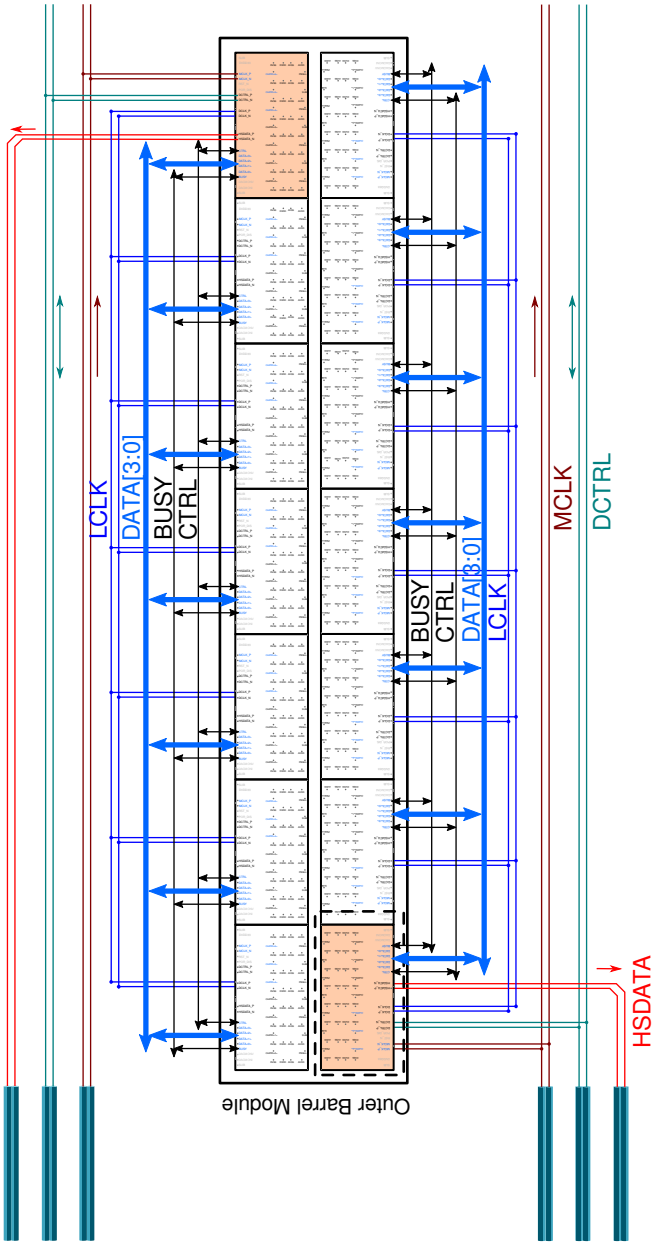

Figure C.2: Schematic diagram of the electrical interconnections between ALICE ITS Upgrade Outer Barrel modules and off-detector electronics.