R&D for the sPHENIX MAPS-based Vertex Detector (MVTX)

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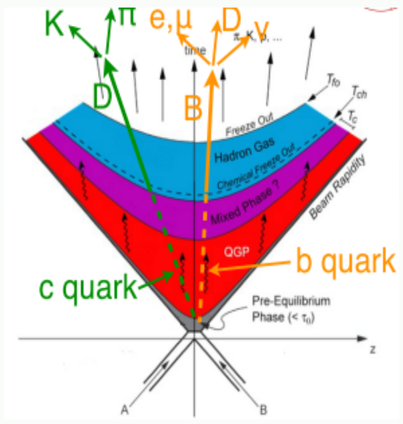
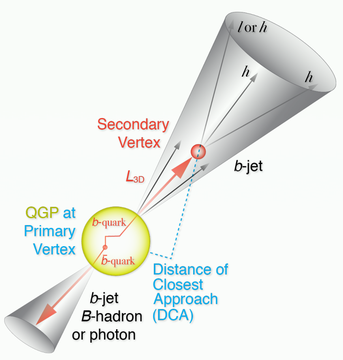
Abstract

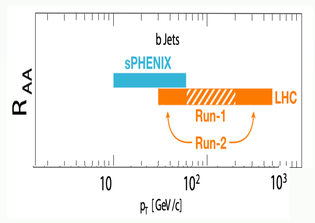
One of the three physics pillars of the proposed sPHENIX experiment is to study the QGP properties with heavy bottom quark jets (B-jets) produced in high-energy heavy ion collisions. B-jets offer a unique set of observables due to the large bottom quark mass, but need to be measured across an unexplored kinematic regime, particularly at low pT where the expected mass-dependence effects are large but also the underlying background are also high. To meet the experimental challenges, we propose to use a 3-layer Monolithic-Active-Pixel-Sensor (MAPS) based pixel detector, originally developed for the ALICE ITS upgrade, for the sPHENIX inner most tracking system, covering radius from 2cm to 4cm and rapidity over +/- 1.1. The very fine 28x28 um pixels allow us to precisely determine the B-decay secondary vertex from the primary interaction point and identify B-jets in heavy ion collisions with high efficiency and high purity. We take advantage of 15+ years of ALICE ITS upgrade R&D work to develop custom readout and mechanical systems to meet the sPHENIX requirements. In this presentation, we show the current status of R&D effort of integrating the MAPS-based detector into the sPHENIX system.

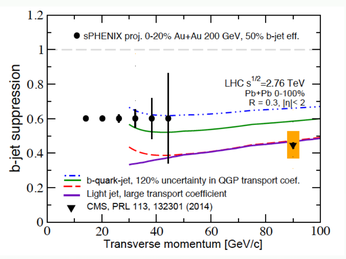
Physics Goals

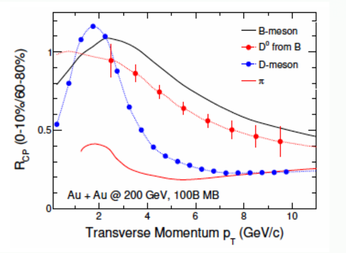
The physics goals of the proposed vertex detector project are aligned with the key challenges and physics opportunities outlined in the 2015 NSAC Long-Range Plan: "There are two central goals of measurements planned at RHIC, as it completes its scientific mission, and at the LHC: (1) Probe the inner workings of QGP by resolving its properties at shorter and shorter length scales. The complementarity of the two facilities is essential to this goal, as is a state-of-the-art jet detector at RHIC, called sPHENIX. (2) Map the phase diagram of QCD with experiments planned at RHIC."





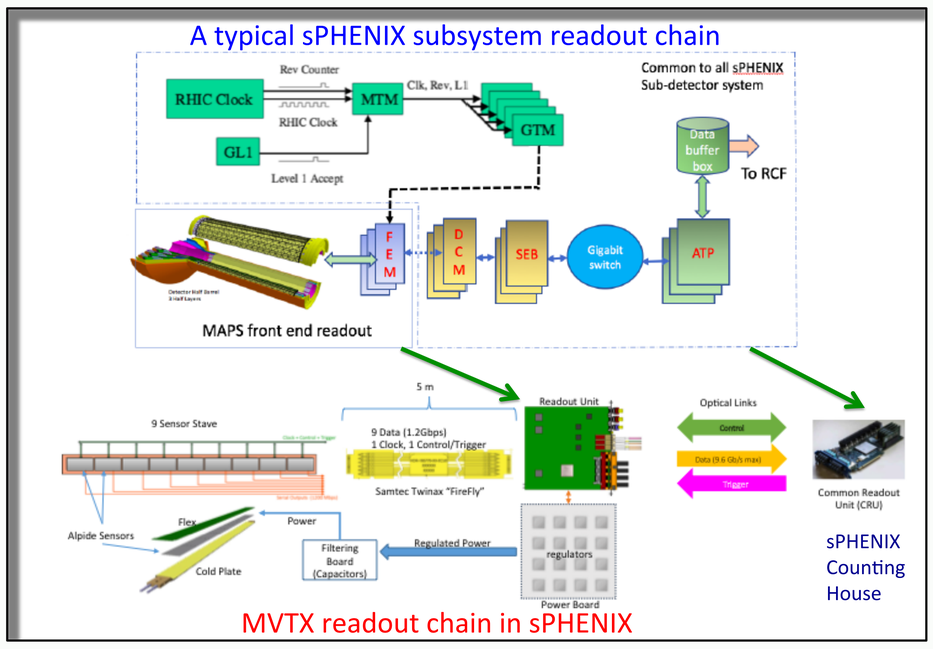






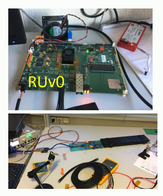
Readout Integration R&D

MVTX readout system interfaces the MAPS staves and the sPHENIX DAQ, and also the trigger and slow control system that monitor and record the status of MAPS chips.

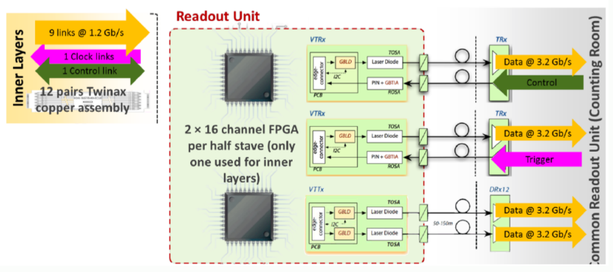


Readout Unit (RU) R&D

- One RU per stave, 48 total
- 9 1.2 Gb/s firefly links, 1 clock, 1 control
- GBT optical to CRU
- 6U VME, RUv0 available



MOSAIC test bench @LANL high-speed readout of MAPS chips

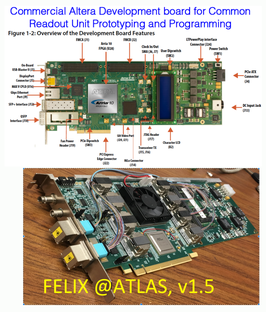


Common Readout Unit (CRU)

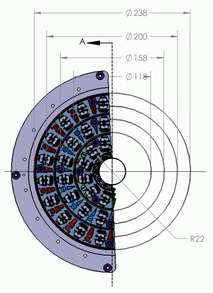
- 48 bi-directional GBT links
- TTC-FTL for timing/trigger
- Arria-10 FPGA
- PCIe40 Gen3 x16 interface
- Two RUs per CRU

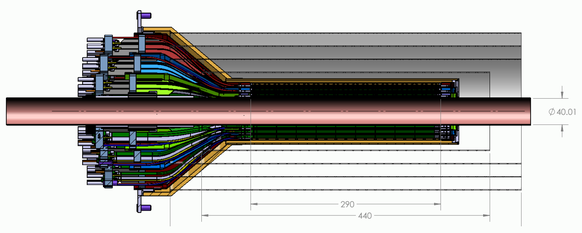
Reprogram firmware for sPHENIX

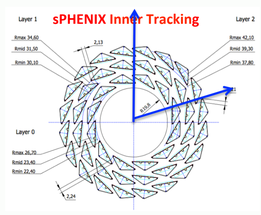
Alternative R&D:
- Altera evaluation board
- ATLAS FELIX @BNL, 48 bi-dir. GBT, PCIex16 Gen3

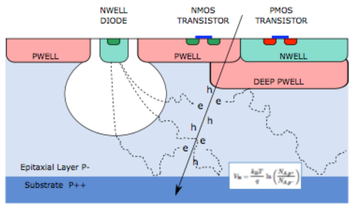


MVTX Detector Design Parameters









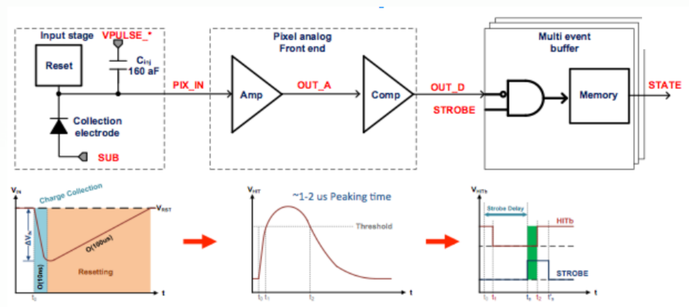
Tower Jazz 0.18 μm CMOS
- feature size 180 nm
- metal layers 6
- gate oxide 3nm

substrate: $N_A \sim 10^{18}$
epitaxial layer: $N_A \sim 10^{13}$
deep p-well: $N_A \sim 10^{16}$

	Layer 0	Layer 1	Layer 2
Radial position (min.) (mm)	22.4	30.1	37.8
Radial position (max.) (mm)	26.7	34.6	42.1
Length (sensitive area) (mm)	271	271	271
Active area (cm^2)	421	562	702
Number of pixel chips	108	144	180
Number of staves	12	16	20

Advantages of MAPS

- Very fine pitch (28x28 μm)
- High efficiency (>99%)
- low noise (<10^{-6})
- High speed, 2~4 μS
- Ultra-thin, 50μm (~0.3% X_0)
- On-pixel digitization
- low power dissipation

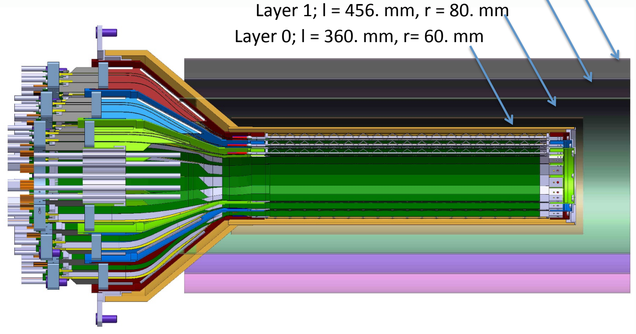


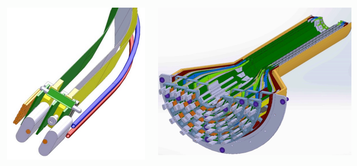
Mechanical Integration R&D

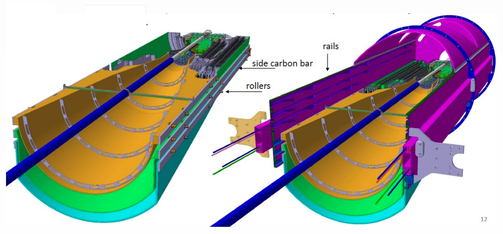
MVTX, INTT & TPC Integration & Installation

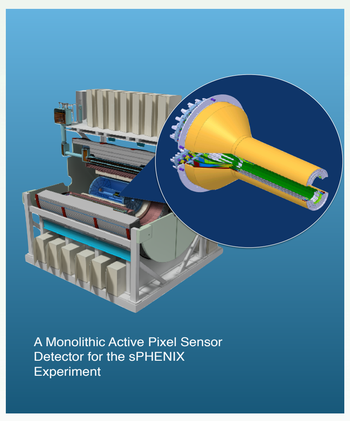
Intermediate Tracker (INTT)

Layer 3; l = 456. mm, r = 120. mm
Layer 2; l = 456. mm, r = 100. mm
Layer 1; l = 456. mm, r = 80. mm
Layer 0; l = 360. mm, r= 60. mm



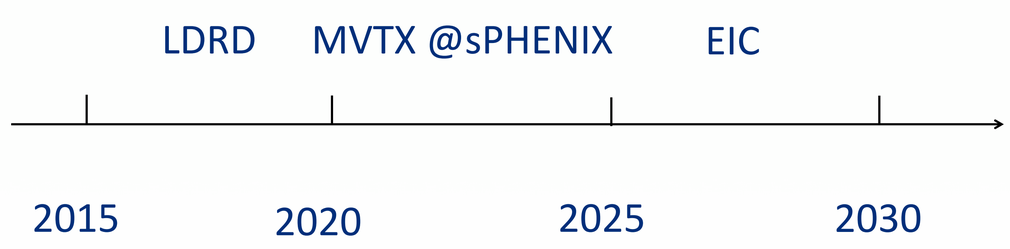






Outlook

- A proposal was submitted to DOE ($5M).
- LANL LDRD supports early R&D ($5M)
- Construction FY18 - FY21
- MVTX ready for sPHENIX Day-1, FY22
- Future application, EIC experiments



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