# Electronics Hardware Status: 09/07/2017

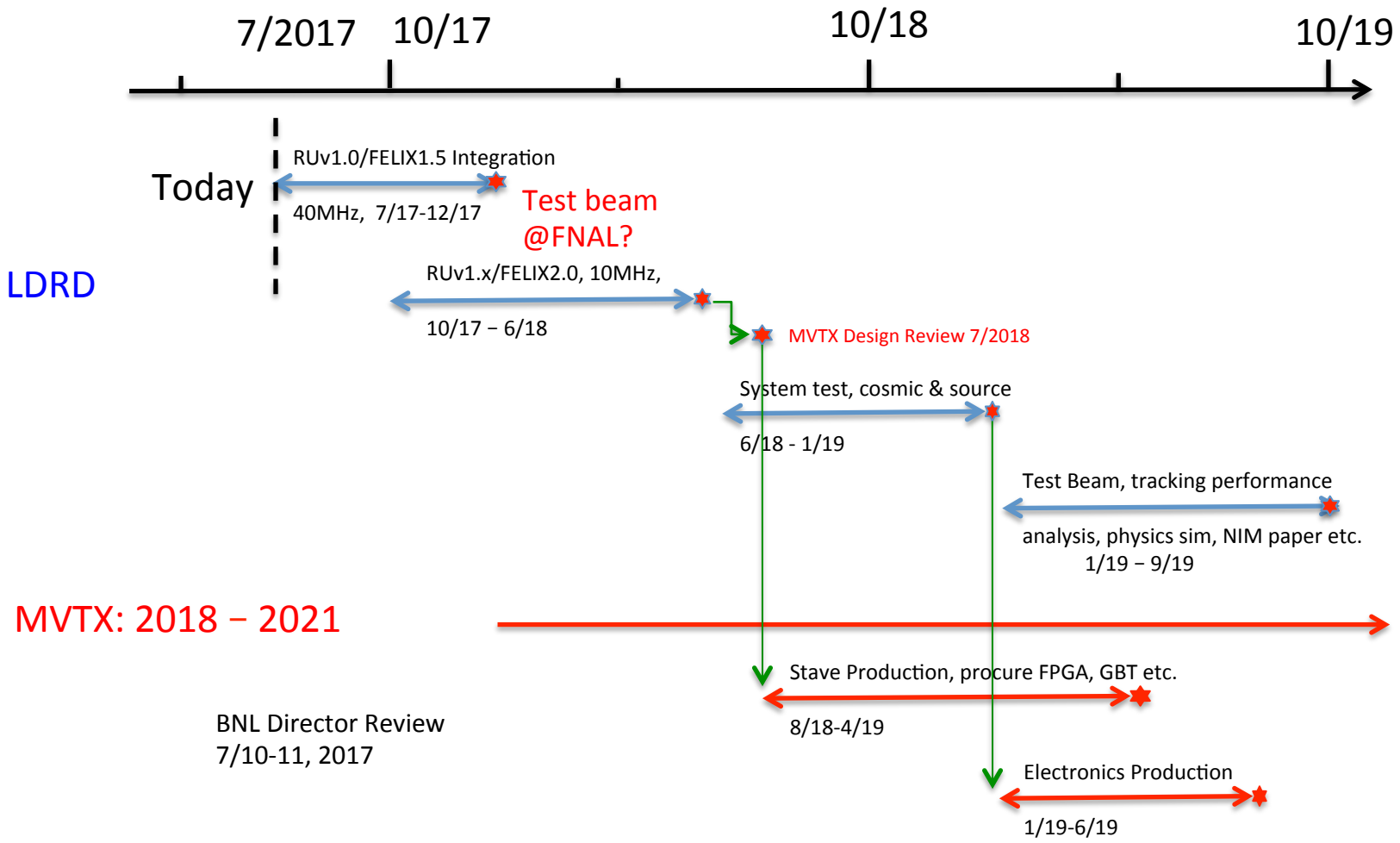
- RUv1:
  - One RUv1.0 to be shipped to LANL this week (?)
    - **RUv1 status (*Marcel*)**
    - Tuesday 1 Sep or Tuesday 13 Sep 6 boards at CERN
    - Testing week 12-17, available: Matteo
      - Prepare a Laptop (provided by Utrecht) with all necessary firmware/software
      - Together with PA3 programming
    - ***Action***: prepare official test-suite (***Marcel***)
      - Likely to be implemented in Utrecht
      - Collecting items from all other sites
      - ***Attiq*** has already a nice suite for the PA3 testing
    - Further 14 boards production
      - Marcel gonna asking for other manufacturer
    - Jo: completed GBT testing (3 chip, both direction, VTTx, VTRx)
      - Interface with power board through both connectors
    - Book a Power Board for testing with RUv1
      - Ask Markus (***Piero***)
    - JTag boundary scan: Krzysztof looking for it
    - Building ancillary electronic for testing the board (***Austin***)
    - Testing of GBT fusing (on mezzanine with USB dongle from GBT group) successful (***Jo***)
      - Use Java interface to control the dongle

- FELIX v2.0
  - PCB arrives at BNL this week
  - Two weeks to assemble the board at BNL
  - One assembled board available by the end of this months, w/ a RHIC Timing mezzanine card

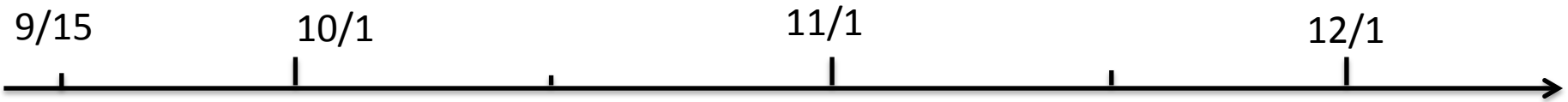
- Power unit is here!
  - MOSAIC operation (?)

- Stave Production @CERN
  - Need your help! Travel to CERN
  - Jirka (from Czech) is helping us to help ALICE stave production

# LDRD – MVTX Key Tasks/Milestones



# Key Tasks and Milestones: ~ Dec. 2017




---- ALPIDE + KC705+FELIX ---------- RUv1.0+FELIXv1.5

---------- FELIX + RCDAQ

---------- RUv1.0 + FELIX v1.5 + Trigger --------- Full Chain

---------- PU + ALPIDE + MOSAIC/RU and DCS - Slow Control Software ----- sPHENIX GTM@LANL

---------- RUv1.0 + FELIX v2.0 + RCDAQ ---------- RHIC Timing/Trigger -→

---------- Physics simulations

- GBT chain integration FELIXv1.5 + KC705 − Done
  - Sho, Alex, Mark
- ALPIDE readout − Sho, Alex, Mark, Xuan
  - w/ KC705 + FELIX, ~9/30
  - w/ RUv1.0, ~10/30 (assuming RUv1.0 arrives by ~9/15)
  - RUv1.0 data format, ~10/30
  - MOSAIC evaluation, ~10/30, Xuan
- FELIX+RCDAQ integration − Kun, Sho, Alex
  - FELIX v1.5: ~9/30
  - FELIX v.2.0: ~10/20 (assuming v.2 available by ~9/30)
- Timing & Triggers − Alex, Sho, Mark, Ming
  - FELIX v1.5 + 40MHz Timing & Trigger, 11/15?
  - FELIX v2.0 + RHIC-mezzanine integration, 11/30
  - Setup GTM @LANL, ~11/15
- Power Unit and Slow Controls software/GUI
  - RUv1.0 + PU, ~10/30
  - Darren, Sanghoon, Cesar
- Complete full chain ALPIDE + RUv1.0 + FELIX v1.5 + RCDAQ
  - 12/20
- Physics simulations for full proposal − Sanghoon, Darren
  - B-jet tagging, ~12/5 update plots

Other tasks:

- Cable test − Pat, Mark, Xuan
  - 11/15
  - MVTX/INTT integration
- Telescope
  - cooling system
  - Tracking software
- Complete proposal
  - Cost, schedule & resources
  - Risk registry
  - WBS Dictionary
  - Preliminary project plan
  - Implement review recommendations

# sPHENIX Test beam schedule - FY18

- Packed and ready Monday/Tuesday, February 12/13, 2018
- Ship to Fermilab Wednesday, February 14, 2018
- Arrive and unload at Fermilab Thursday, February 15, 2018
- Rig into FTBF Wednesday, February 21, 2018
- ORR Thursday, February 22, 2018
- First beam Friday, February 23, 2018
- Co-habitate with EDIT school March 5-16, 2018
- Rig out of FTBF Wednesday, March 28, 2018
- Ship home Thursday, March 29?

# (s)PHENIX Timing, Trigger and Controls

- Mode-bit: 11-bit timing signal sent to FEM on every RHIC clock
  - RHIC clock. 9.4MHz
    - 1x RHIC
    - 4x RHIC
  - PHENIX GL1-Trigger
    - "Dead for 4 BCLKs"
    - 5 events buffer
    - 32-bit Lvl-1 triggers for PHENIX, plan to have more bits for sPHENIX
  - Global system commands
    - PHENIX Start
    - PHENIX Stop
  - Detector specific commands

- Glink Interface
  - Timing interface is placed onto a HP HDMP-1012 Transmitter (GLink).
  - Virtual ribbon cable provides hig speed serial path for 20 parallel bits.

http://www.phenix.bnl.gov/phenix/project_info/electronics/timing/tc/current_tc.htm

Table 1. Timing & Control Interface Bit Definitions

| Bit Name | Bit Definition |
|---|---|
| Beam Clock | Beam Clock - 108ns Period |
| Beam ClockX4 | 4X Beam Clock - 27ns Period |
| LVL-1 | LVL_1 Accept |
| MB7 | Extra Bit - No Assigned Function |
| MB6 | Extra Bit - No Assigned Function |
| MB5 | Extra Bit - Pulse Enable (optional) |
| MB4 | Reserved For Command Encoding |
| MB3 | Reserved For Command Encoding |
| MB2 | Reserved For Command Encoding |
| MB1 | Reserved For Command Encoding |
| MB0 | Reserved For Command Encoding |

Example: MuTr & FVTX GTM

| MB1 | MB0 | Command |
|---|---|---|
| 0 | 0 | No-op (Reset None) |
| 0 | 1 | Resync Reset |
| 1 | 0 | Initialization Reset |
| 1 | 1 | Special Reset |

# Glink Interface

PHENX Granule Timing Module (GTM), 9U VME board

FELIX + GTM interface

- 20-bit
- CLOCK
  - 1x (9.4 MHz)
  - 4x (37.6 MHz)
- Trigger

- NO MVTX busy feedback
- EnDat0/1: Master/Slave
- User bits: for calibration etc.

| Data Line | Function |
|---|---|
| D0 | Mode Bit 0 |
| D1 | Mode Bit 1 |
| D2 | Mode Bit 2 |
| D3 | Mode Bit 3 |
| D4 | Mode Bit 4 |
| D5 | Mode Bit 5 |
| D6 | Mode Bit 6 |
| D7 | Mode Bit 7 |
| D8 | Beam Clock (9.4Mhz) |
| D9 | LVL1 Accept |
| D10 | Mode Enable |
| D11 | EnDat0 |
| D12 | EnDat1 |
| D13 | User Bit 0 |
| D14 | User Bit 1 |
| D15 | User Bit 2 |
| D16 | Reserved |
| D17 | Reserved |
| D18 | Reserved |
| D19 | Reserved |

Table 3. GLINK Bit Assignments

# sPHENIX Timing & Trigger

- Setup (s)PHENIX Timing System @LANL
  - GTM module + Linux Server
    - Fiber output
    - Trigger
    - NO busy feedback for MVTX readout
  - MiniDAQ (Win98)?, was in 1008

# sPHENIX Project Update/Issues

- DOE/RHIC annual site visit yesterday 9/6/17. Tim and Jehanne were emphatic about ONP's support for sPHENIX.
- Meeting with Berndt and David last Friday to discuss the recommendations from the Director's review. They made it clear that It is in our best interest to quickly close as many recommendations as we practically can and then focus on the bigger issues of total cost and profile.

- Start a budget "scrubbing" process now so that 4 weeks from now we have a lower baseline from which to descope the project to $32M.
  - All L2 Managers must scrutinize their files for cost savings.
  - The engineering team can help with value engineering.