MAPS Readout Electronics

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LDRD DR Feasibility Review 12/5/16

Participants and Expertise

LANL P-25 (Physics), AOT (EE) Groups

Expertise gained from $5M PHENIX FVTX project + others:

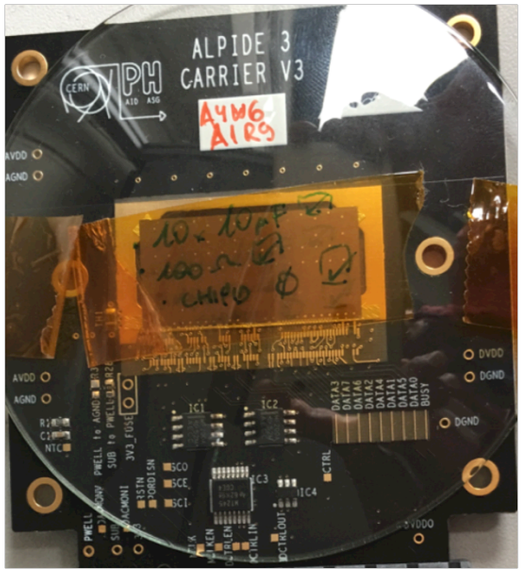
- Si pixel sensors and custom ASIC readout
- Analog / digital electronics design and layout
- High speed differential and fiber optic data transmission
- Use of modern FPGAs from Xilinx, Actel
- FPGA programming with Verilog and VHDL
- Custom high density interconnects (FPC)
- Event building and formatting

Have joined ALICE collaboration as associate member

With expert help from BNL, LBNL, MIT, UNM, UT Austin

Outline

ALPIDE monolithic Si pixel sensor
(ALICE Pixel Detector)



MAPS readout:

General design

Readout Unit

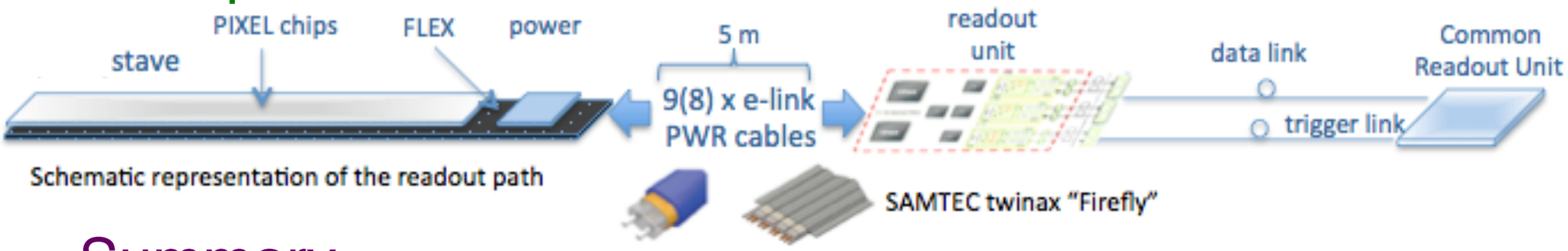
Radiation hard design and fiber optic

Common Readout Unit

Development board

Test bench

Expected data rates

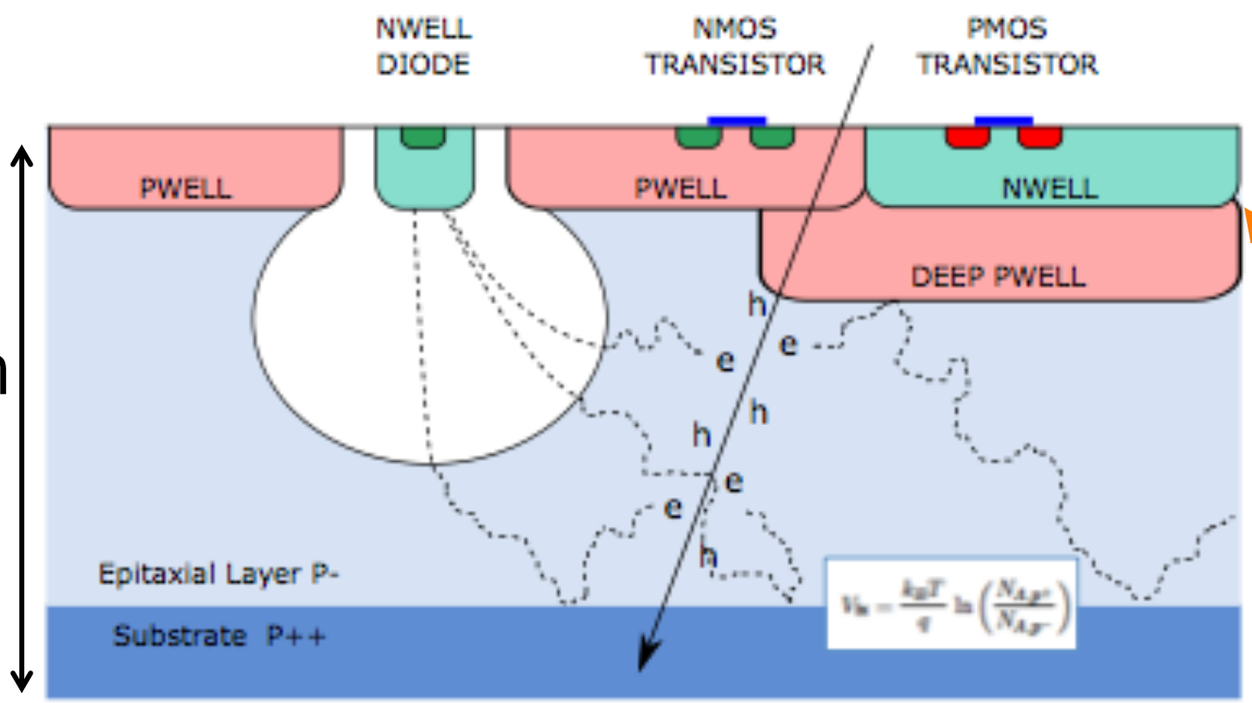


Summary

5 meter cable

ALPIDE Monolithic Pixel Technology

CMOS Pixel Sensor using TowerJazz 0.18µm CMOS Imaging Process



deep p-well allows for circuitry

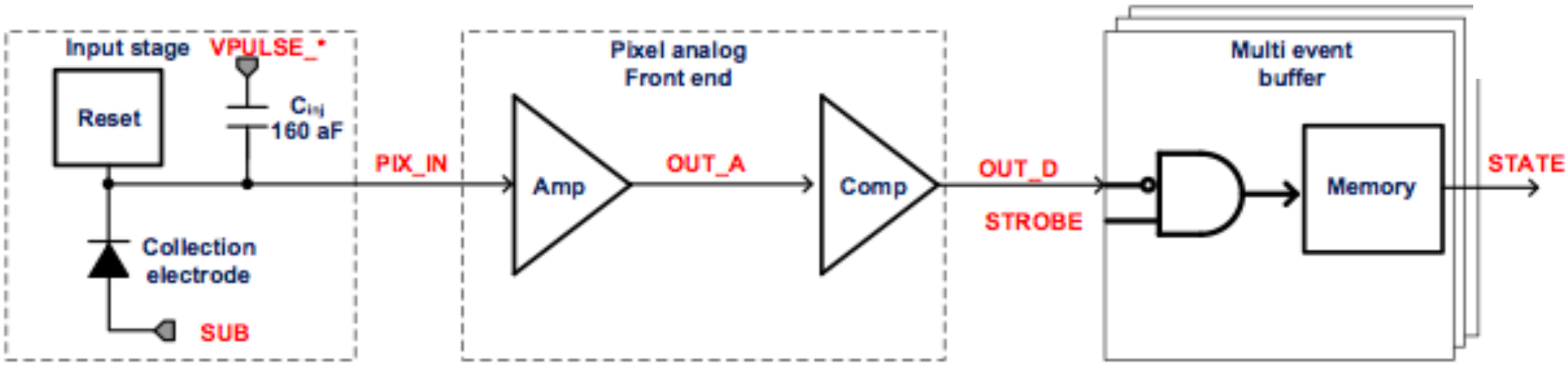
Tower Jazz 0.18 µm CMOS

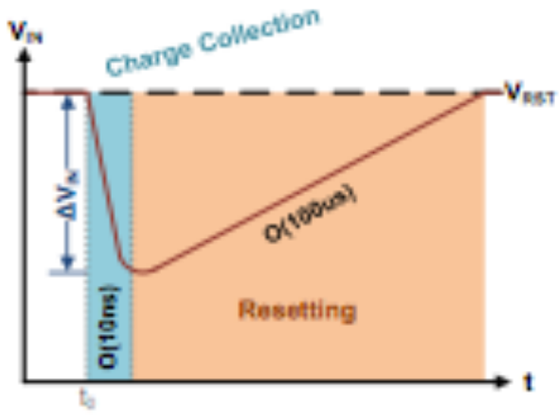
- feature size 180 nm
- metal layers 6
- gate oxide 3nm

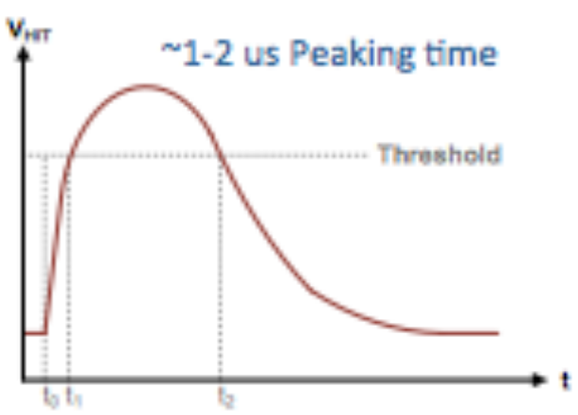
substrate: $N_A \sim 10^{18}$
epitaxial layer: $N_A \sim 10^{13}$
deep p-well: $N_A \sim 10^{16}$

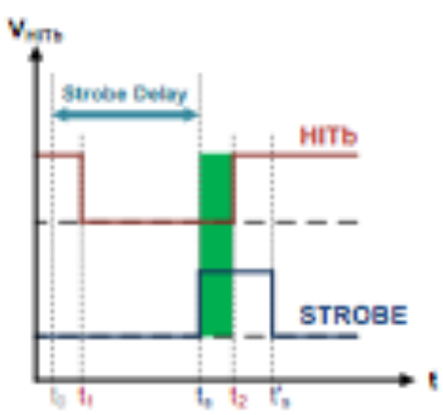
- High-resistivity (> 1kΩ cm) p-type epitaxial layer (18µm to 30µm) on p-type substrate
- Small n-well diode (2 µm diameter), ~100 times smaller than pixel => low capacitance
- Application of (moderate) reverse bias voltage to substrate (contact from the top) can be used to increase depletion zone around NWELL collection diode
- Deep PWELL shields NWELL of PMOS transistors to allow for full CMOS circuitry within active area

ALPIDE Operation









ultra low-power front-end circuit
40nW / pixel

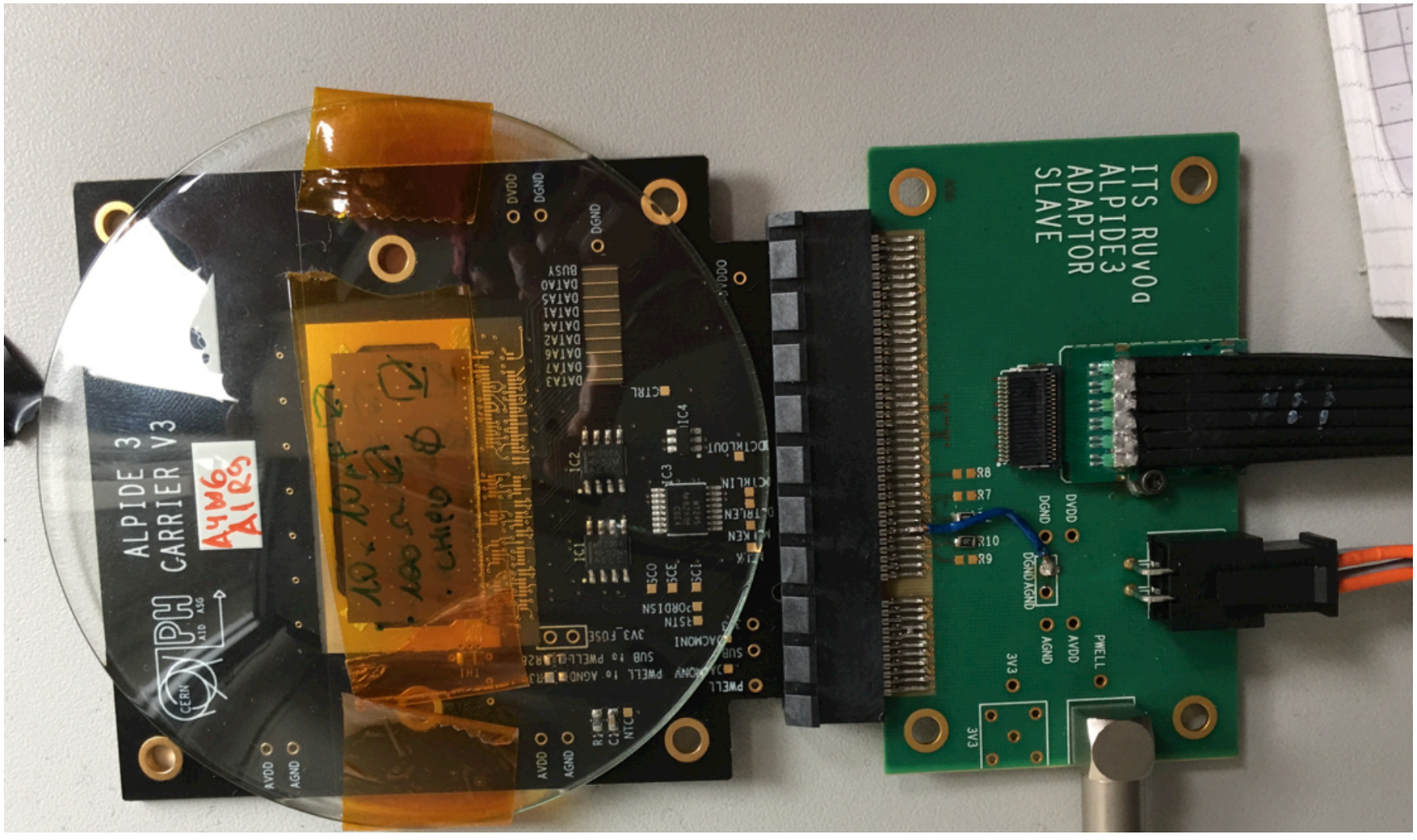
Front-end acts as delay line

- Sensor and front-end continuously active
- Upon particle hit front-end forms a pulse with ~1-2μs peaking time
- Threshold is applied to form binary pulse
- Hit is latched into a (3-bit) memory if strobe is applied during binary pulse

MAPS chip

Single Chip High Speed Readout

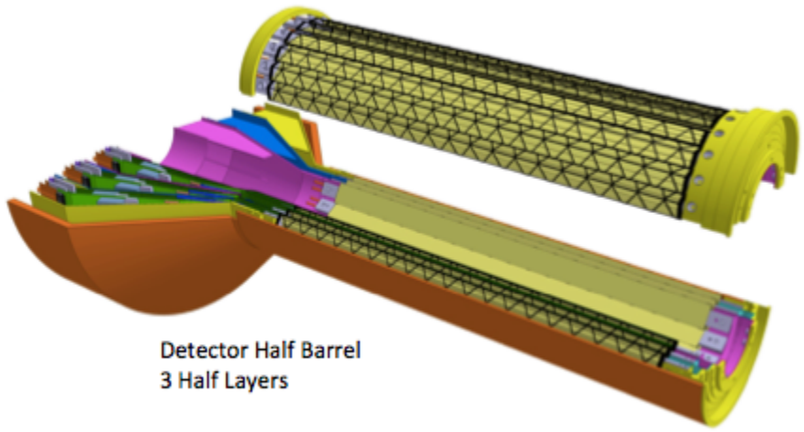
15x30mm
active area



Have one MAPS chip and slow readout working at LANL, more on the way

MAPS Readout Description

Staves



Detector Half Barrel
3 Half Layers

Passive electrical (copper) links, up to 1.2 Gb/s (data and control @ 40 Mb/s)

GBT optical

Trigger

One way, passive optical splitting, no busy back

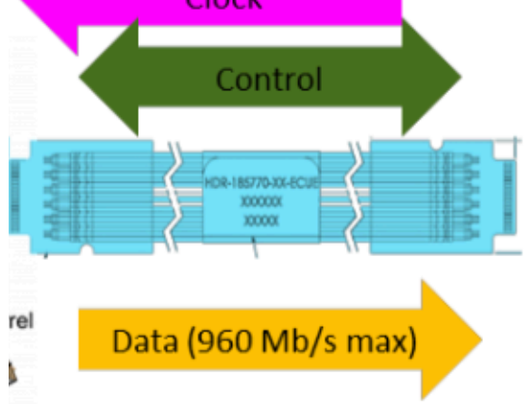
x 24

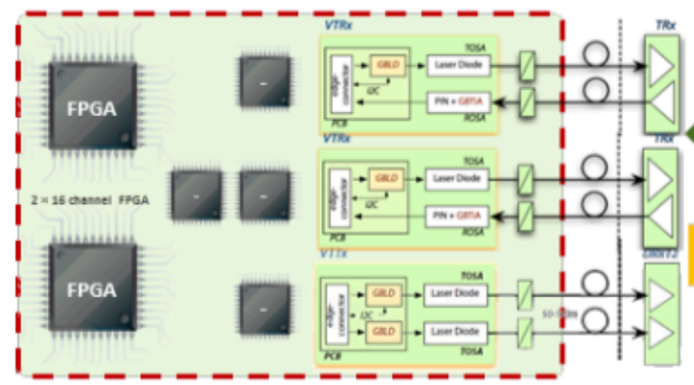
Clock

Control

Data (960 Mb/s max)

5 meter cable





GBT optical

Control

Data (9.6 Gb/s max)

Common Readout Unit & O2

x 48

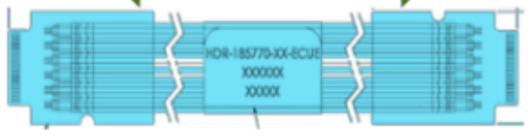
Identical Readout Units (RU) cover the full ITS

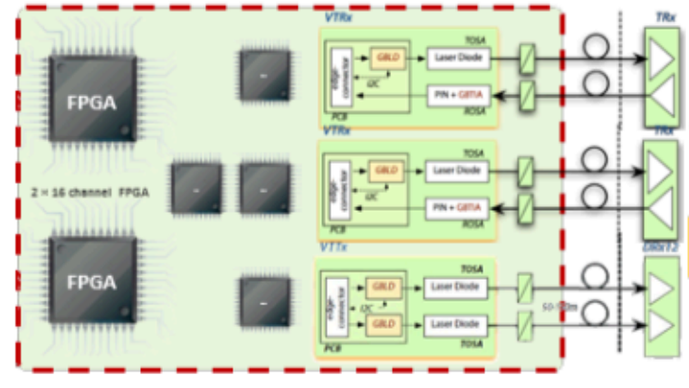
Each Readout Unit is connected to one stave

Clock

Control

Data (960 Mb/s max)





GBT optical

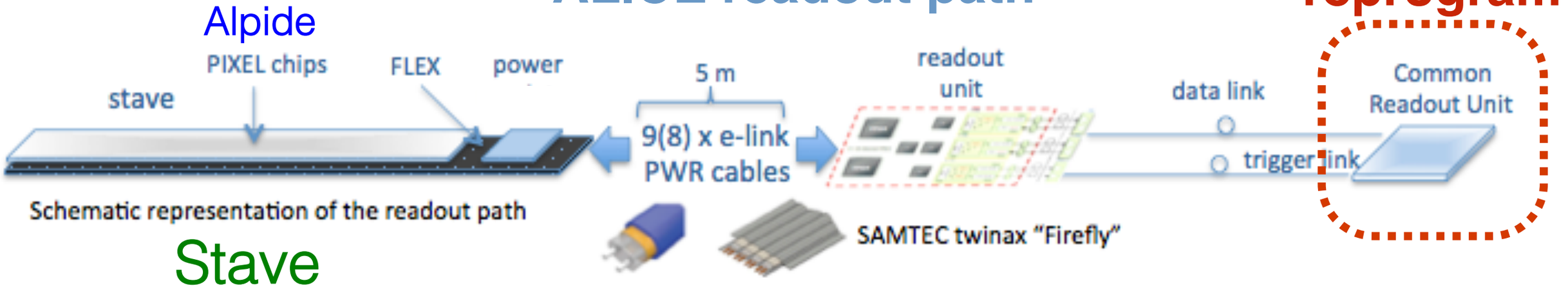
Control

Data (9.6 Gb/s max)

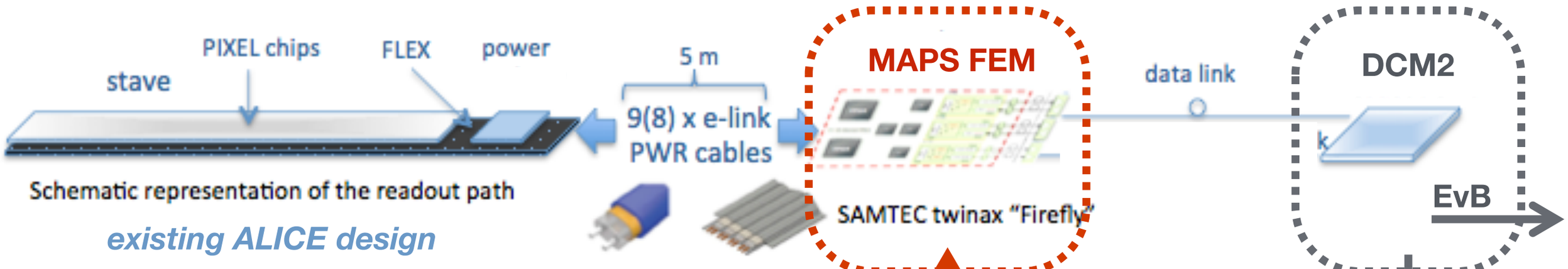
MAPS Electronics

ALICE readout path

Plan A: reprogram



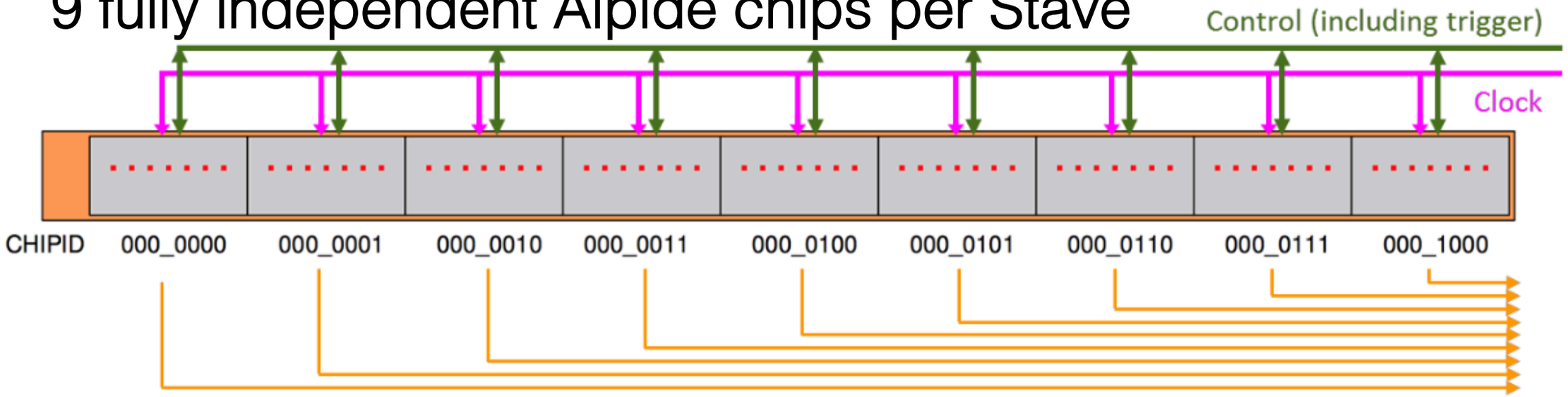
Plan B: sPHENIX readout path (held only as contingency)



Larger effort, requires new hardware and FPGA code!

Stave Readout

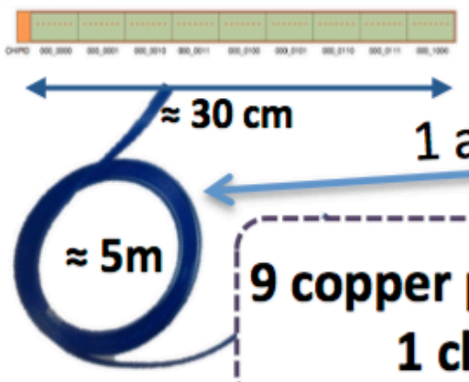
9 fully independent Alpide chips per Stave

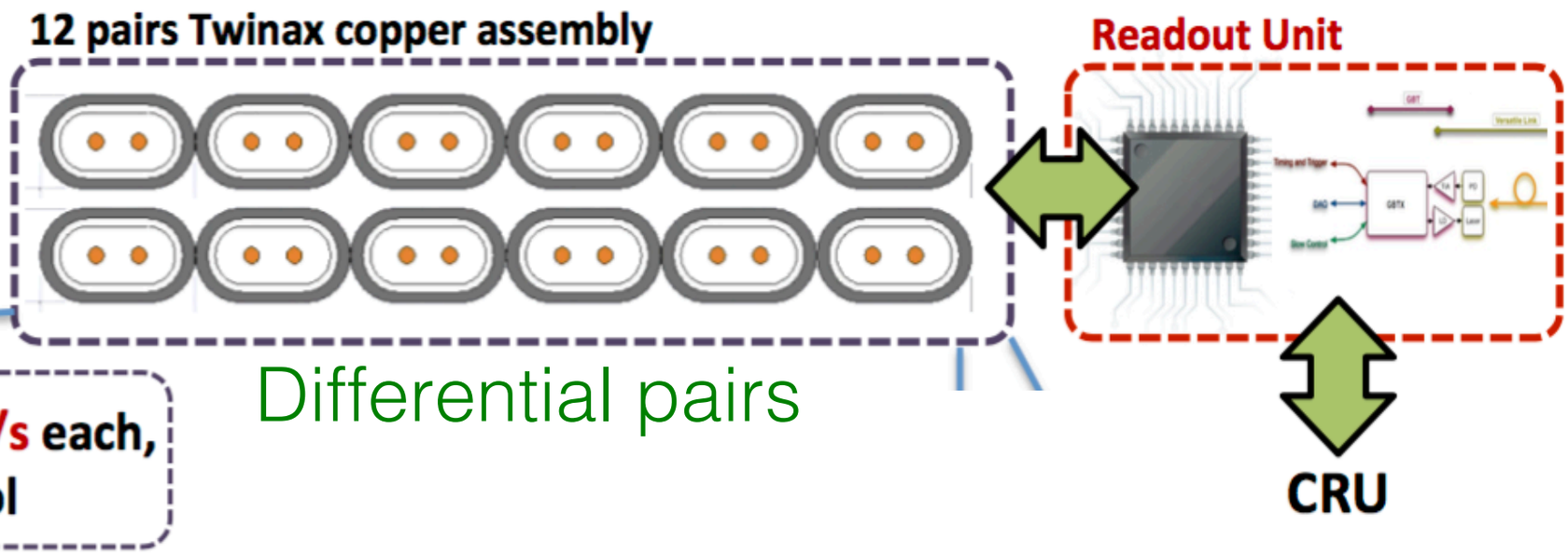


Continuous readout →

Stave

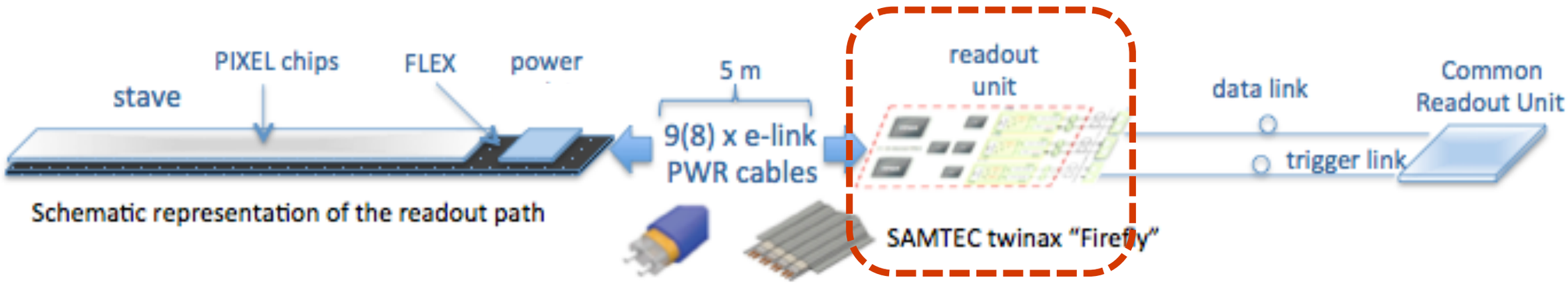
Inner layers (0, 1, 2) staves:





Medium Risk - Staves available in Summer, 2017

ALICE Readout Unit Logic



Schematic representation of the readout path

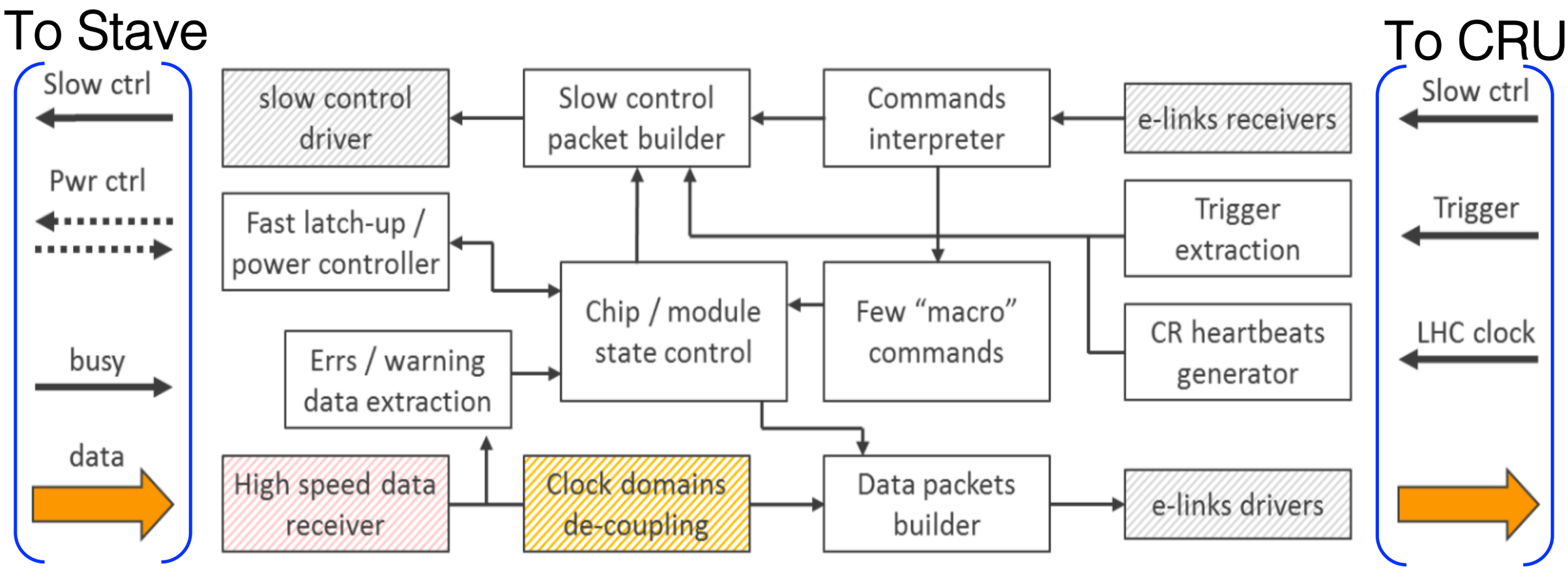
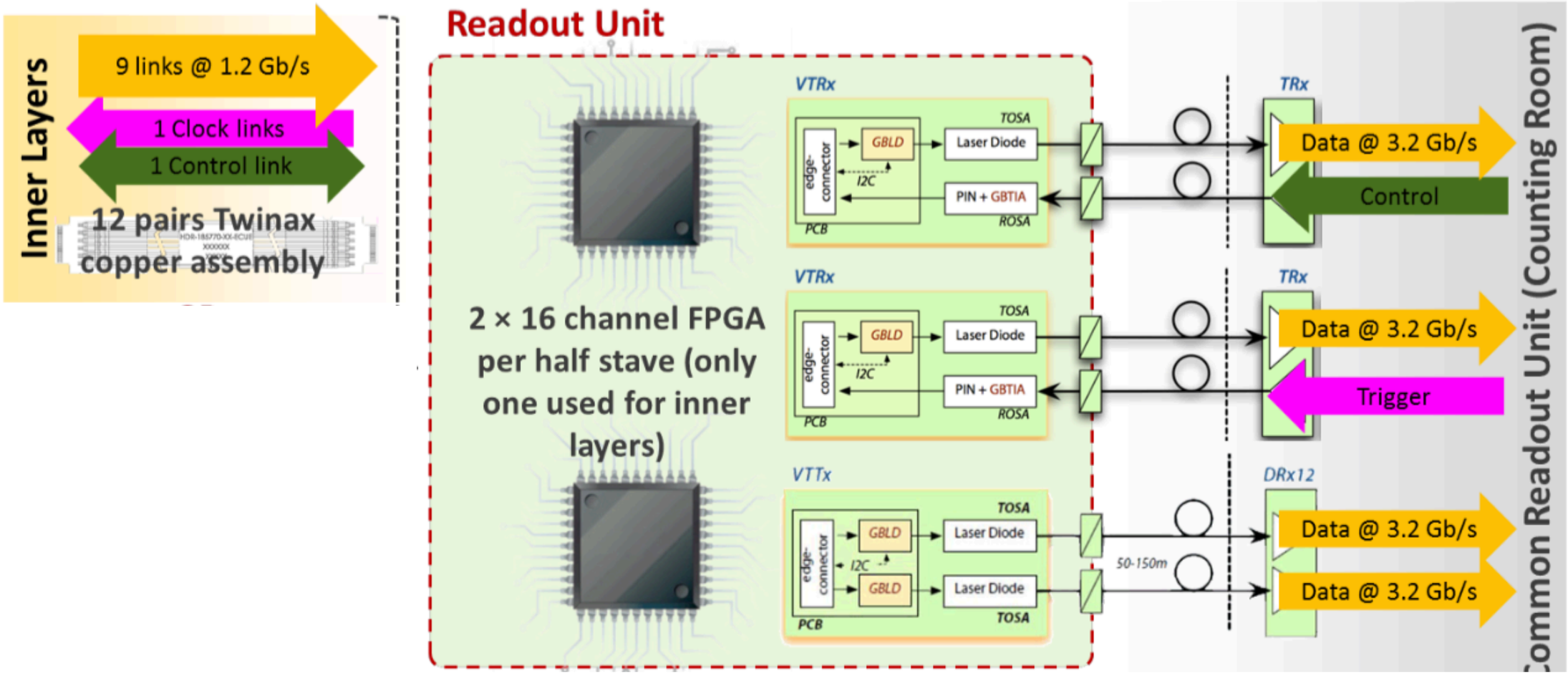
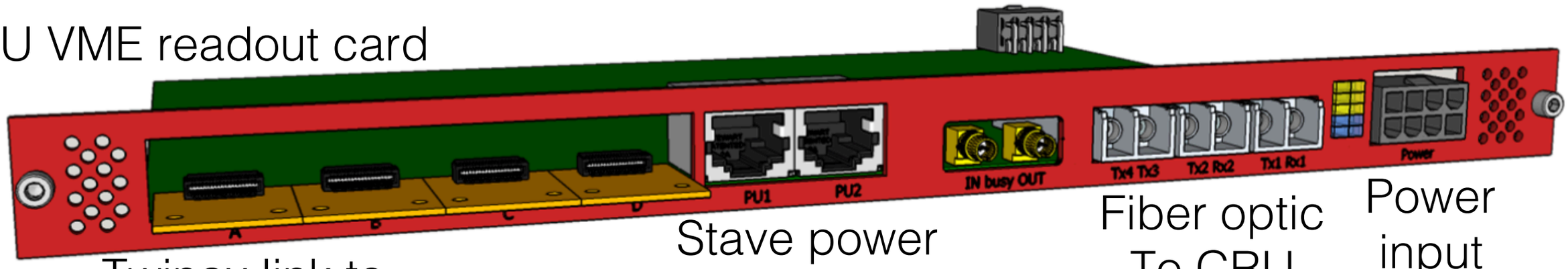


Figure 9 –Readout Electronics main functions.

ALICE Readout Units



6U VME readout card



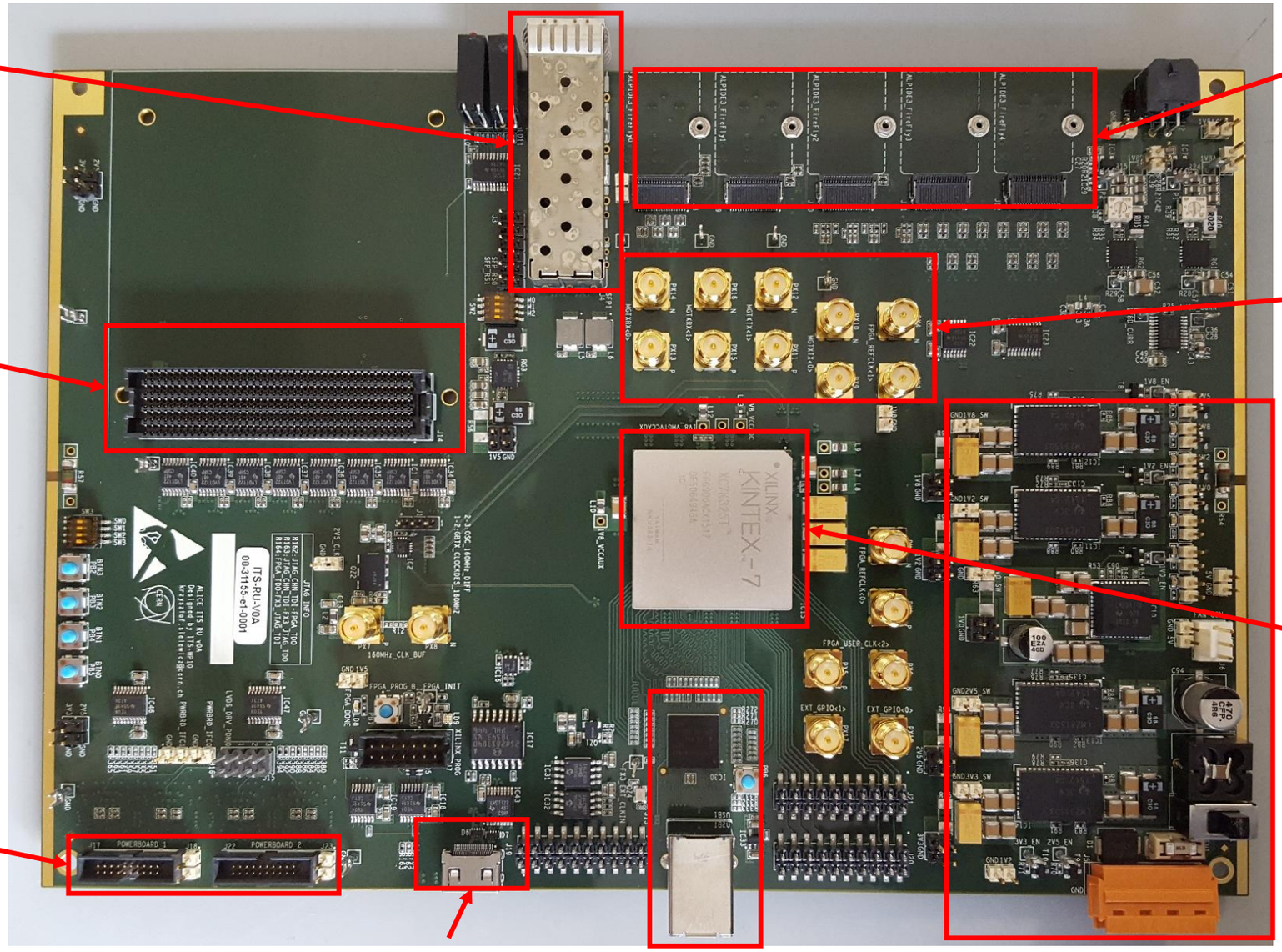
Twinax link to one stave

Stave power control

Fiber optic To CRU

Power input

Readout Unit Prototype Version 0a (“RUv0a”)



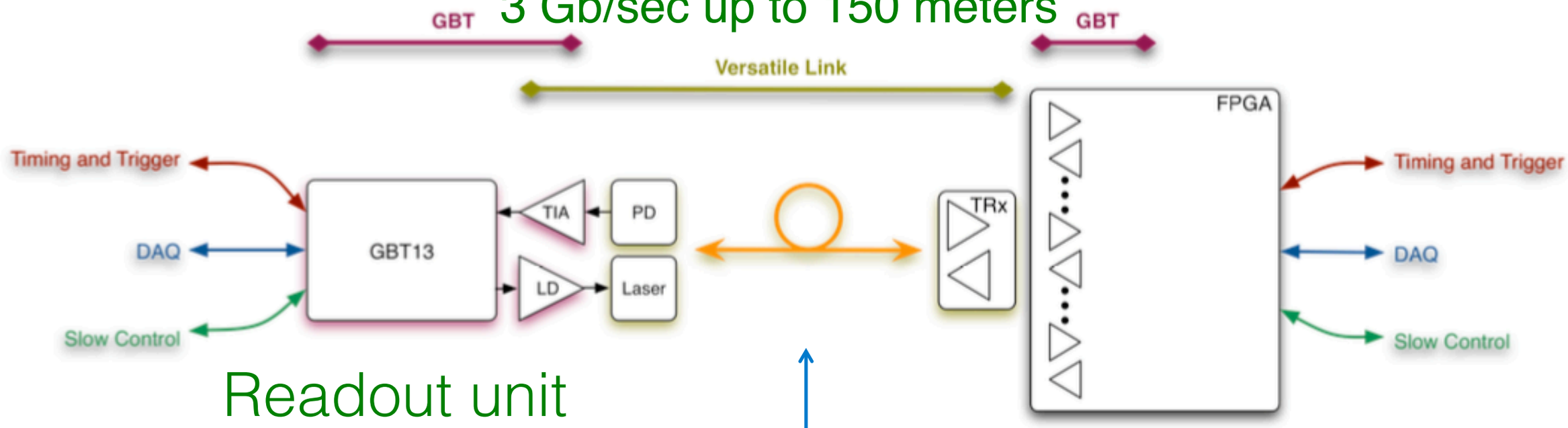
6U VME card

Low risk, currently being tested by ALICE

Expect version ‘0’ readout unit at LANL in spring, 2017

CERN Versatile Link – Bidirectional Fiberoptic

3 Gb/sec up to 150 meters



Readout unit

On-Detector

Custom Electronics & Packaging

Radiation Hard

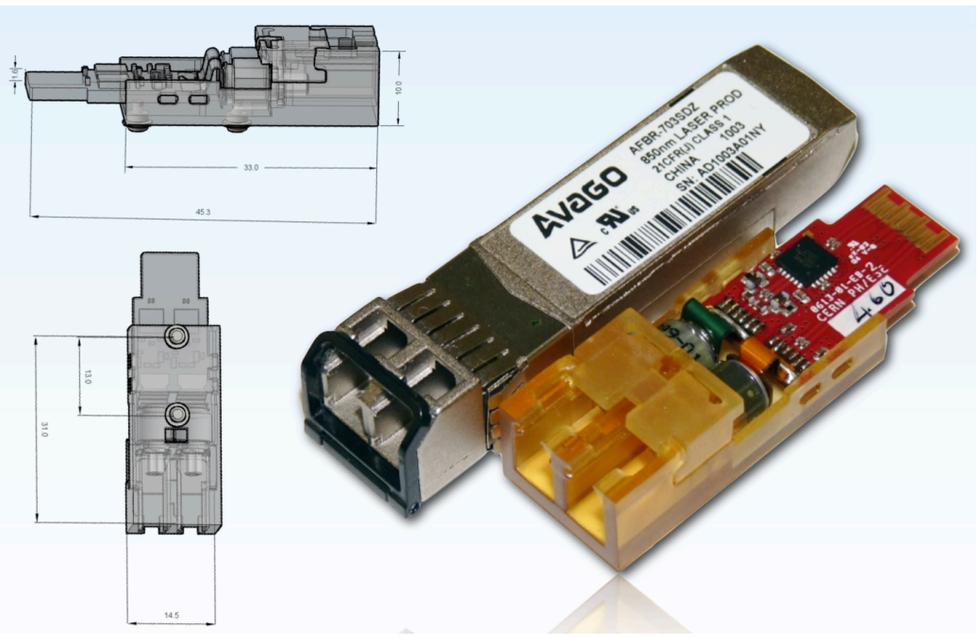
Off-Detector

Commercial Off-The-Shelf (COTS)

Custom Protocol

Common readout unit

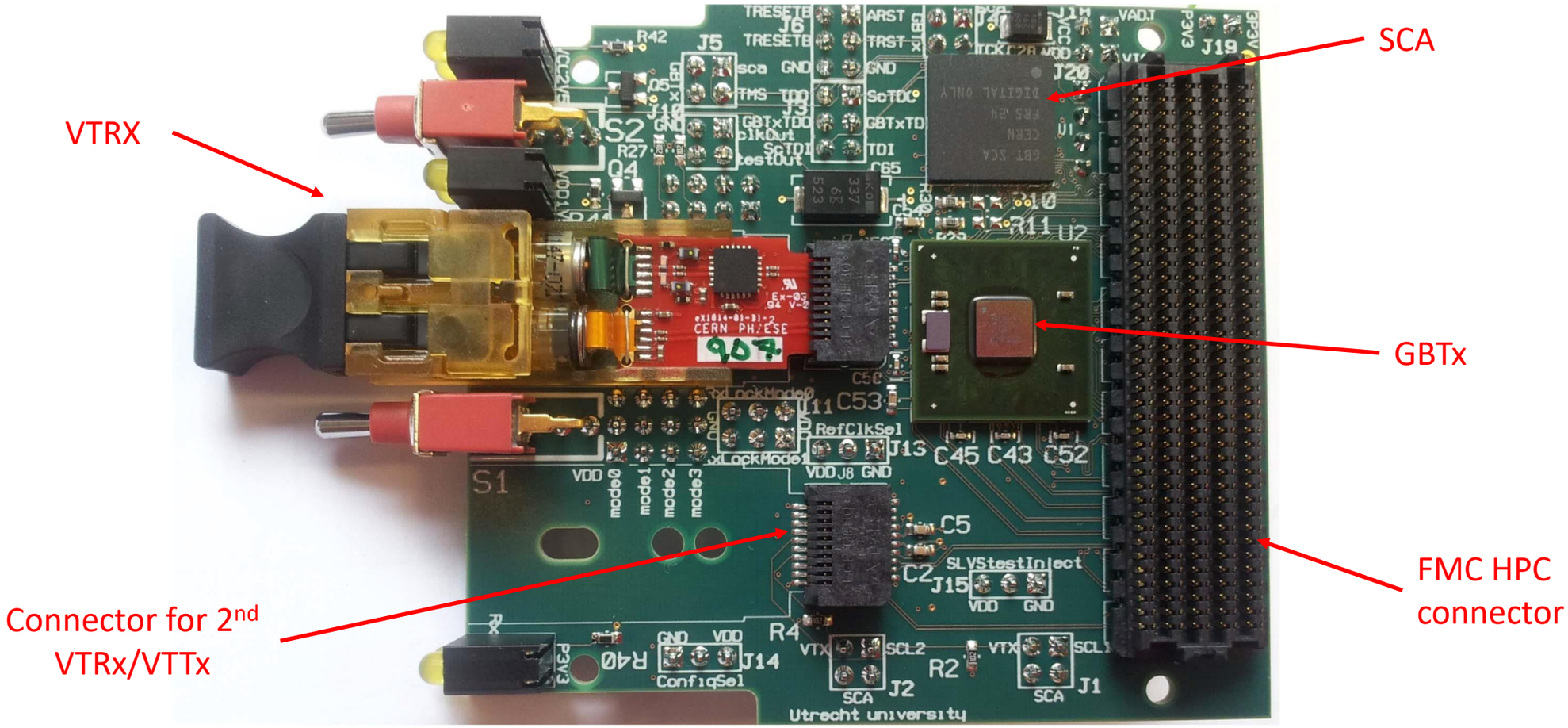
In counting house



Long fiber run from Hall to Rack Room over custom CERN optical link

Fiber optic transceiver daughterboard for readout unit

GBT FMC Mezzanine (“GBTxFMC”)



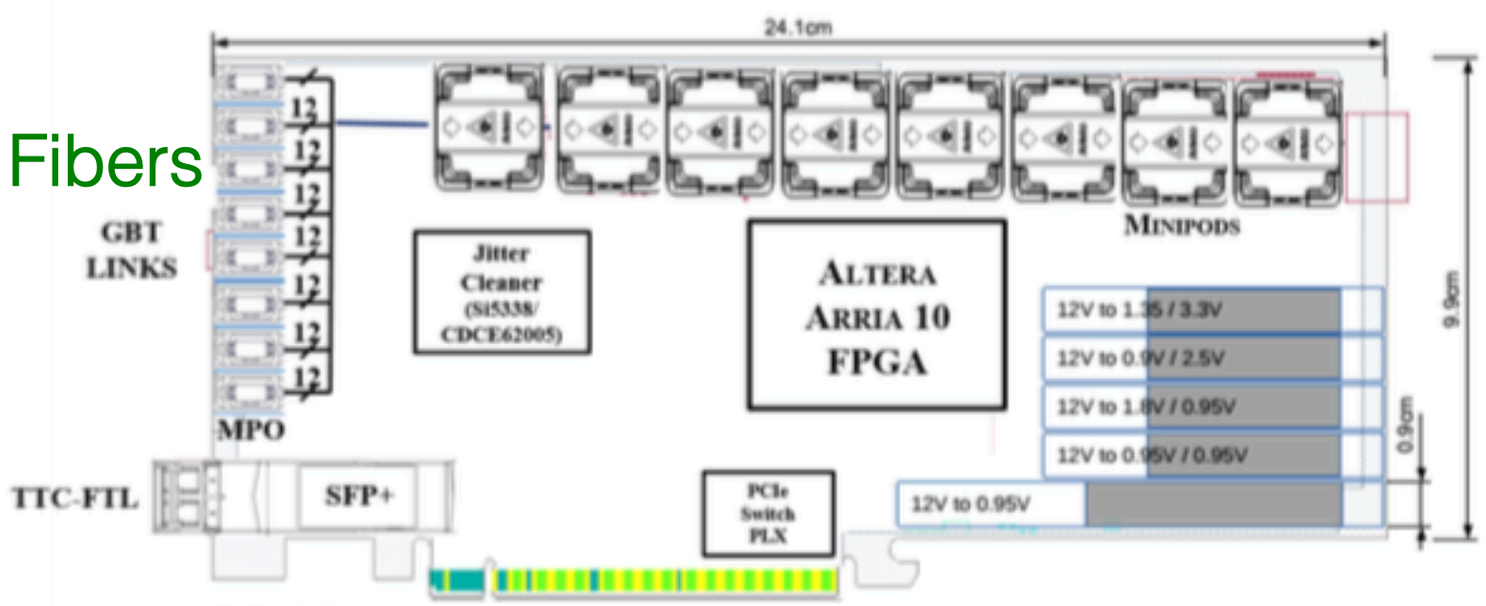
Low risk, tested and operational order for LANL in process

ALICE Common Readout Units

PCI express card

(a) PCie40.

Avago optical engines



(b) PCIe40 Schematic.

Will be used by several ALICE and sPHENIX subsytems

Each CRU reads out two Readout units, sends slow controls, trigger back

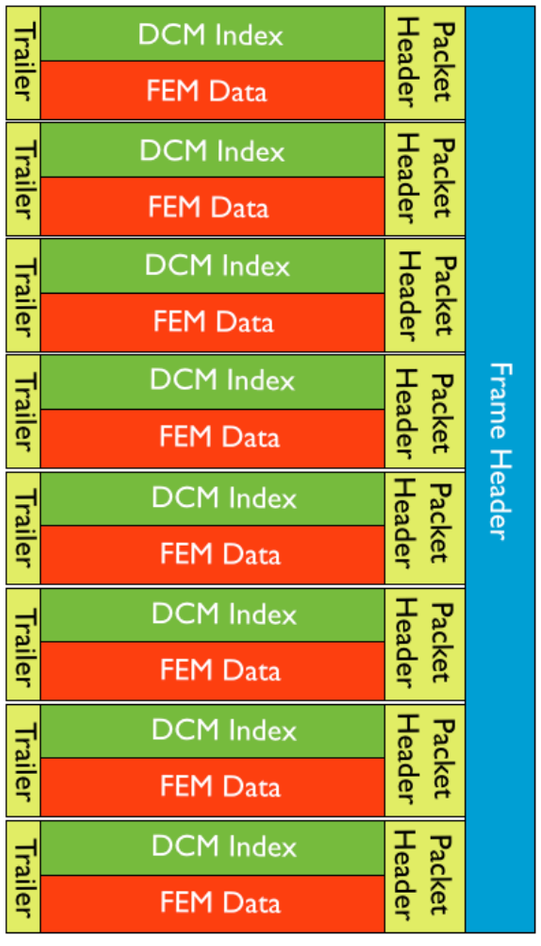
CRU cards reside in CPU chassis

Medium risk, CRU still in development at LHCb experiment

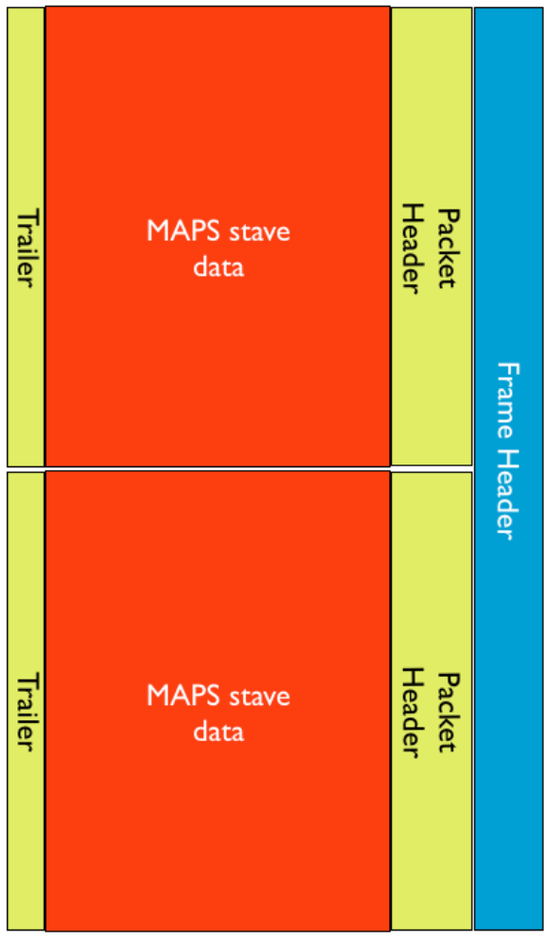
Expected at LANL in summer, 2017

Data Stream Reformatting

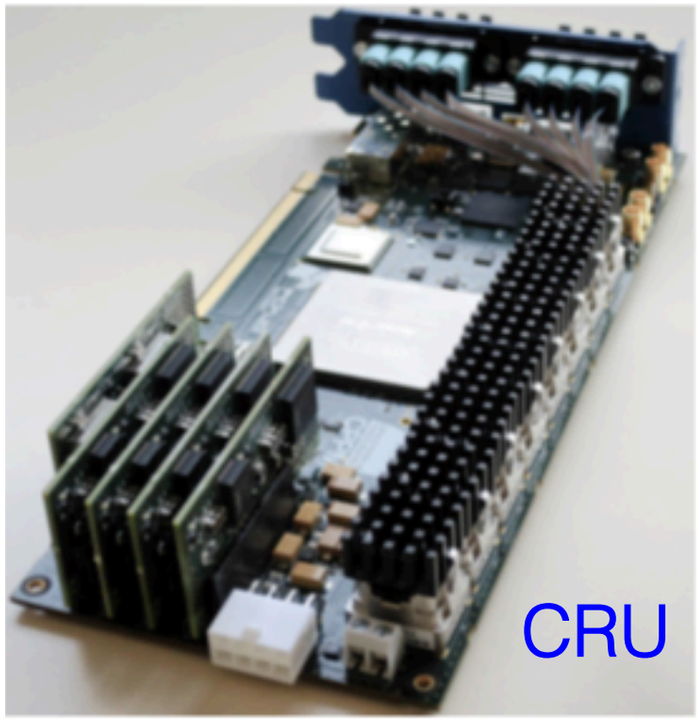
Traditional sPHENIX Frame



sPHENIX MAPS Common Readout Frame



Reformat options: FPGA or CPU…



(a) PCie40.

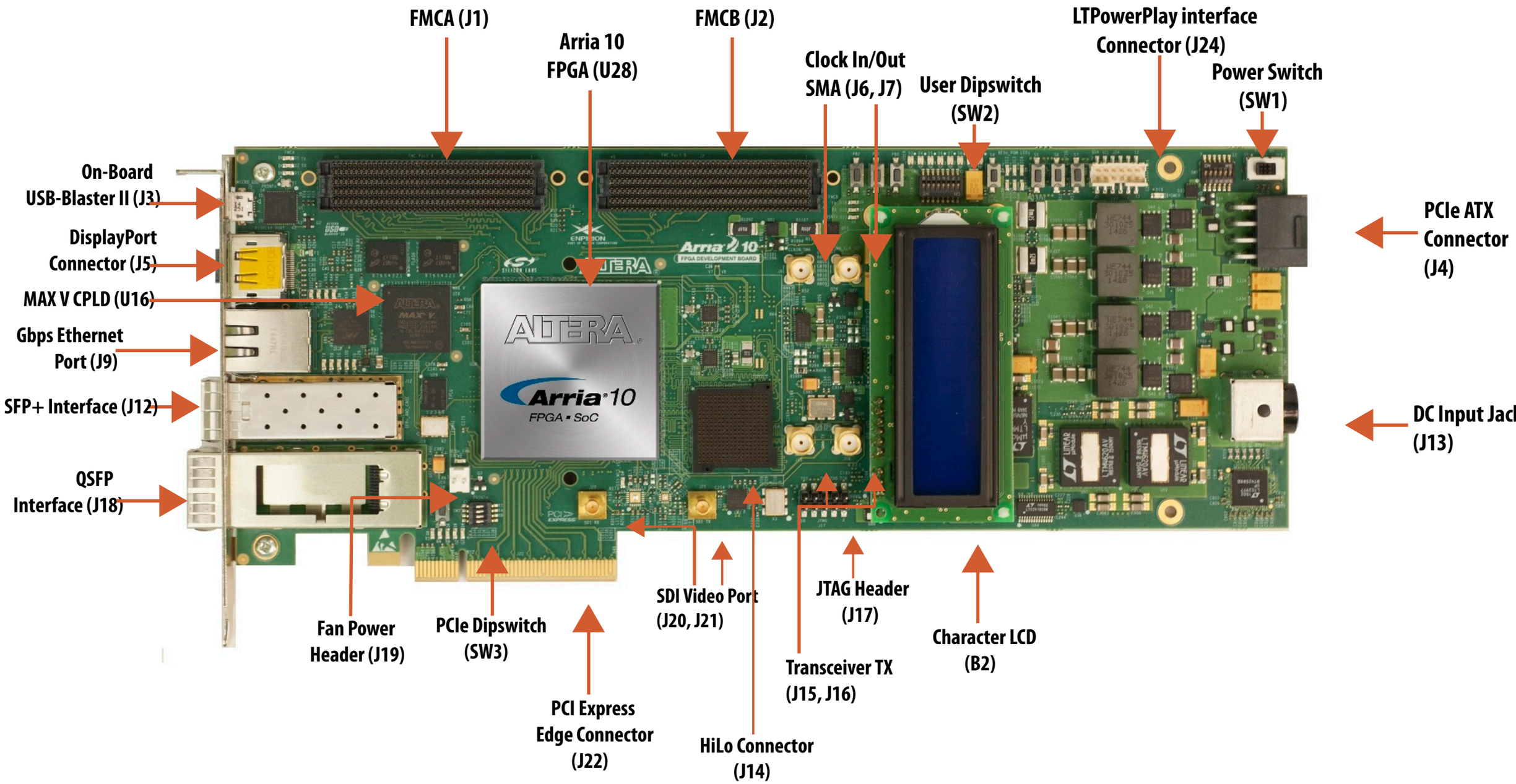
ALICE Format Data

Transport Headers and Trailers

Medium risk – mainly an FPGA programming effort, plus integration of clock, trigger, busy

Commercial Altera Development board for Common Readout Unit Prototyping and Programming

Figure 1-2: Overview of the Development Board Features

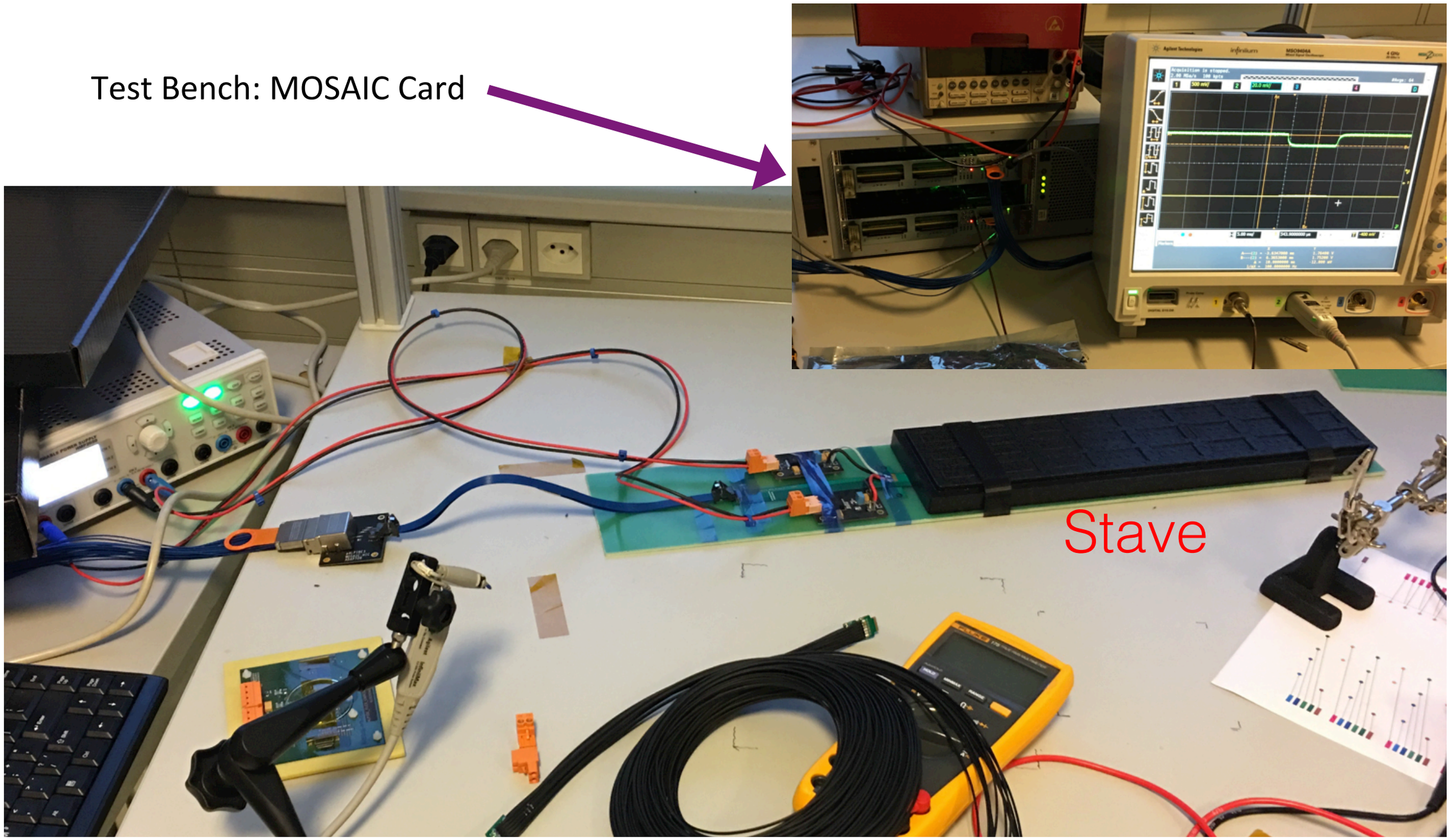


Risk reduction – Allows FPGA code development with same FPGA, fiber optic and PCI-x readout. Ordered

Alice Test Bench

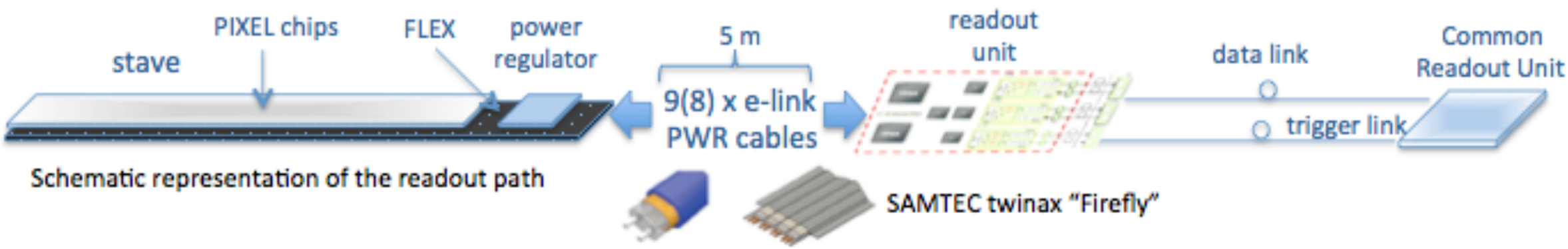
9-Chip Module High Speed Readout

Test Bench: MOSAIC Card



Risk reduction – provides high speed readout of stave now

Au+Au Relative Bandwidth



ALICE ITS IB is physical signal dominated

Event multiplicity reduction: RHIC / LHC = 7000/20000 = 0.35

Collision rate increase: RHIC / LHC = 200 kHz / 150 kHz = 1.33

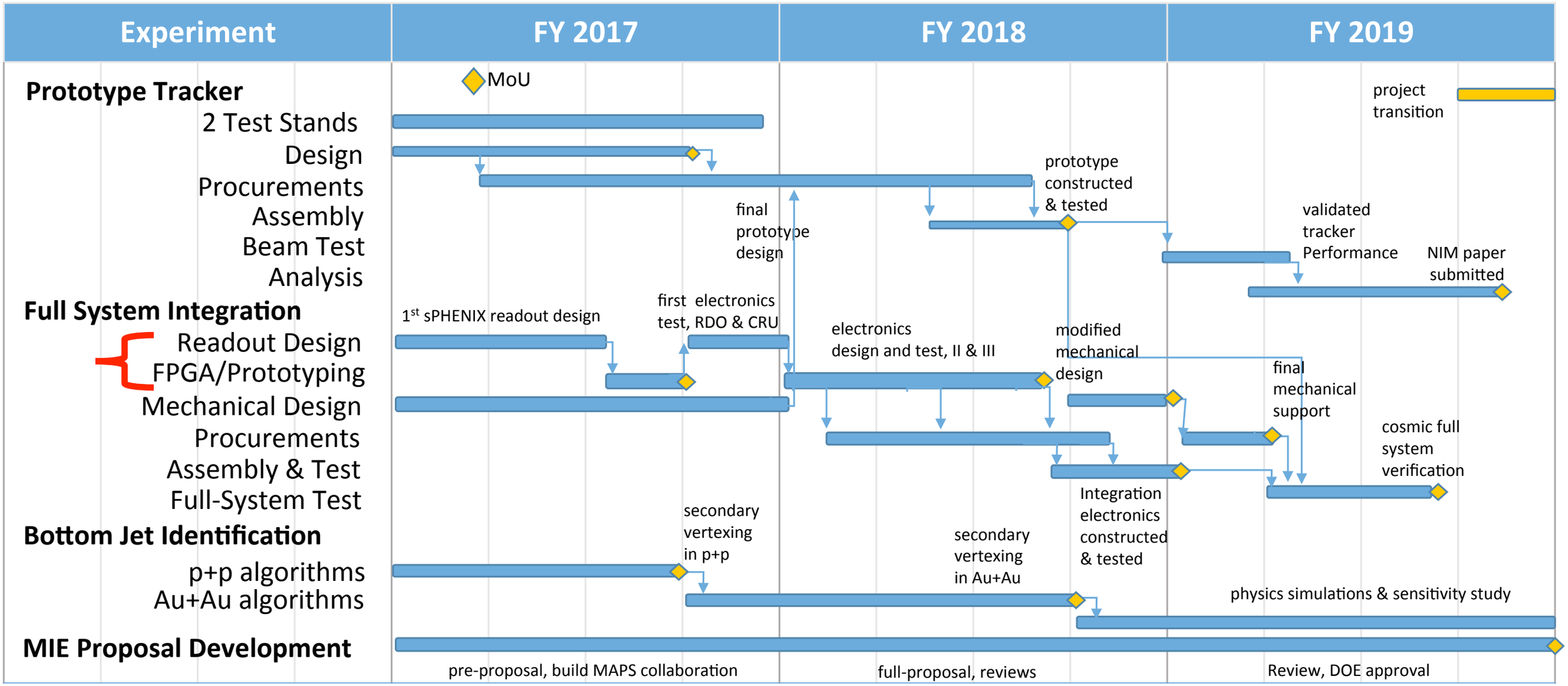
Continuous Stave-to-ROU link is ~50% bandwidth of ALICE ITS IB

Trigger rate reduction: RHIC / LHC = 15 kHz / 50 kHz = 0.30

Triggered ROU-to-CRU link is only ~15% bandwidth of ALICE ITS IB

Risk reduction – Easily manageable data rates

Schedule


Experiment
FY 2017
FY 2018
FY 2019
Prototype Tracker
2 Test Stands
Design
Procurements
Assembly
Beam Test
Analysis
Full System Integration
Readout Design
FPGA/Prototyping
Mechanical Design
Procurements
Assembly & Test
Full-System Test
Bottom Jet Identification
p+p algorithms
Au+Au algorithms
MIE Proposal Development
MoU
project transition
prototype constructed & tested
final prototype design
validated tracker Performance
NIM paper submitted
1st sPHENIX readout design
first electronics test, RDO & CRU
electronics design and test, II & III
modified mechanical design
final mechanical support
cosmic full system verification
Integration electronics constructed & tested
secondary vertexing in p+p
secondary vertexing in Au+Au
physics simulations & sensitivity study
pre-proposal, build MAPS collaboration
full-proposal, reviews
Review, DOE approval

Summary

Use all of existing MAPS readout infrastructure!

Reprogram Common Readout Unit for sPHENIX
- Add sPHENIX trigger and clock
- Add sPHENIX data formatting
- New FPGA coding

Have formed a large team of experts
- Are now associate members of ALICE
- Have access to ALICE hardware and collaborators

Low to medium risk with many paths to risk reduction