MAPS Readout Electronics

Cesar Da Silva, Andi Klein, Xuan Li, Sanghoon Lim, Ming Liu, Mike McCumber, Pat McGaughey, Mark Prokop

Los Alamos National Laboratory

LDRD DR Feasibility Review 12/5/16

articipants and Expertise

LANL P-25 (Physics), AOT (EE) Groups

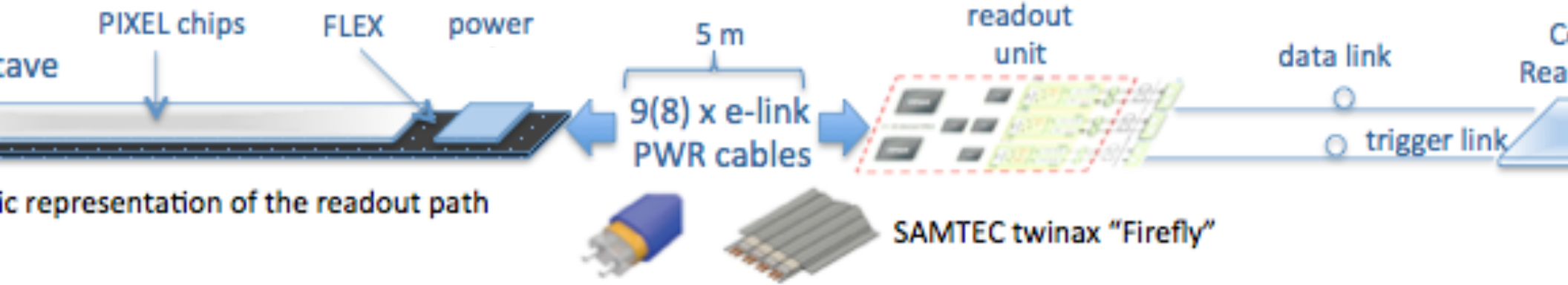
rtise gained from $5M PHENIX FVTX project + oth
pixel sensors and custom ASIC readout
alog / digital electronics design and layout
gh speed differential and fiber optic data transmiss
e of modern FPGAs from Xilinx, Actel
PGA programming with Verilog and VHDL
stom high density interconnects (FPC)
ent building and formatting
joined ALICE collaboration as associate member

expert help from BNL, LBNL, MIT, UNM, UT Austi

LPIDE monolithic Si pixel sensor (ALICE Pixel Detector)

APS readout:

- General design
- Readout Unit
  - Radiation hard design and fiber optic
- Common Readout Unit
  - Development board
- Test bench
- Expected data rates

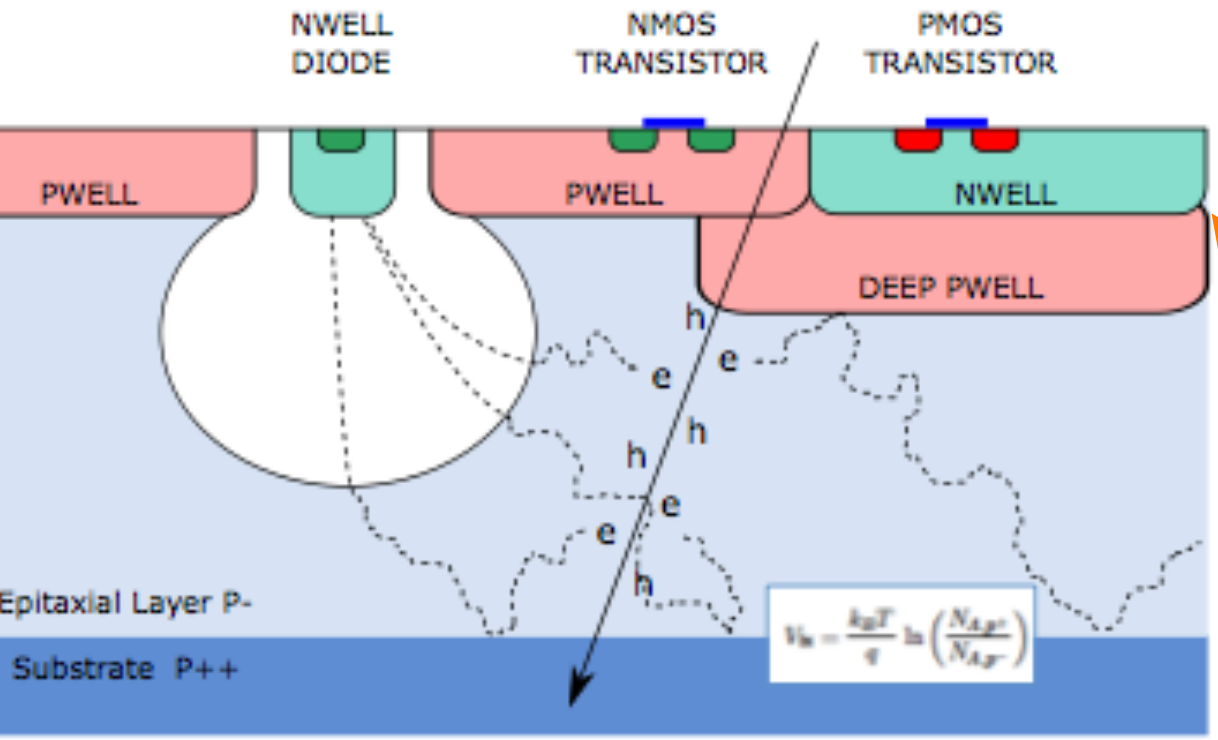


ic representation of the readout path

5 meter cable

ummary

MOS Pixel Sensor using TowerJazz 0.18µm CMOS Imaging Process



deep p-well allows for ci

Tower Jazz 0.18 µm CMOS

- feature size 180 nm
- metal layers 6
- gate oxide 3nm

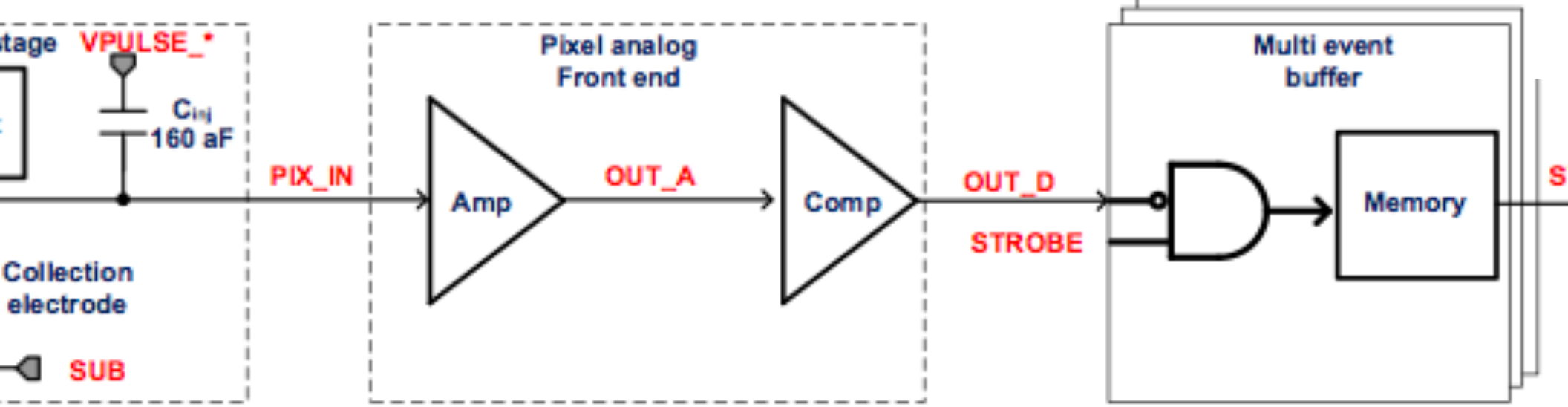
substrate: $N_A \sim 10^{18}$
epitaxial layer: $N_A \sim 10^{13}$
deep p-well: $N_A \sim 10^{16}$

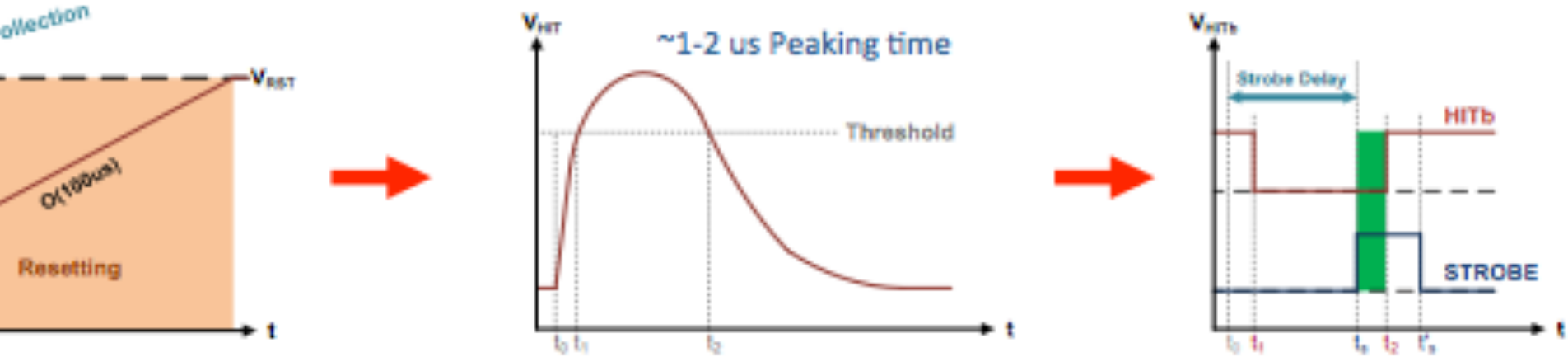
High-resistivity (> 1kΩ cm) p-type epitaxial layer (18µm to 30µm) on p-type substra

Small n-well diode (2 µm diameter), ~100 times smaller than pixel => low capacitan

Application of (moderate) reverse bias voltage to substrate (contact from the top) used to increase depletion zone around NWELL collection diode

Deep PWELL shields NWELL of PMOS transistors to allow for full CMOS circuitry wit active area





ultra low-power front-en
40nW / pixel

nd acts as delay line

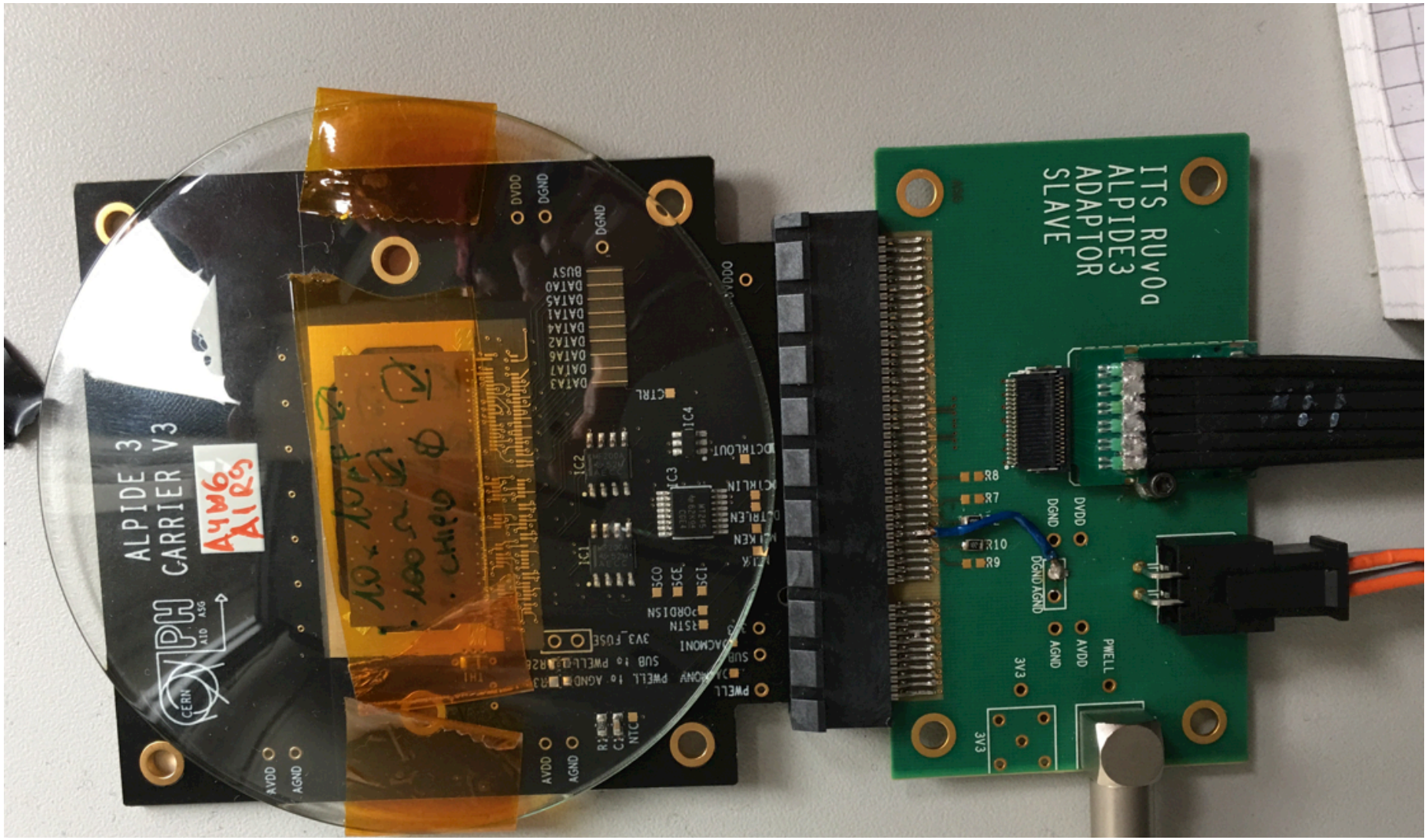
or and front-end continuously active

n particle hit front-end forms a pulse with ~1-2µs peaking time

shold is applied to form binary pulse

Single Chip High Speed Readout

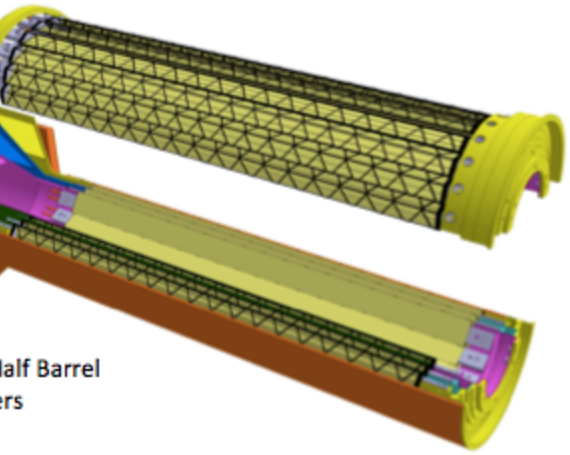
mm
area



e one MAPS chip and slow readout working at LA
more on the way

MAPS Readout Description

Staves



Passive electrical (copper) links, up to 1.2 Gb/s (data and control @ 40 Mb/s)

GBT optical

Trigger

One way, passive optical splitting, no busy back

Clock

Control

Data (960 Mb/s max)

5 meter cable

GBT optical

Control

Data (9.6 Gb/s

FPGA

FPGA

x 48

Identical Readout Units (RU) cover the full ITS

Readout Unit is
to one stave

Clock

Control

Data (960 Mb/s max)

GBT optical

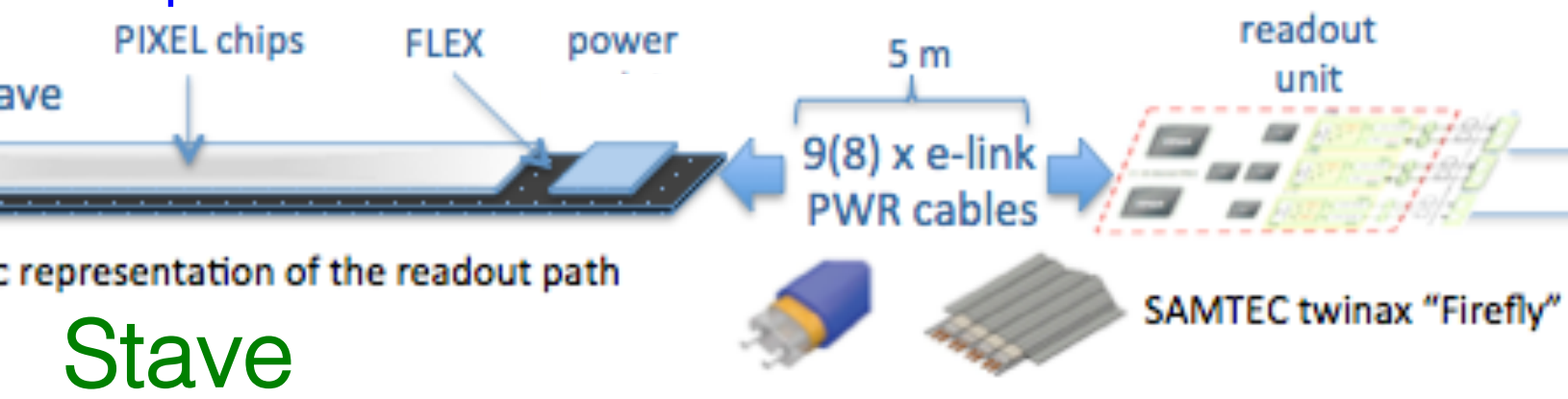
Control

Data (9.6 Gb/s

FPGA

FPGA

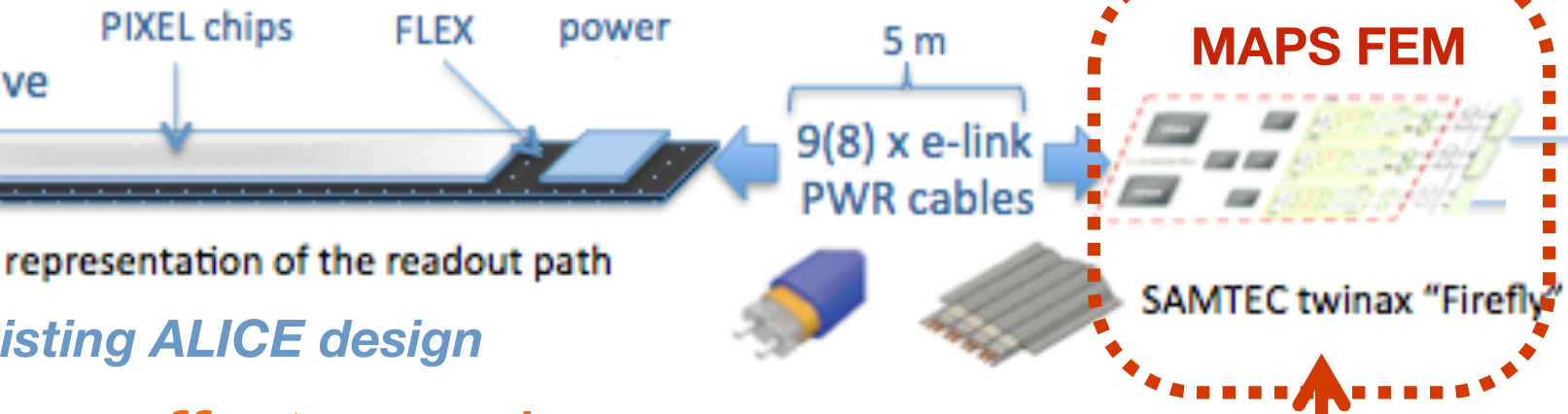
ALICE readout path



Stave

Pla
repro
Co
Read

an B: sPHENIX readout path (held only as contingenc



isting ALICE design

ger effort, requires new
dware and FPGA code!

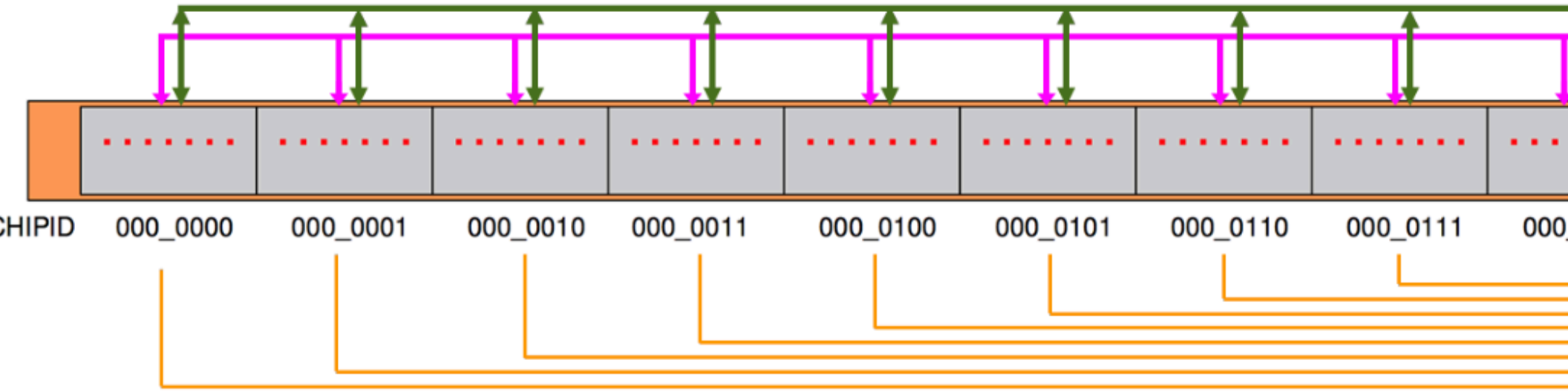
trigger in

modified design,
starting with ALICE boards

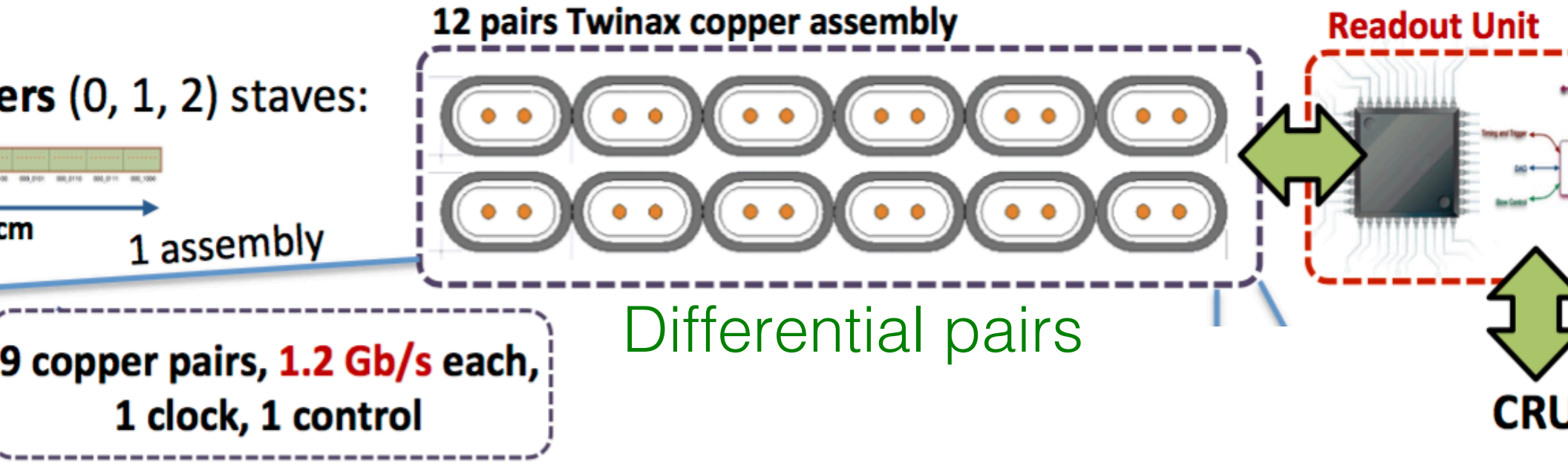
DC
k
bus
exi

Stave Readout

9 fully independent Alpide chips per Stave

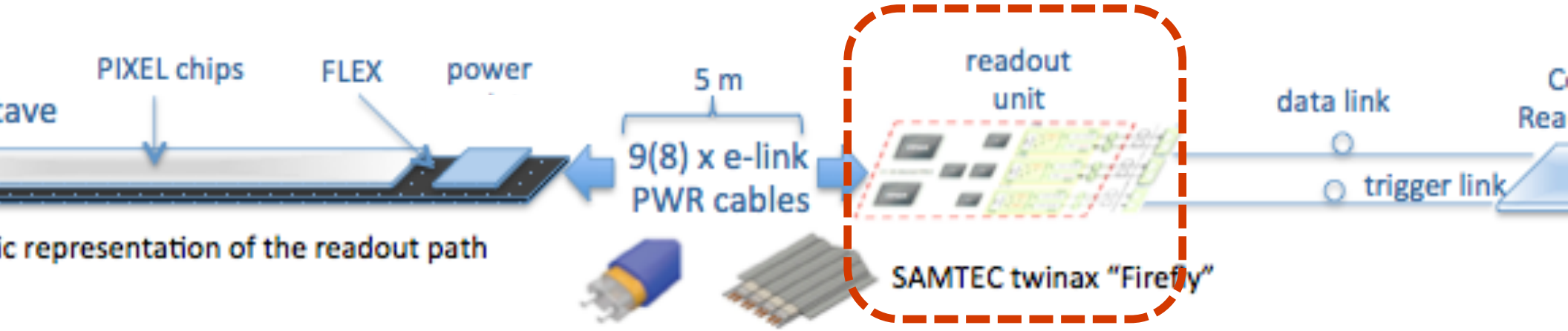


Continuous readout →



Medium Risk - Staves available in Summer 2017

ALICE Readout Unit Logic



ic representation of the readout path

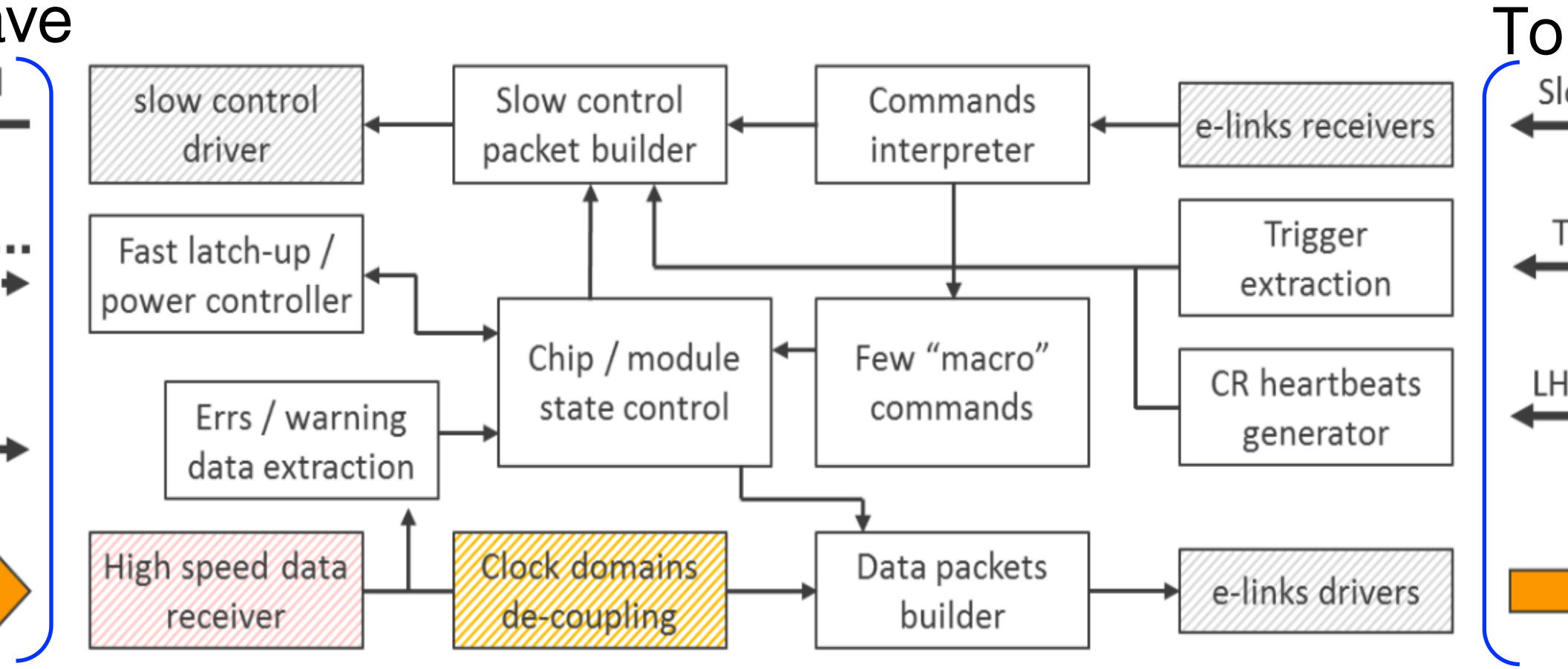
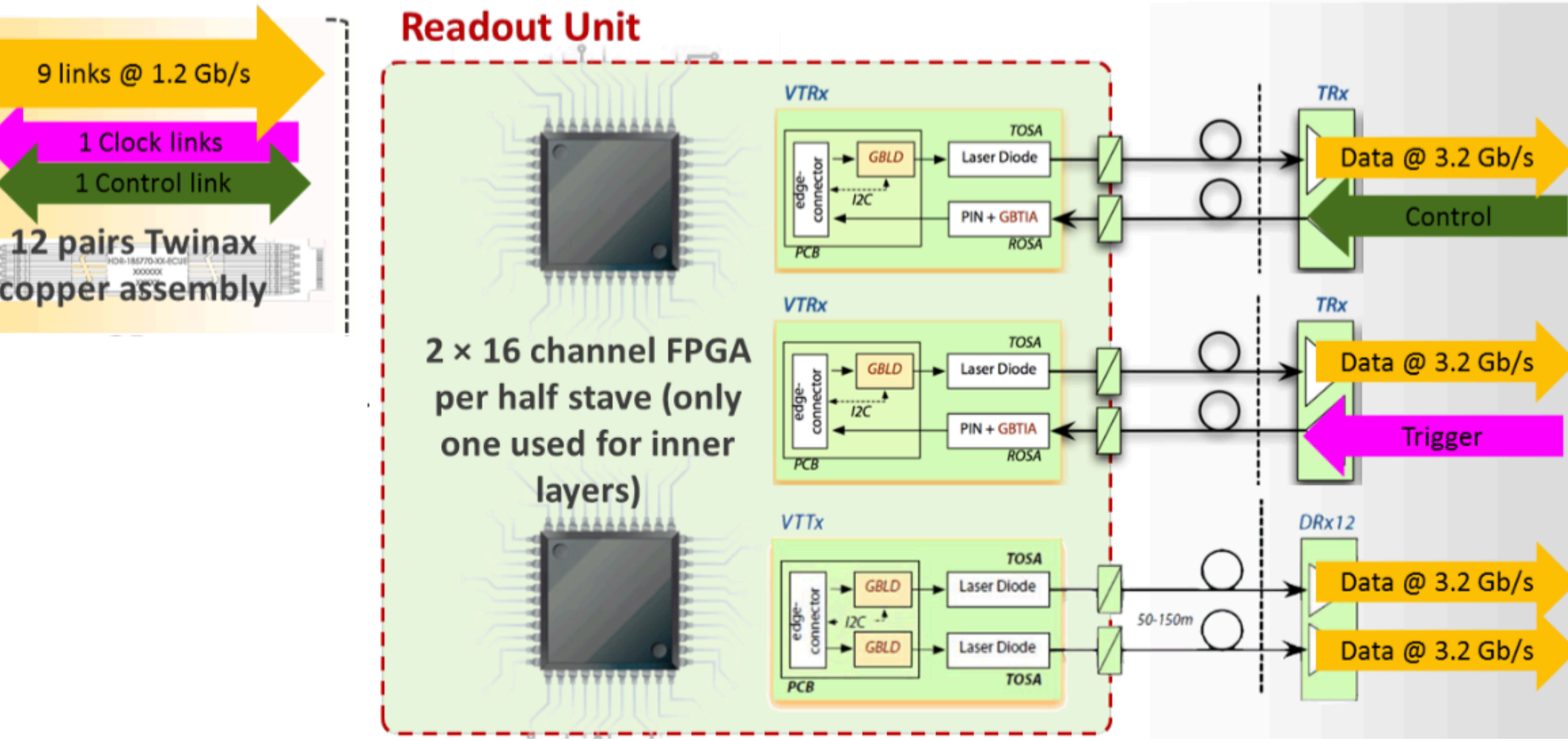
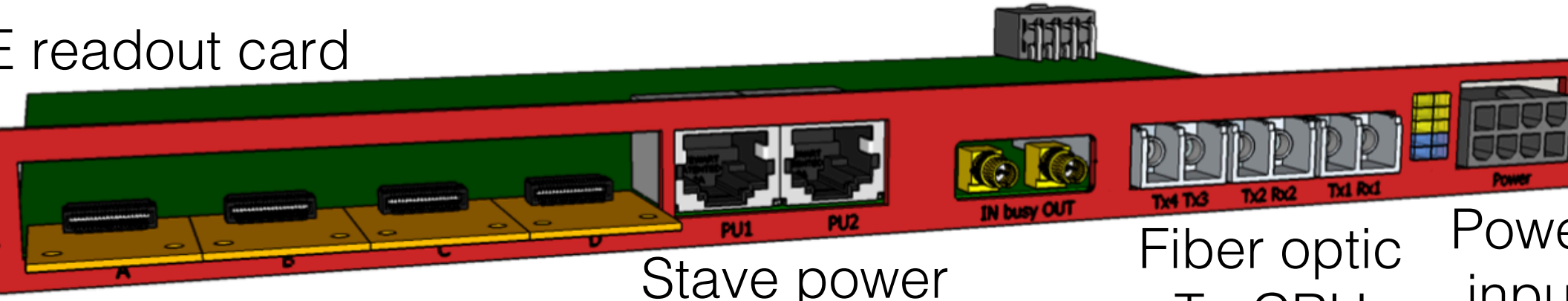
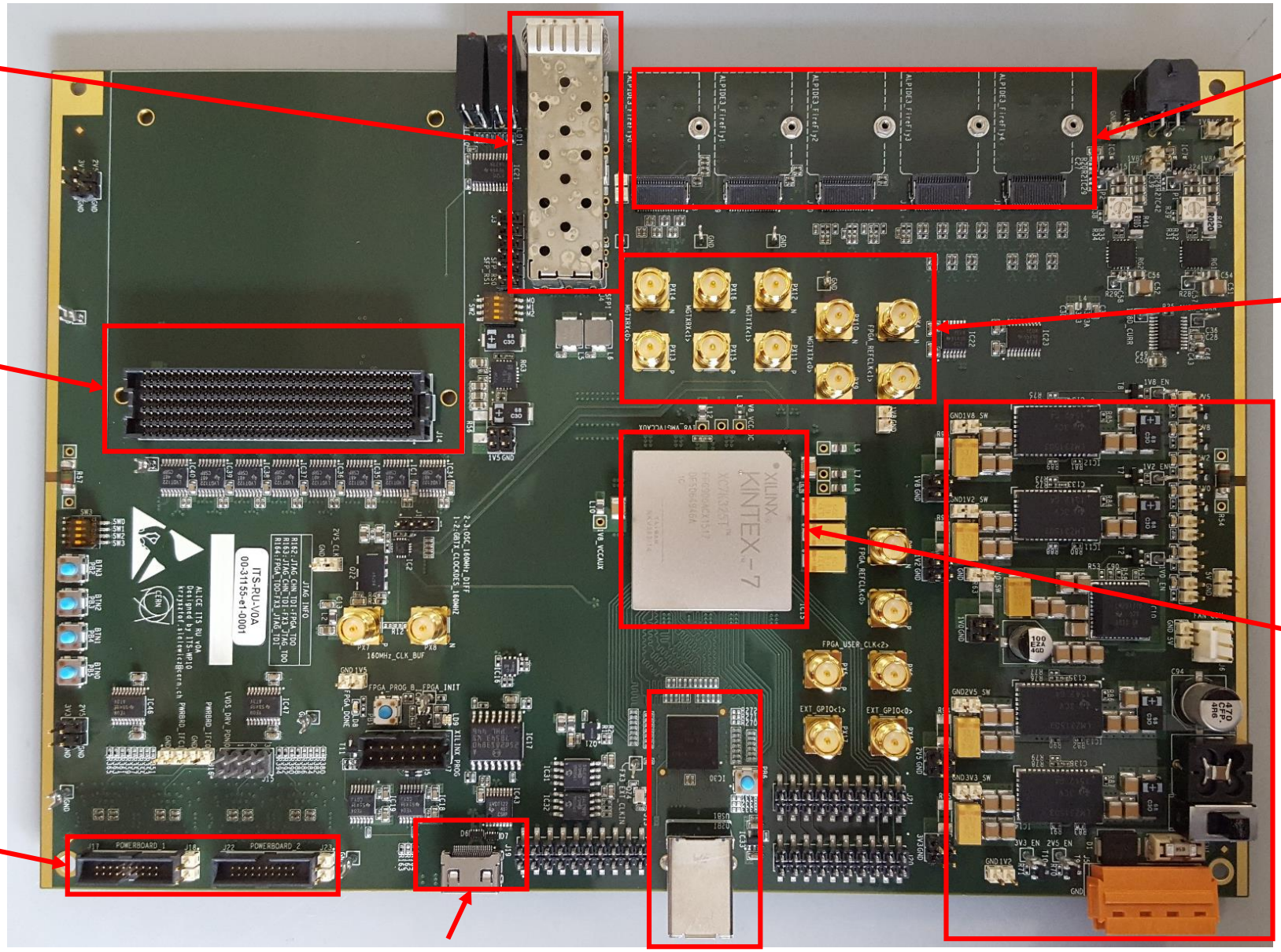


Figure 9 –Readout Electronics main functions.

ALICE Readout Unit



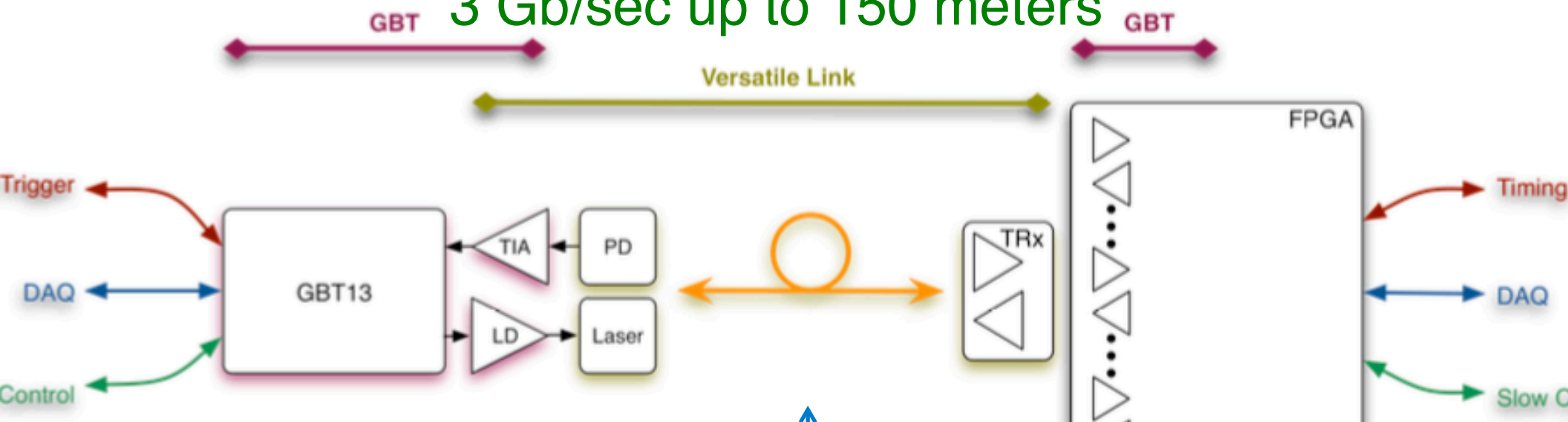




Low risk, currently being tested by ALICE

ject version ‘0’ readout unit at LANL in spring, 201

3 Gb/sec up to 150 meters



Readout unit

On-Detector

Custom Electronics & Packaging

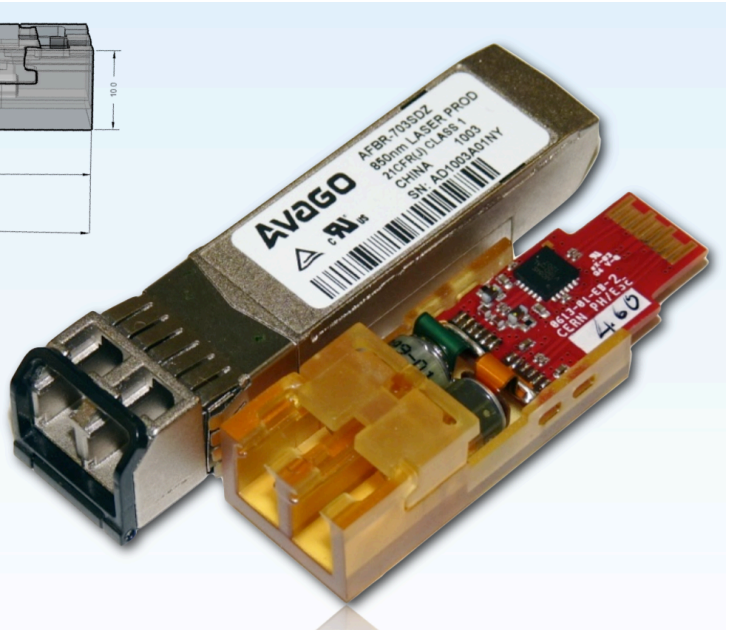
Radiation Hard

Off-Detector

Commercial Off-The-Shelf (COTS)

Custom Protocol

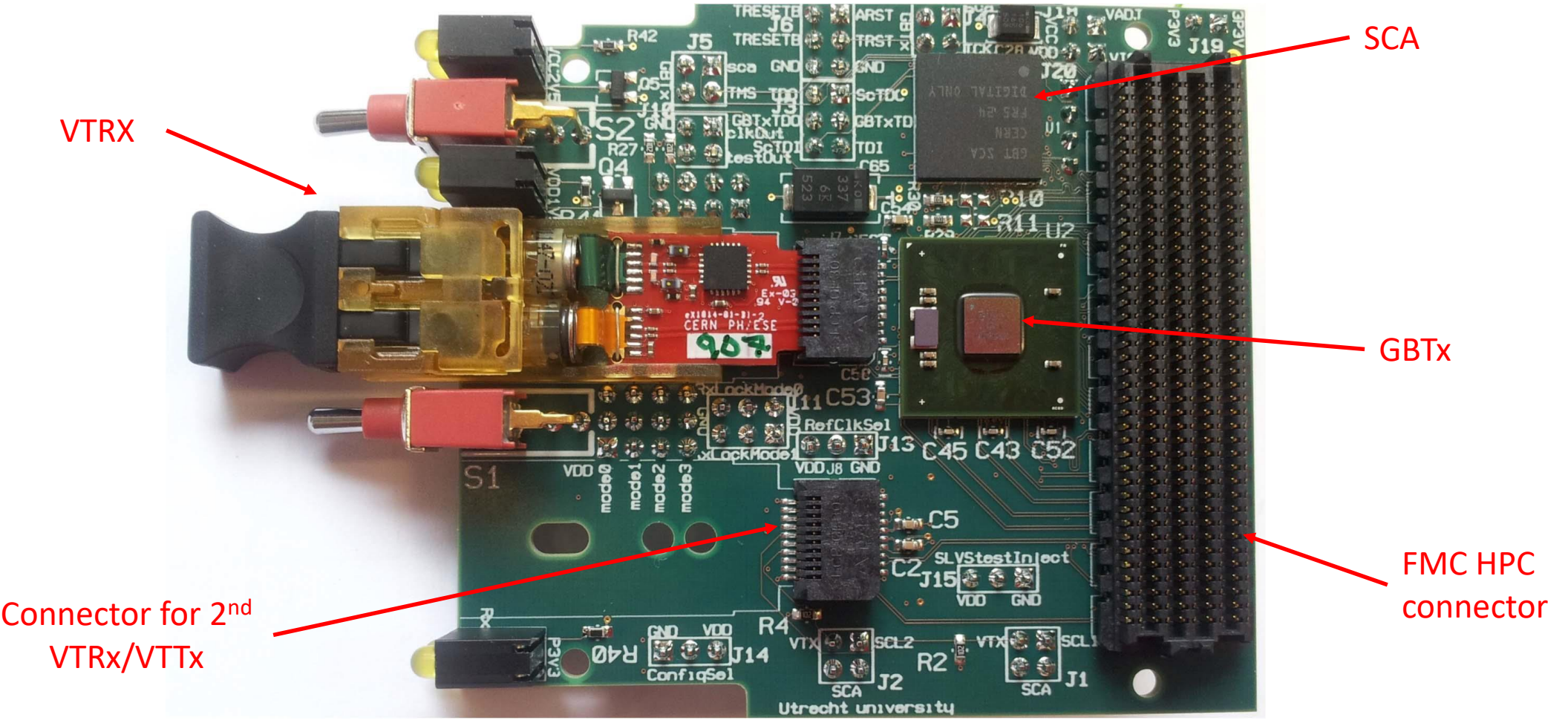
Common readout unit
In counting house



Long fiber run from Hall to Rack Room
over custom CERN optical link

readout unit

GBT FMC Mezzanine ("GBTxFMC")



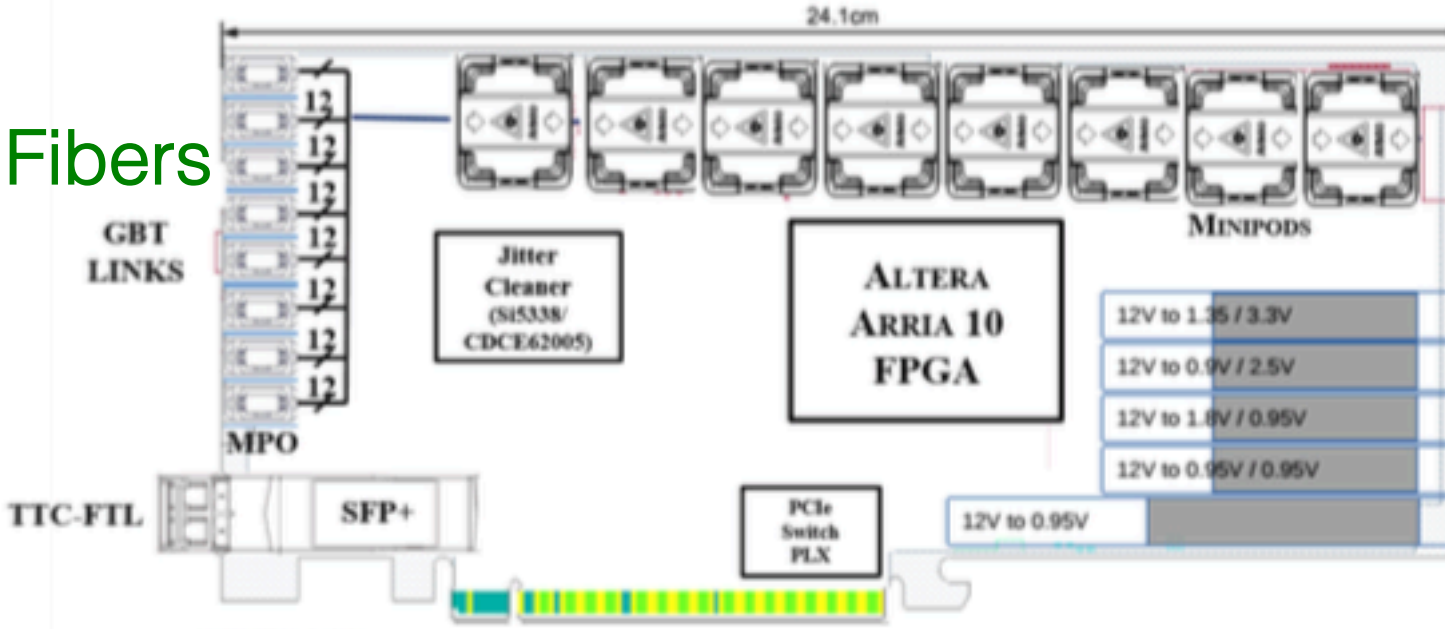
Low risk, tested and operational

order for LANL in process

CI express card

(a) PCie40.

Avago optical engines



(b) PCIe40 Schematic.

be used by several ALICE and sPHENIX subsytem

CRU reads out two Readout units, sends slow

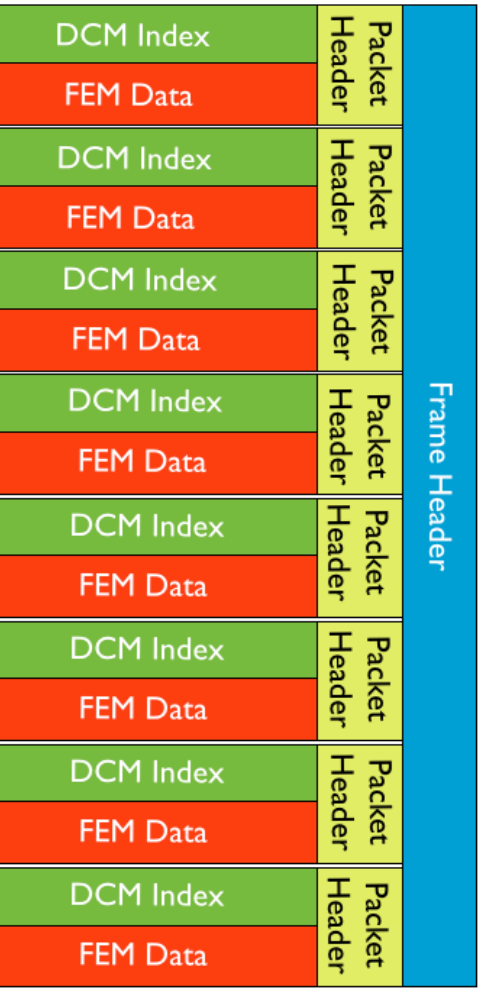
ontrols, trigger back

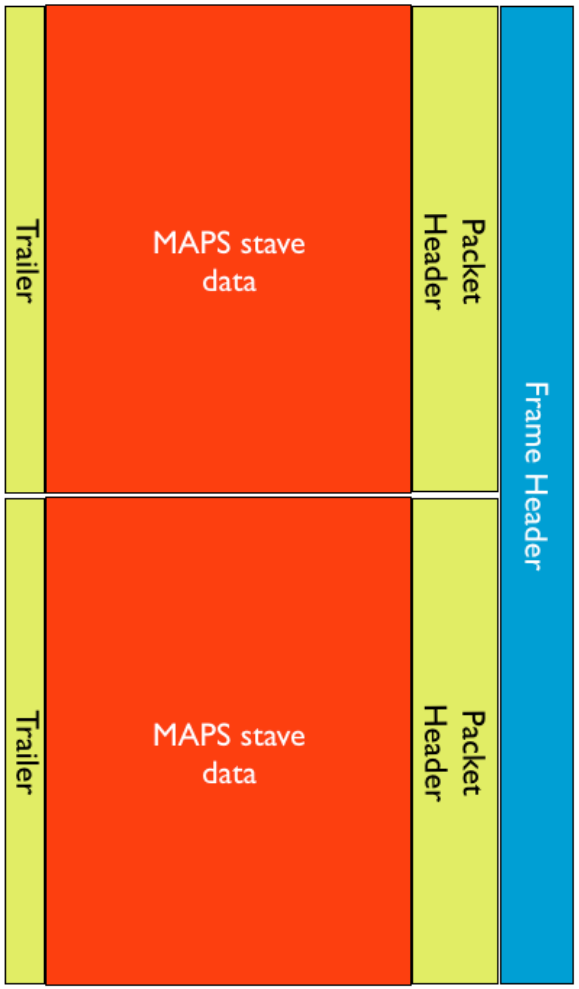
cards reside in CPU chassis

um risk, CRU still in development at LHCb experi

Traditional
ENIX Frame

sPHENIX MAPS
Common Readout Frame





Reformat o
FPGA or C

(a) PCie40.

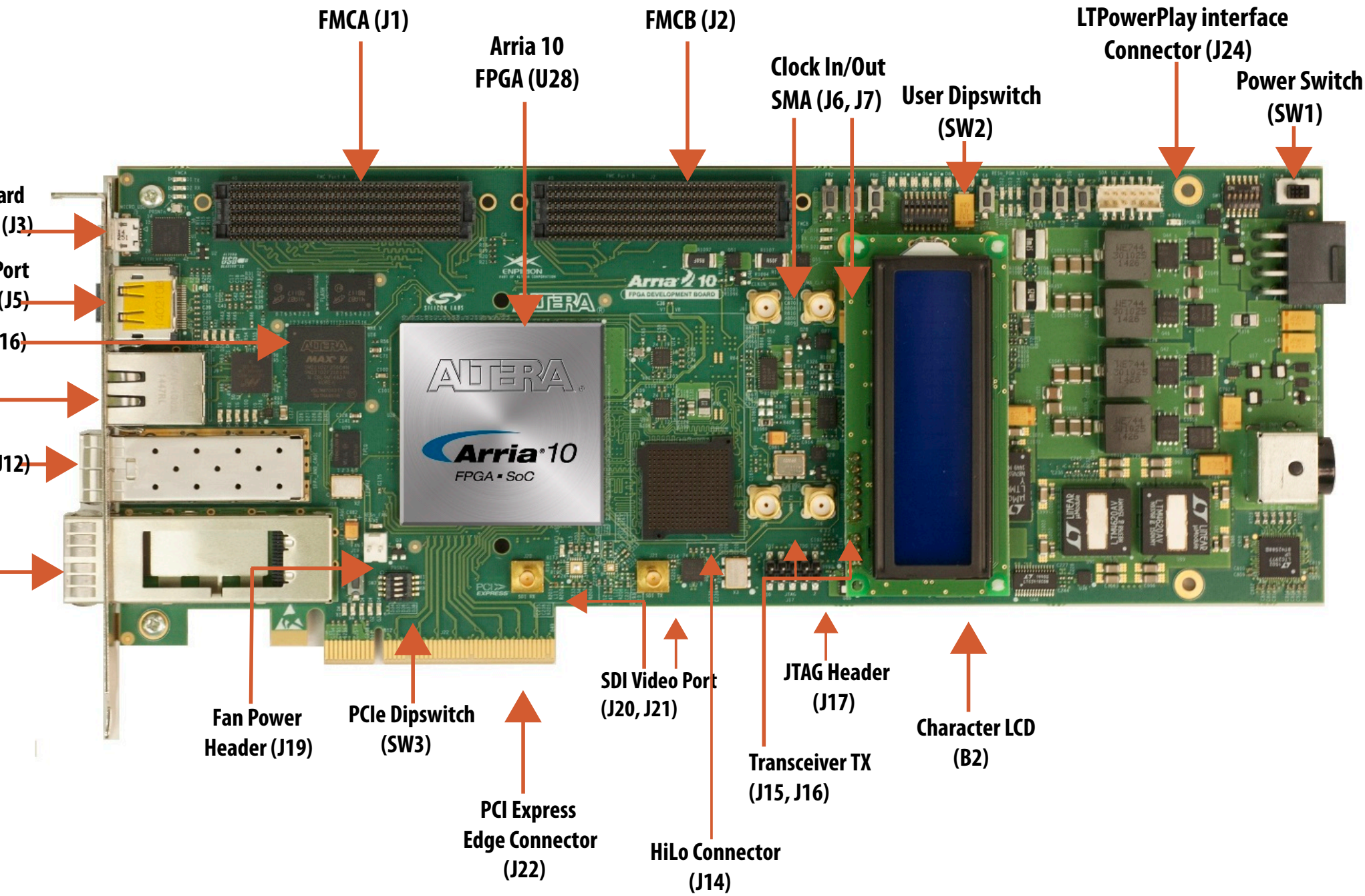
ALICE Format Data

Transport Headers and Trailers

edium risk – mainly an FPGA programming effort,

Readout Unit Prototyping and Programming

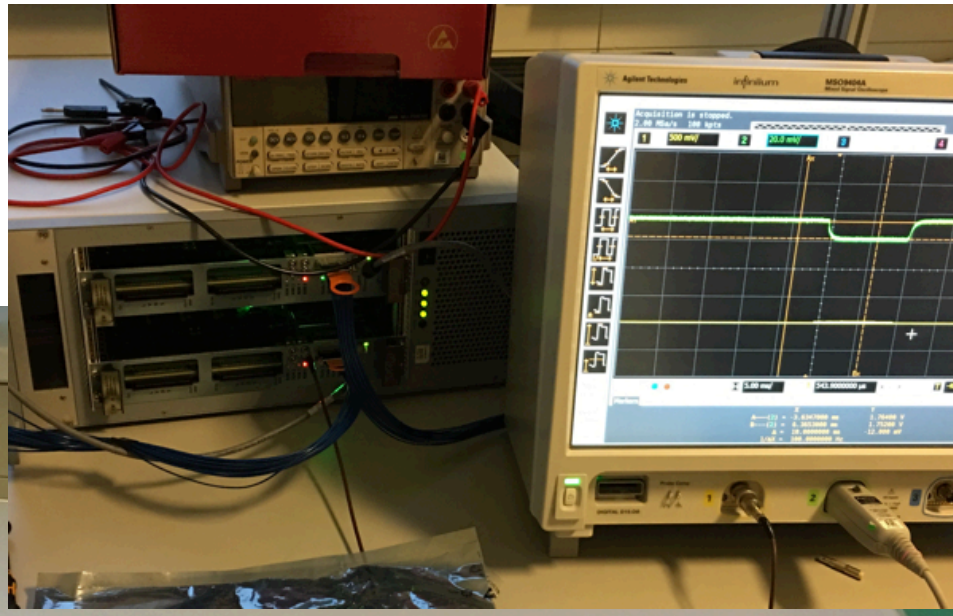
-2: Overview of the Development Board Features



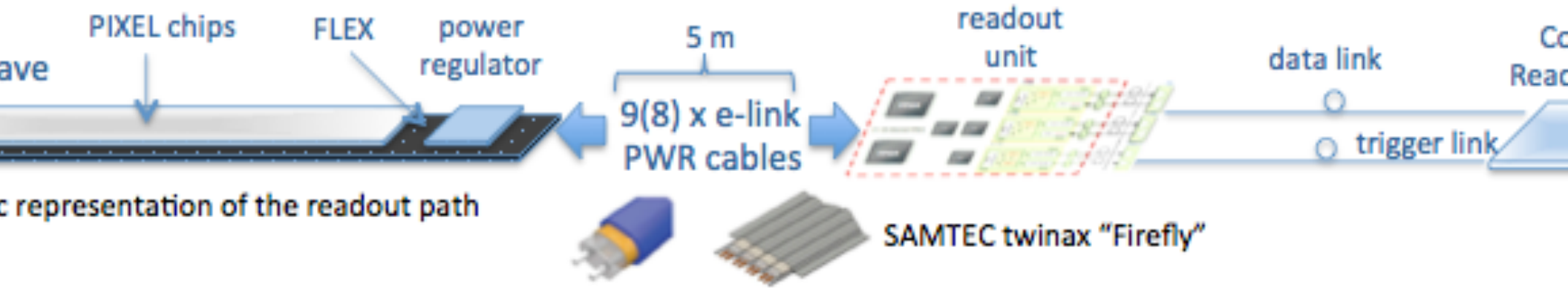
reduction – Allows FPGA code development with

9-Chip Module High Speed Readout

Test Bench: MOSAIC Card



Stave



ALICE ITS IB is physical signal dominated

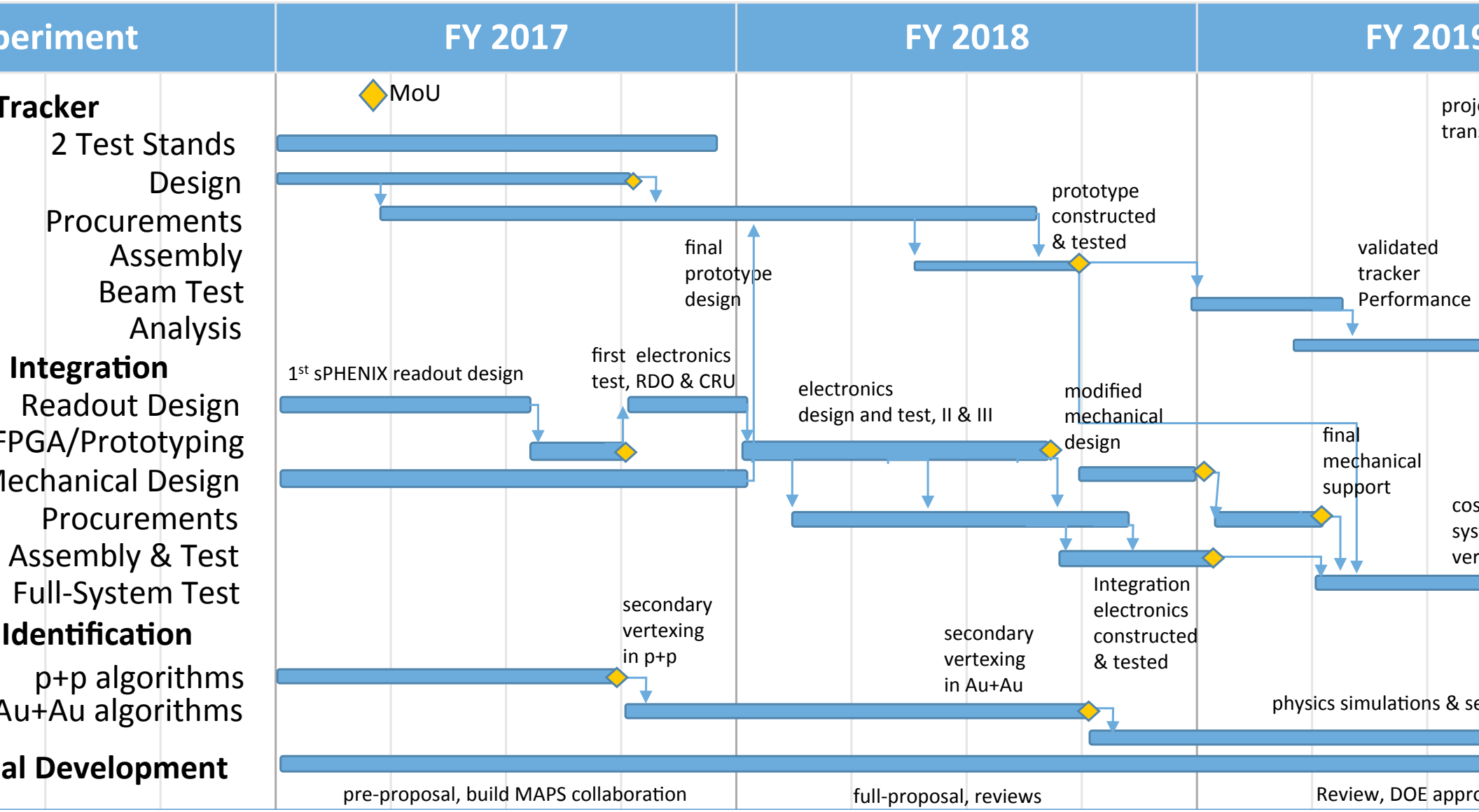
ent multiplicity reduction: RHIC / LHC = 7000/20000 = 0.35
llision rate increase: RHIC / LHC = 200 kHz / 150 kHz = 1.33

ontinuous Stave-to-ROU link is ~50% bandwidth of ALICE ITS IB

rigger rate reduction: RHIC / LHC = 15 kHz / 50 kHz = 0.30

ggered ROU-to-CRU link is only ~15% bandwidth of ALICE ITS I

sk reduction – Easily manageable data rates


periment
FY 2017
FY 2018
FY 201
Tracker
2 Test Stands
Design
Procurements
Assembly
Beam Test
Analysis
Integration
Readout Design
FPGA/Prototyping
Mechanical Design
Procurements
Assembly & Test
Full-System Test
Identification
p+p algorithms
Au+Au algorithms
al Development
MoU
1st sPHENIX readout design
first electronics test, RDO & CRU
final prototype design
prototype constructed & tested
electronics design and test, II & III
modified mechanical design
validated tracker Performance
final mechanical support
Integration electronics constructed & tested
secondary vertexing in p+p
secondary vertexing in Au+Au
physics simulations & se
pre-proposal, build MAPS collaboration
full-proposal, reviews
Review, DOE appro

Use all of existing MAPS readout infrastructure!

Reprogram Common Readout Unit for sPHENIX
- Add sPHENIX trigger and clock
- Add sPHENIX data formatting
- New FPGA coding

Have formed a large team of experts
- Are now associate members of ALICE
- Have access to ALICE hardware and collaborat

Low to medium risk with many paths to risk reducti