MAPS LDRD

Experimental Cost, Schedule, Risk and Procurements

Cesar da Silva , Ming Liu

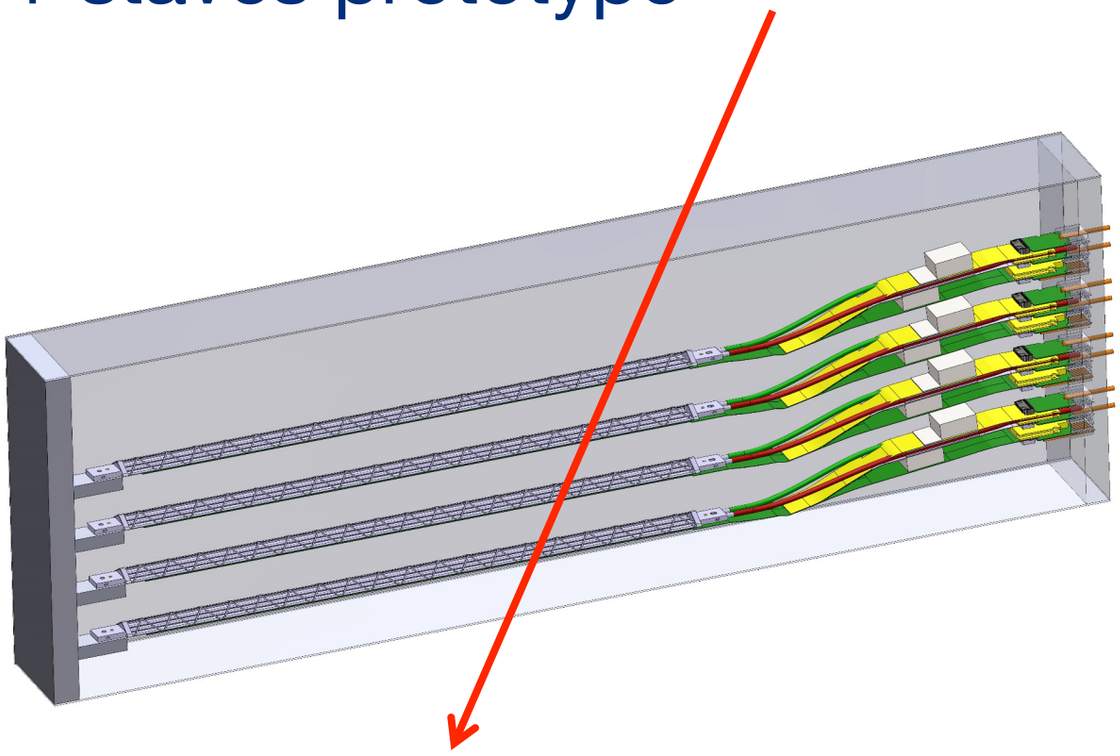
Charge

- Project Organization
- Project Plan
- Technical Aspects
- Cost
- Schedule
- Risk
- Critical Procurements

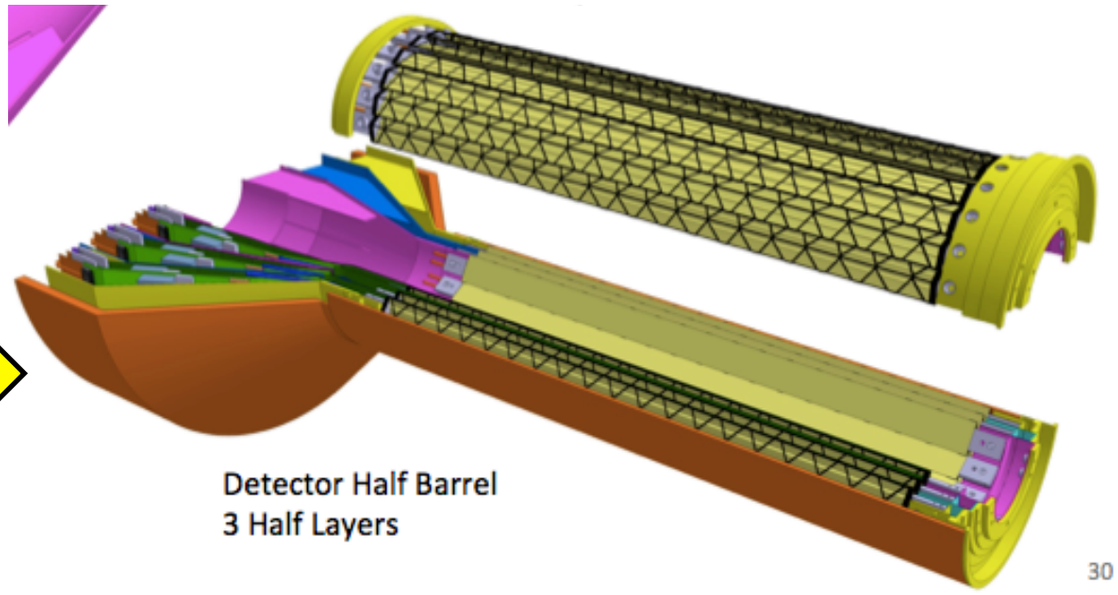
Technical Goals

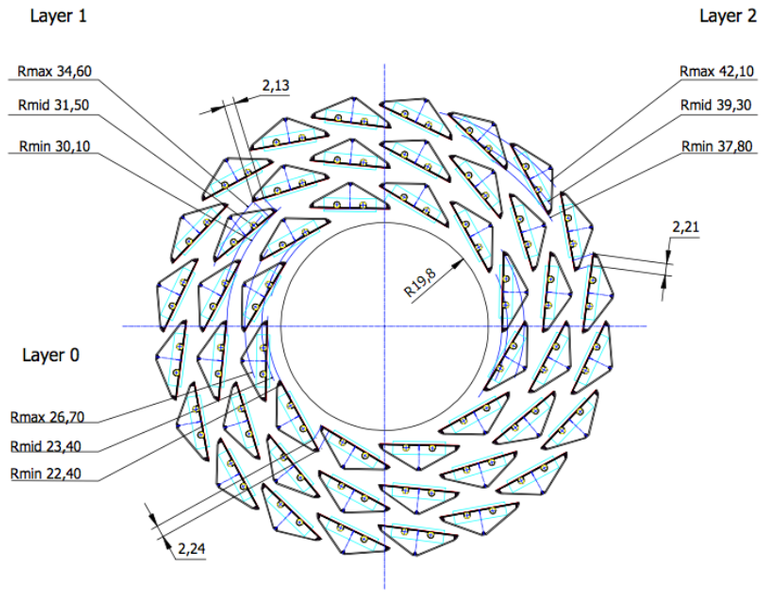
LDRD GOAL

4-staves prototype

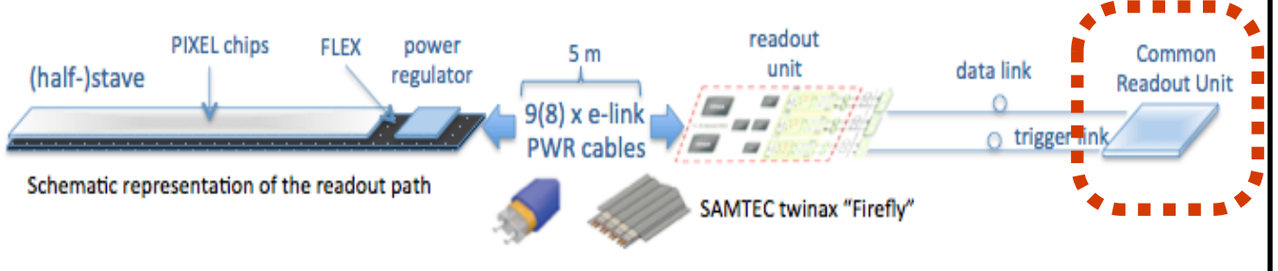


DOE MAPS PROJECT GOAL





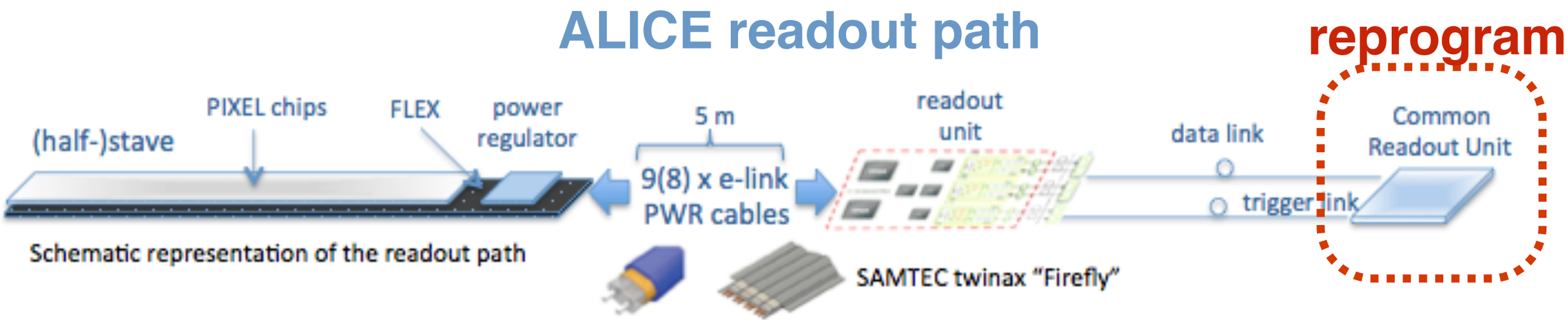
Readout firmware



Schematic representation of the readout path

LDRD MAPS Electronics Goal

Plan A: reprogram



- Obtain 4 staves from CERN, get readout board and common readout unit chain working at LANL
- rewrite the FPGA code to wrap the data with the sPHENIX formatting
- test it with sPHENIX readout system

- Plan B: design a readout interface board to convert ALICE data format into sPHENIX standard

Project Organization

Co-PIs
Mike McCumber
Ivan Vitev

Advisor
Melynda Brooks

Project Manager
Ming Liu (LANL)

Program Manager for LANL NP programs
Joe Carlson

Test Stand
WBS 3.2, 3.3
Hubert van Hecke

- *Procurement*
- *Setup*

Stave Production
WBS 3.4
Ming Liu

- *Procurement*
- *Assembly at CERN*
- *Tests*

Readout Electronics
WBS 3.5
Pat McGaughey

- *Review*
- *Firmware Programming*
- *Tests*

Mechanics
WBS 3.9
Walt Sondheim

- *Structure Design for prototype*
- *Final detector design*

Theoretical Effort
WBS 3.16
Ivan Vitev

- *pQCD*
- *Lattice/Hydro*
- *Molecular Dynamic Simulation*

Software
WBS 3.13
Sanghoon Lim

- *Simulation*
- *Offline*
- *B-jet tagging*

Initial Assignments

① sPHENIX readout and trigger requirements (DCM2, JSEB etc) – Mike and Ming

② MAPS CRU readout - Mark, Ming, Pat

- Physical parameters (PCIex4)
- Data format
- Electrical signal, lack of busy etc
- sPHENIX trigger/busy inputs and clock

③ Detailed specs/understanding of MAPS/ ALIPED-3(4 ~ final) test card – Pat, Cesar and Andi

④ BNL specifies cabling/material electrical and fire safety etc – Walt, Hubert, Eric*

⑤ Radiation enviroenment, damage, occupancy, SEU; Configuration and Operation, programing and initializatio etc – Mark, Xuan

⑥ Power needs:

- (LANL LDRD) Hubert and Ming;
- (BNL sPHENIX) Hubert, Eric*
- Staves, readout control etc. (A, V)

* From BNL

⑦ Mechanics – Walt, Hubert, Jin*

- Structure, cooling, alignment, assembly and integration

⑧ Integration into sPHENIX – Walt, Eric

⑨ Test stands setup and operation

- Single chip readout – Mike, Pat
- Staves and cosmic ray - Xuan Cesar
- Mockup, electrical, readout, power – Sanghoon, Hubert, Walt

⑩ FPGA firmware – Andi, Mark, Cesar, Ming and Pat

- VHDL, Verilog

11 Software – Sanghoon and Andi

- Slow controls, electronics
- Test software, root-based

12 Beam test – Ming and team

- LANL, FNAL, rad damage at LANSCE

13 Web page – Hubert, Pat

- R+W access
- Tree structure
- https://p25ext.lanl.gov/maps/

Project Management

Work Breakdown Structure

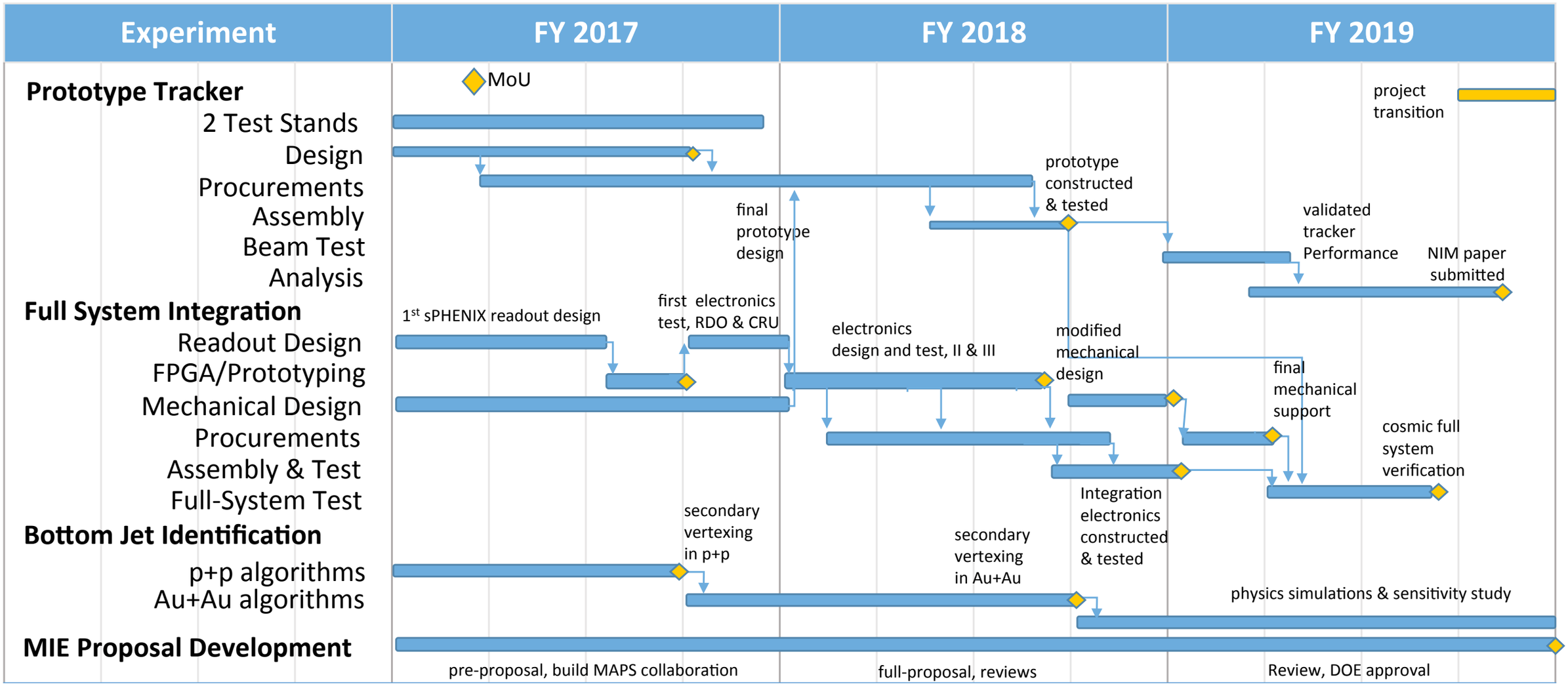
WBS	Task Name	Duration	Start	Finish	Fixed Cost	Cost	Activity	Cost per Unit	Resource Cost
1	**ALICE ITS Key Tasks**	**0 days**	**Mon 1/2/17**	**Mon 1/2/17**	**$0.00**	**$0.00**		**$0.00**	**$0.00**
1.1	ALICE MAPS Production (7/17)	240 days?	Mon 11/28/16	Fri 10/27/17	$0.00	$0.00		$0.00	$0.00
1.2	ALICE ITS IB FPC Production (9/17)	135 days	Mon 2/27/17	Fri 9/1/17	$0.00	$0.00		$0.00	$0.00
1.3	ALICE ITS IB Stave Frame Production Ends (1/18)	240 days?	Wed 2/1/17	Tue 1/2/18	$0.00	$0.00		$0.00	$0.00
1.4	ALICE ITS IB Stave Assembly (3/18)	266 days	Mon 2/27/17	Mon 3/5/18	$0.00	$0.00	ITS co	$0.00	$0.00
1.5	ALICE ITS Electronics Pre-Production (7/17)	100 days	Mon 3/13/17	Fri 7/28/17	$0.00	$0.00	ITS El	$0.00	$0.00
1.6	ALICE ITS Electronics Production (6/18)	240 days	Mon 7/31/17	Fri 6/29/18	$0.00	$0.00	ITS El	$0.00	$0.00
2	**LDRD Milestones & Critical Tasks**	**781 days**	**Mon 10/3/16**	**Mon 9/30/19**	**$0.00**	**$0.00**		**$0.00**	**$0.00**
2.1	LDRD Start and End	781 days	Mon 10/3/16	Mon 9/30/19	$0.00	$0.00		$0.00	$0.00
2.2	Complete MoU LANL-ALICE	0 days	Fri 12/9/16	Fri 12/9/16	$0.00	$0.00		$0.00	$0.00
2.3	Setup ALICE Readout Test Stands	0 days	Fri 9/15/17	Fri 9/15/17	$0.00	$0.00		$0.00	$0.00
2.4	Preliminary readout design to interface sPHENIX DAQ	0 days	Wed 11/1/17	Wed 11/1/17	$0.00	$0.00		$0.00	$0.00
2.5	Prototype Test during sPHENIX Test Beam Run	21 days	Fri 2/1/19	Fri 3/1/19	$0.00	$0.00		$0.00	$0.00
3	**LANL LDRD**	**781 days**	**Mon 10/3/16**	**Mon 9/30/19**	**$0.00**	**$2,959,568.00**	**LANL**	**$0.00**	**$2,579,068.00**
3.1	MOU btw LANL and ALICE for R&D	50 days	Mon 10/3/16	Fri 12/9/16	$0.00	$18,400.00		$0.00	$18,400.00
3.2	**Obtain Designs from ALICE**	**30 days**	**Mon 12/12/16**	**Fri 1/20/17**	**$0.00**	**$82,800.00**		**$0.00**	**$82,800.00**
3.3	**Setup Alice Readout Test Stand**	**200 days**	**Mon 12/12/16**	**Fri 9/15/17**	**$0.00**	**$135,760.00**		**$0.00**	**$75,760.00**
3.4	**Procure R&D ALICE Staves**	**195 days**	**Mon 2/27/17**	**Fri 11/24/17**	**$0.00**	**$553,720.00**		**$0.00**	**$466,720.00**
3.5	**Procure ALICE Electronics & Cables**	**205 days**	**Mon 12/12/16**	**Fri 9/22/17**	**$0.00**	**$150,020.00**		**$0.00**	**$71,520.00**
3.6	**Readout R&D**	**345 days**	**Mon 1/23/17**	**Fri 5/18/18**	**$0.00**	**$137,840.00**		**$0.00**	**$137,840.00**
3.7	**Electronics Final Design Review**	**12 days**	**Mon 5/21/18**	**Tue 6/5/18**	**$0.00**	**$25,088.00**		**$0.00**	**$15,088.00**
3.8	Prototype readout assembled and tested	90 days	Wed 6/6/18	Tue 10/9/18	$0.00	$23,760.00		$0.00	$23,760.00
3.9	**Mechanical Support and Cooling**	**200 days**	**Mon 1/23/17**	**Fri 10/27/17**	**$0.00**	**$236,160.00**		**$0.00**	**$181,160.00**
3.10	**Prototype Assembly and Test**	**90 days**	**Mon 2/26/18**	**Fri 6/29/18**	**$0.00**	**$114,240.00**		**$0.00**	**$114,240.00**
3.11	Mechanical Conceptual Design	60 days	Mon 7/2/18	Fri 9/21/18	$0.00	$18,240.00		$0.00	$18,240.00
3.12	Mechanical Conceptual Design Review	**12 days**	**Mon 9/24/18**	**Tue 10/9/18**	**$0.00**	**$33,920.00**		**$0.00**	**$23,920.00**
3.13	**Softrware Tool Development and Analysis**	**500 days**	**Mon 1/23/17**	**Fri 12/21/18**	**$0.00**	**$351,200.00**		**$0.00**	**$351,200.00**
3.14	**Detector Optimizaation and Physics Simulations (MIE)**	**700 days**	**Mon 10/3/16**	**Fri 6/7/19**	**$0.00**	**$946,000.00**		**$0.00**	**$896,000.00**
3.15	**Test Beam Operation**	**187 days**	**Fri 1/11/19**	**Mon 9/30/19**	**$0.00**	**$132,420.00**		**$0.00**	**$102,420.00**

Costs

WBS	Task	T&E	M&S	RISK
3.1	MOU btw LANL and ALICE	19K		Low
3.2	Obtain design from ALICE	83K		Low
3.3	Setup Alice Readout Test Stand	10K	100K	Low
3.4	Procure ALICE staves	260K	290K	Medium
3.5	Procure ALICE electronics & cables	70K	80K	Medium
3.6	Readout R&D	140K		
3.8	Prototype Readout Assembled	24K		
3.9	Mechanical Support and Cooling	130K	110K	Low
3.10	Prototype Assembly and Test	55K	55K	Low
3.13	Software (FPGA, online, controls)	350K		Low
3.14	Detector optimization and physics simulations (MIE)	850K	50K	Low
3.15	Test beam operations	50K	80K	Low
3.16	Theoretical Effort	1.8M		Low

20% contingencies applied. Except electronics with 40% contingency.
Estimates based on ALICE ITS procurements and recent FVTX experience.

Schedule



- MAPS sensors by mid 2018
- 2 test stands by August 2017
- 4 fully assembled staves for system test, by the end of 2018
- Preliminary mechanical design by Nov 2018

Major Procurement I: Stave Production

- Procure 4 production staves at CERN (3/2017 – 10/2017)
  - Produce staves from the ALICE stave production line
  - Pay CERN Materials and Labor ($290K)

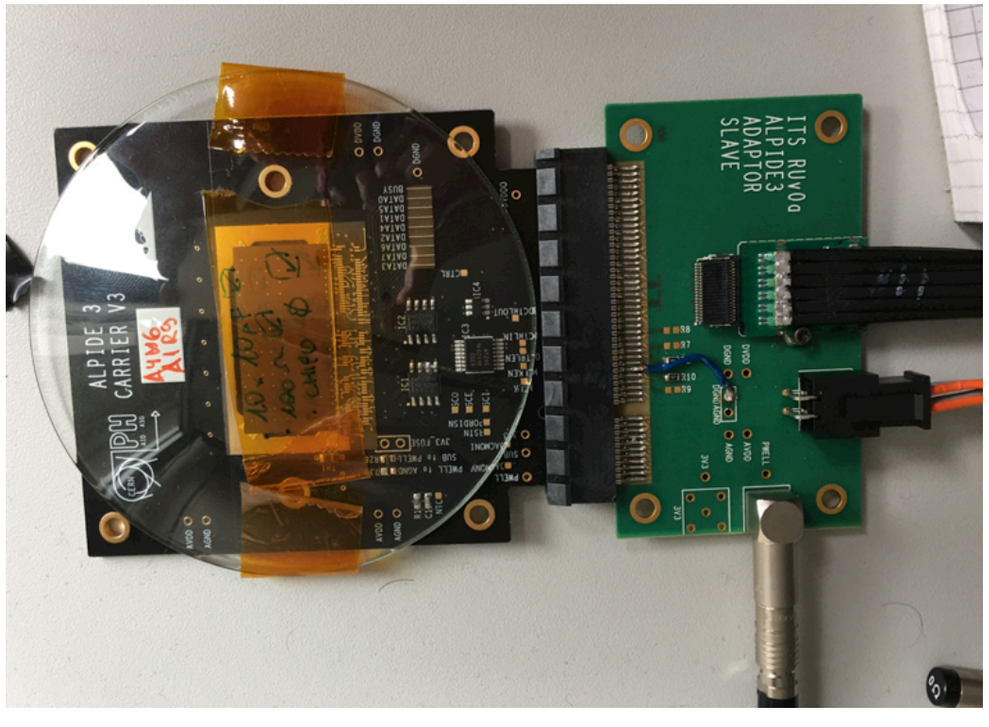
- Train LANL personnel on the job (3/2017 -10/2017)
  - MAPS chips QA at CERN
  - MAPS chips assembly on the Flexible Printed Circuit (FPC) at CERN
  - Module QA at CERN labs
  - Mount FPC modules to space frame, test and QA staves at CERN
  - Test staves at LANL
  - LANL labor T&E ($260K)

Risk I: ALICE Staves Procurement

- ALICE stave production officially ends on March 2018
- Medium risk on ALICE stave production schedule
  MAPS chip production review just done (~mid Nov. 2016)
  Mechanic review scheduled ~Dec. 2016
  Flexible Printed Circuit production review early 2017

Risk Mitigation on LANL telescope staves:

- develop and test the readout with a 5-layer single chip MAPS telescope
- ALPIDE chips with fast readout already available
- Readout system may be ready by the time the 4 staves are available
- Use early prototype staves for LANL R&D



Single-chip MAPS with fast readout

Major Procurement II : Readout Electronics

- Produce readout electronics and cables at CERN, LANL-ALICE MoU
  - part of the ALICE readout electronics production
  - Pay CERN Materials and Labor ($80K)
- Train LANL personnel on the job
  - MAPS chips readout at CERN
  - MAPS 9-chips stave high speed readout at CERN
  - Electronics module QA at CERN labs
  - LANL labor T&E ($70K)
- LANL Readout R&D (1/2017 – 6/2018)
  - Programing FPGA with prototype CRU (a commercial test board)
  - LANL T&E ($140K)

Risk II: Readout Electronics

- Common Readout Unity (CRU) development for the sPHENIX trigger, busy and data format requirements

- Medium risk on ALICE readout electronics production schedule:
  RU v0 being tested, next version expected spring 2017
  CRU being prototyped, key components tested, first prototype expected summer 2017

Risk Mitigation on readout electronics:

- A pre-final version of the CRU has been used by ALICE

- A CRU board or the design file (Gerber file) can already be obtained for our single-chip MAPS telescope for tests and FPGA programming

- Possibility to deal with data formatting in computers trough regular software

PCie40

Summary

- **Tasks, organization and schedule of the work established**

- **ALICE ITS previous work and our experience with FVTX will help in the accomplishment of this project**

- **We are already ALICE Associated Member with access to drawings and boards**

- **Two moderated risks and mitigations identified**