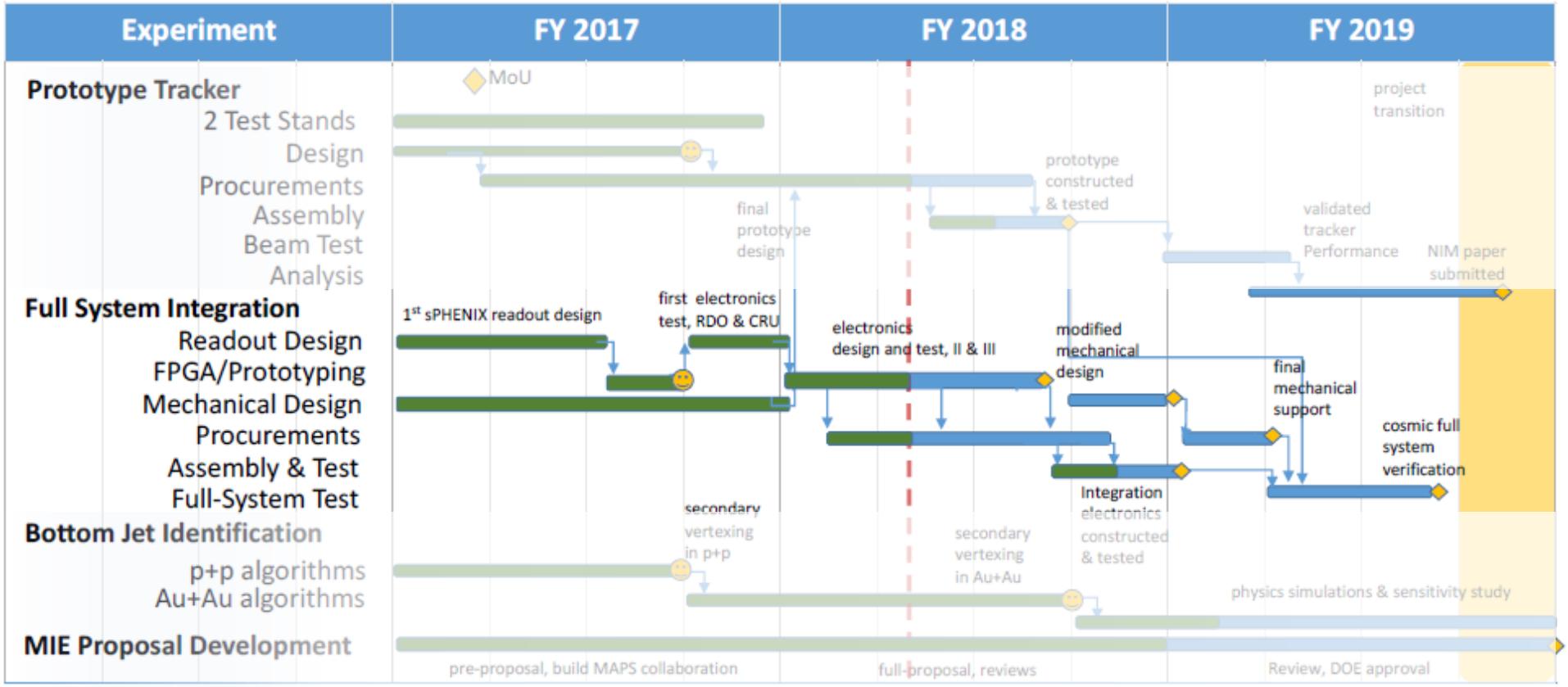
sPHENIX LDRD Readout System Review

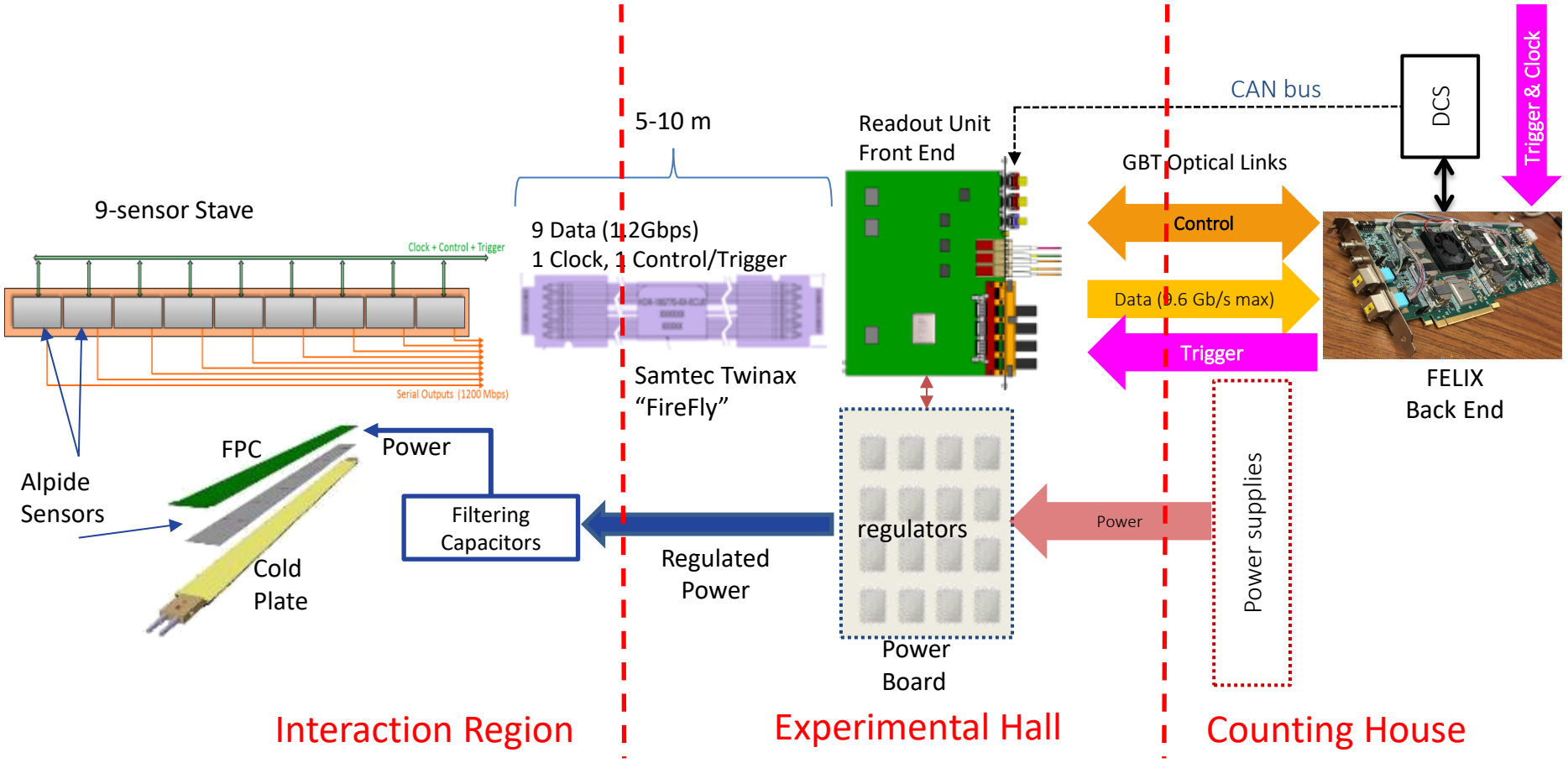
Alex Tkatchev

P-25

Schedule


Experiment
FY 2017
FY 2018
FY 2019
Prototype Tracker
2 Test Stands
Design
Procurements
Assembly
Beam Test
Analysis
Full System Integration
Readout Design
FPGA/Prototyping
Mechanical Design
Procurements
Assembly & Test
Full-System Test
Bottom Jet Identification
p+p algorithms
Au+Au algorithms
MIE Proposal Development
MoU
project transition
prototype constructed & tested
final prototype design
validated tracker Performance
NIM paper submitted
1st sPHENIX readout design
first electronics test, RDO & CRU
electronics design and test, II & III
modified mechanical design
final mechanical support
cosmic full system verification
Integration electronics constructed & tested
secondary vertexing in p+p
secondary vertexing in Au+Au
physics simulations & sensitivity study
pre-proposal, build MAPS collaboration
full-proposal, reviews
Review, DOE approval

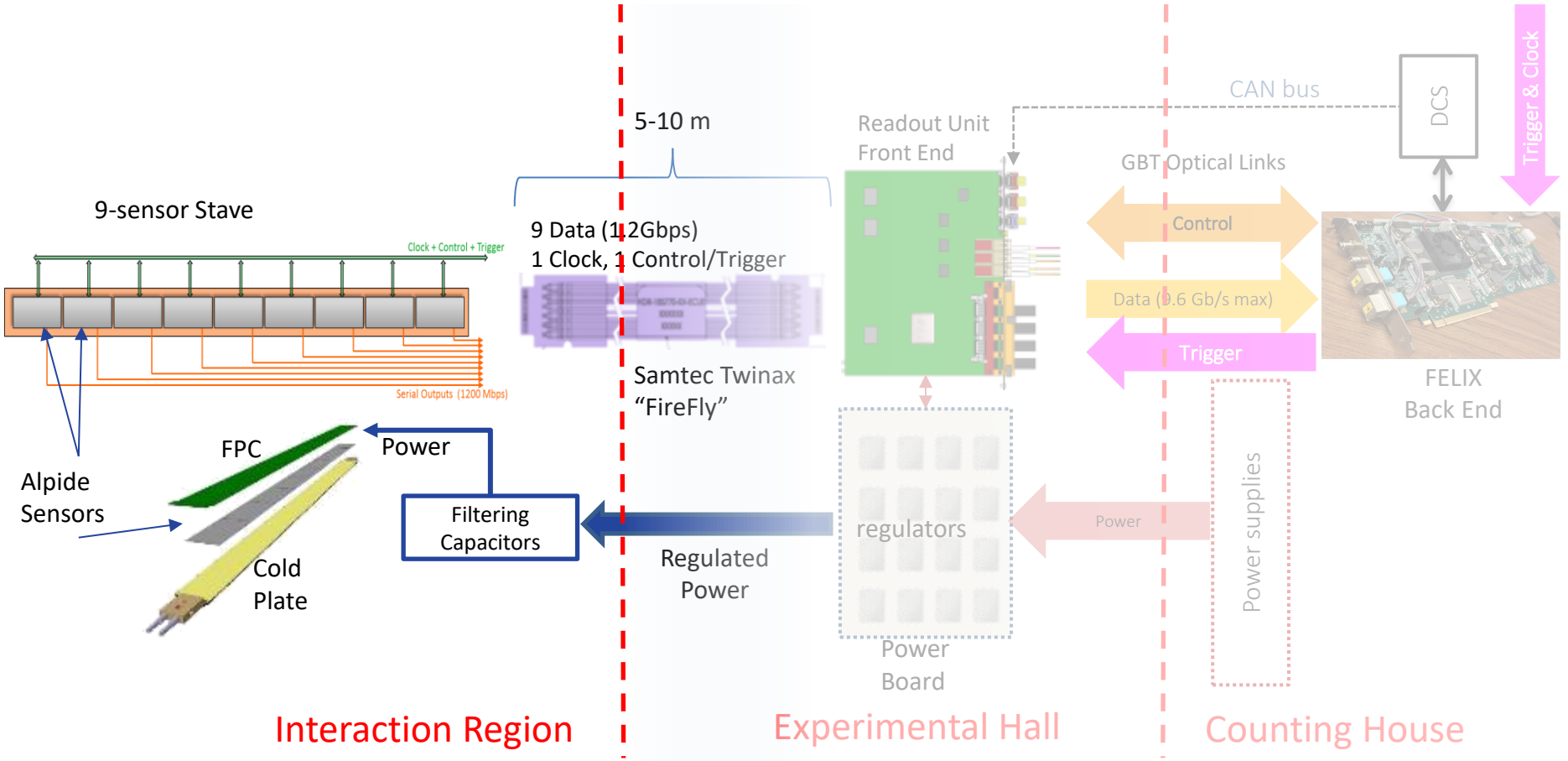
MVTX Electronics Overview



MVTX Detector Electronics consists of three parts

Sensor-Stave (9 ALPIDE chips) | **Front End**-Readout Unit | **Back End**-FELIX

Sensor

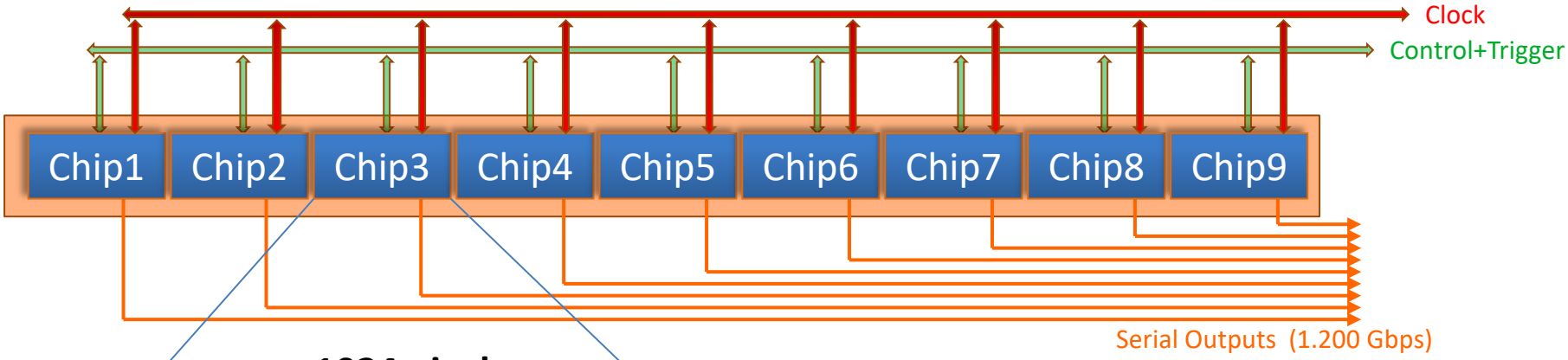


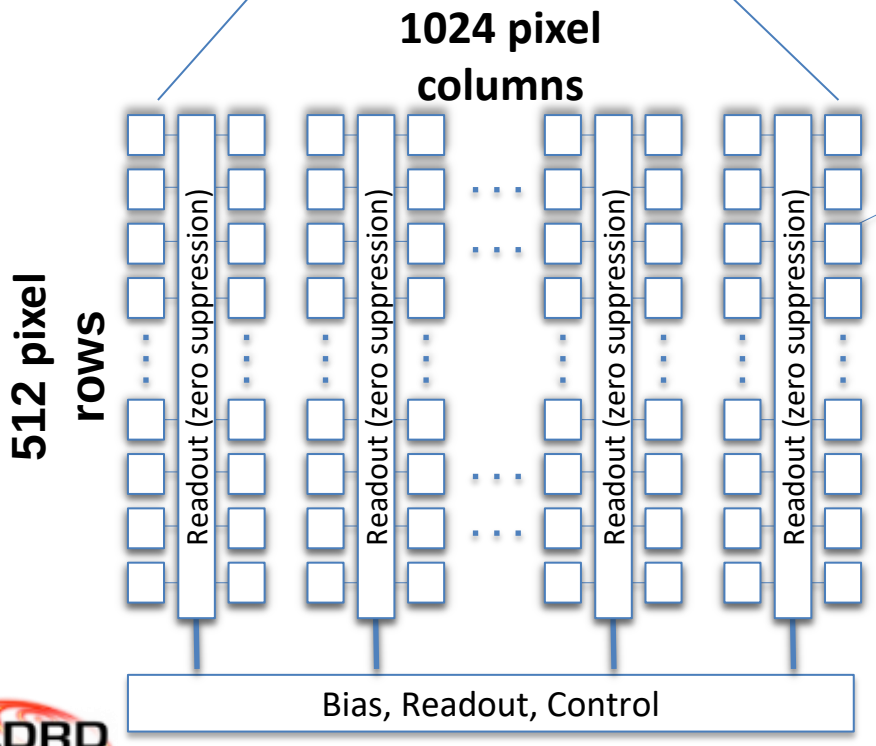
MVTX Detector Electronics consists of three parts

Sensor-Stave (9 ALPIDE chips) | **Front End**-Readout Unit | **Back End**-FELIX

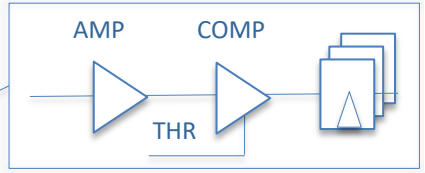
Stave

Stave– 9 chips, common clock and control, independent data lines





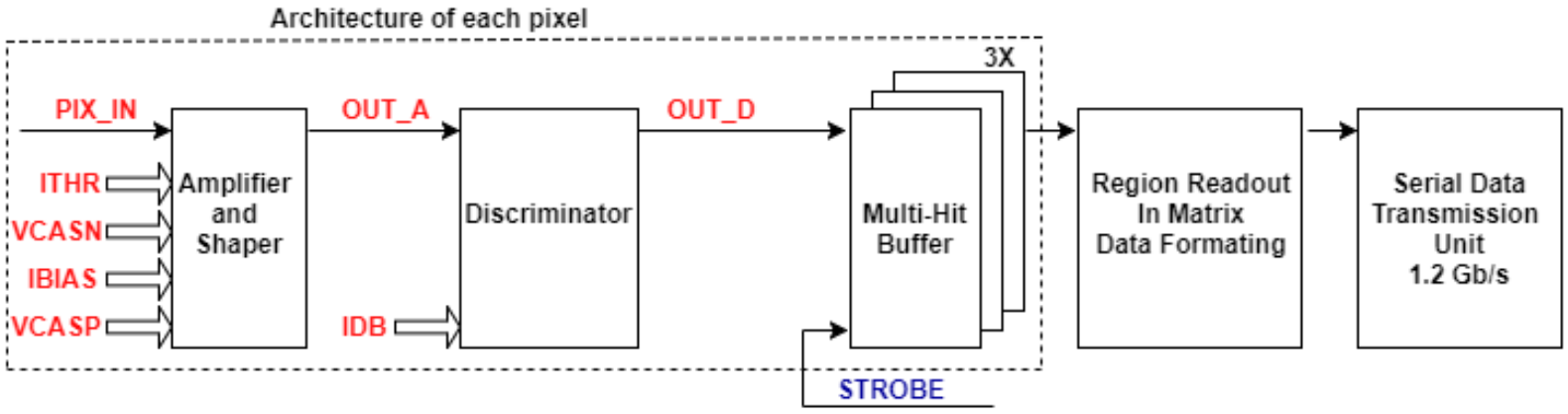
State Of the Art:

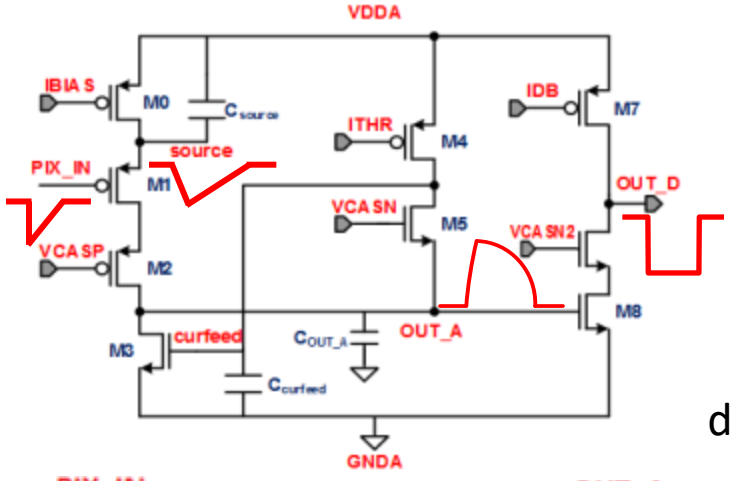


In pixel:
- Amplification
- Discrimination
- 3 hit storage registers (MEB)

ALPIDE Architecture Highlights
- Multi-event buffering capability reduces Readout Unit data throughput requirements
- Digital data output
- Integrated test and masking
- Data output rate at 1.2 Gb/s, 0.6Gb/s, or 0.4Gb/s

ALPIDE Characterization





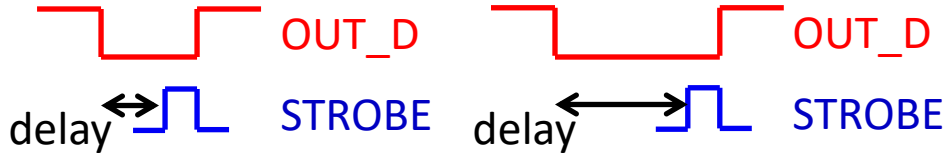
Main bias parameters:

IBIAS first stage bias current

VCASN, ITHR define OUT_A baseline voltage level

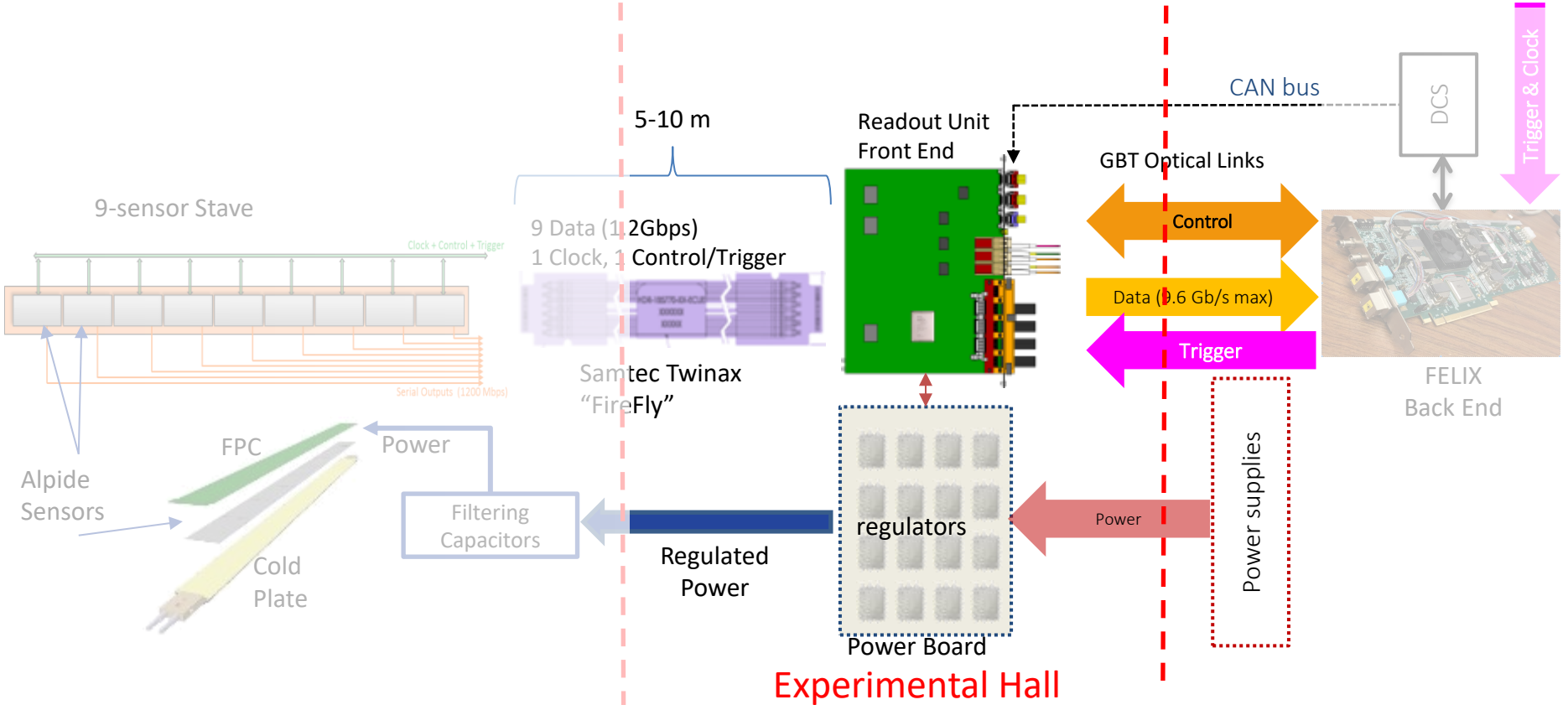
ITHR defines return to baseline

IDB second stage threshold



STROBE Latches Data into the Multi Hit Buffer

MVTX Overview Readout Unit



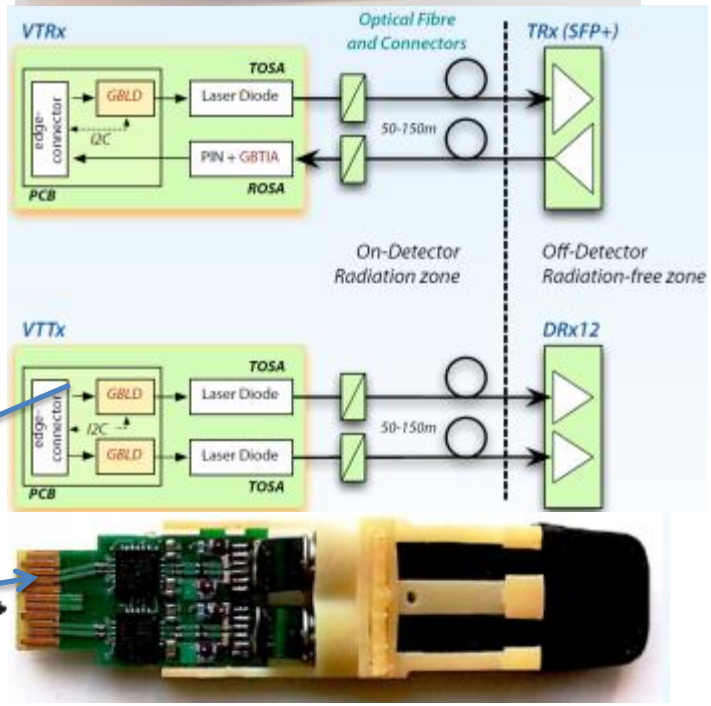
Front End-Readout Unit

- Data **readout** from **Stave**
- Stave **status** and **power control**
- **Control** and **monitoring** to/from the **sensors**
- **Trigger** & **busy** management
- **Data** building and **transmission** through the rad-hard Giga Bit Transceivers

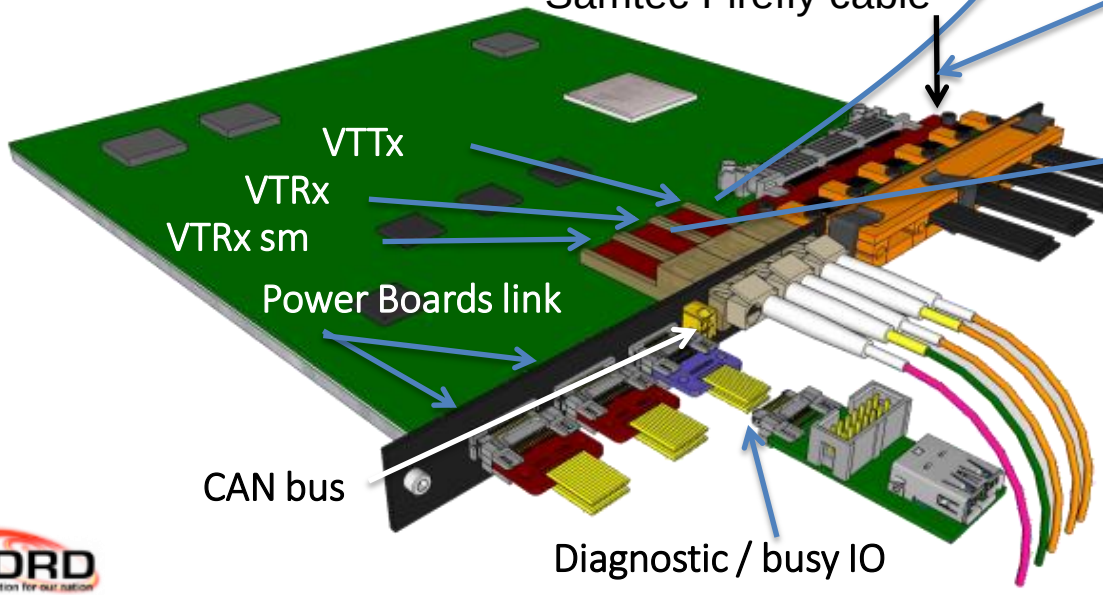
Readout Unit

State Of the Art:

- Xilinx Kintex Ultrascale **FPGA**
- ProAsic FPGA (Manage Radiation Upsets)
- GBT ASIC (Rad. Tolerant Giga Bit **Transceiver**)
  - VTRx: Transciver up & down link
  - VTTx: Double Transmitter 2 * up link:
- Samtec firefly copper twinax **cable** interface
  - 9 independent 1.2Gb/s data streams
  - 1 40MHz Clock
  - 1 Control Line



Transition Board
Samtec Firefly cable



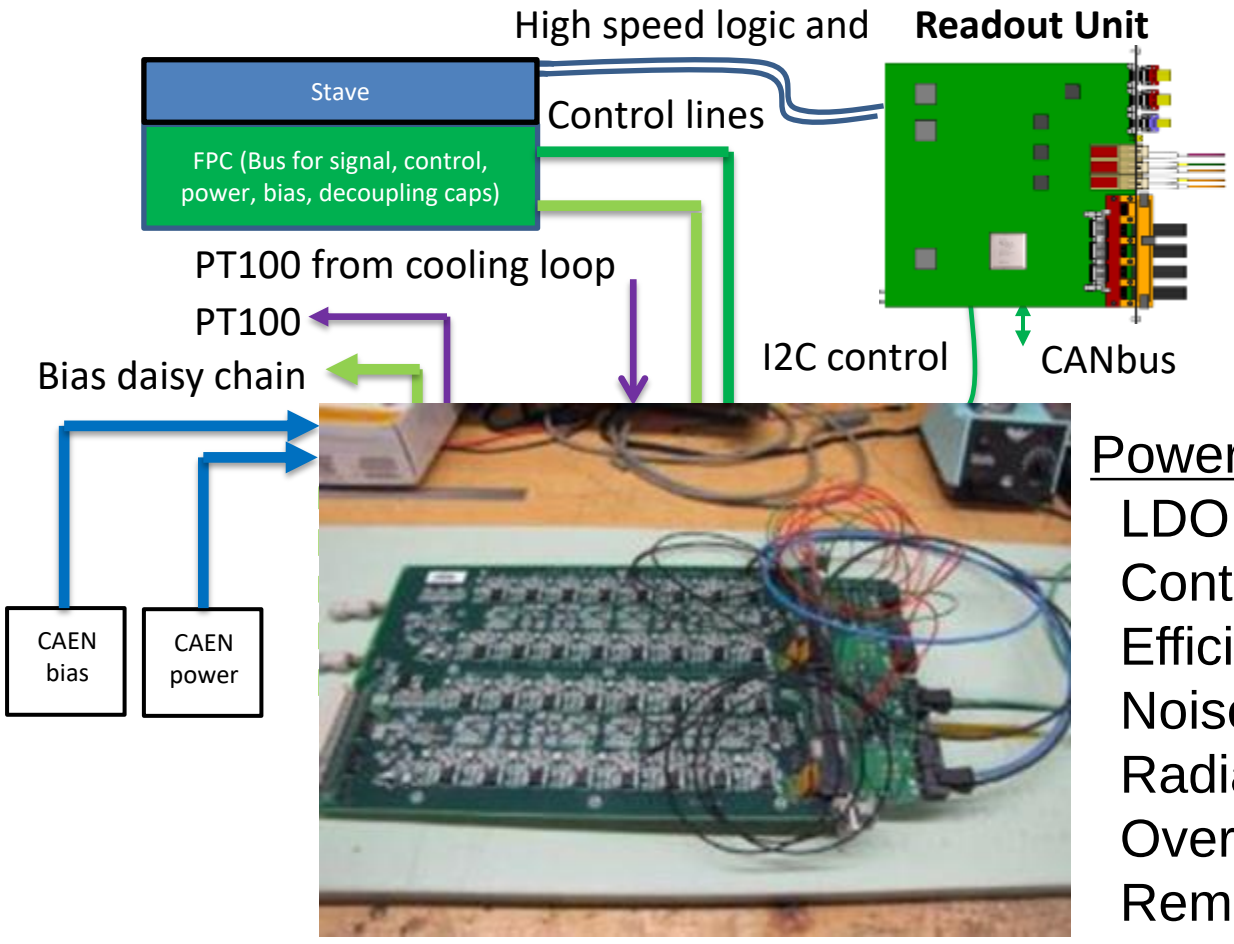
→ 2 uplink (data) to FELIX

→ 1 uplinks (data/CTRL) to FELIX

← 1 downlink (CTRL) from FELIX

← 1 trigger downlink directly to ensure low latency

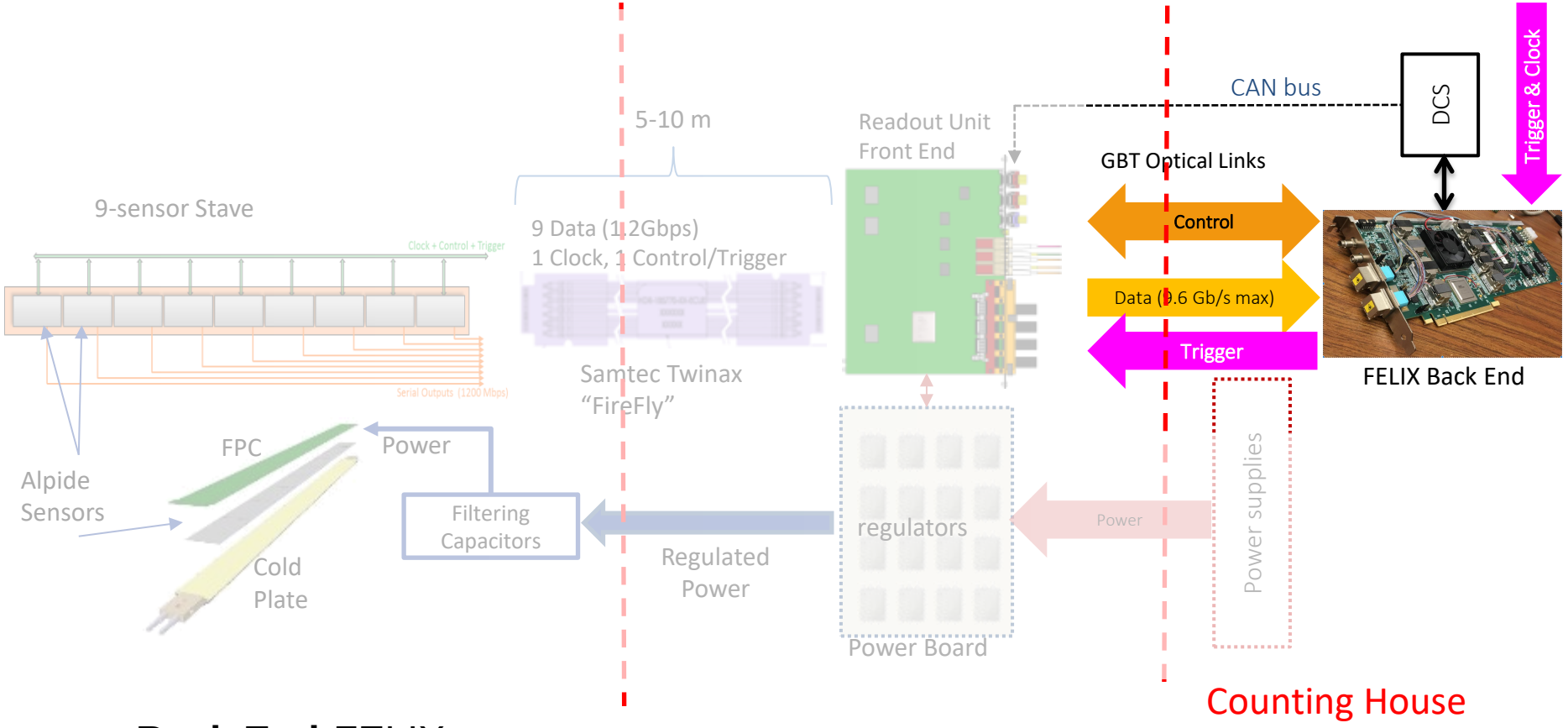
System Power Overview



Power Board Requirements:

- LDO regulator architecture
- Control Interface to Readout Unit
- Efficiency > 99%
- Noise rate < 10^{-6}
- Radiation Tolerant
- Overcurrent protection
- Remote current readout
- Remote voltage readout
- Remote voltage setting

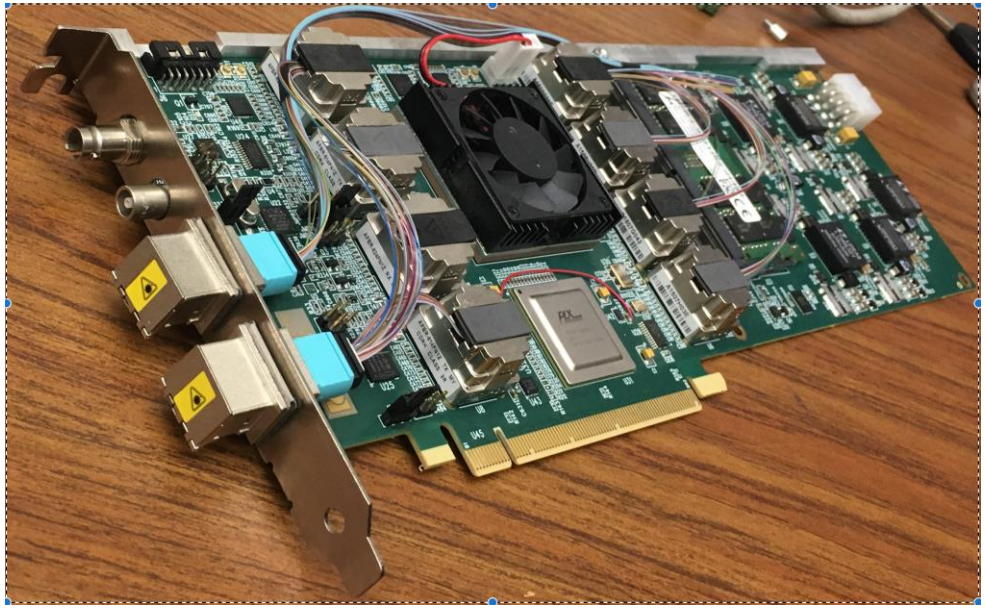
MVTX Overview FELIX

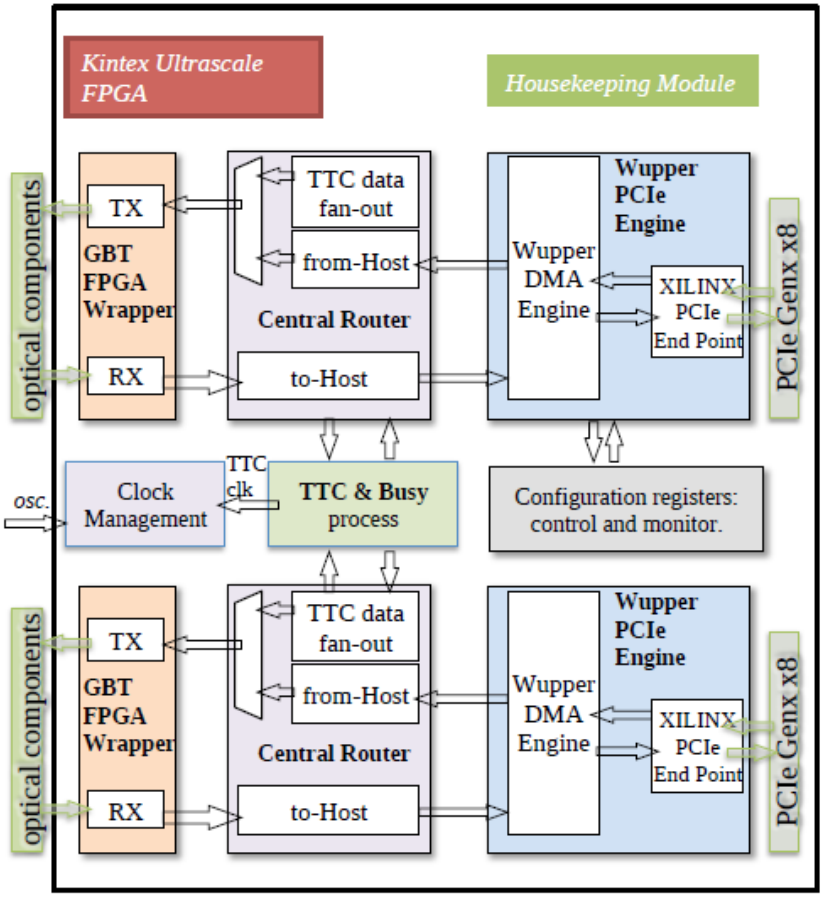


Back End-FELIX:

- Data **readout** from 8 Readout Units
- Slow Control and **Monitoring** to/from sensors
- **Trigger** and Timing systems interface
- **Data aggregation** and sub-event packaging
- Data **transmission** through the PCIe to Server CPU

FELIX





State Of the Art:

- Xilinx Kintex Ultrascale FPGA
- 48 bi-directional GBT links
- 16 lane Gen3 PCIe

Performance Summary:

- PCIe Tx > 100 Gb/s
- FEE Rx < 80 Gb/s

Data Rate Requirements

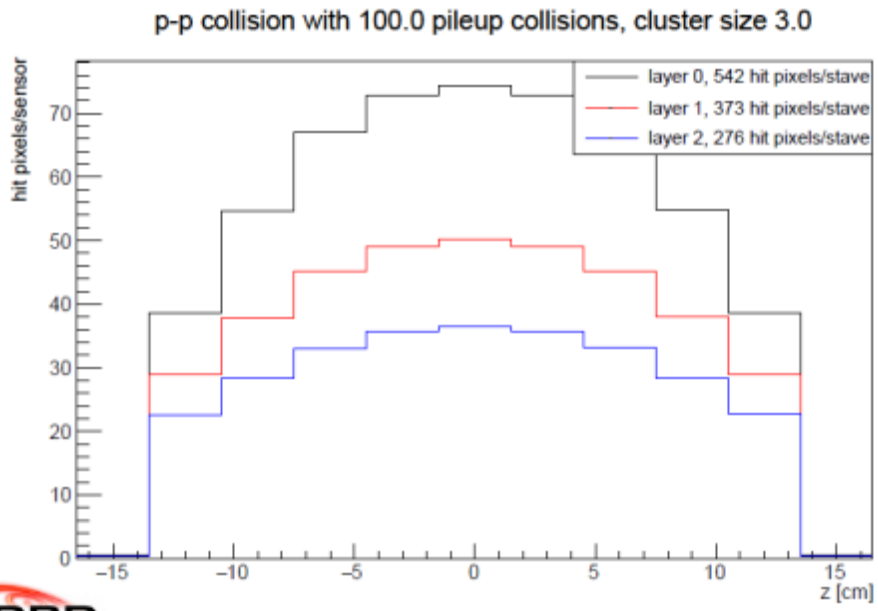
	10^{-4} noise occupancy	Hit occupancy only		Hit + noise occupancy	
		$p+p$ [MB/s]	Au+Au [MB/s]	$p+p$ [MB/s]	Au+Au [MB/s]
L0 FEM	26	29	107	55	133
DAM	219	173	630	392	848
MVTX	1305	1041	3781	2346	5089

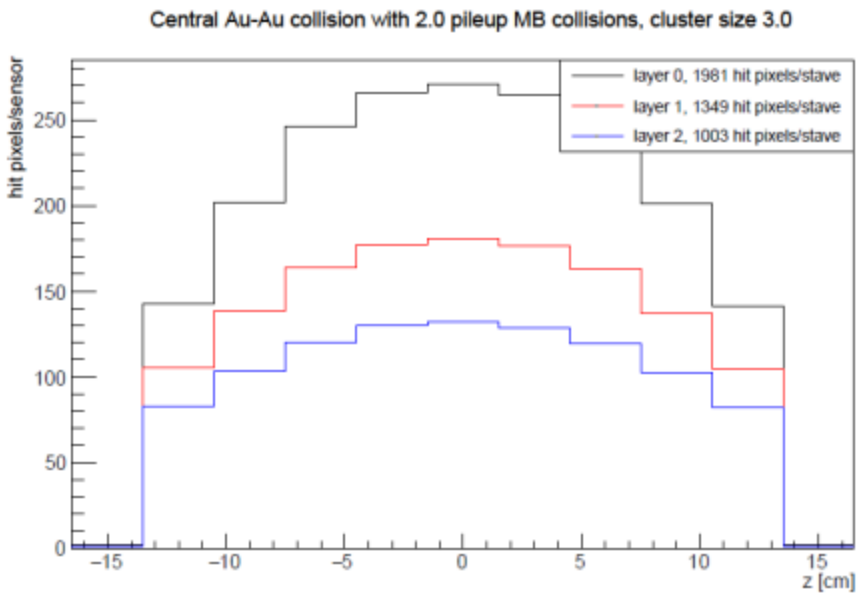
Readout Units 3 GBTX @ 0.4 GB/s = 1.2 GB/s >133MB/s

- GBTx: 3.2-4.48Gb/s, 0.4 GB/s

FELIX (48 input on FELIX, twice the number needed to support 8 RUs (3 links))

- 2x 8-lane PCIe Gen 3 @ 7880 MB/s = 15760 MB/s > 848 MB/s

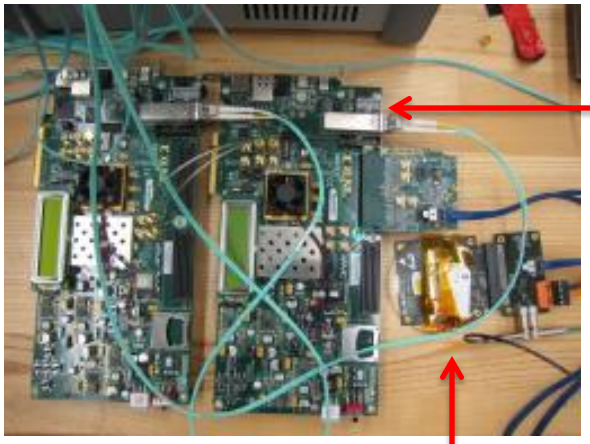




MVTX Readout Electronics

- Hardware
  - 48 ALPIDE Staves (~200M Channels) 
  - 48 Front End Electronics (RUv1) 
  - 6 Back End Electronics (FELIX v2.x) 
  - 6 EBDC server 
  - 3 Power Boards+ Supplies 
  - 48 Stave to RU cables 
  - 144 Fiber optic cables (3 fibers x 48 FEE) 
- Spares at ~20%

R&D Accomplishments

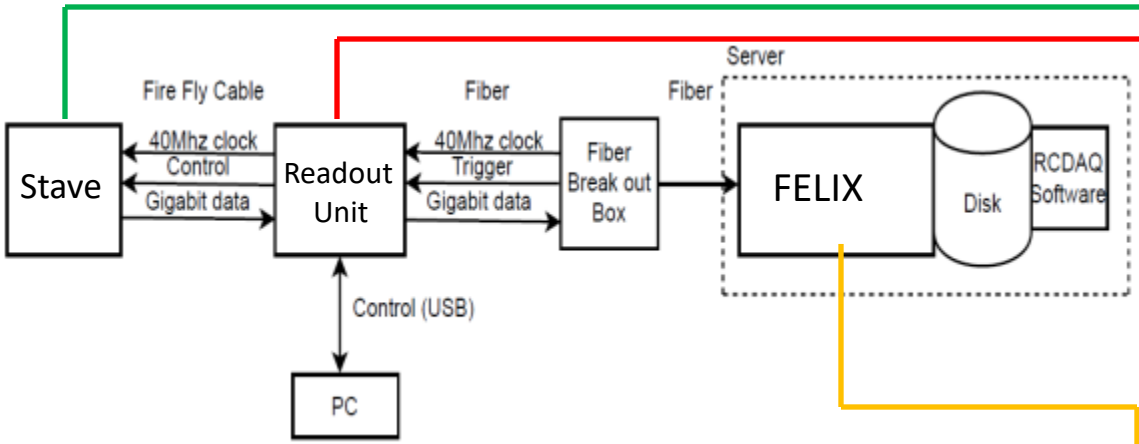


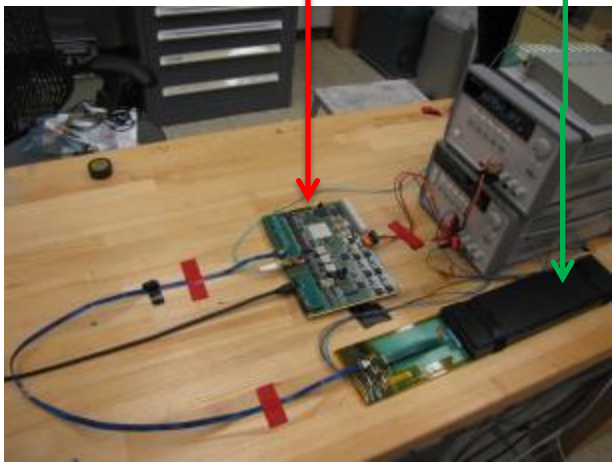
Accelerated Development: Mitigated Readout Unit arrival delay

While RU (Readout Unit) was not available:

- Designed system to emulate RU on Xilinx Development Kits
  - ALPIDE triggered and read out at 15kHz, 448 hits
  - Developed prototype RCDAQ plugin
  - FELIX packs and places ALPIDE data on disk
  - Emulated 8 RU's using 1 fiber link per RU on FELIX, 15kHz

MVTX Full Chain

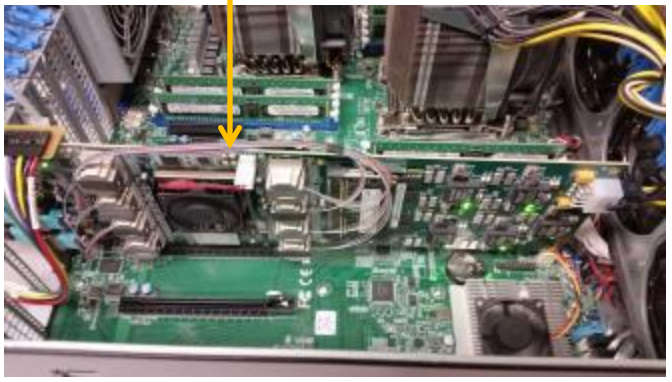




Readout Unit + Stave

Demonstrated Full MVTX Chain Readout

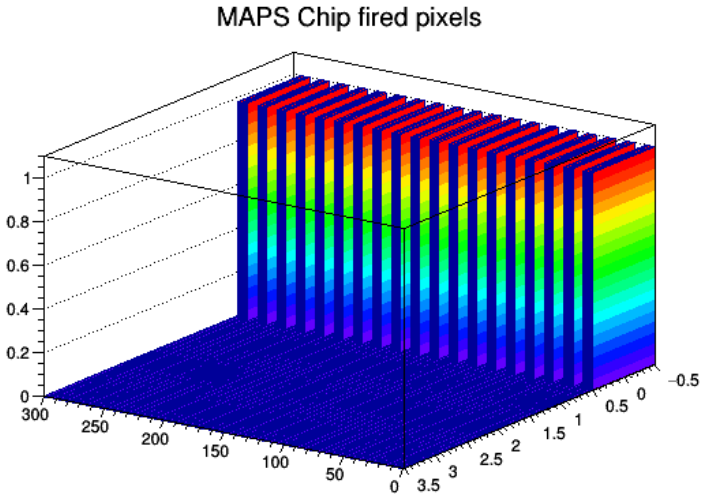
- Once the Readout Unit arrived, successfully configured, triggered and readout Stave:
  - Readout Unit configures Stave using USB interface
  - FELIX distributes clock to Readout Unit
  - Readout Unit distributes clock to the Stave
  - Stave is triggered, sends data at 1.2Gb/s
  - Configured GBT link to recover clock from FELIX
  - Readout Unit receives the data and sends the data to FELIX over fiber using GBT link
  - FELIX packs data, stores it on disk using RCDAQ

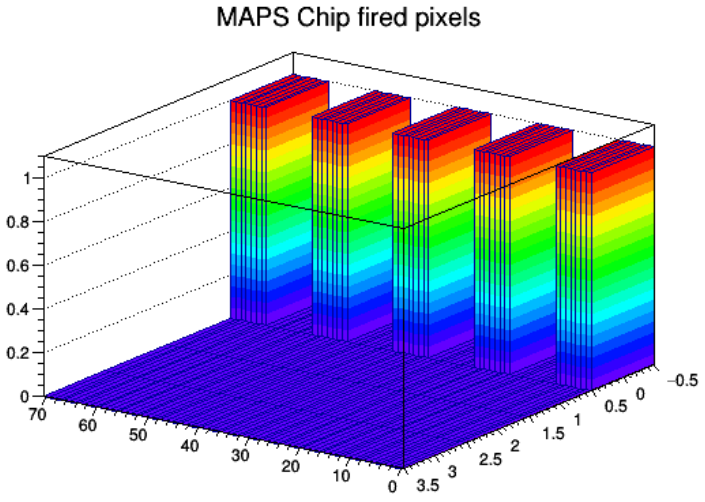


Server + FELIX

RCDAQ

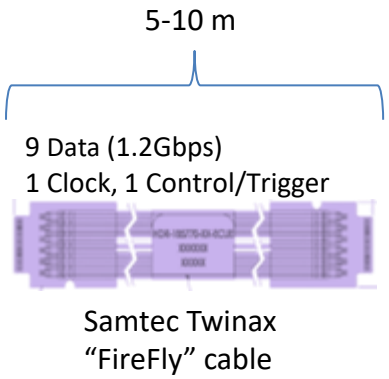
- RCDAQ = sPHENIX DAQ
  - Our accomplishments of integrating FELIX with RCDAQ prove that MVTX should tie into sPHENIX day one.
  - Plots generated by RCDAQ show pulsed Pixels readout by Readout Unit and FELIX

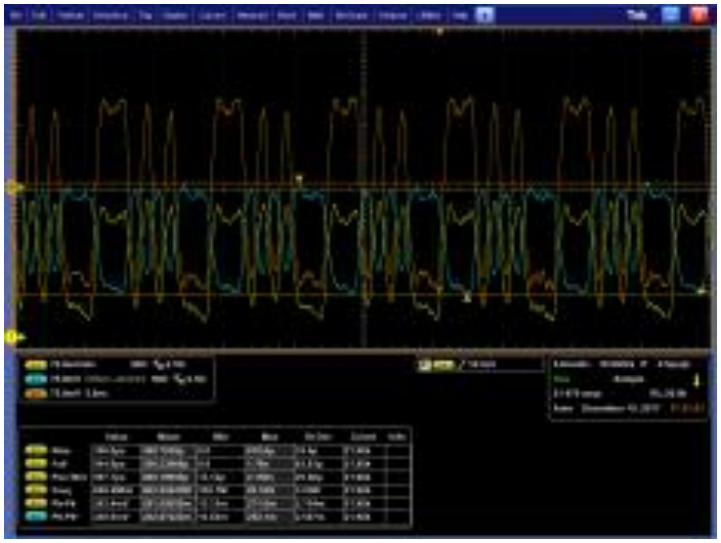




Full MVTX Readout Chain integrated with sPHENIX DAQ

MVTX Stave-RU Extension



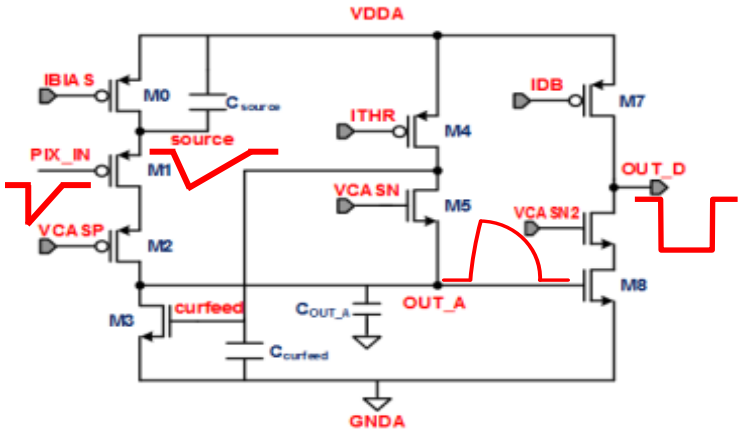


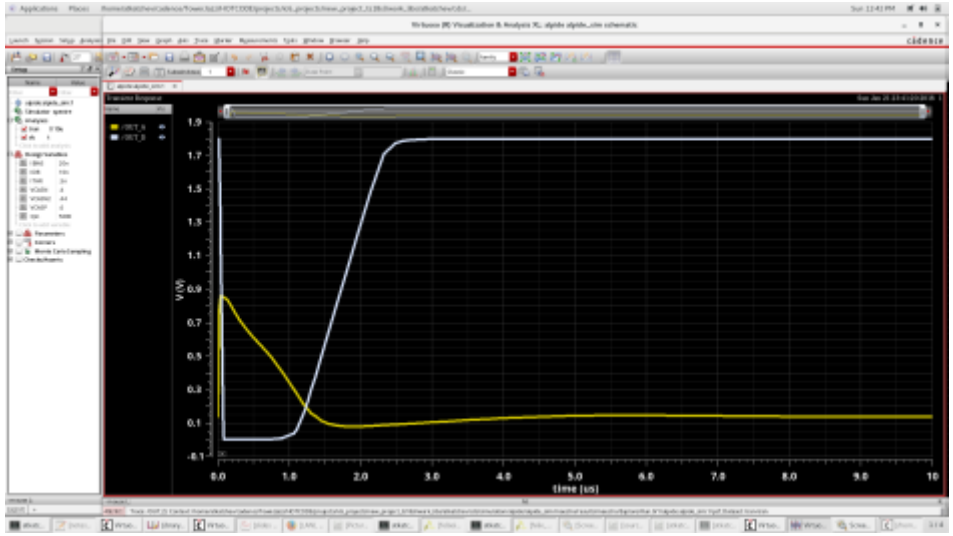
5 Meter

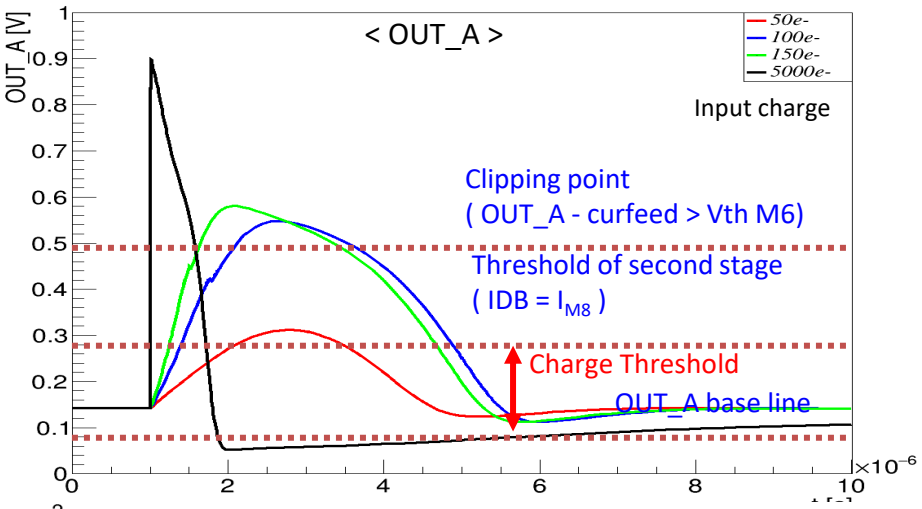
7 Meter

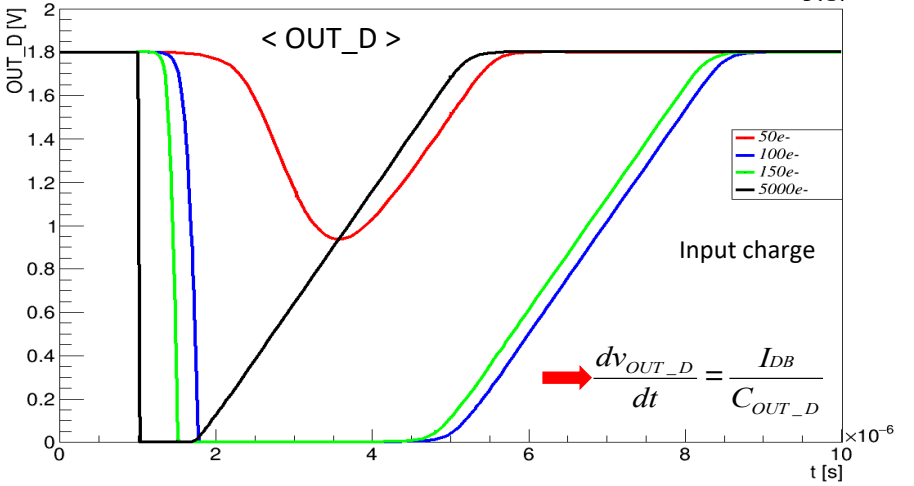
- Flex Cable Manufacturer Identified
- Signal Integrity of the longer Stave-RU interconnect cable for the MVTX mechanical configuration including overall length and necessary data output rate is under evaluation
  - Confirmed Default ALPIDE Data Transmission Settings are not suitable for cable lengths over 5m
  - 2 electronics options
    - Increase ALPIDE Drive Strength
    - Increase ALPIDE Preemphasis

ALPIDE Simulations





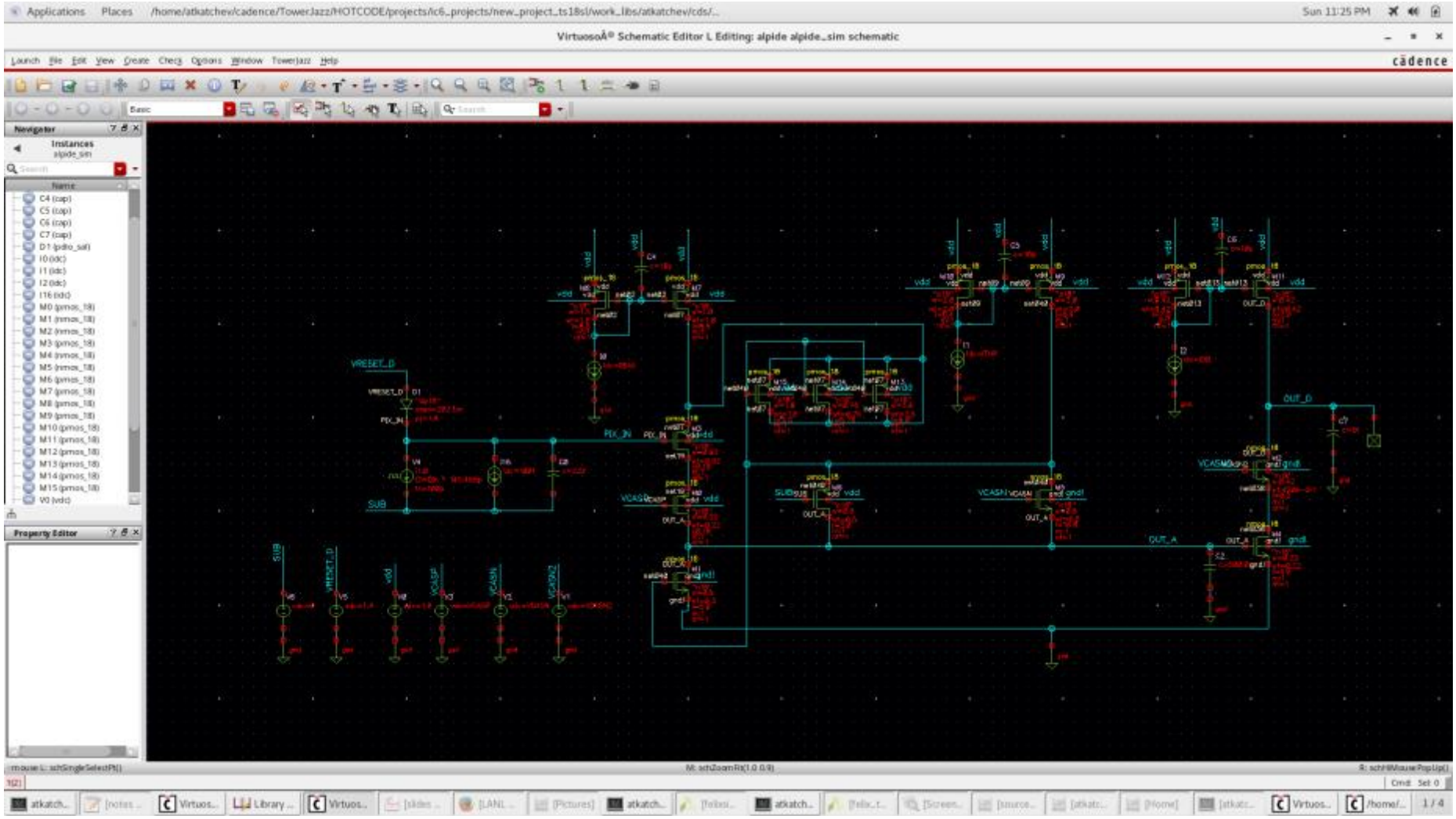




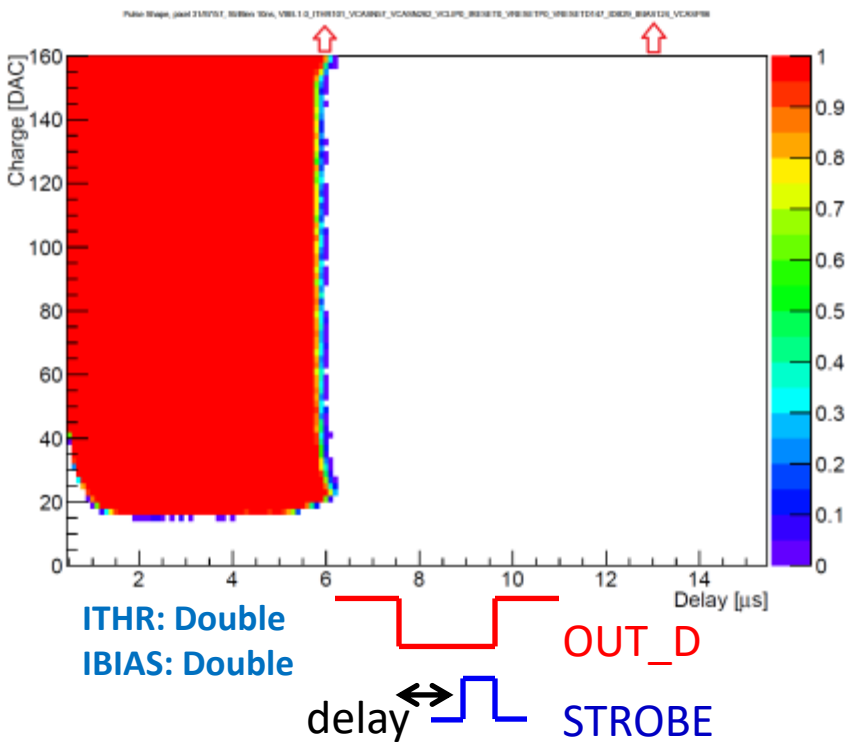
Need to Adapt ALPIDE Bias Parameters for use in MVTX

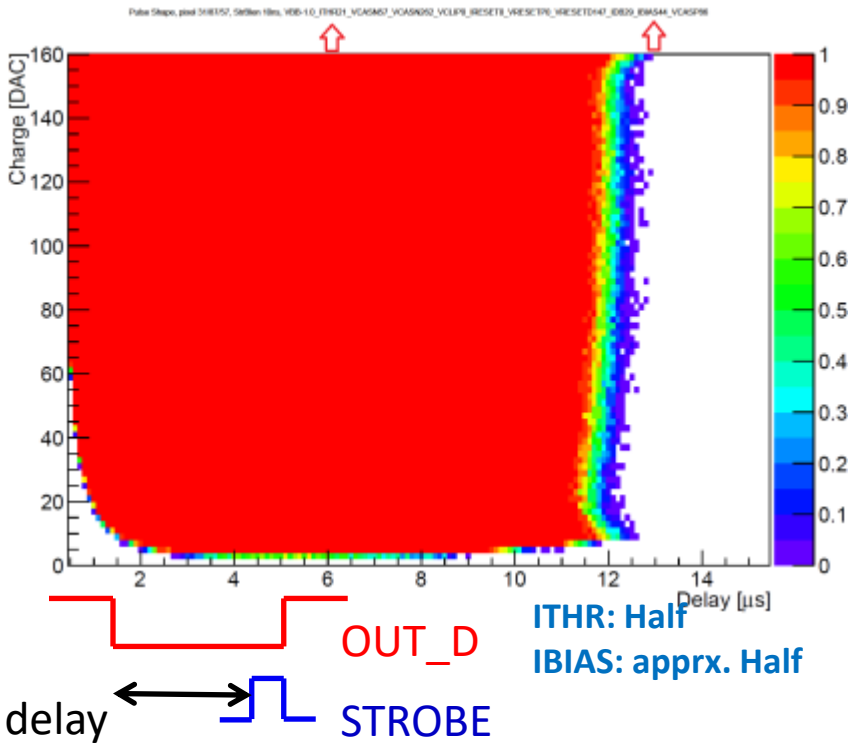
- Obtained evaluation license for Mentor Graphics Virtuoso
- Obtained technology files from Tower Jazz
- Understood the effects of each Bias and Threshold Parameter on the output

ALPIDE Sim. Schematic



Simulation Confirmation





- Pulse Shape Measurement with Charge Injection
  - Pulse Shape is measured by moving the timing of the (small) trigger window with respect to the injection time (“strobe delay”)
  - Values extracted from 2D-measurement vs charge and trigger timing:
    - Time over threshold, maximum pulse length, time walk
- Creates a baseline for laser test stand efforts

Risk Mitigation

Risks:

Previous LDRD Review

- Custom Electronics concerns
- CRU FELIX finalization

BNL Directors Review

- MVTX readout scheme integration into sPHENIX DAQ

Achievements

- Successfully demonstrated full readout chain:
  - STAVE->Readout Unit->FELIX
- Successfully integrated readout chain with RCDAQ (sPHENIX DAQ)
- Validated FELIX and Readout Unit performance for MVTX
  - System triggered at 15Khz
  - emulating 8 RU's on FELIX
- Power System at LANL

Reduced cost of LDRD Contingencies

Future Deliverables

- ALPIDE Characterization & Cluster Size Finalization
- ALPIDE Triggered & Continuous Modes
- Remote Readout Unit programming (over fiber)
- Readout Unit Radiation Upset (Scrubbing) Firmware
- FELIX programming (over PCIe)
- FELIX firmware revisions to adapt MVTX detector specs.
- RCDAQ (sPHENIX DAQ) finalization
- Signal Integrity evaluation of the longer Stave-RU interconnect for MVTX
- System Optimization & Documentation

Most tasks are well underway