sPHENIX LDRD Review

ALPIDE Introduction and Test Stand

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P-25

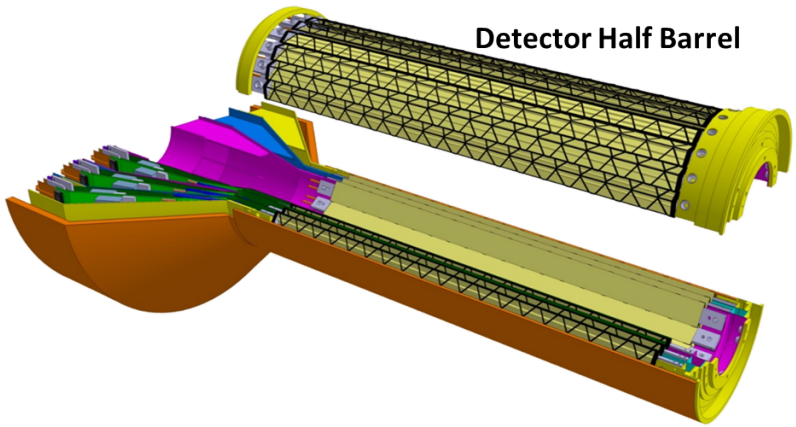
Outline

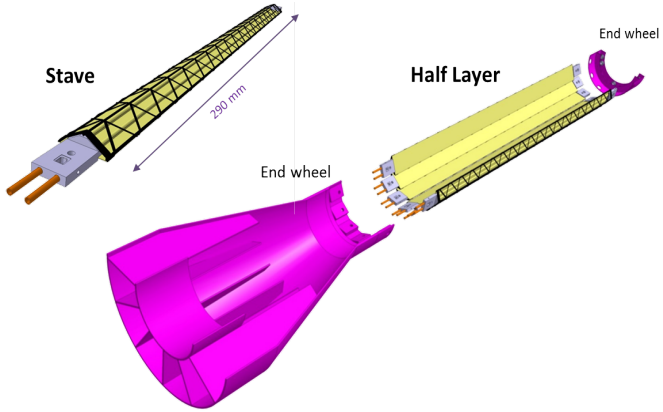
- ALPIDE chip introduction
- LDRD test bench setup
- LDRD test bench achievements
- Summary and Plans

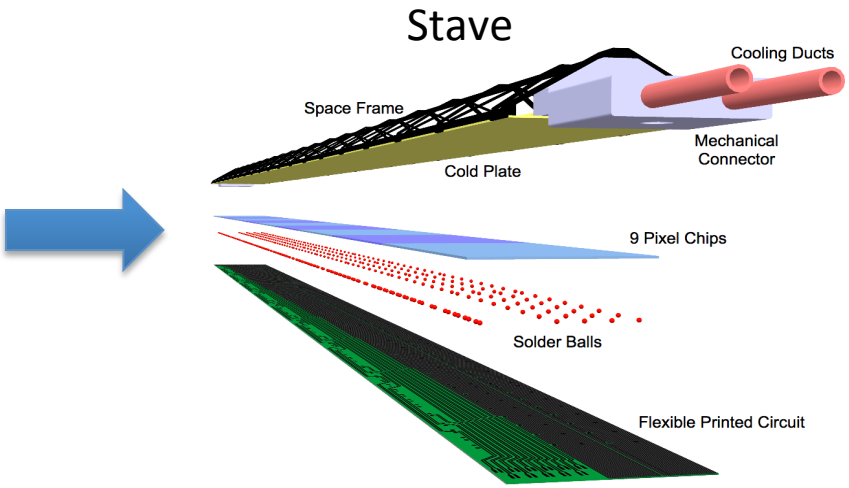
The MVTX Basic Unit: ALPIDE sensor

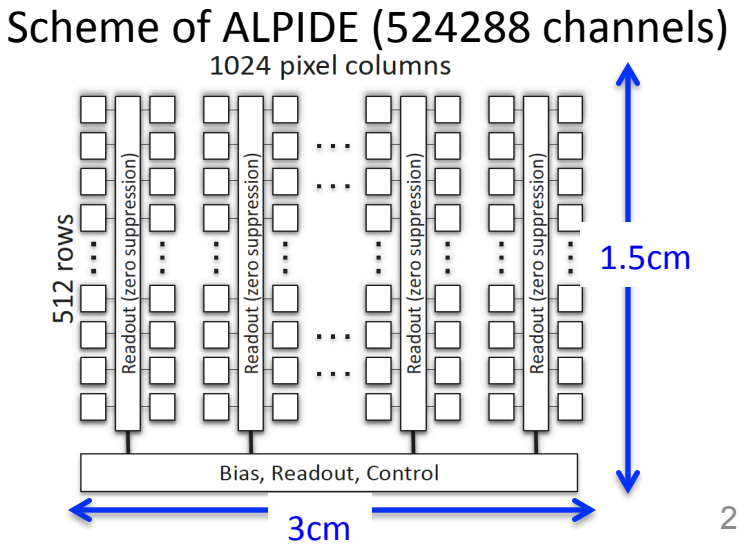
ALPIDE chip Introduction:

The 3-layer MVTX consists of 48 staves and each stave contains 9 ALPIDE chips.



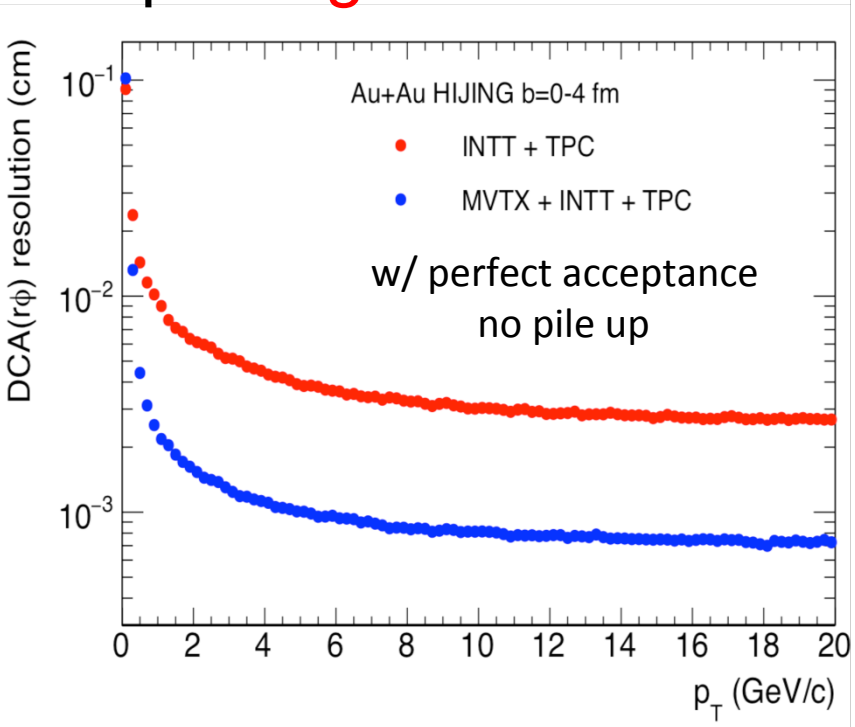


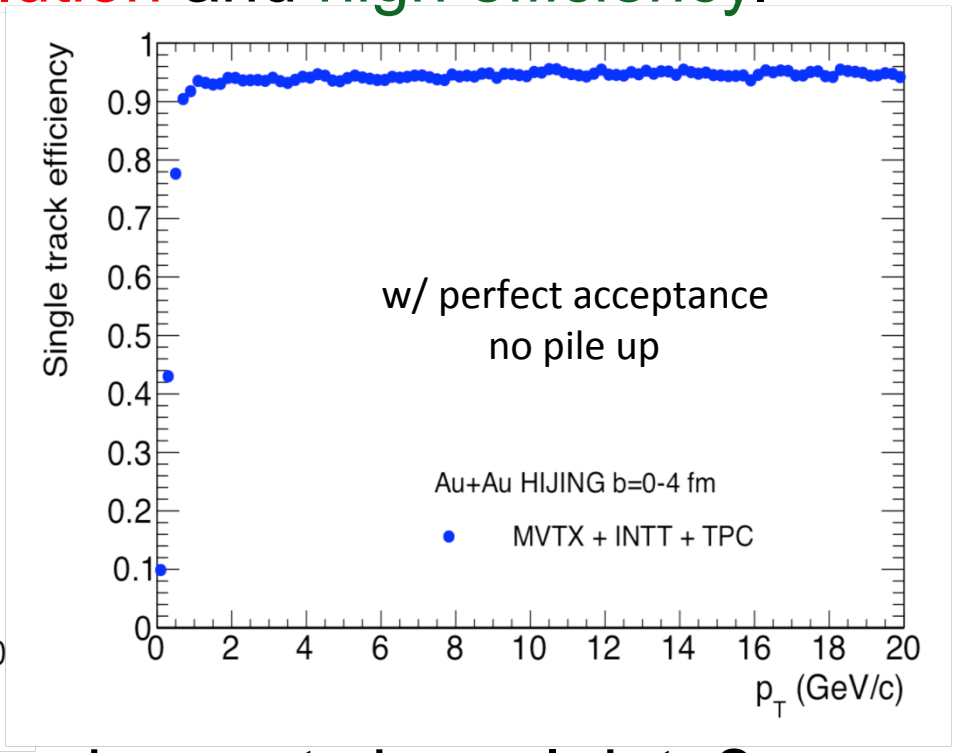




MVTX Performance Requirements

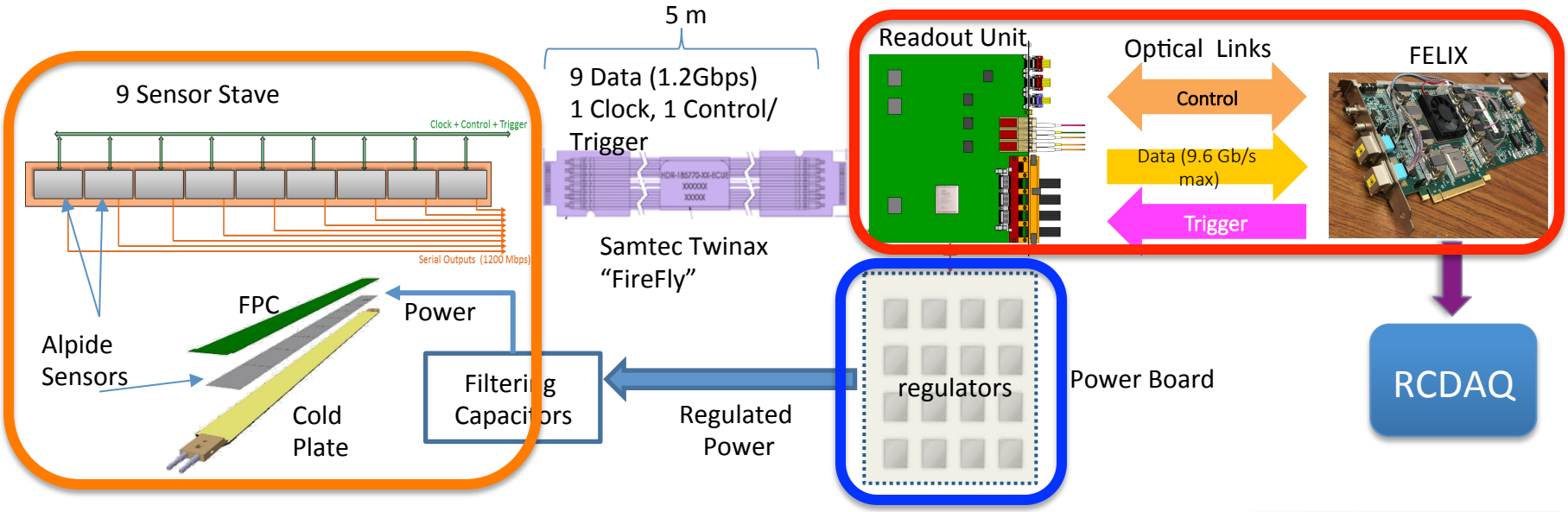
- The heavy flavor program at sPHENIX led by the MVTX requires good vertex resolution and high efficiency.



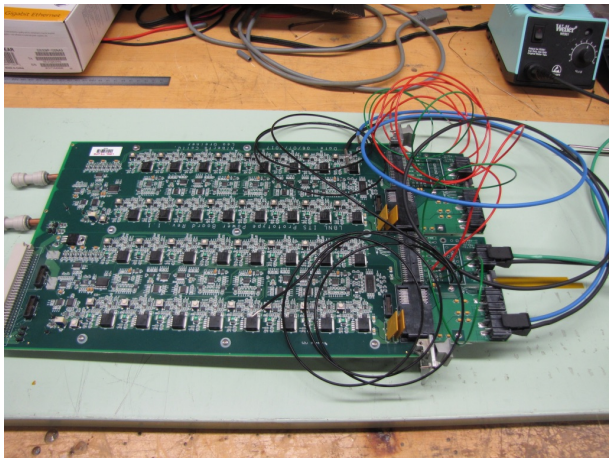


- Can MVTX meet these requirements in real data?
  - Small dead channel fraction →High efficiency.
  - High signal/noise ratio → Low background.

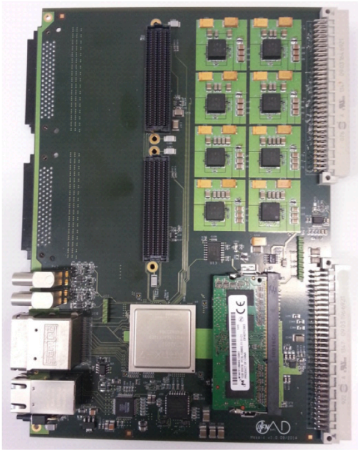
LDRD Test Bench Components



Purchased one stave and 5 individual ALPIDE chips.



Purchased 1 Power Board

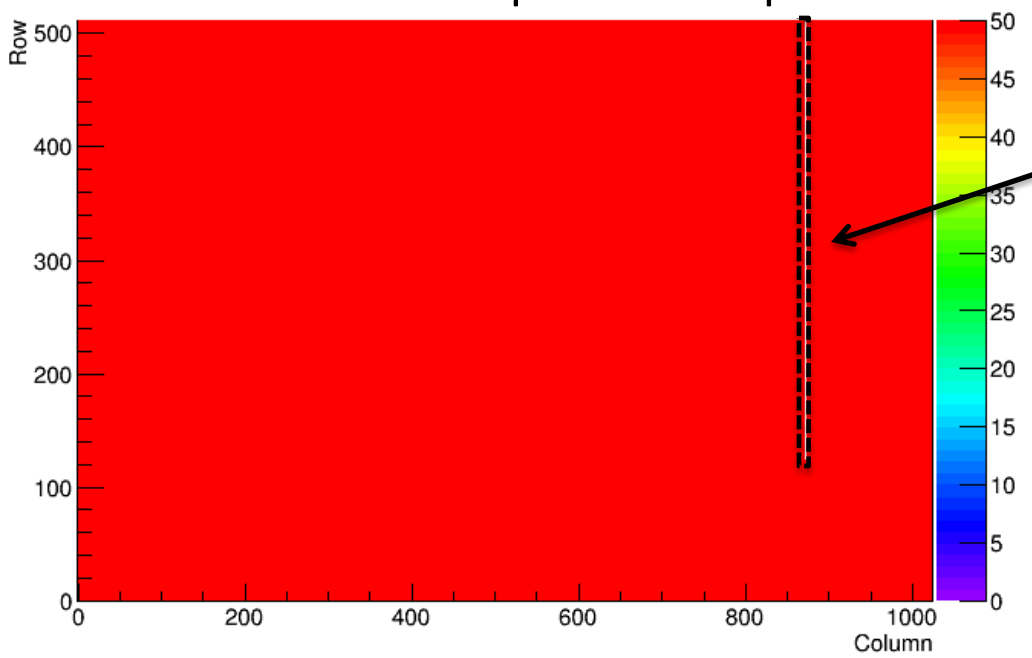


Test bench readout module: MOSAIC

ALPIDE Characterization: Good Active Area

- Measure the dead areas for efficiency evaluation.
- Test with internal pulse generator:
  - Scanned available chips and stave at LANL through digital scan to verify the good channel fraction: the active pixel fraction is >>99%.
  - Similar results with different readout speed.

ALPIDE chip test example



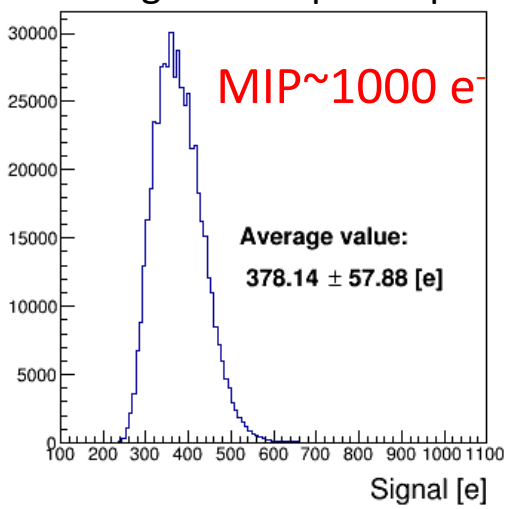
No. of 0 hits
777
Cold channel
1
Hot channel
0
Bad fraction
0.15%

ALPIDE Characterization: Low Noise (I)

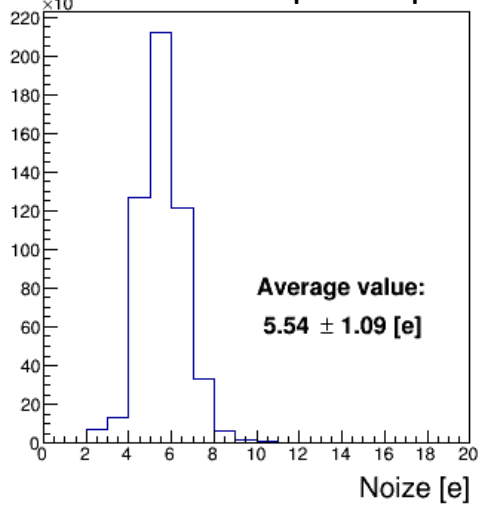
- Charge injection with internal pulse generator:
  - Scanned available chips and stave at LANL through threshold scan: signal/noise based on charge injection study is > 60. Comparable with CERN test (~60).
- Proves the background contribution is low!

Chip test with internal trigger

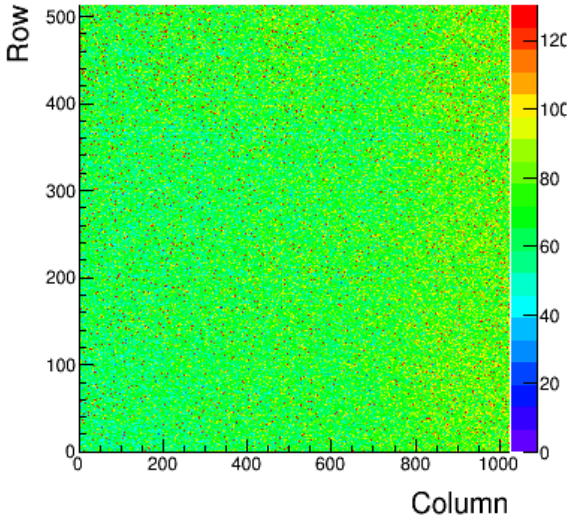
Signal scan per chip



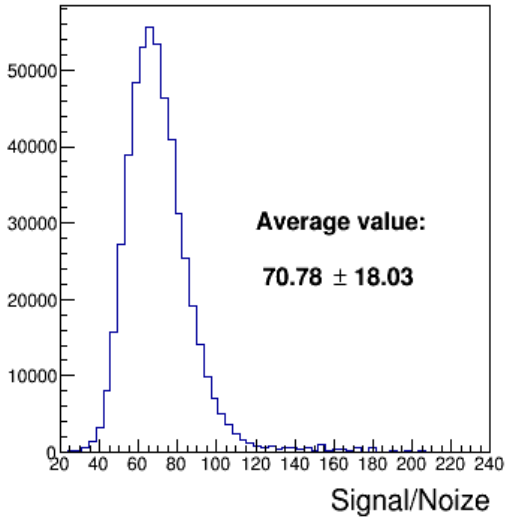
Noise scan per chip



Signal/Noise uniformity



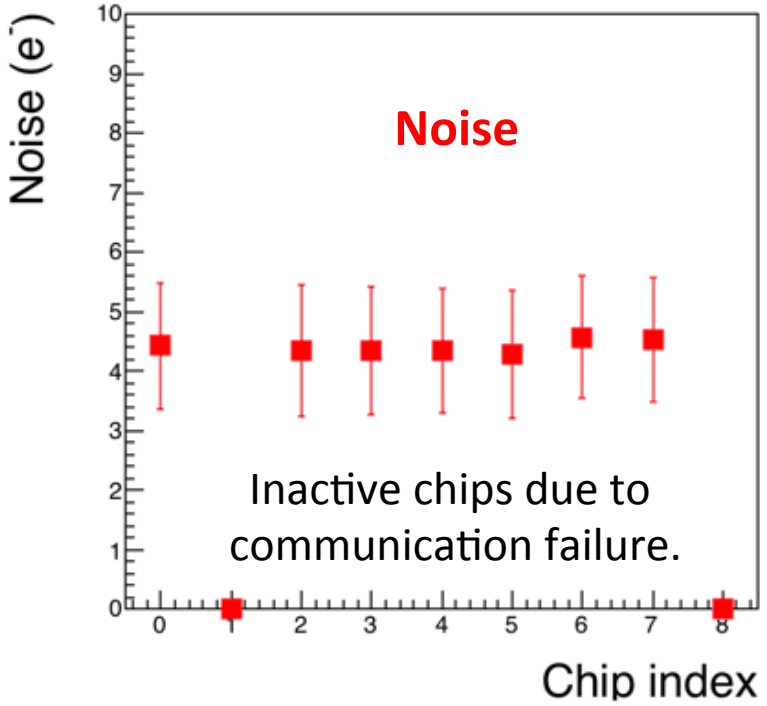
Signal/Noise scan per chip

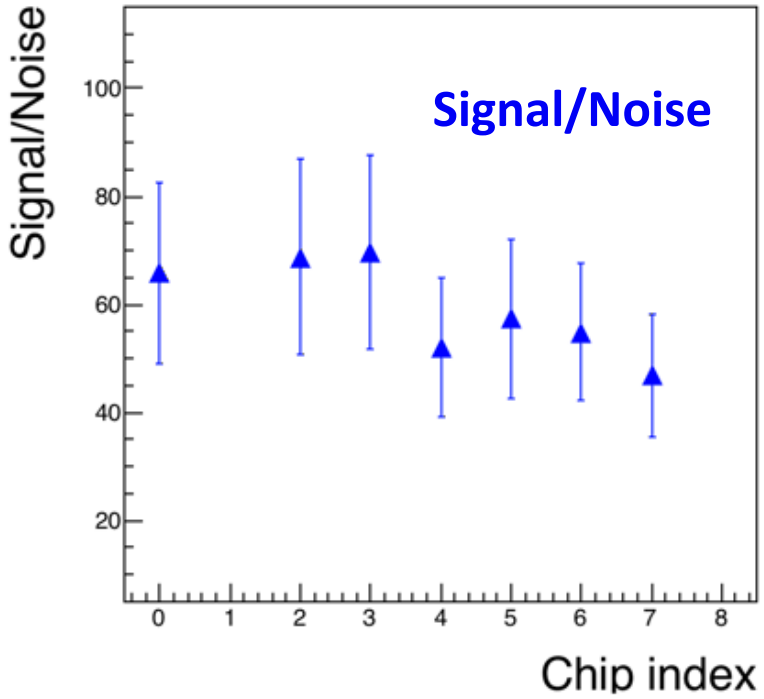


ALPIDE Characterization: Low Noise (II)

- Charge injection with internal pulse generator:
  - Scanned available chips and stave at LANL through threshold scan: signal/noise based on charge injection study is around 60. Comparable with CERN test (~60).

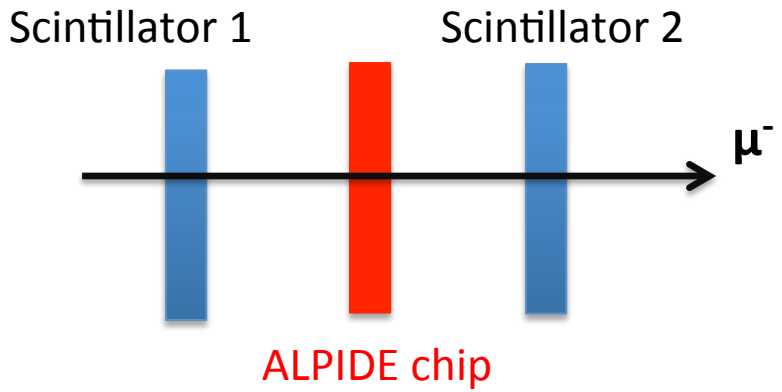
Stave test with internal trigger:
Simultaneous readout of all chips.





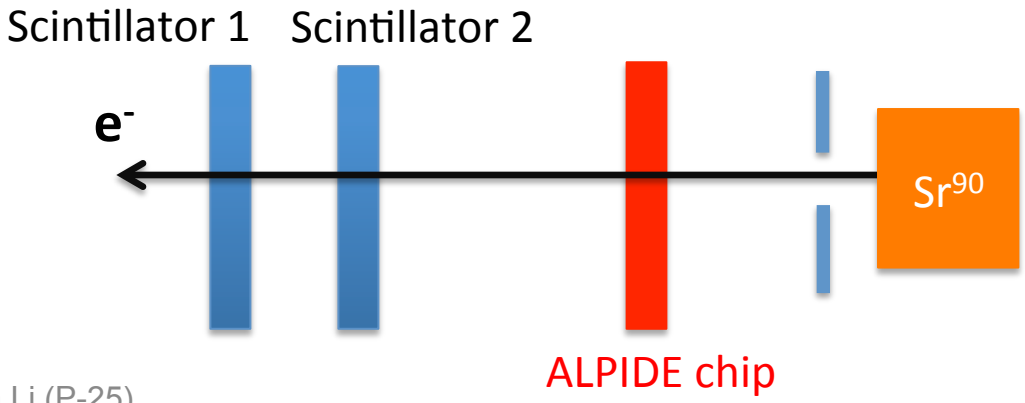
ALIPIDE Performance Evaluation Configuration

- Study the ALPIDE performance with real particles.
- Tests in triggered mode with default delay at 2μs:
  - External trigger with cosmic ray muons (rate: ~0.1HZ).



Cosmic ray setup
Muon average energy 2GeV

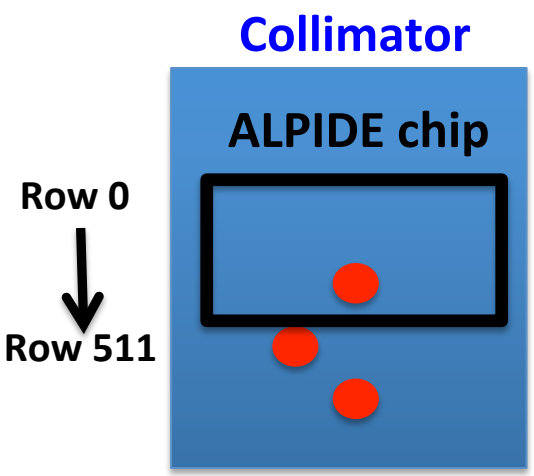
  - External trigger with ^{90}Sr beta decay electrons (rate: ~1Hz).

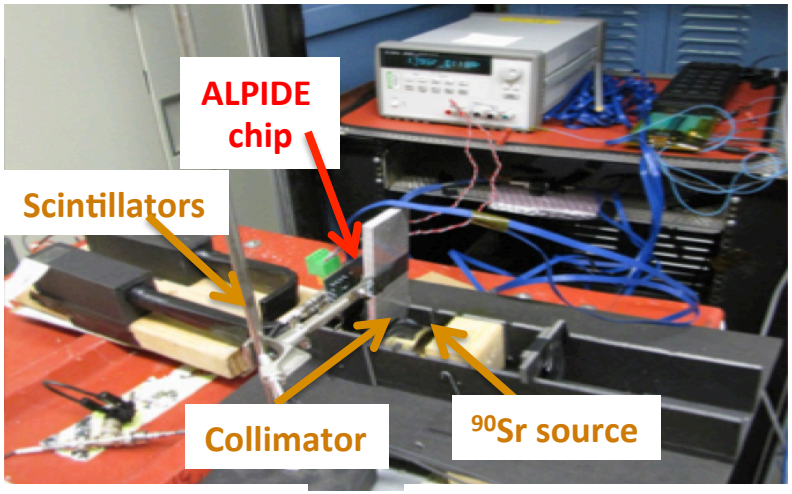


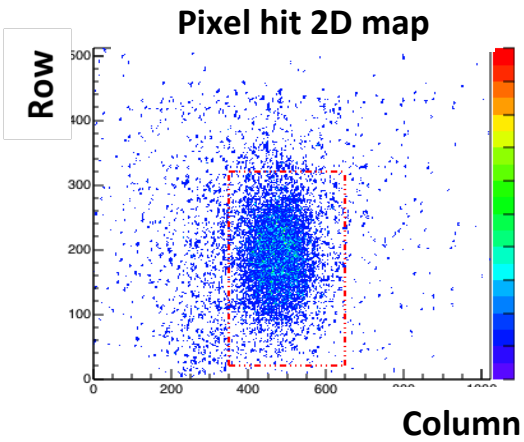
^{90}Sr setup
Electron maximum energy 2MeV

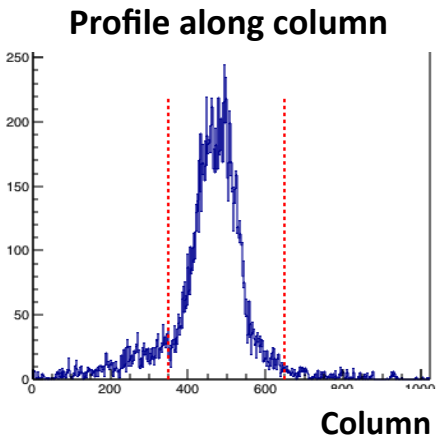
Test Achievements: verify trigger timing and signal detection

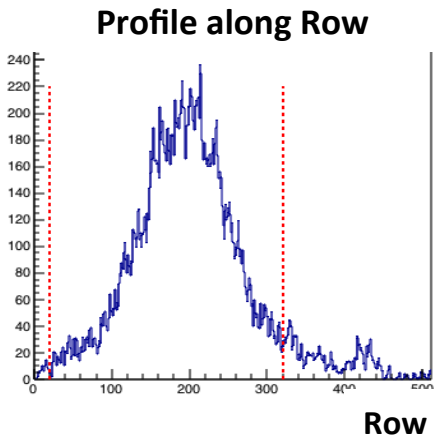
- Time in trigger and observe physical signal.
- For example: ^{90}Sr source test.







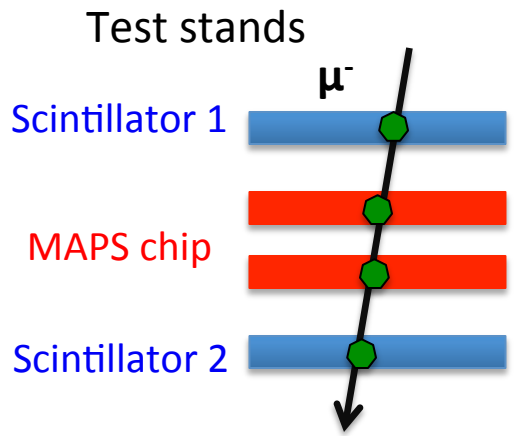


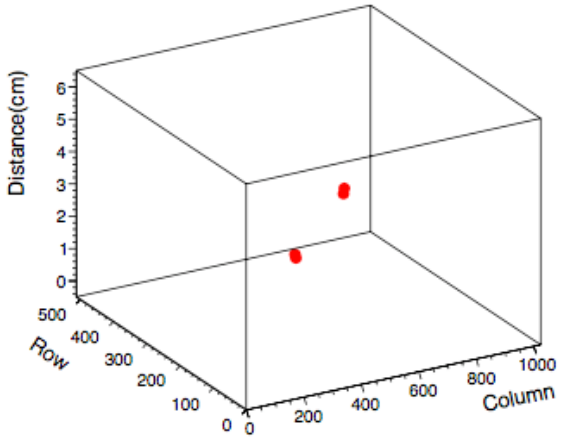


- Clear collimator structure seen in the ALPIDE chip.

Test Achievements: good hit resolution

- Initial look at tracking with two layers of ALPIDE chips.

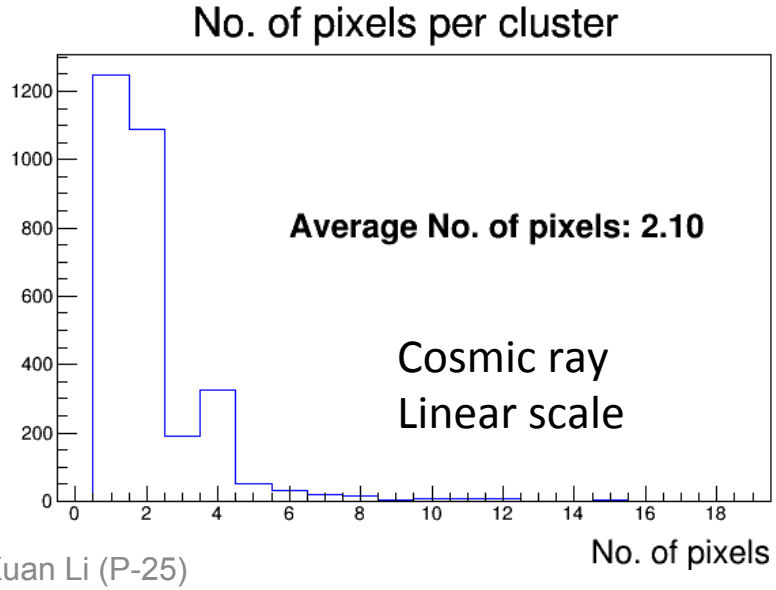




Event Display

Found clusters that belong to a cosmic ray muon track.

- Characterize the cluster size: related to the hit resolution.

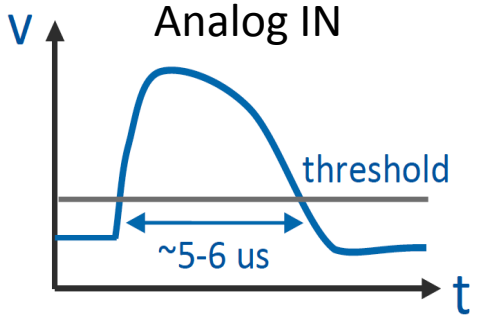


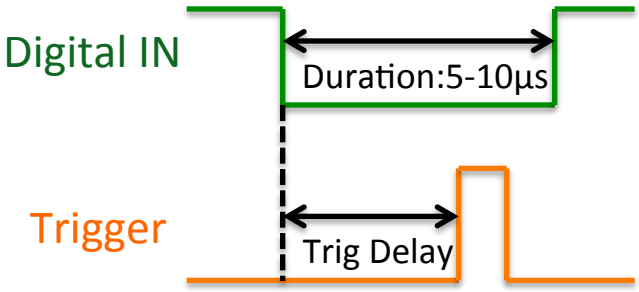
- Comparable with ^{90}Sr source test results and DESY beam test (cluster size < 3 pixels).
- Average cluster size (2 pixels) indicate the hit resolution < 10μm → Meets requirements.

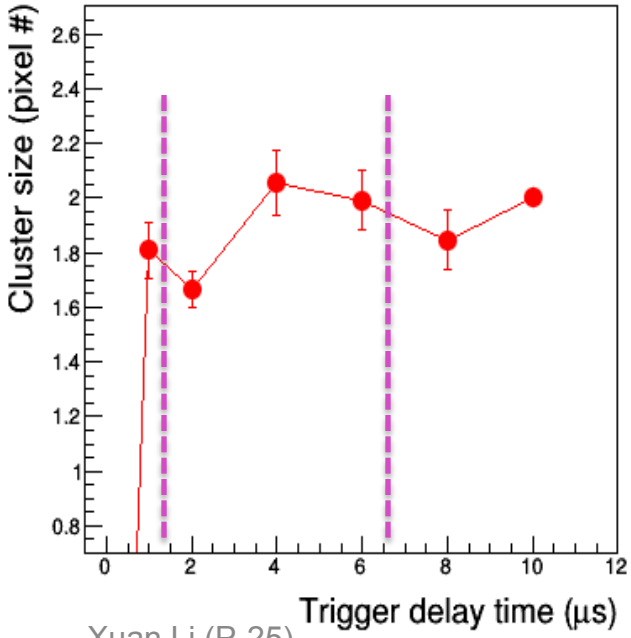
Under study: Trigger delay latency

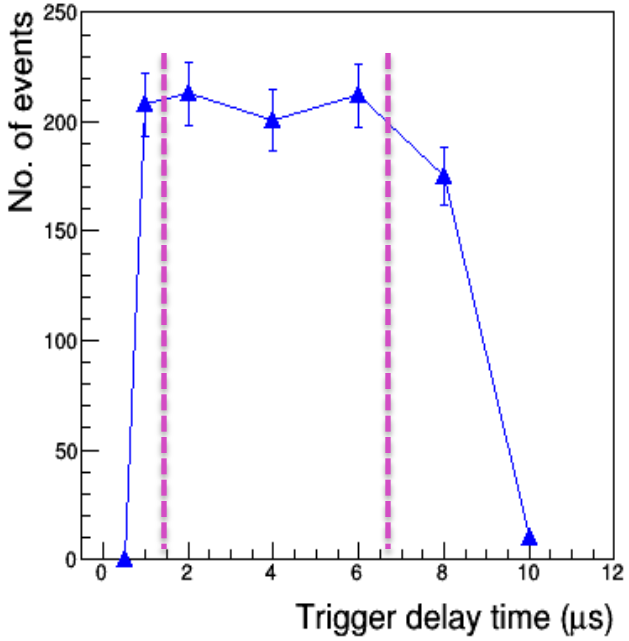
- Can the MVTX adapt to the sPHENIX trigger scheme with default trigger delay at 4-5 μs?

- The default ALPIDE trigger delay is 2μs.
- Need to tune the pulse shaping and trigger delay.





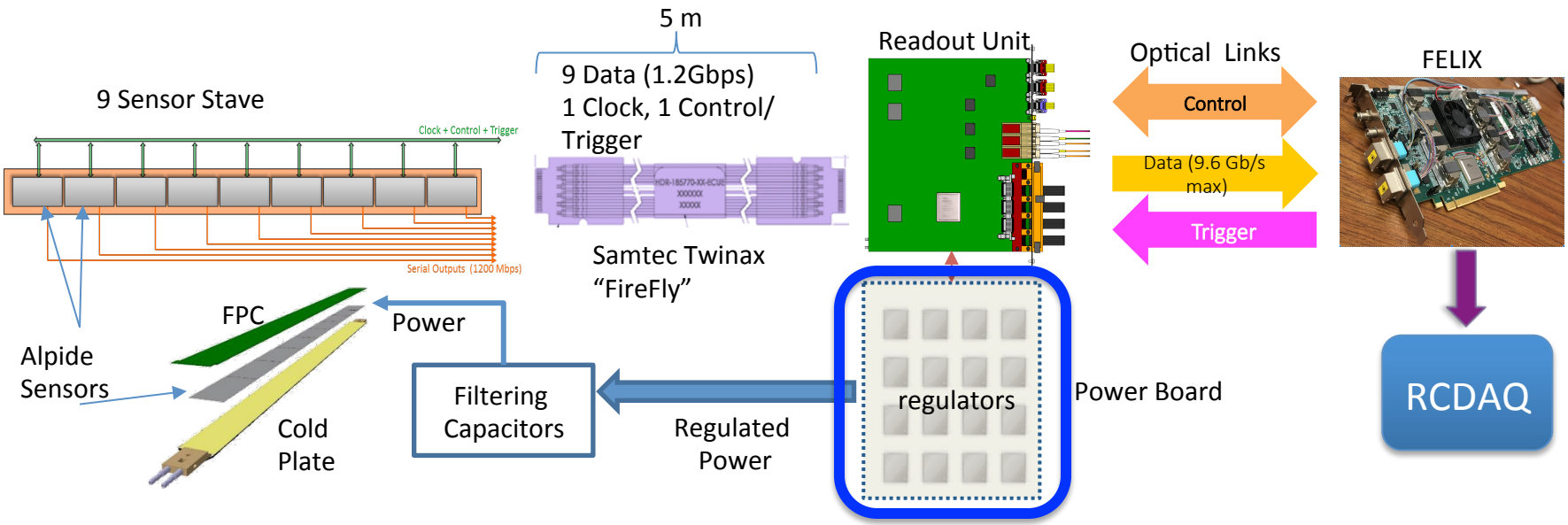


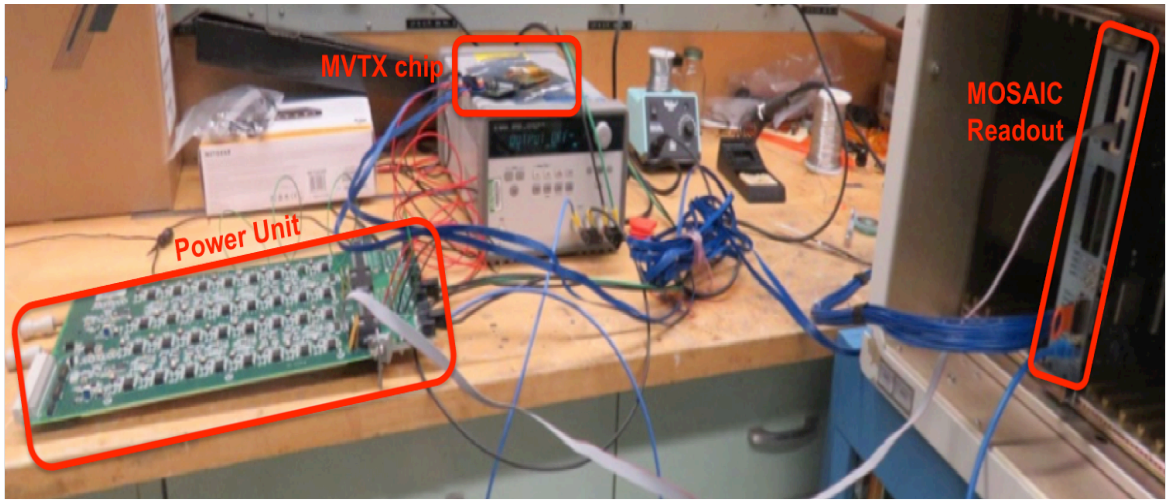


After lowering the threshold to optimize the pulse shaping time:

No significant performance differences with trigger delay from **2μs to 6μs**.

Integration: Power Board Test

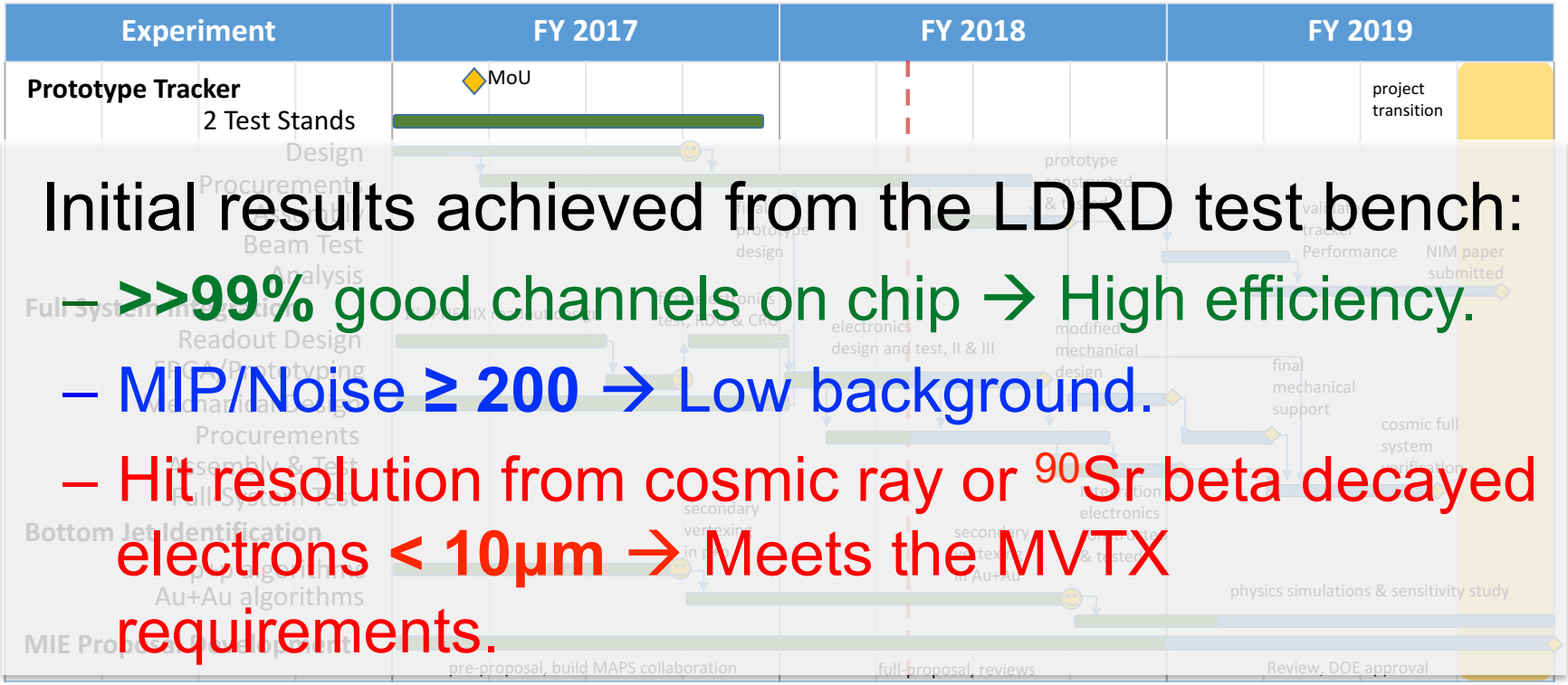




MOSAIC GUI for PB

Successfully operating the ALPIDE using the Power Board prototype!

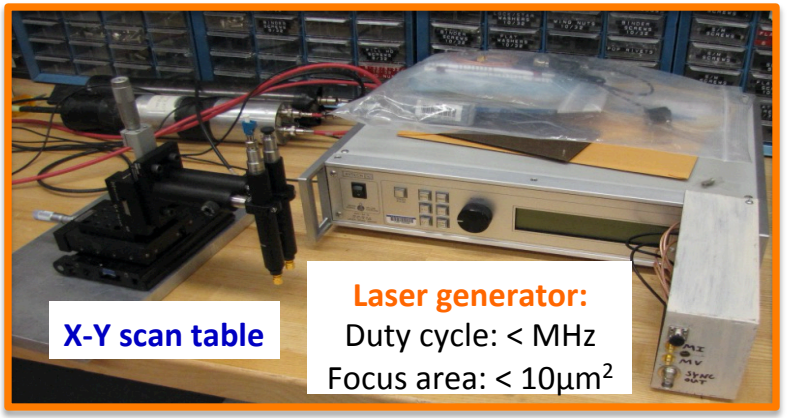
Summary



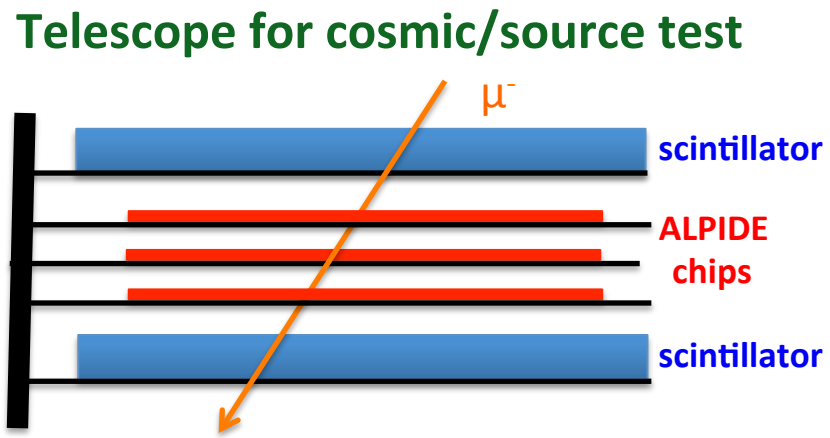
- Initial results achieved from the LDRD test bench:
  - **>>99%** good channels on chip → High efficiency.
  - MIP/Noise **≥ 200** → Low background.
  - Hit resolution from cosmic ray or ^{90}Sr beta decayed electrons **< 10μm** → Meets the MVTX requirements.
  - Proof of principle study proves the feasibility to adapt the MVTX to the sPHENIX trigger scheme.
  - Successful test of the Power Board prototype as part of the MVTX electronics.

Plans

- Set up the laser test bench to study the efficiency, noise rate, trigger delay time, threshold, pulse shaping, etc.



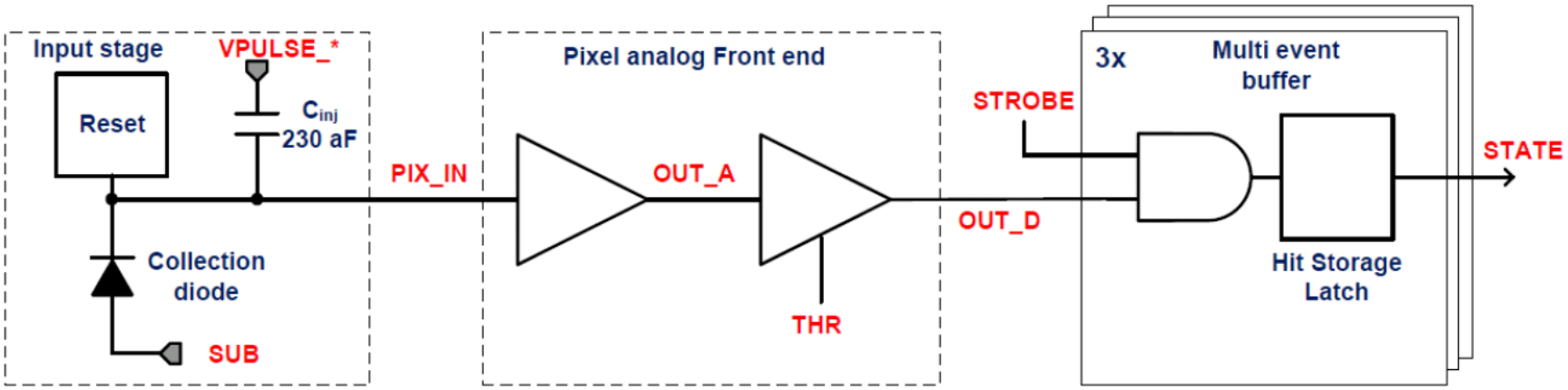
- Set up the telescope containing multiple layers of ALPIDE chips (staves) to study the track resolution, efficiency, etc, from cosmic ray and source tests.

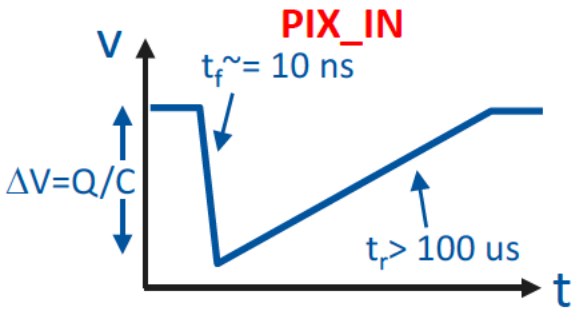


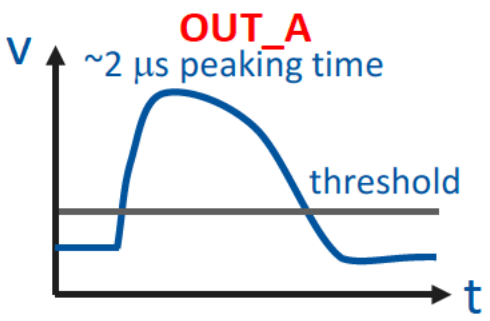
- Complete optimizing the ALPIDE performance with the RU+FELIX+PB full readout chain this summer.

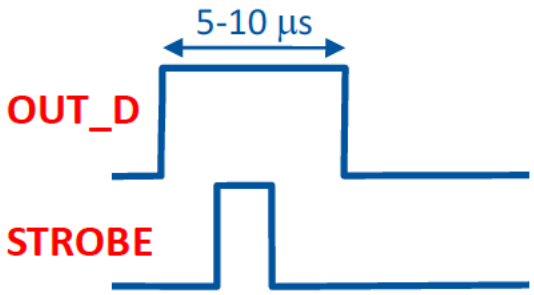
Backup

- ALPIDE pixel block diagram.





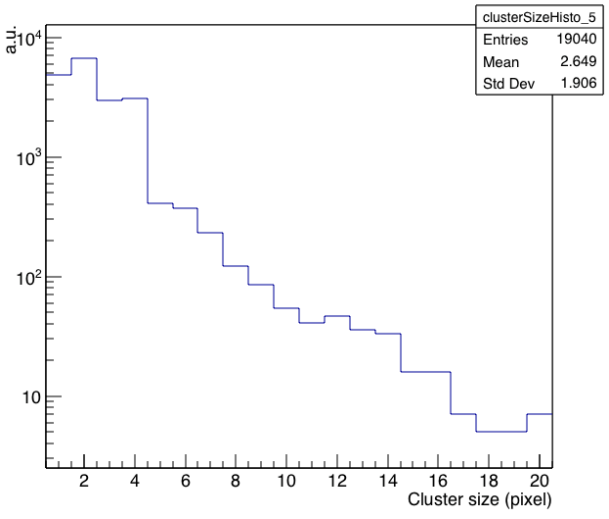




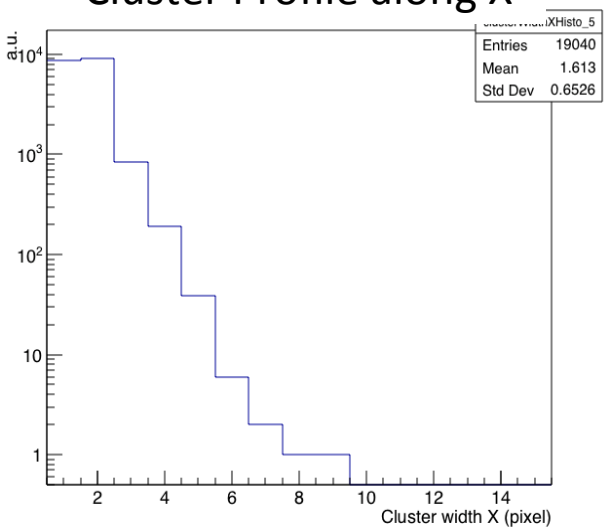
Backup

- Cluster evaluation by the CERN team from 450 MeV e- beam test.

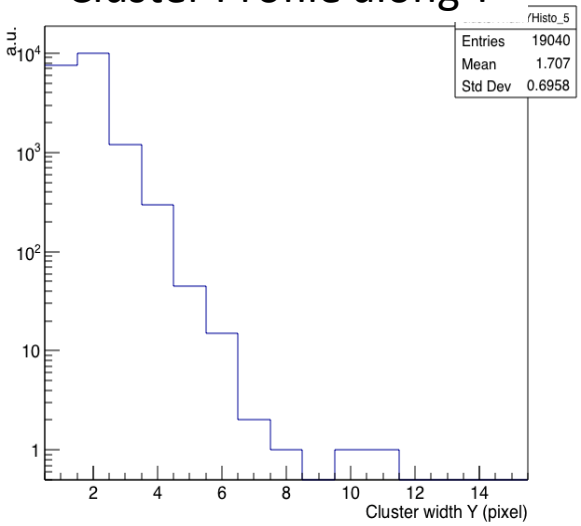
Cluster Size



Cluster Profile along X



Cluster Profile along Y



- Even particle energies are different, similar results are achieved between the test bench studies with cosmic ray or ^{90}Sr beta decayed electrons.

Achievements: cluster determination

- Cluster size determined from ^{90}Sr beta decayed electrons.
- The average cluster size determined from ^{90}Sr source is comparable with cosmic ray test.