# **MVTX Status**

Camelia, Grazyna and Ming sPHENIX L2 Meeting 05/13/2021

# Stave Production Completed at CERN

- next step: shipping!
  - 114 HICs assembled
  - 84 staves completed
  - Yield for sPHENIX staves from assembled HICs = 73.7%

- 79 GOLD staves, 94%:
  - 44 GOLD/OK
  - 35 GOLD/CAN
- 5 SILVER staves, 6%:
  - 3 SILVER/OK
  - 2 SILVER/CAN

### **Shipping status:**

- 3 gold and 1 silver staves @LBNL
  - Stave testing and QA in progress
- 4 Silver-staves shipping in preparation:
  - Double check issues observed in previous shippings (abnormal pressure drops recorded by the logger)

We have 2 transport cases, capable of shipping 20 staves per trip

# Mechanical Design and Production

- Carbon fiber+Al pieces (Workshape/France)
  - 1st half of detector:
    - all looks good so far for the layers & SB
    - CYSS (the conical shell that houses all layers): going through 2nd iteration to deal with some spring-back
    - Shipment: end of May
      - Designing France->LBL shipment box to be used also as:
        - Main assembly fixture in LBL
        - LBL->BNL shipping box (w/ half fully assembled detector)
  - 2nd half: expected in LBL after ~3-4 weeks (some parts already made)

### Insertion mock-up

- Essential work this year: define insertion sequence, define procedure to safely transfer from rails to X-wing, survey strategy, etc
- Support (X-wing) + insertion mechanism: ready to be ordered
- o Ordering connectors, cooling lines, etc







# Readout Integration Progress

- New data format and readout modes
  - Triggered readout
  - Continuous readout
- mGTM integration in progress @LANL
  - Powered up, testing underway
- CAEN power system in progress
  - Working w/ vendor on control SW
- Slow control and monitoring
  - 2 CANbus controllers ordered and received

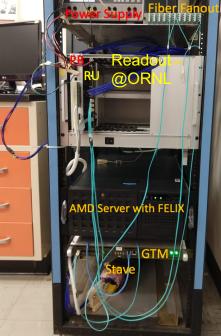
- Readout system setup @ORNL
  - First event readout with internal trigger sequencer

#### Proposal

- 17.02 160MHz clocks = 1 RHIC strobe
- Use 32bit Orbit counter plus 8 bits of the BC counter (BC[11:4]) to transmit BCO (40bit)
- Internal 40MHz counter is used to generate HB triggers (e.g. every 16 counts shown here)
  12us = 480 40MHz counts -> 9bit counter?
- 4 lowest bits of this counter transmitted as lower 4 bits of BC[11:0]







### Schedule and Risks

### **MVTX** detector construction plan:

- CFC production
  - 1st half-detector available end of May @LBNL
  - 2nd half ~end of June
- Assembly test fit @LBNL
  - June July, testing
  - Review ~end of July/early Aug. (?)
- Half-detector assembly @LBNL
  - per present P6:
    - Aug. Dec., 2021
    - Ship to BNL in Jan, 2022
- BNL commissioning (~Jan 2022)
  - Setup clean tent @1008 (PHENIX Laser room?)
  - Money in P6 to buy one for MVTX (BNL)
- Installation @IR ~9/2022
  - is IR gonna be ready for MVTX or we know/expect already X month delays? (question for Ed)

#### Other activities:

- Insertion mockup @Bates (over summer)
- Cooling system (over summer/fall)
  - detector (Bates), electronics (LANL)
  - In the end: ship and final test @BNL
- Detector safety system integration
  - Under discussion with BNL
- Stave test & QA @LBNL
  - MOSAIC system for single stave readout from the half-detector
  - Special readout cables @PP3

# ITS IB Installation 5/12/2021.... and MVTX Insertion System



