MVTX Stave Production Readiness

Ming Liu

LANL

10/12/2018

sPHENIX PMG Meeting

MVTX Detector

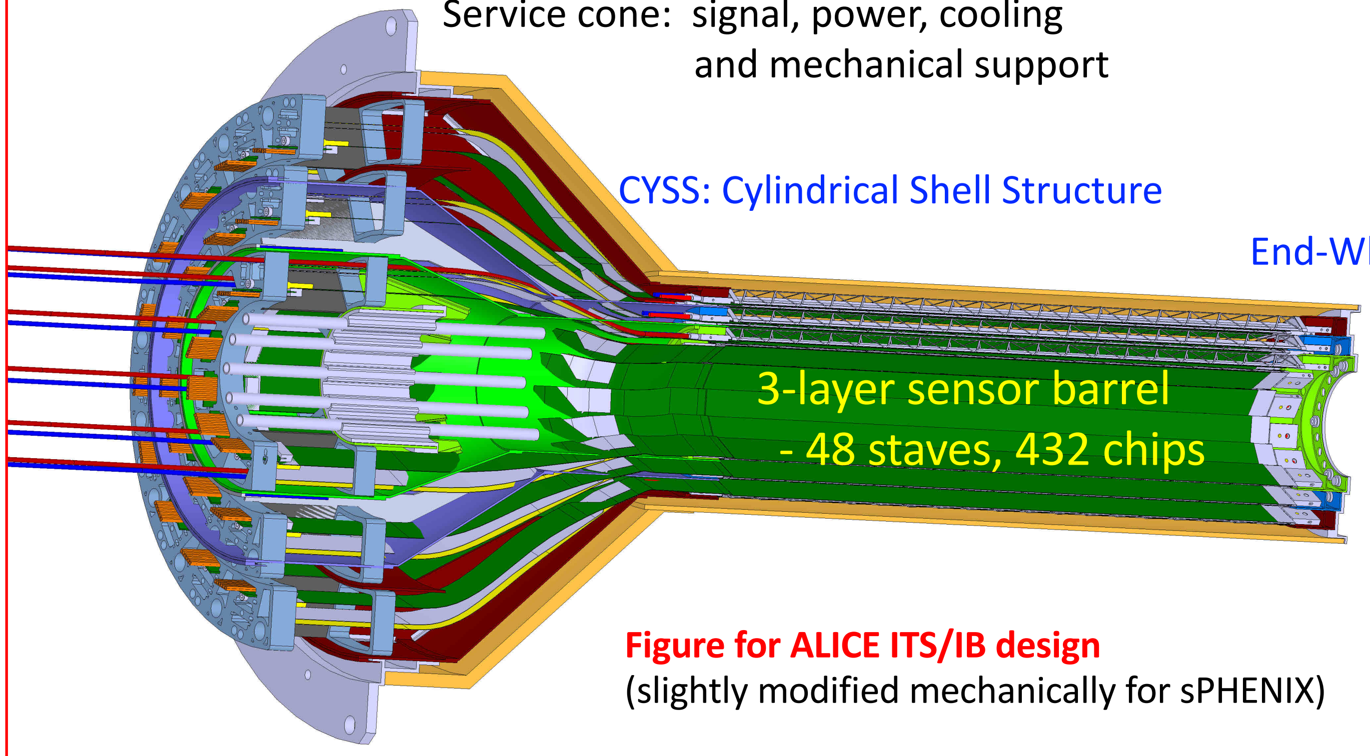
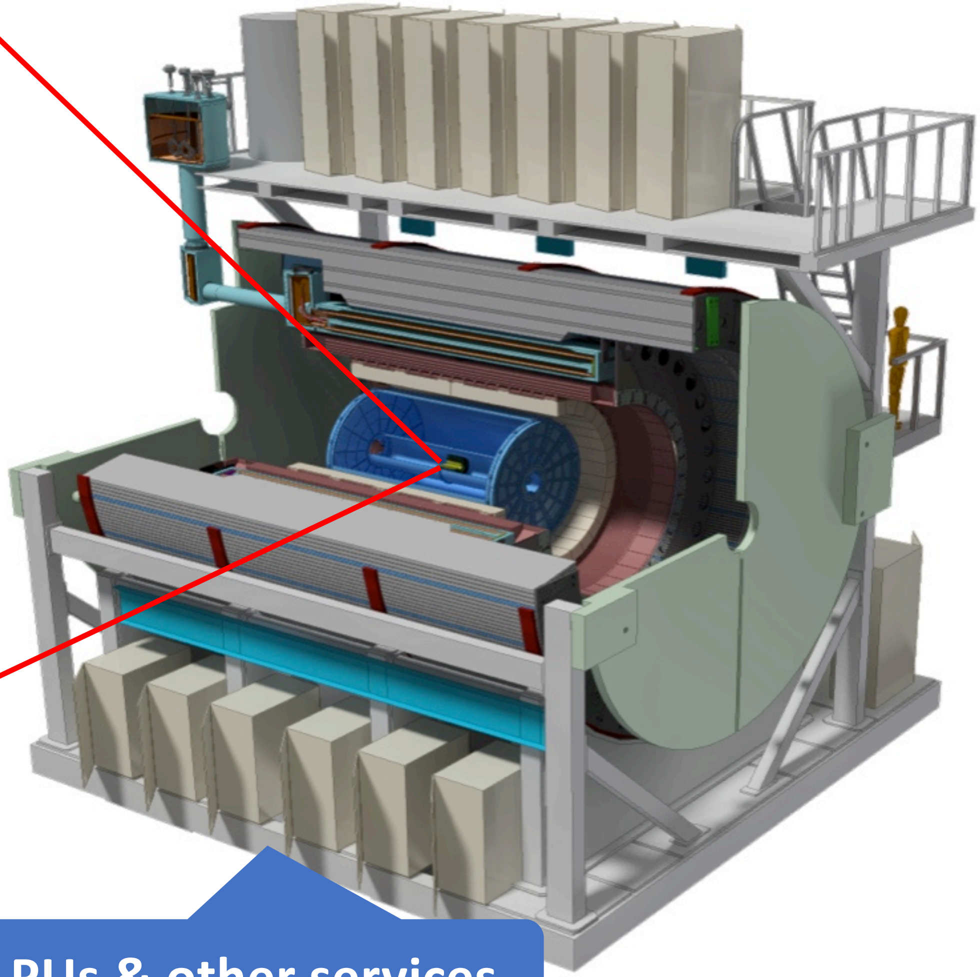


Figure for ALICE ITS/IB design
(slightly modified mechanically for sPHENIX)

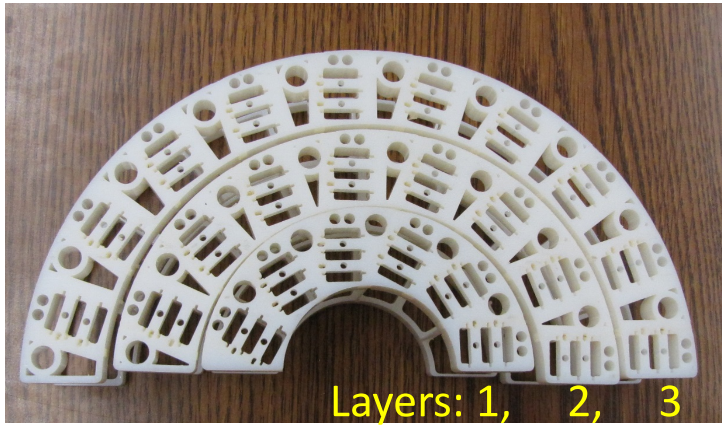


MVTX RUs, PUs & other services

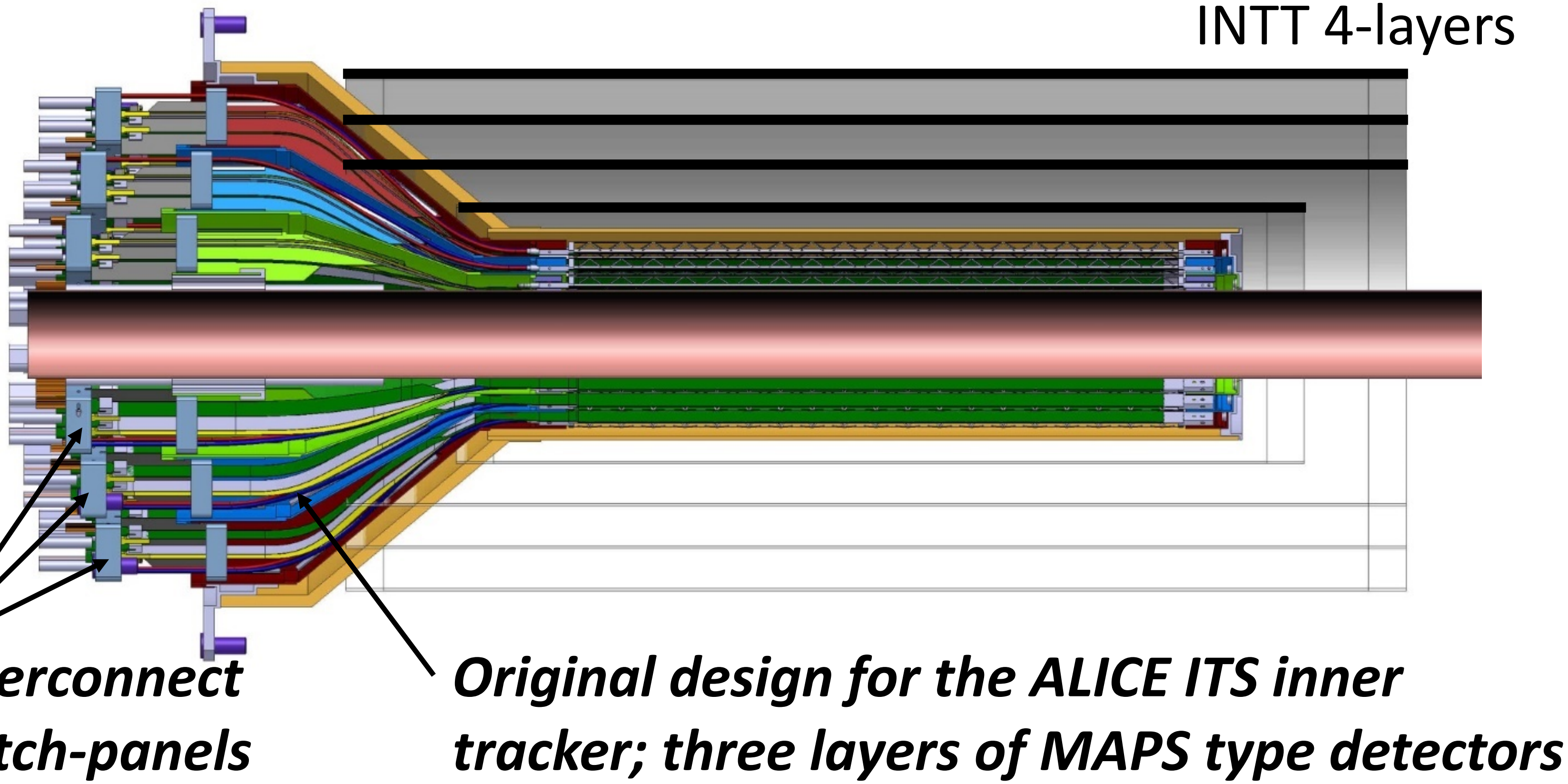
MVTX parameters

	Layer 0	Layer 1	Layer 2
Radial position (min.) (mm)	23.7	31.4	39.1
Radial position (max.) (mm)	28.0	35.9	43.4
Length (sensitive area) (mm)	271	271	271
Active area (cm^2)	421	562	702
Number of pixel chips	108	144	180
Number of staves	12	16	20

INTT-MVTX Conflict: a Resolution

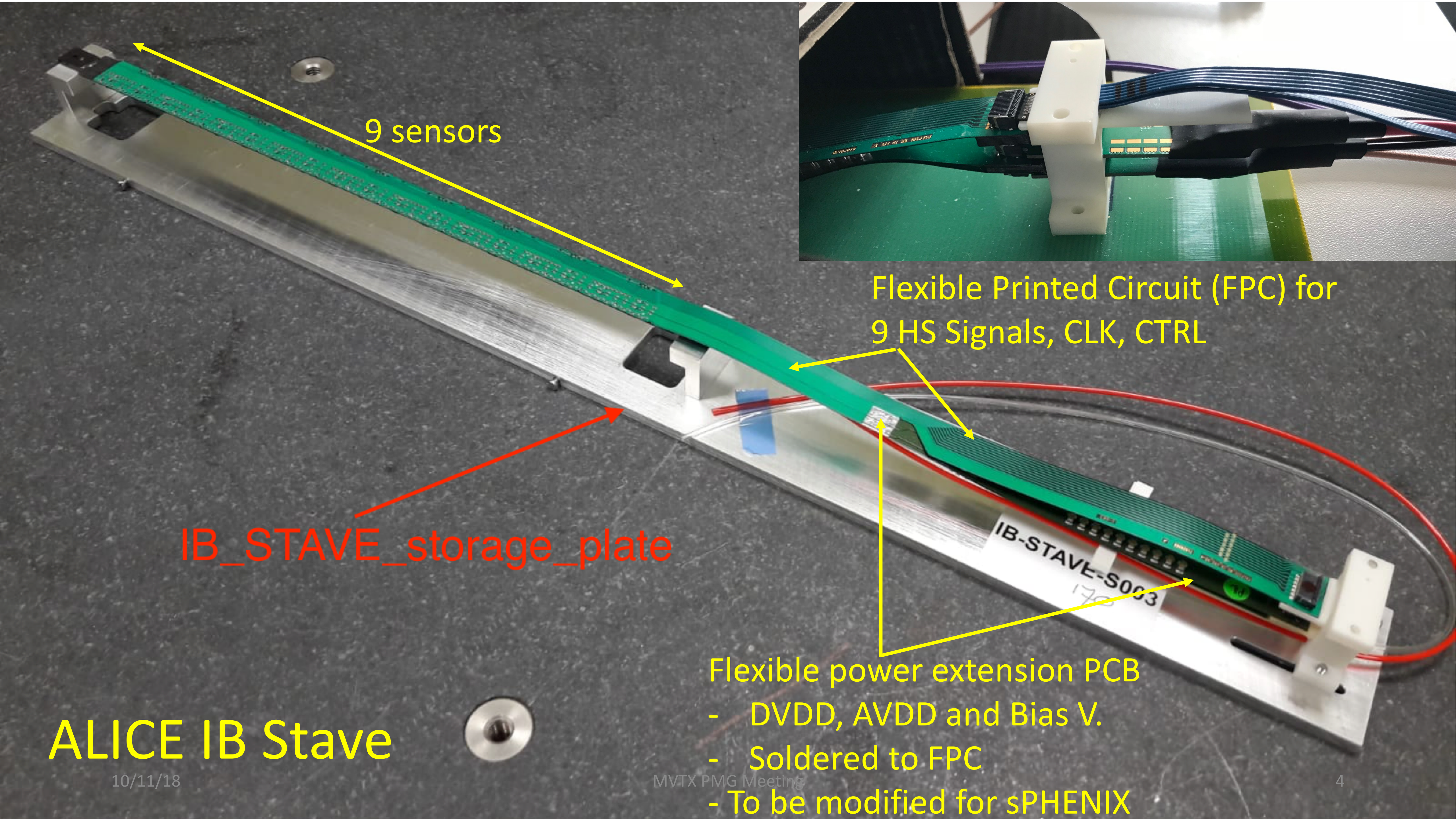


ALICE IB Patch-Panel 3-D Model
- All connectors are located at the same Z position
- One can move some connectors out in Z to reduce “R”



- Longer power cables!
- HS FPC untouched!

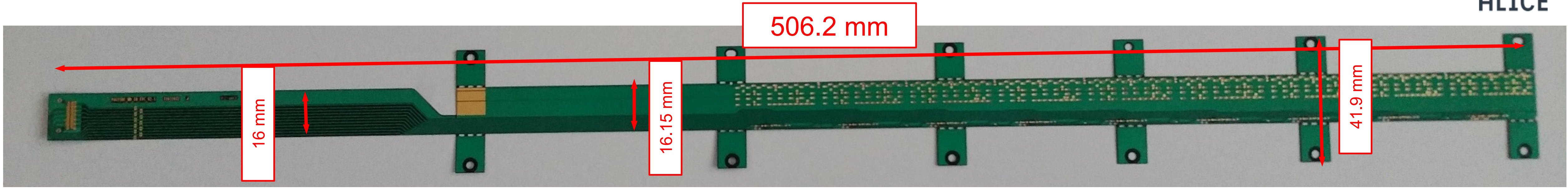
The INTT shown only includes ladders; no extension cables, connectors, cooling barbs, etc.

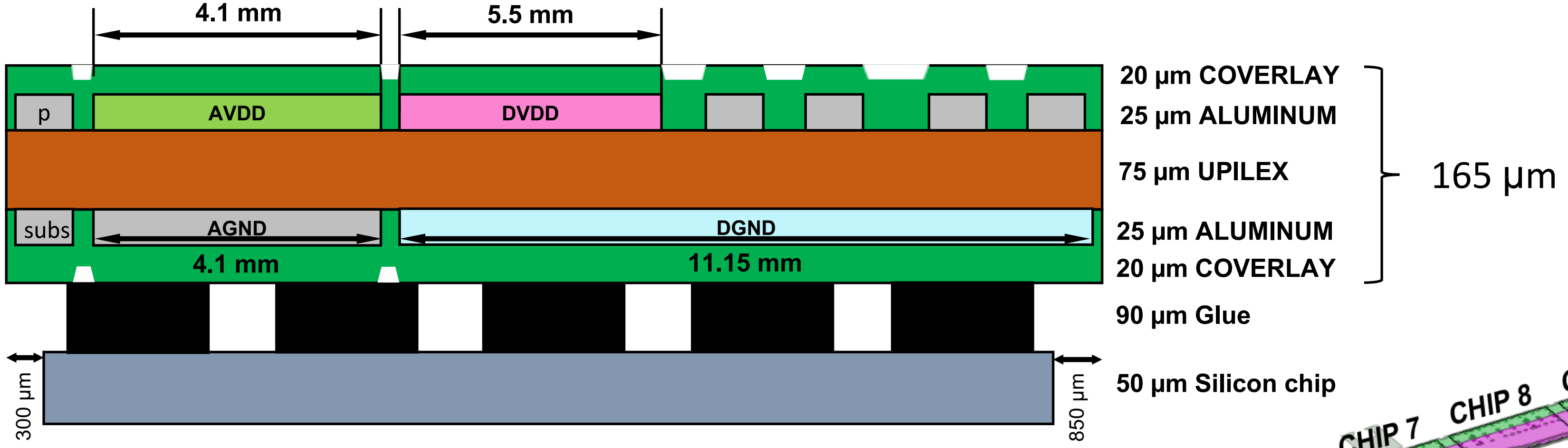

9 sensors
Flexible Printed Circuit (FPC) for
9 HS Signals, CLK, CTRL
IB_STAVE_storage_plate
IB-STAVE-S003
Flexible power extension PCB
- DVDD, AVDD and Bias V.
- Soldered to FPC
- To be modified for sPHENIX
ALICE IB Stave

IB FPC Layout

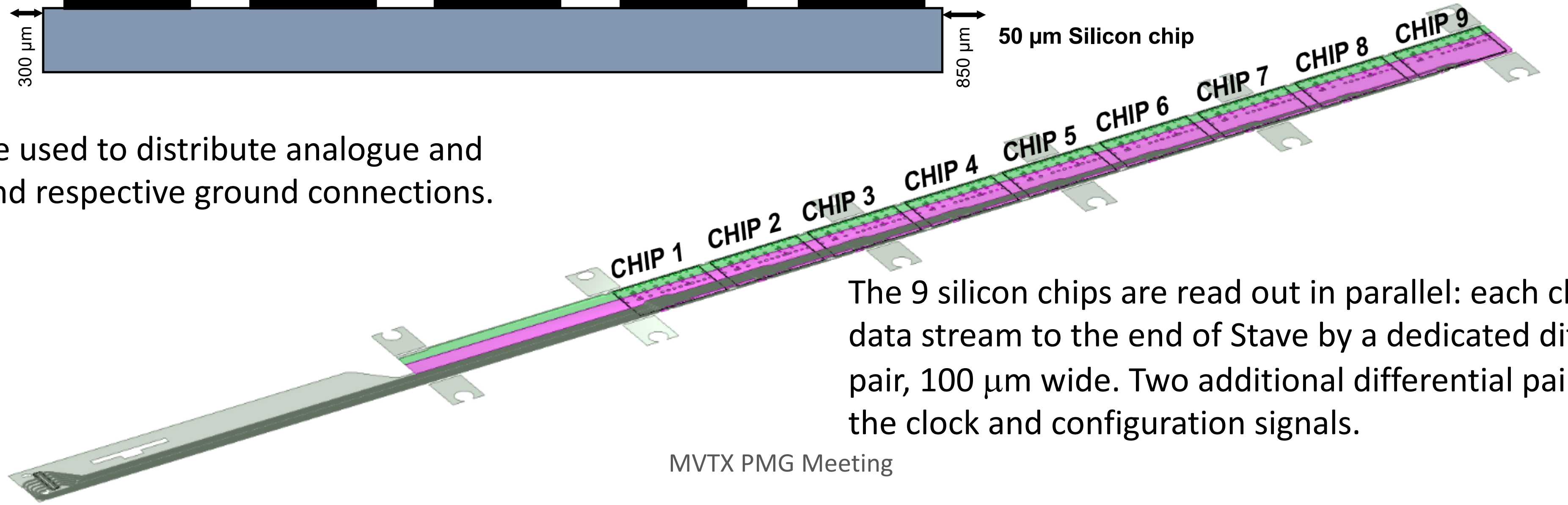
From Antonello Di Mauro

ALICE ITS Upgrade





Large planes are used to distribute analogue and digital power and respective ground connections.

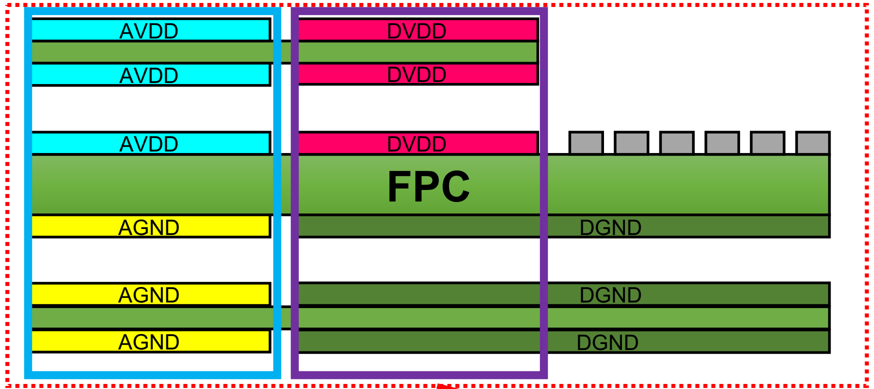


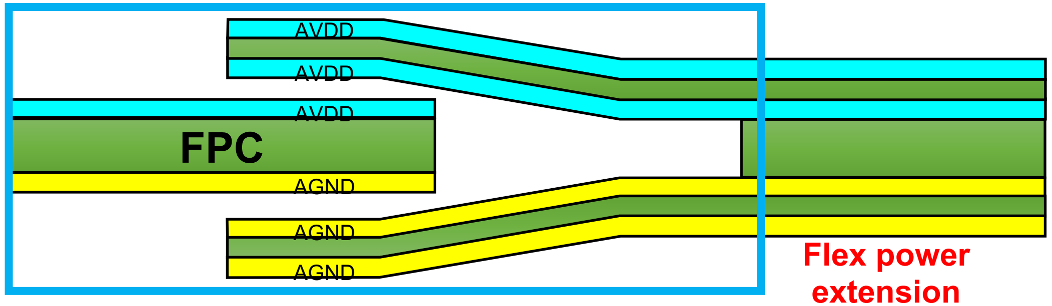
The 9 silicon chips are read out in parallel: each chip sends its data stream to the end of Stave by a dedicated differential pair, 100 μm wide. Two additional differential pairs distribute the clock and configuration signals.

FPC Extension for Connection to Electrical Services

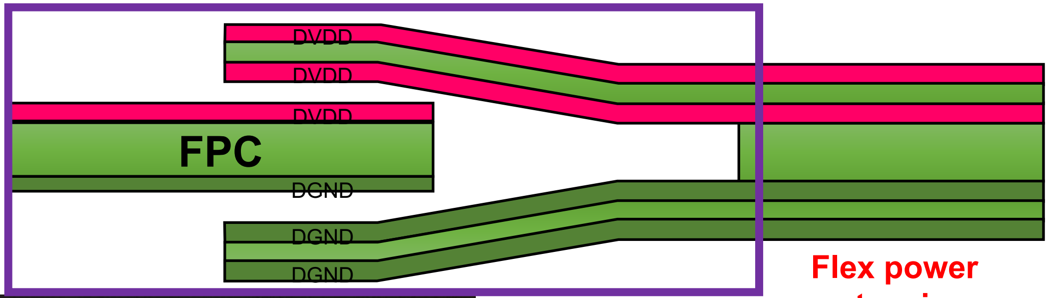
The connection to the service cables is achieved by a double FPC extension which is soldered to the HIC

x-section at interconnection between FPC and extensions

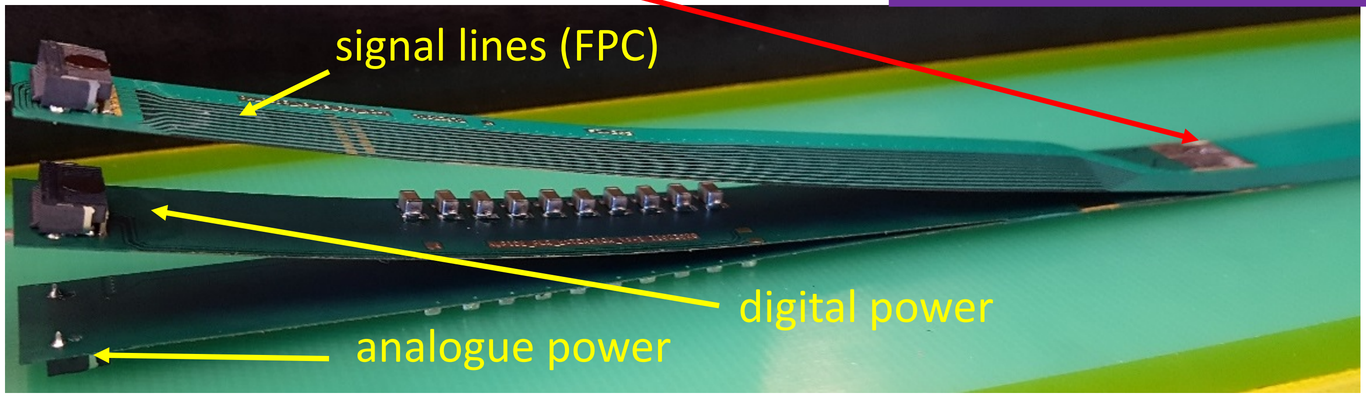




Flex power extension



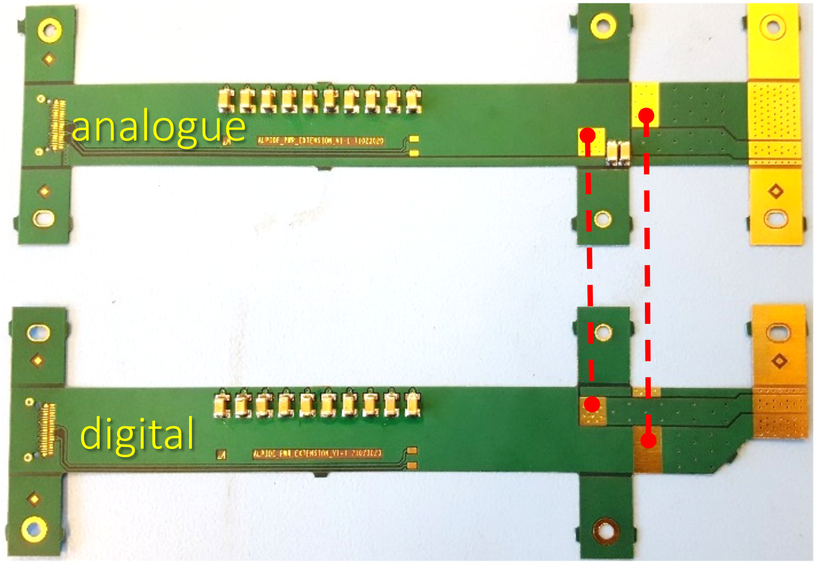
Flex power extension

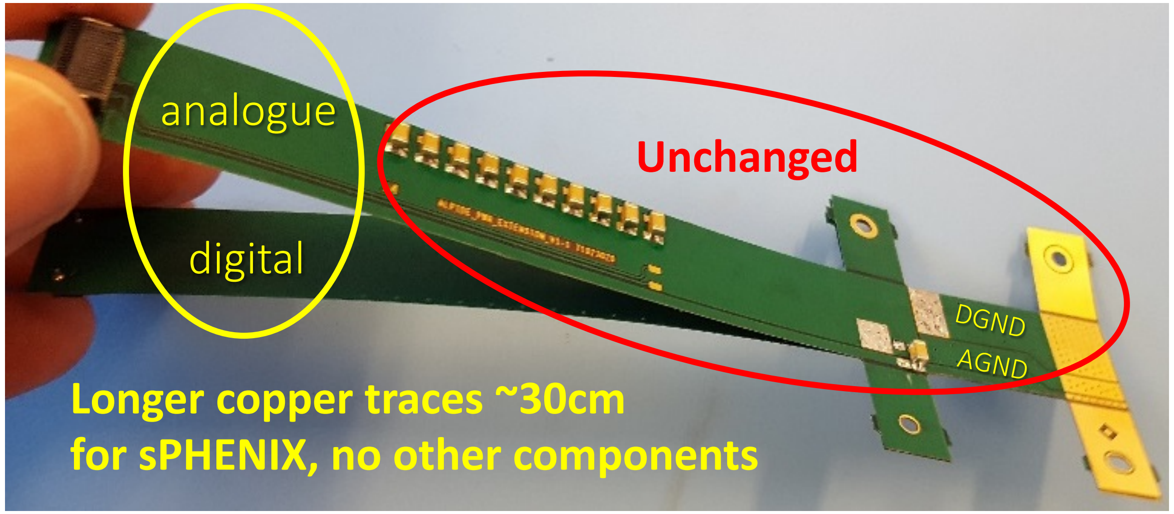


Modified for sPHENIX: 15cm -> 40cm

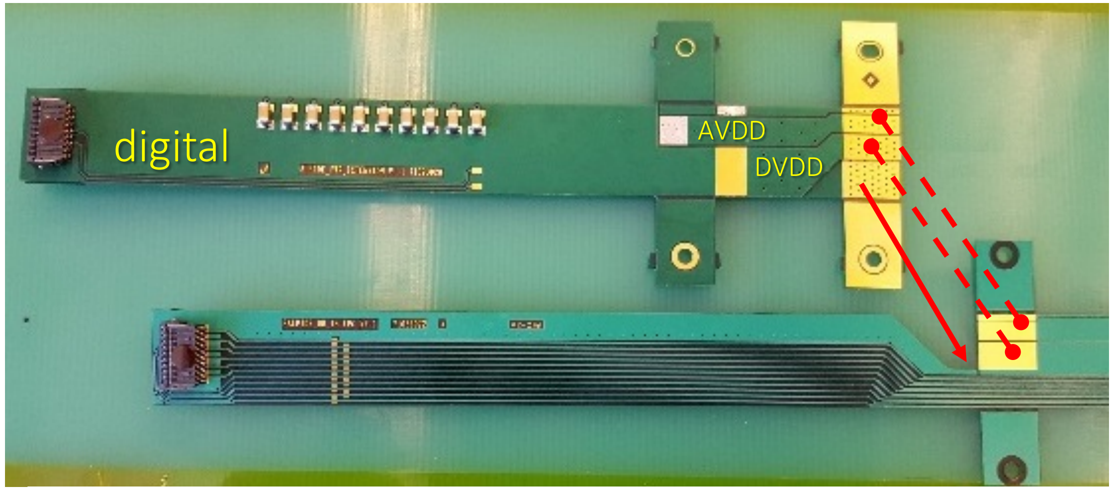
FPC Extension for Connection to Electrical Services

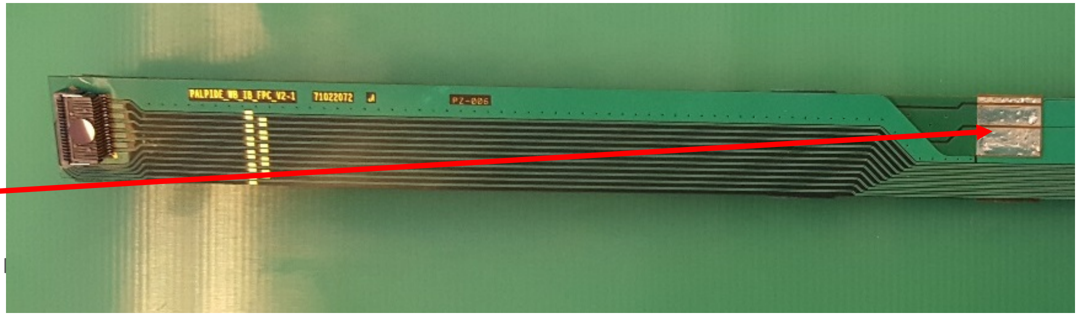
2-layer flex, PI: 50 µm, Cu: 35 µm, solder mask: 20 µm





The two flexes are connected together, AVDD is transferred from top to bottom

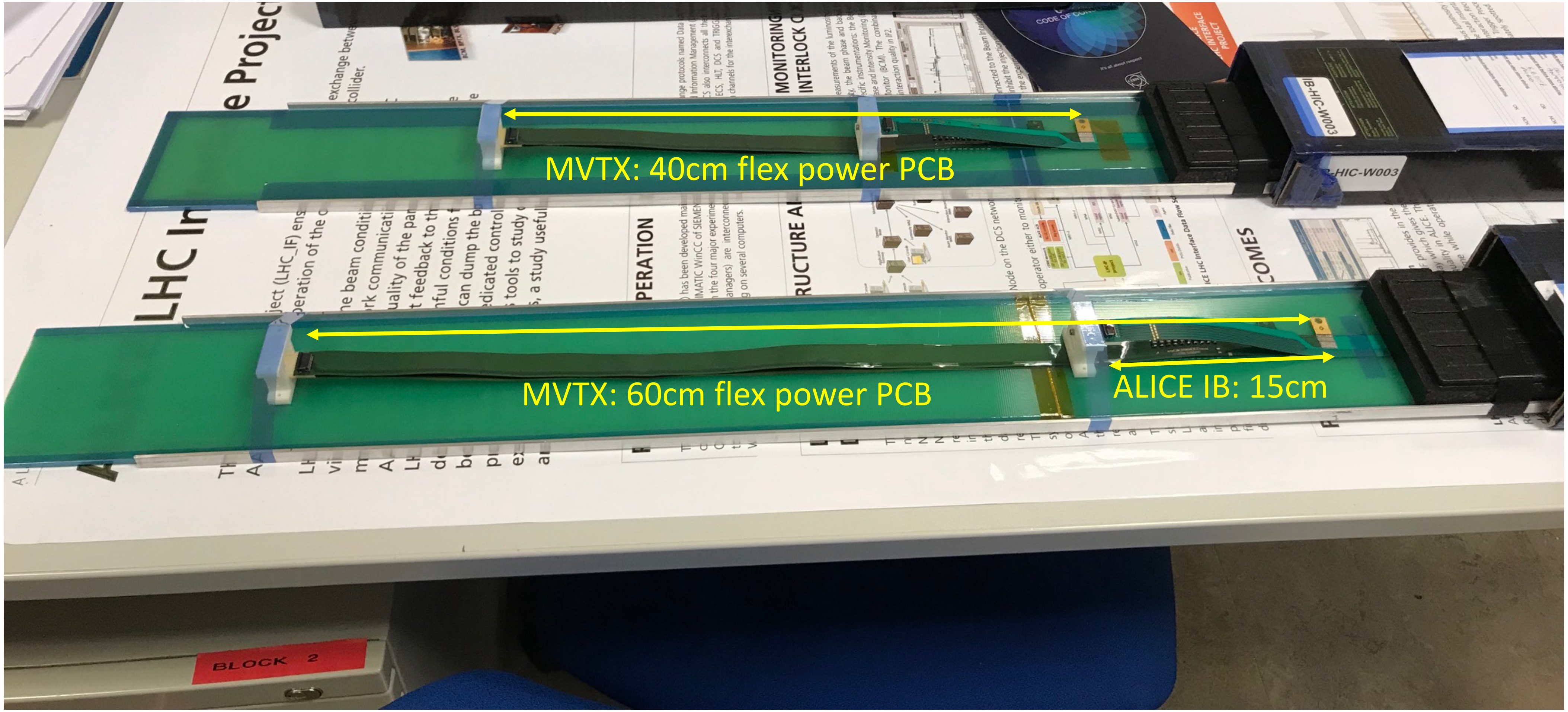




The PWR extension is connected to the FPC by iron soldering and wings are cut.

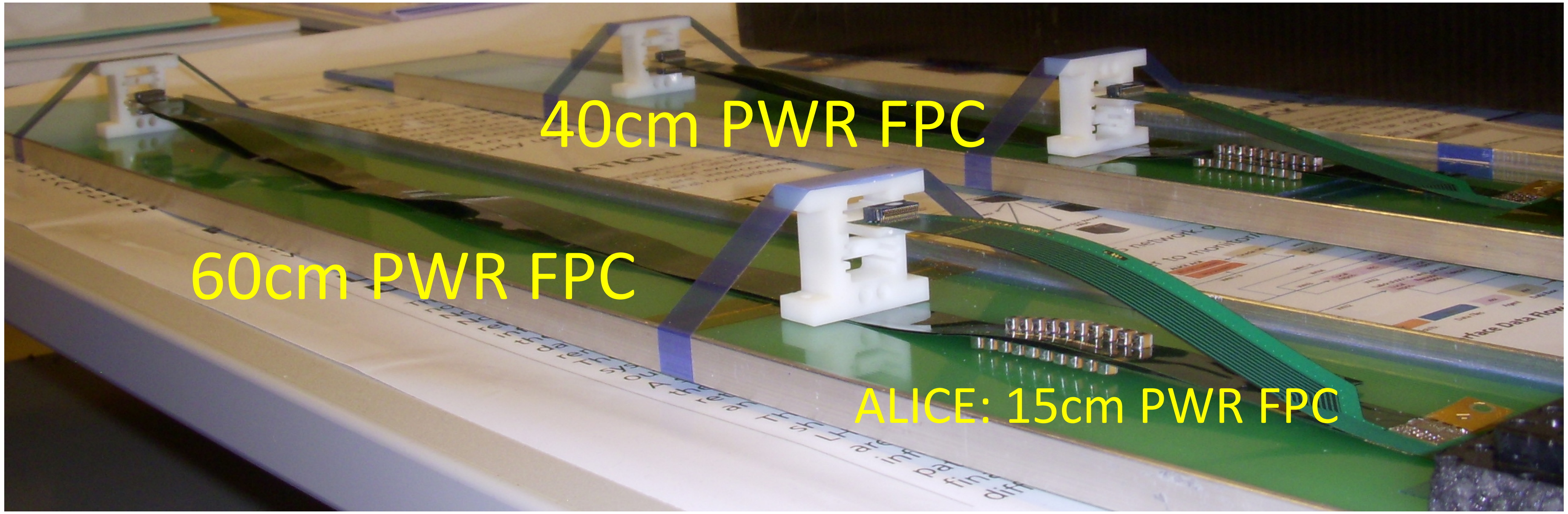
Two HICs Produced and Tested at CERN w/ Extended Power Cables

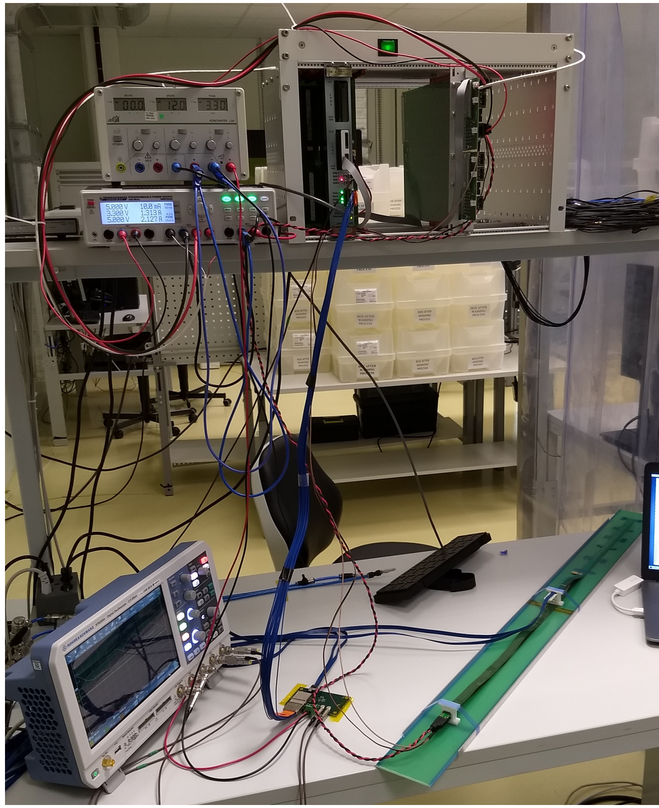
NO noticeable difference in sensor performance, as expected



Test Stave/HIC with extended power PCB

- Built and tested two HICs at CERN in the week of 9/17
  - No change in sensor performance (noise, threshold) observed, as expected;





Followed identical
ALICE IB QA test procedure,
with a 8m SamTec cable!

More details presented by Dr. Sho Uemura at last Friday's sPHENIX general meeting 9/23/2018

HICs Test Results from CERN

- Threshold and noise (from charge injection turn-on curve) are indistinguishable
- Other tests also see no change: supply currents, high-speed data transmission

After: same ALICE HICs, replaced power FPCs

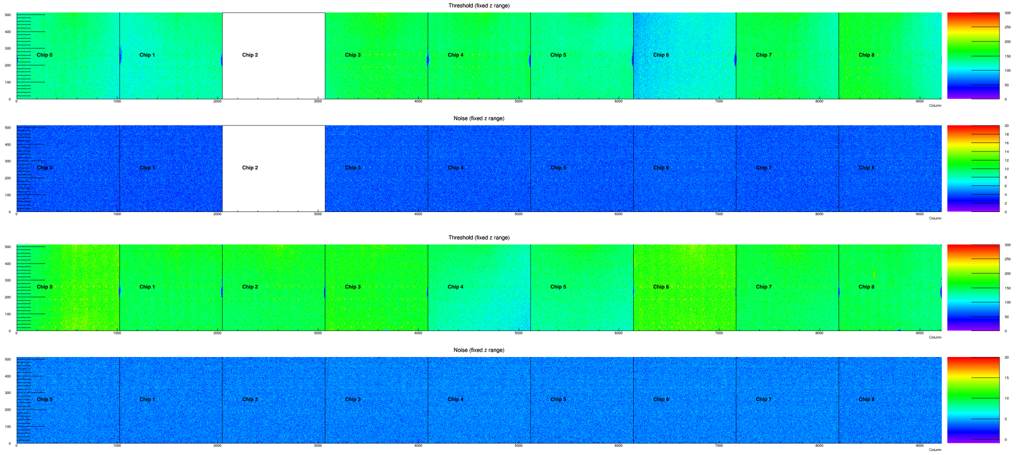
- 15 cm: **Before: 2 ALICE IB HICs**

Thr.

Noise

Thr.

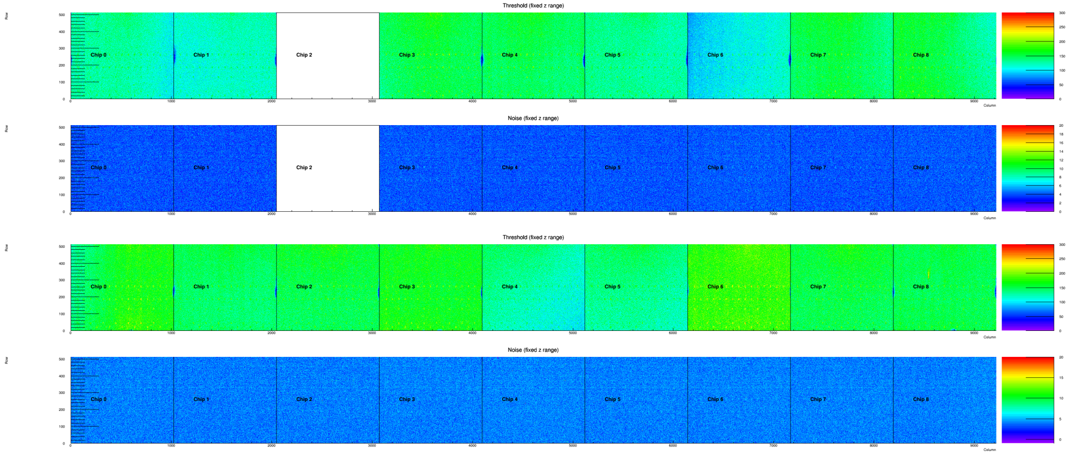
Noise



HIC1

HIC2

- top 40 cm, bottom 60 cm:



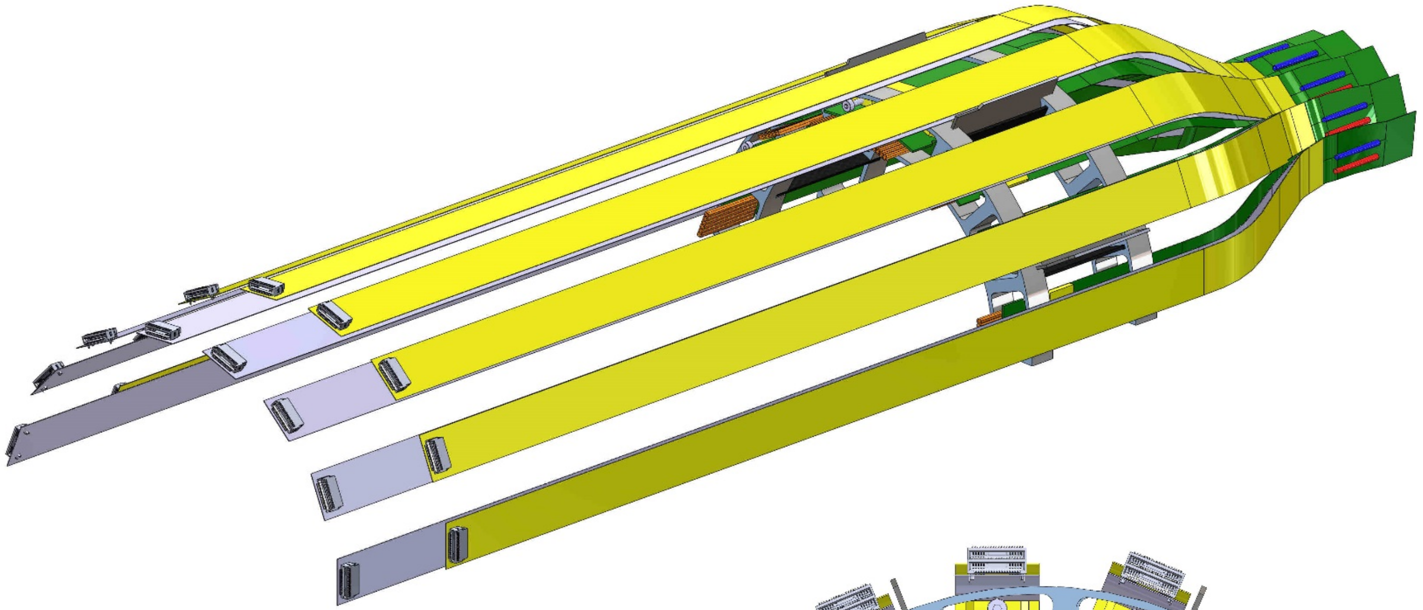
Chip-0

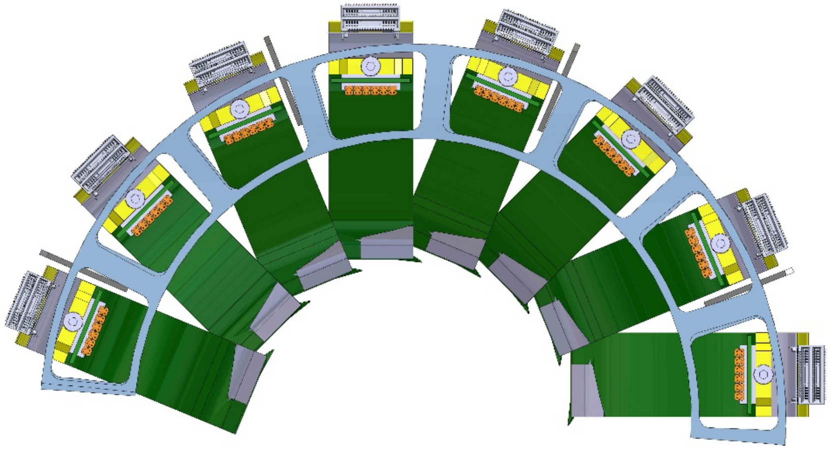
Chip-8

Noise level: ~4 e's; Threshold: ~180e's; MIP: ~1000 e's

MVTX middle layer – power extension cable assembly including the reduced ID & OD patch-panel

From Walt Sondheim





Power PCB cost: Unit price ~ Cable length

Components: ~$40/pair
Assembly: ~$2K

CiREXX INTERNATIONAL

PCB Fabrication Quotation

Quote Number: 157999-77502
Quote Date: 4/5/2018

Design • 24 Hour Turn Fabrication • Assembly

Company: LOS ALAMOS NATIONAL LABS
Part Number: EXTENSION_V1-2
Dwg Rev: *A/W Rev:*
File Name: 1.PDF

Cust ID:
Customer Name: ALEX TKATCHEV
E-mail Address: atkatchev@lanl.gov
Business #: 505-667-9437
Fax #:

Board Quantity	Delivery	Unit Price	Test	Tooling	Total
10	10 Day Turn	$150.89	$250.00	$200.00	$1,958.90
50	10 Day Turn	$61.27	$250.00	$200.00	$3,513.50
100	15 Day Turn	$56.40	$250.00	$200.00	$6,090.00

15cm Flex PCB (ALICE): $61/pair

Specialities

Flex
Rigid-Flex
Roger's / FR4
All Roger's Metal Backed Boards
HDI - Blind Via Boards
Heavy Copper Boards
Copper Filled Vias
Stacked Vias

Certifications

UL 94V-0
Mil. Spec. 31032
ISO 9001
AS9100
ITAR Registered

www.cirexx.com

* * *Information and assumptions used to generate your quote:*

Layers: 2
Material Type FLEX
Board Thickness: 0.007
Board Size: 2.346 x 5.905
Rout Type: ROUT INDIVIDUALLY
Array Size: x
Boards perArray:

	Min T/W	Min A/G
Outer Layers:	0.0050	0.0050
Inner Layers:		

Hole Count: 277
Smallest Hole Size: 0.008
Netlist:

Gold Tips: None
Board Finish: ENIG
Controlled Impedance: No
Controlled Dielectrics: Yes
Plated Edges:
Milled Areas:
Counter Sinks:
Counter Bores:
Extra Mechanical Drill Steps:
Extra Laser Drill Steps:
Extra Lamination Steps:
Via fill Process Steps
ITAR: NO
Build to: IPC-6013 CLASS 2

* * *Comments:*

NO IPC CALL OUT FOR CLASS CERTIFICATION ASSUMED CLASS 2 NO GERBERS ASSUMED TRACE AND SPACE. PDF HAS WHAT APPEARS TO BE 2 PARTS LEFT AND A RIGHT ASSUMED RFQ AT 1-100PCS MEANS SETS 1-100 OF EACH. NO FINISH CALL-OUT ASSUMED ENIG.

CiREXX INTERNATIONAL

PCB Fabrication Quotation

Quote Number: 158167-77622
Quote Date: 4/13/2018

Design • 24 Hour Turn Fabrication • Assembly

Company: LOS ALAMOS NATIONAL LABS
Part Number: EXTENSION_V1-2 (VERSION 15.750)
Dwg Rev: *A/W Rev:*
File Name: 1.PDF

Cust ID:
Customer Name: ALEX TKATCHEV
E-mail Address: atkatchev@lanl.gov
Business #: 505-667-9437
Fax #:

Board Quantity	Delivery	Unit Price	Test	Tooling	Total
10	10 Day Turn	$202.27	$250.00	$200.00	$2,472.70
50	15 Day Turn	$123.51	$250.00	$200.00	$6,625.50
100	Scheduled	$118.00	$250.00	$200.00	$12,250.00

40cm Flex PCB (MVTX): $123/pair

Specialities

Flex
Rigid-Flex
Roger's / FR4
All Roger's Metal Backed Boards
HDI - Blind Via Boards
Heavy Copper Boards
Copper Filled Vias
Stacked Vias

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AS9100
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Counter Sinks:
Counter Bores:
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Extra Laser Drill Steps:
Extra Lamination Steps:
Via fill Process Steps
ITAR: NO
Build to: IPC-6013 CLASS 2

* * *Comments:*

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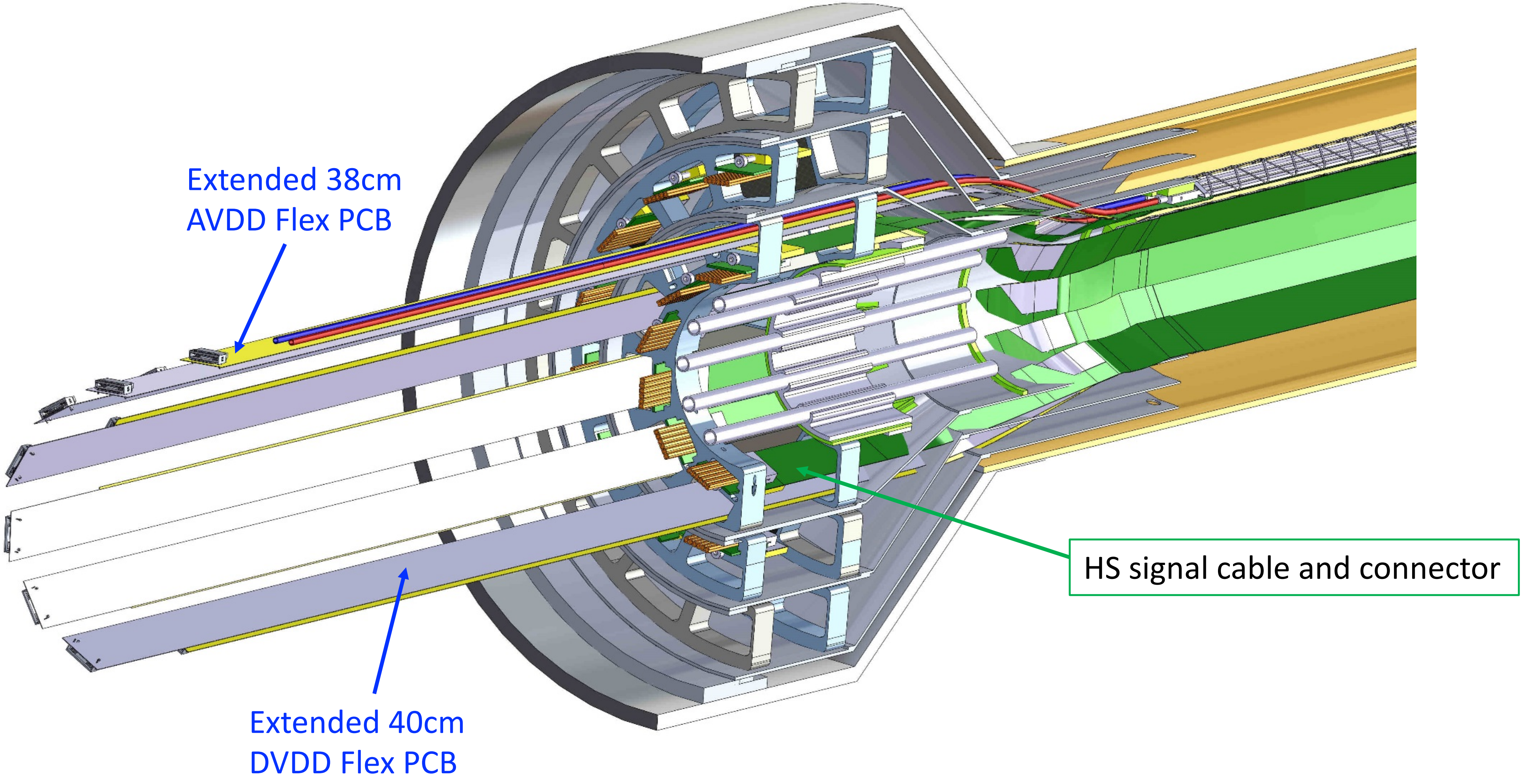
EP 4/12 ----COPIED FROM 157999 CHANGED BOARD LENGTH PER CUSTOMERS EMAIL

Latest CAD model patch panels;

From Walt Sondheim



Summary:
Modifications of the Power Extension PCB w.r.t. ALICE IB Design

- What to be modified:
  - Extend the Flex Power PCB length from 15cm(ALICE) to 40cm(sPHENIX)
  - Keep all noise filtering capacitors at current locations, just extend the passive copper traces.
- Risks and impacts
  - 40cm Power extension PCB production
    - OK, industry standard
    - Extra cost on materials ($61/pair vs $123/pair, 84+ pairs, total cost <$20K)
  - Stave assembly (need more inputs from ALICE)
    - Wire bonding machine operation clearance?
      - Solder power PCB after the wire bonding to make a HIC?
    - Jigs modified to hold the longer flex power PCB?
    - Extra cost?
  - Shipping and storage
    - Longer support Al-plate required for shipping and handling
    - Extra cost, on-going discussion between ALICE and LBNL on modification and fabrication

Technical risks: minimal

Recommendation BNL Director's Review: July 19-20, 2018

- Procure longer power cables, test and confirm any production issues with CERN team as soon as possible.

Sensor Irradiation Test

Findings

BNL Director's Review: July 19-20, 2018

- Irradiation of the ALPIDE sensors to the required 1 Mrad has not yet been done. Extrapolation of results of irradiations up to 500 krad imply it is likely the sensors will continue to operate satisfactorily at 1 Mrad.
- The mitigation strategy of replacing the inner two layers should the sensors only operate up to 500 krad was presented; it is to replace the inner two layers from the pool of 75% spare staves they intend to purchase.

Recently (in 9/2018) ALICE carried out irradiation test up to 2.7MRad:
Sensor can still function well with high efficiency and low noise

Sensor Radiation Hardness – OK at 2.7MRad

- Continuous effort by ALICE (@NPI, Czech)
- BNL review recommendation: test sensor up to 1MRad

https://indico.cern.ch/event/758048/

Conclusion

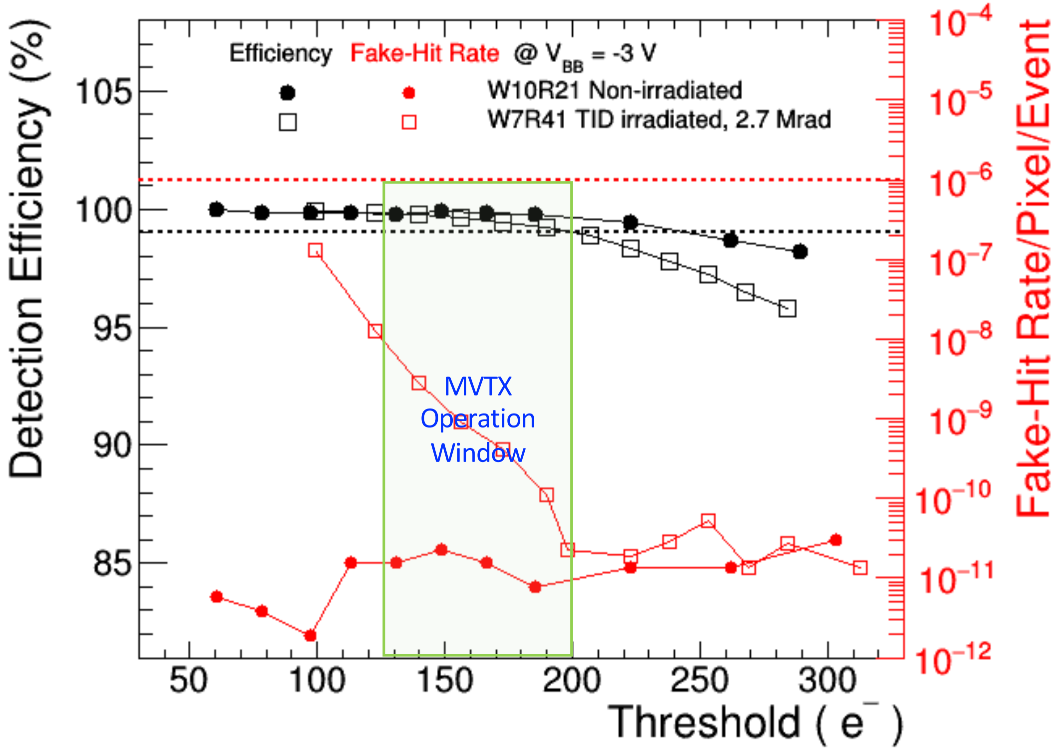
Irradiated ALPIDE sensor (2700 krad) over a large range of threshold settings

has :

1) good efficiency up to threshold ~190 e (Ithr = 100 DAC units) at Vbb = - 3 V, Vcasn = 90, Vcasn2 = 102

2) fake hit rate remains orders of magnitude smaller than the requirement (<< 10^{-6})

Irradiated chip#41 (2.7Mrad) : efficiency & fake hit rate



red line - fake hit rate- sensitivity limit of ALPIDE
black line - efficiency - the project goal (99%)

For non irradiated 2 noisy pixels were masked out.
No pixel was masked out for the 2.7Mrad chip.

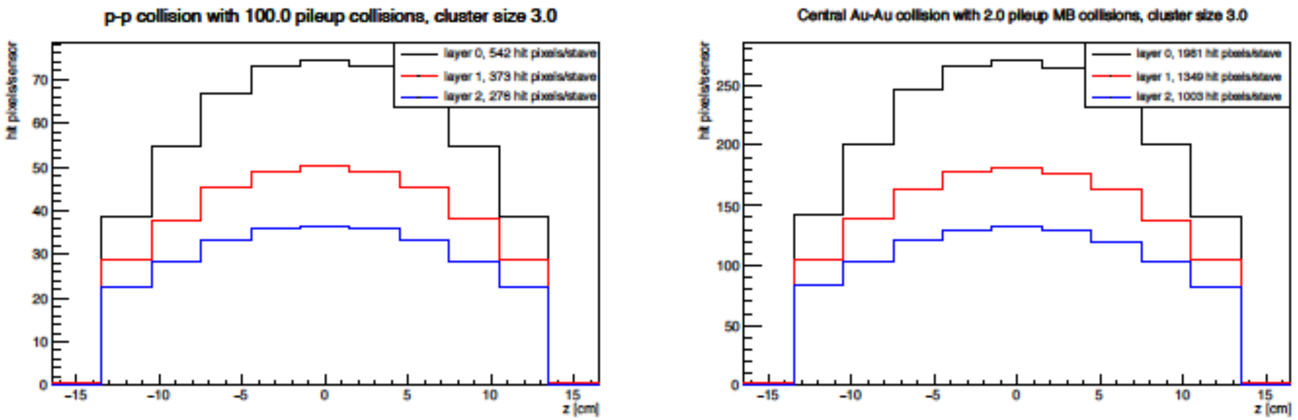
sPHENIX MVTX Max. Hit and Noise Rates

From MVTX proposal

	10^{-4} noise occupancy	Hit occupancy only		Hit + noise occupancy	
		$p+p$ [MB/s]	Au+Au [MB/s]	$p+p$ [MB/s]	Au+Au [MB/s]
L0 FEM	26	29	107	55	133
DAM	219	173	630	392	848
MVTX	1305	1041	3781	2346	5089

Table 2: Raw (uncompressed) data rates based on a worst-case noise occupancy of 10^{-4}, the hit occupancies of Fig. 9 at 15 kHz trigger rates, and the sum of the hit and noise.

sPHENIX MVTX targeted noise level: $<10^{-5}$

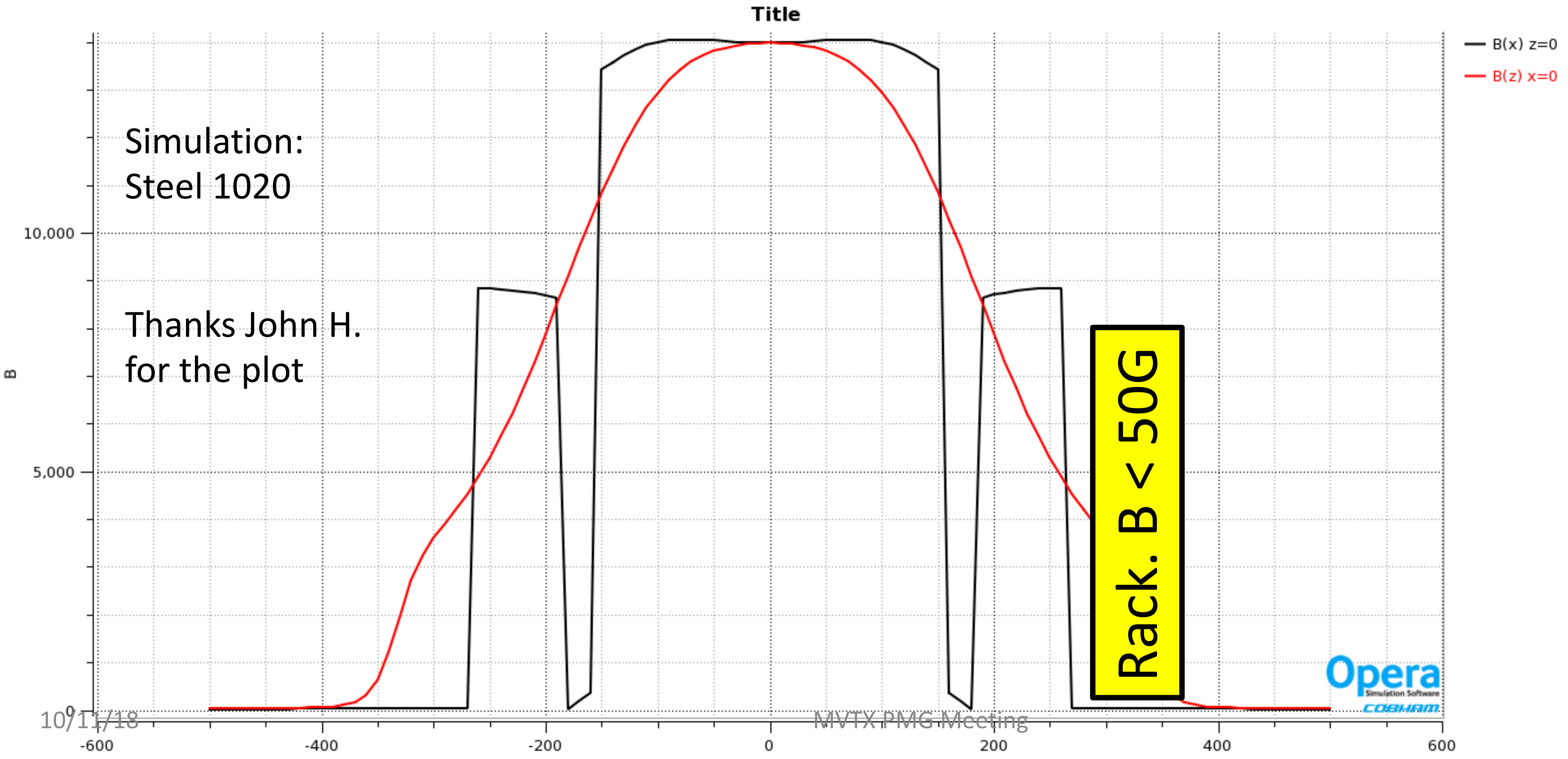


Very conservative estimate

Figure 9: Average hit occupancy per event. Conservative assumptions are made regarding integration time (10 μs) and cluster size (3 pixels/cluster). In addition, the pileup collisions are assumed to occur inside the MVTX acceptance ($|Z_{Vertex}| < 10$ cm) when in fact they will be widely distributed along the beam axis.

Expected B-field in the Rack Area (RU, PU Electronics)

- Low fringe field, < 50Gauss outside of HCal
- ALICE RU and PU designed to operate in 0.5T field



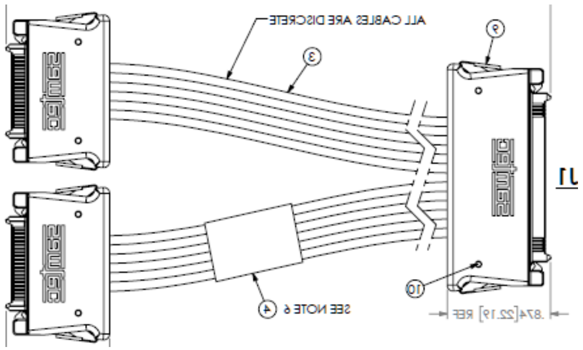
SamTec Cables Tested and Finalized for ITS: ~8m!

- Two cables per IB stave: 2.65m + 5.30m

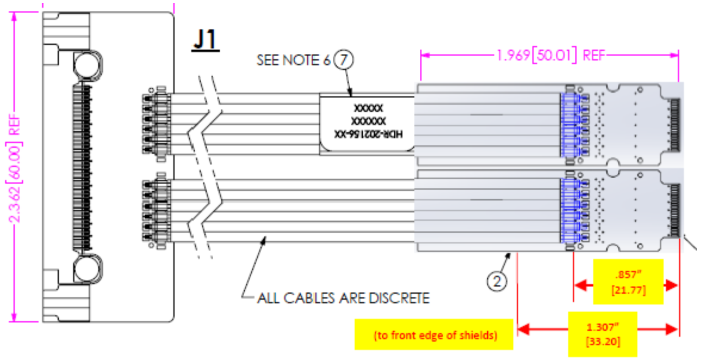
HDR-203194 (Type B)

HDR-206142 (Type A)

RUs



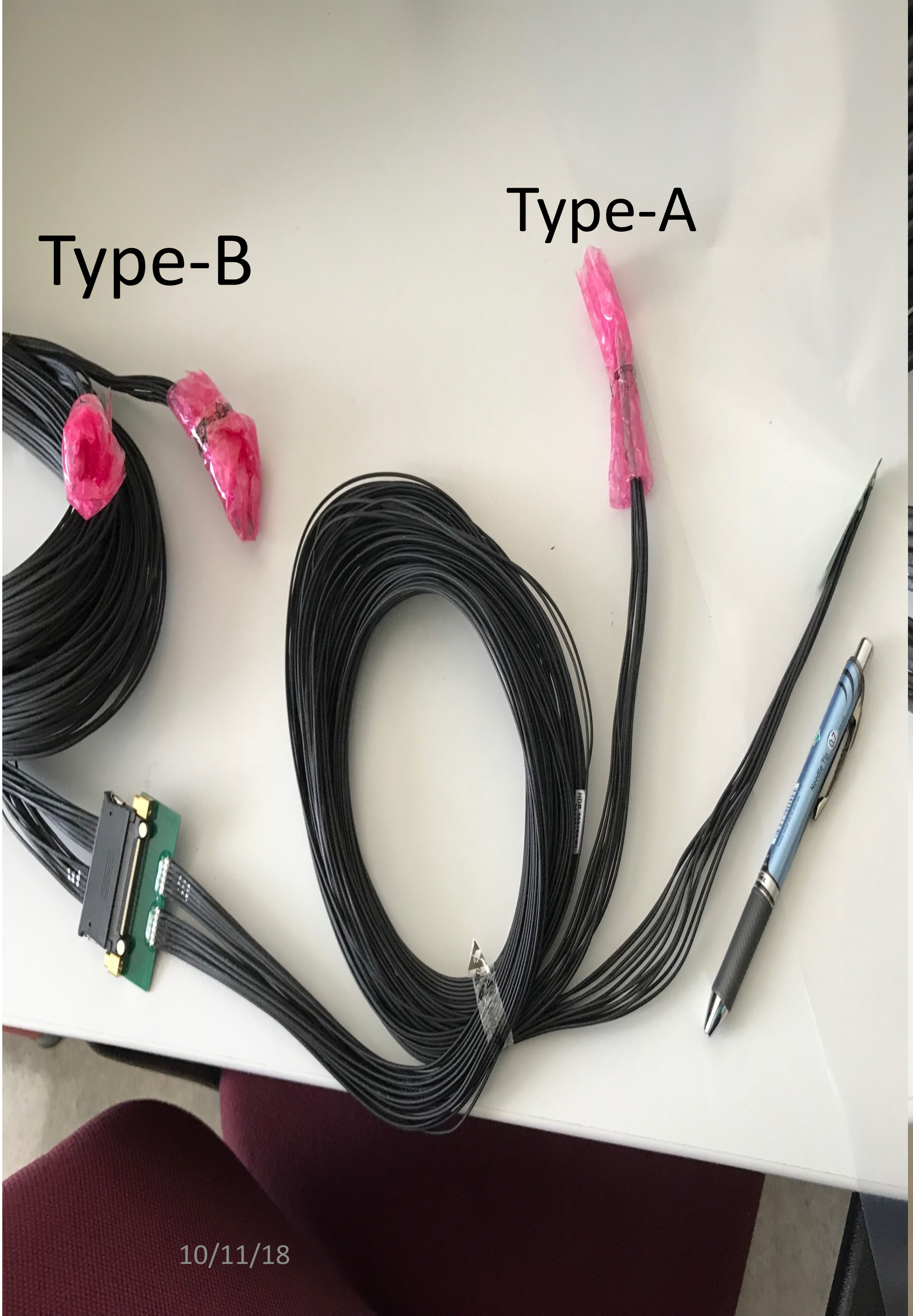
PP2

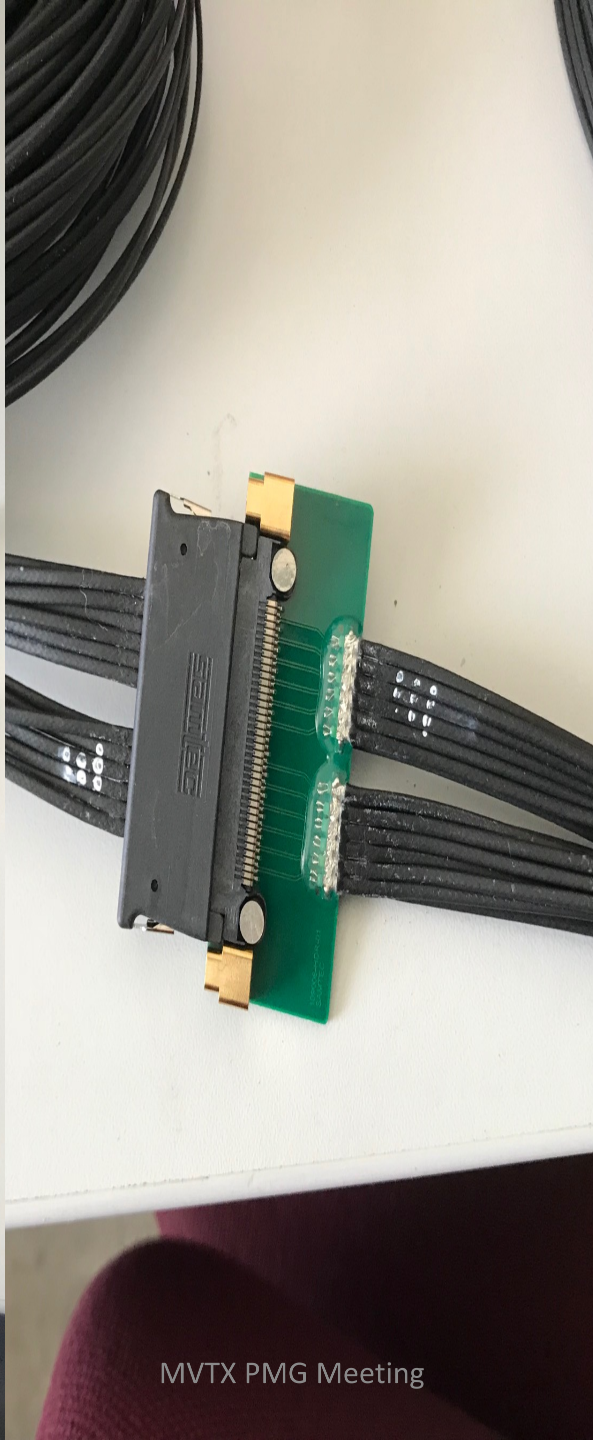


Staves

L: 5300 mm

L: 2650 mm


Type-B
Type-A




Type-A

Summary:

- Technically sPHENIX/MVTX staves are ready for production
- Cost being updated

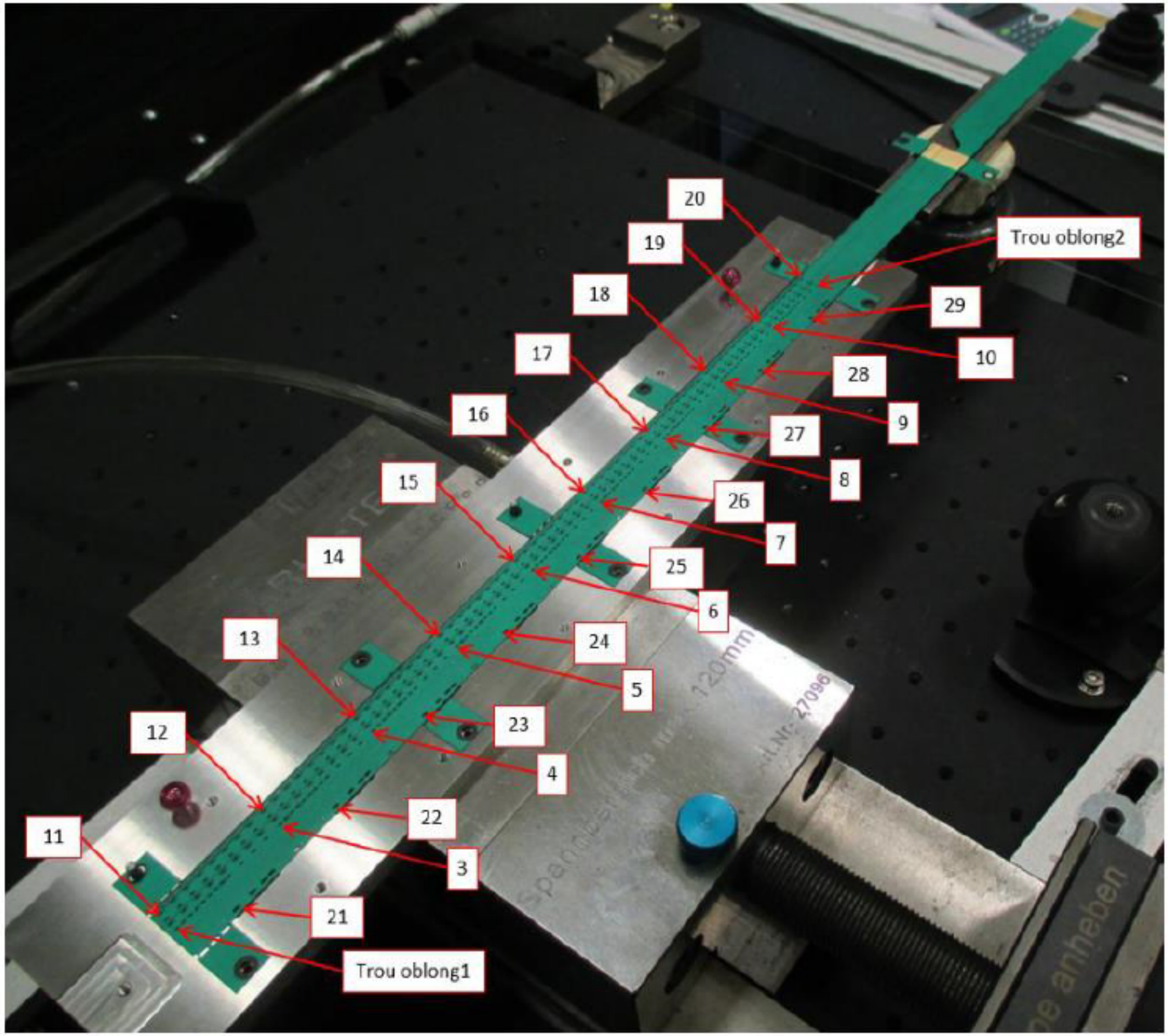
Backup slides

sPHENIX/MVTX IB Stave Assembly Procedure (to be confirmed/optimized by ALICE)

1. Prepare sensors and FPC
2. Glue 9 sensors to FPC
3. Wire bonding 9 sensors to FPC
4. Solder power flex PCB to FPC
    - (or do #3 wire bonding after soldering power flex PCB?)
5. Glue HIC to coldplate/carbon space frame
6. A stave is ready for QA

New FPC metrology procedure

- Alignment issues were pointed out during HIC assembly, related to a deviation from straight line shape → more detailed metrology, mapping every 30 mm lengthwise



IB STAVE Assembly Procedure

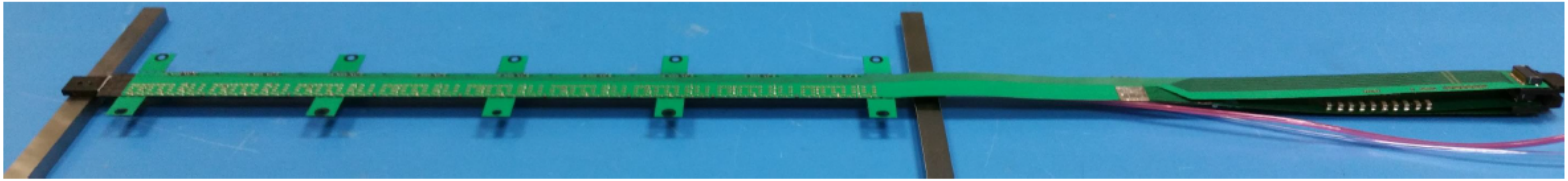
From Antonello Di Mauro

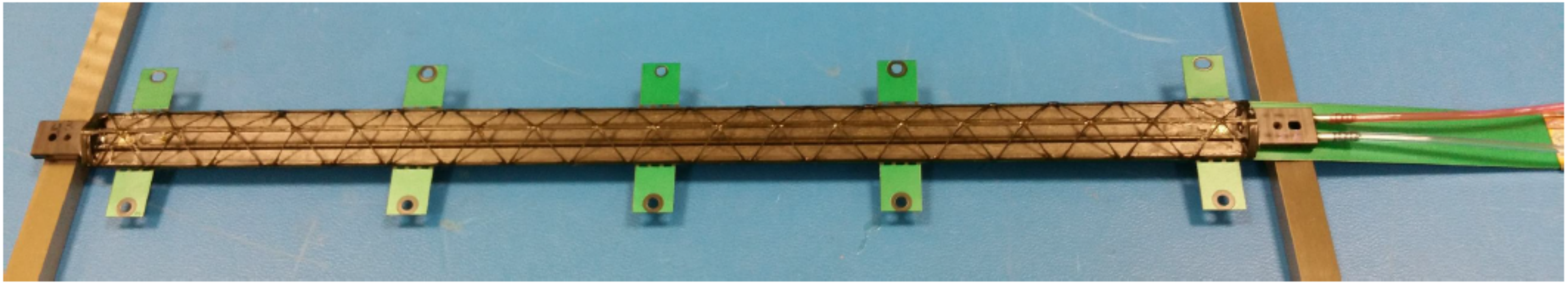
ALICE

Objective

glue the HIC to the IB spaceframe & coldplate, such to provide HIC support, alignment, and thermal contact to the coldplate

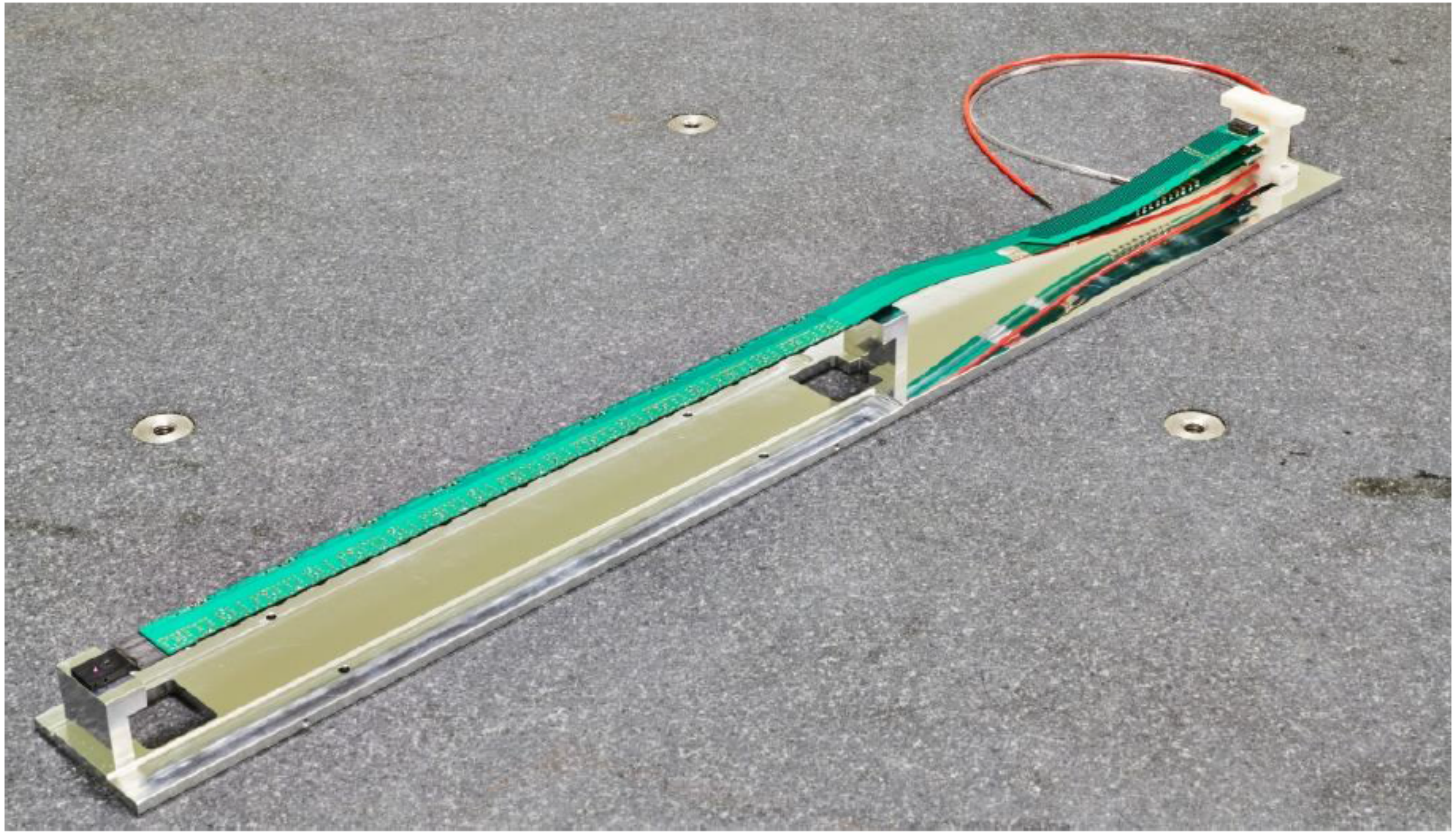
Only minor changes wrt to EDR





HIC / STAVE assembly

- HIC and STAVE supports for storage (final version) available
- Assembly resumed this week
- Plan to reach a production rate up to 4 HICs/ STAVES / week in the coming weeks



Actions @CERN

Many thanks to CERN colleagues!

Many are not shown here!