# ALICE

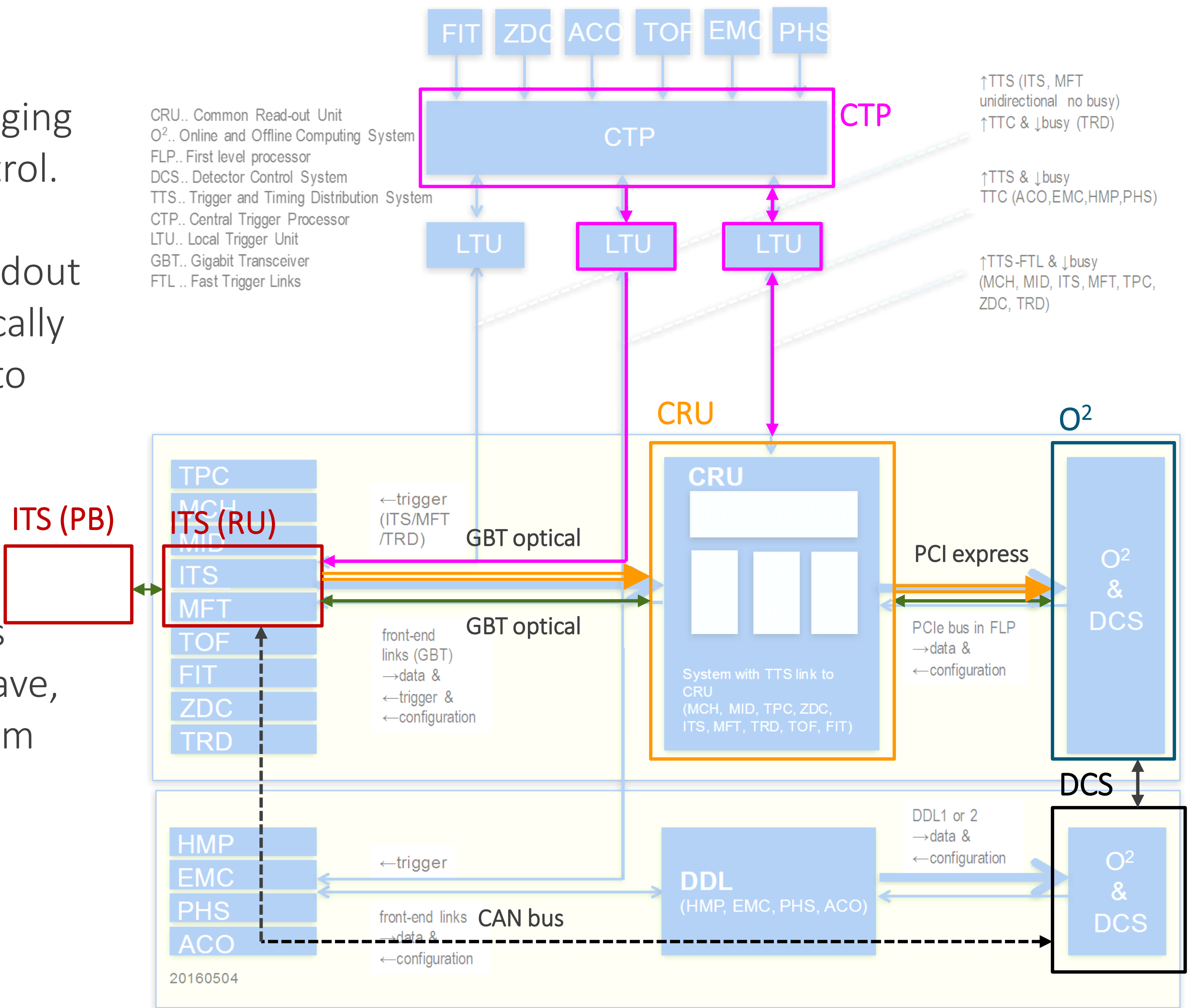
# Readout Electronics Overview

ITS Readout Electronic – **Production Readiness Review** – 13 Apr 2018 – CERN

# System Layout

# Layout – ITS interfaces overview in the ALICE upgrade framework

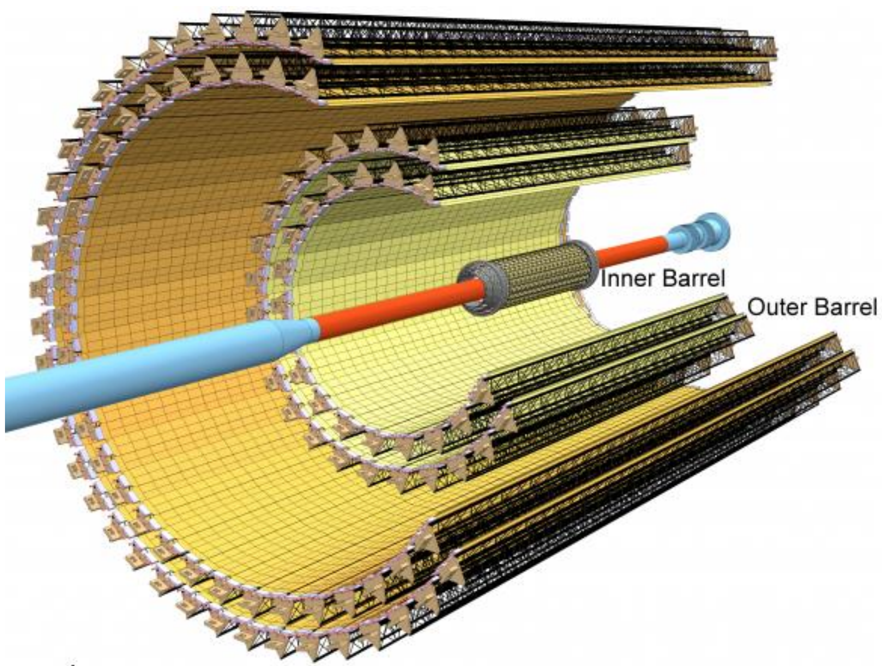
- The $O^2$ system performs data acquisition, packaging and detector control.
- The Common Readout Unit (CRU) is optically (GBT) connected to the ITS front-end electronics.
- Each CRU controls more than one stave, reads the data from the detector and broadcast control commands to the connected staves.

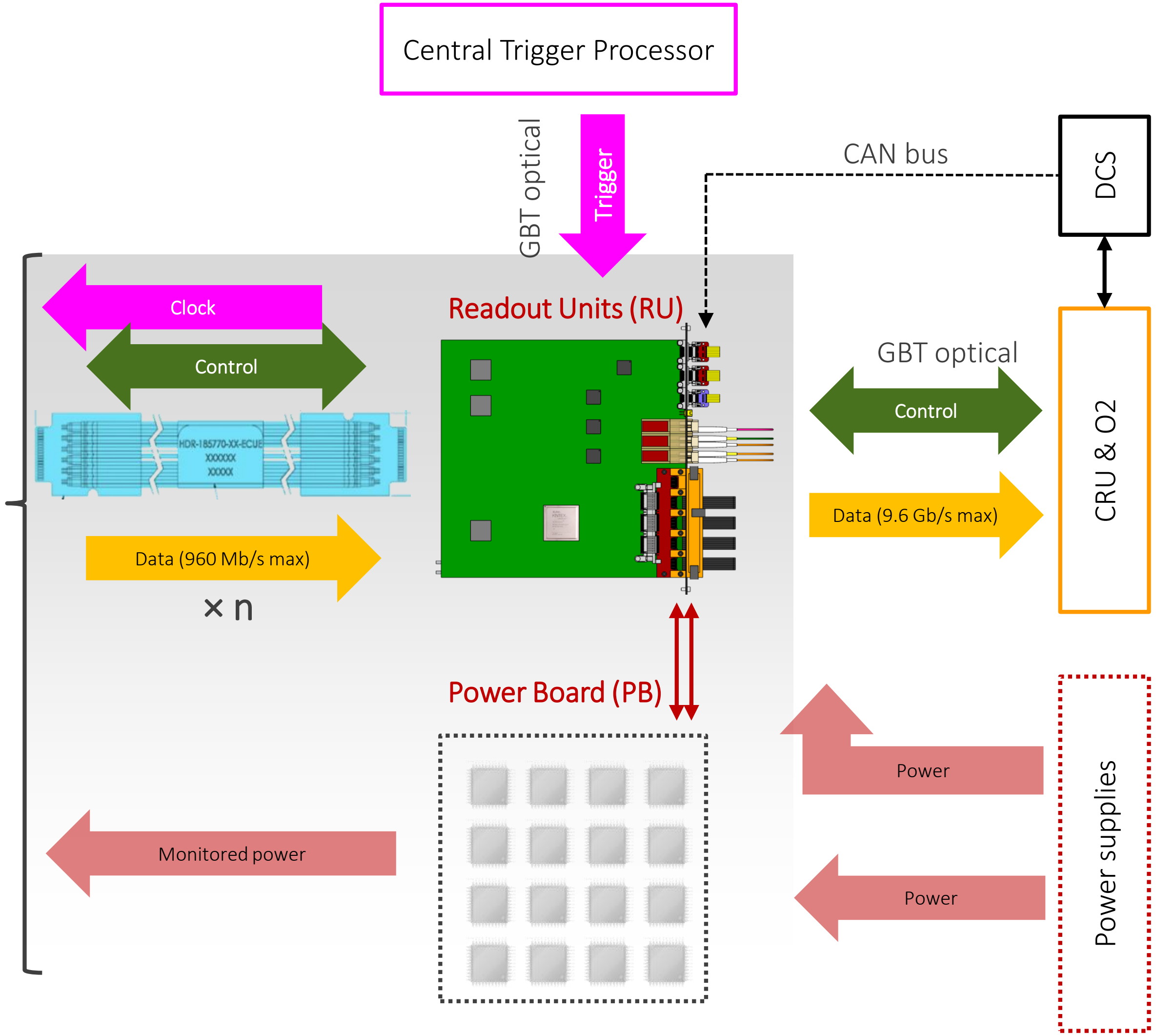



- The Central Trigger Processor (CTP) sends the trigger optically to the ITS, and also checks the status of each CRU in the experiment.
- The DCS has two paths toward/from the ITS: the main one through the $O^2$/CRU via the optical connections used also for data shipping, the other backup through the CAN bus used to monitor/control the power supplies.

# Layout – ITS Readout Electronics Layout (from later “Overview” talk)

The ITS front-end electronics are divided into **192** modular **Readout Units**, each connected to one ITS stave, and optically interfaced with both the Common Readout Unit (CRU) and the Central Trigger Processor (CTP).



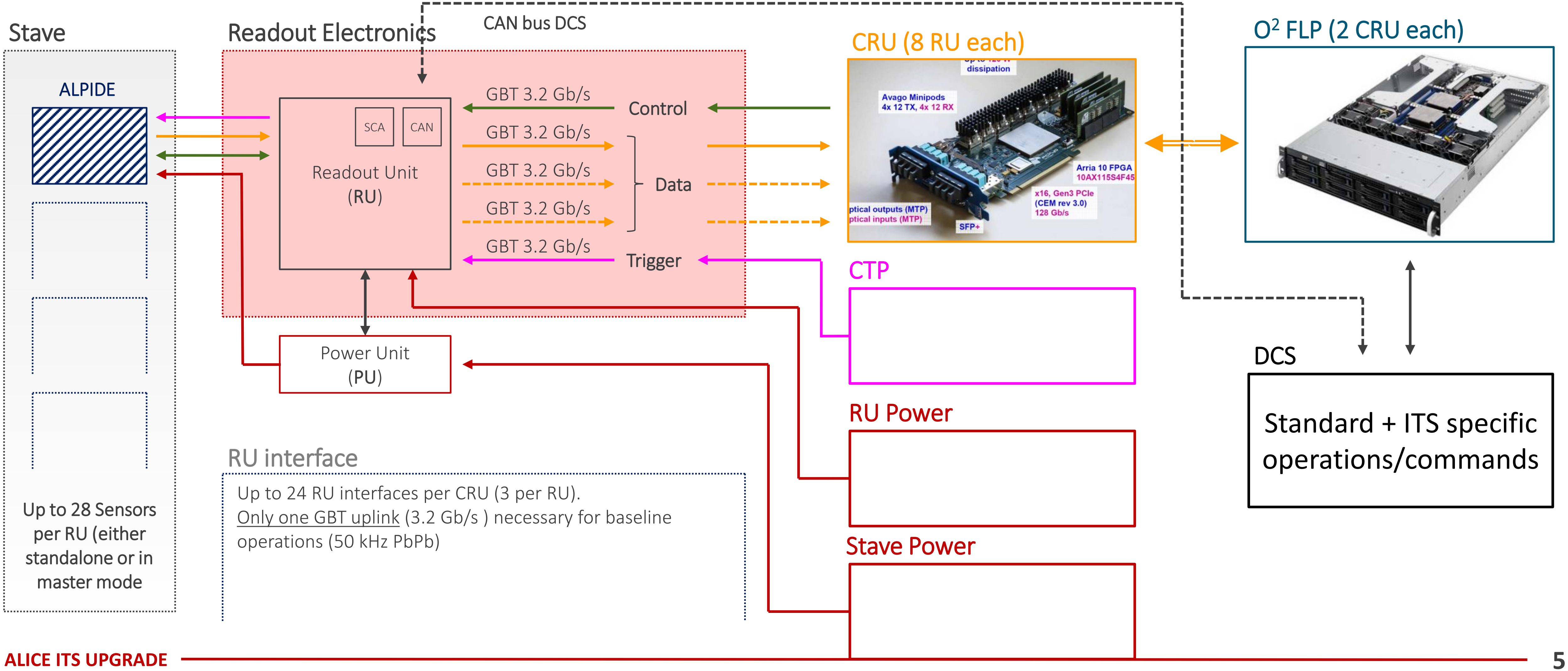




Each Readout Unit is connected to one stave, both for Inner and Outer Barrels

× 192 staves

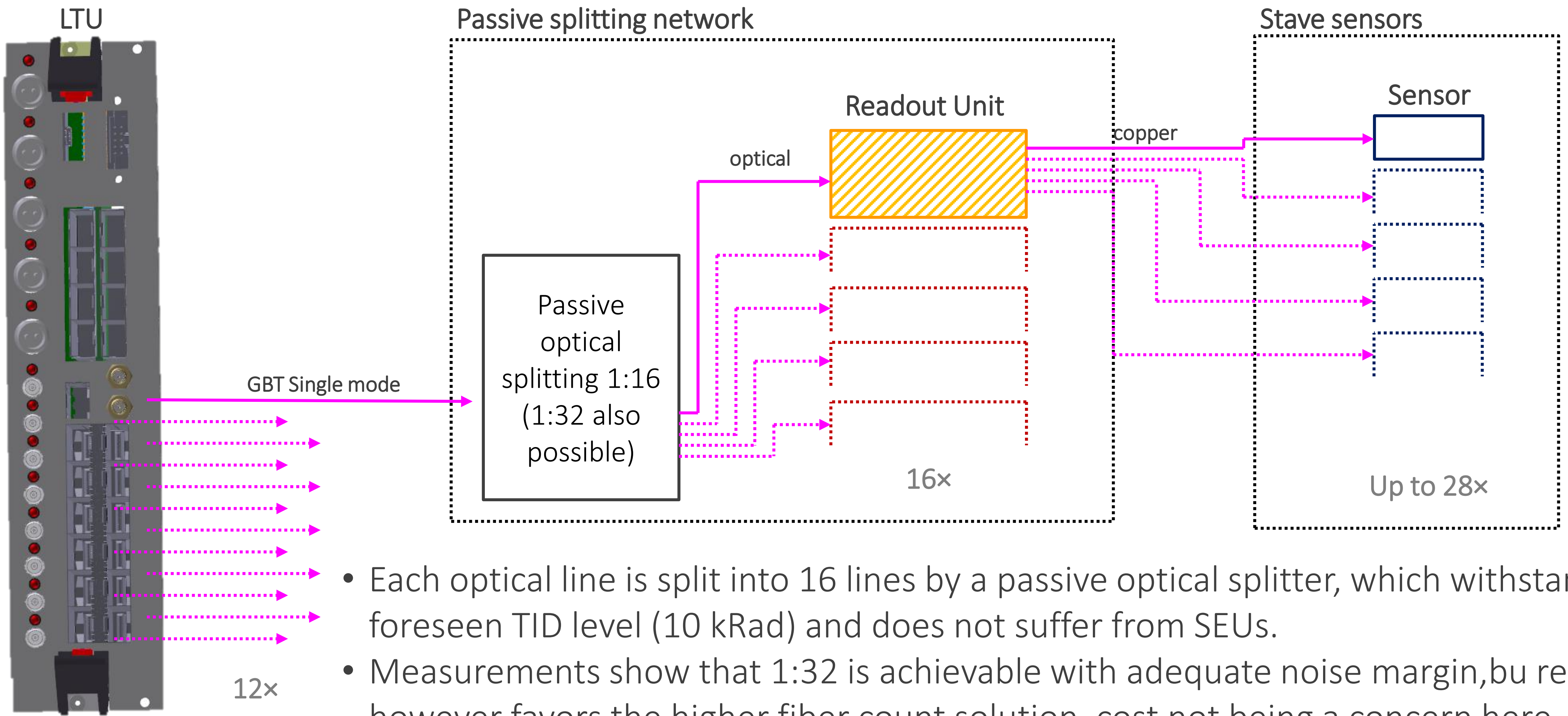
# Layout – Components and connections overview

- The ITS front-end electronic is divided into modular **Readout Units** (RU), identical for each layer.
- Each readout unit controls an entire stave, including power to the sensors (through custom-made **Power Units**).
- The CRU interfaces with the Readout Unit only, which in turn manages the trigger and the power for the stave.



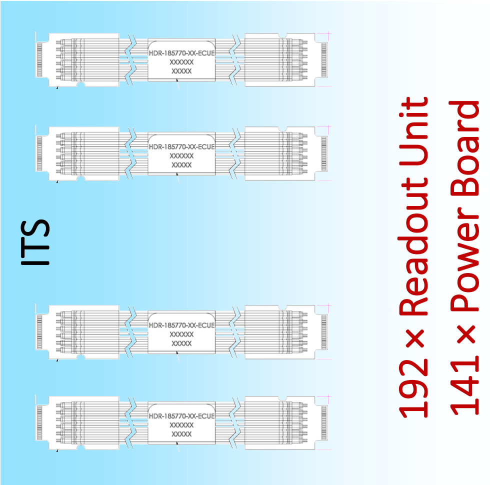
# Layout – Trigger distribution to the Readout Units and the sensors

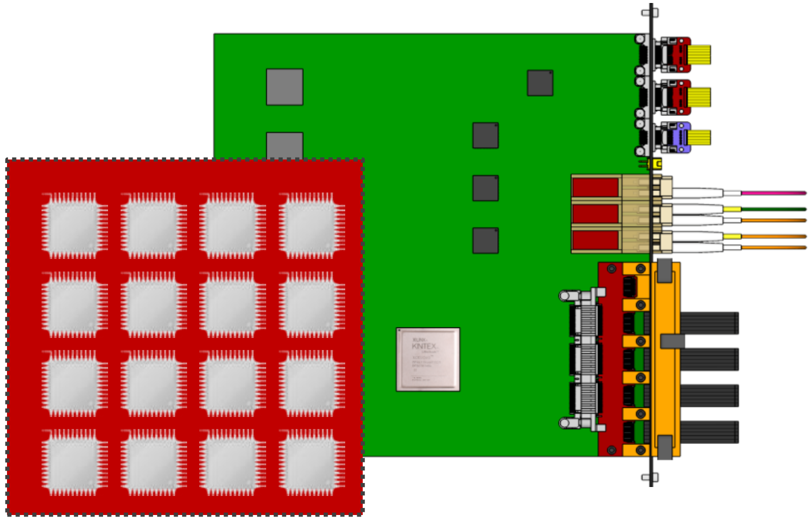
The CTP drives a set of Local Trigger Units (LTUs), each responsible for delivering the trigger to a specific detector. **To meet ITS timing requirements, trigger will not pass through the CRU**. Instead, ITS will have its own LTU directly driving 12 (or 6) Single Mode, 1030nm SFP+ Modules, using passive splitter to feed each RU with a trigger fiber.

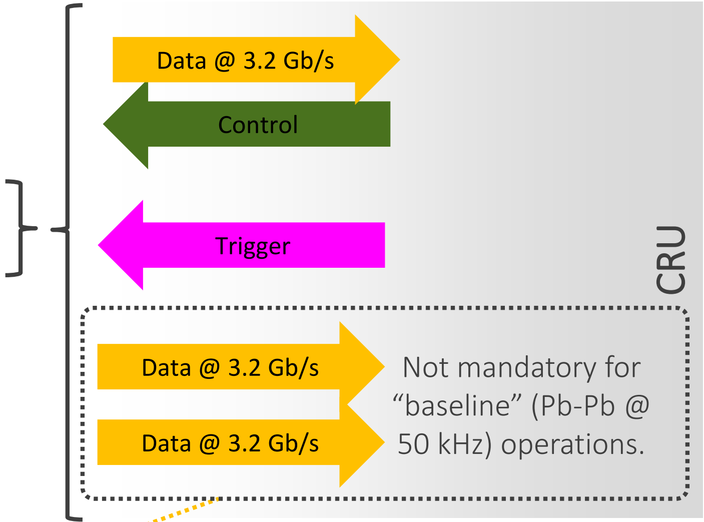



- Each optical line is split into 16 lines by a passive optical splitter, which withstands the foreseen TID level (10 kRad) and does not suffer from SEUs.
- Measurements show that 1:32 is achievable with adequate noise margin,bu redundancy however favors the higher fiber count solution, cost not being a concern here.

# Layout – Readout Unit and Power Boards count



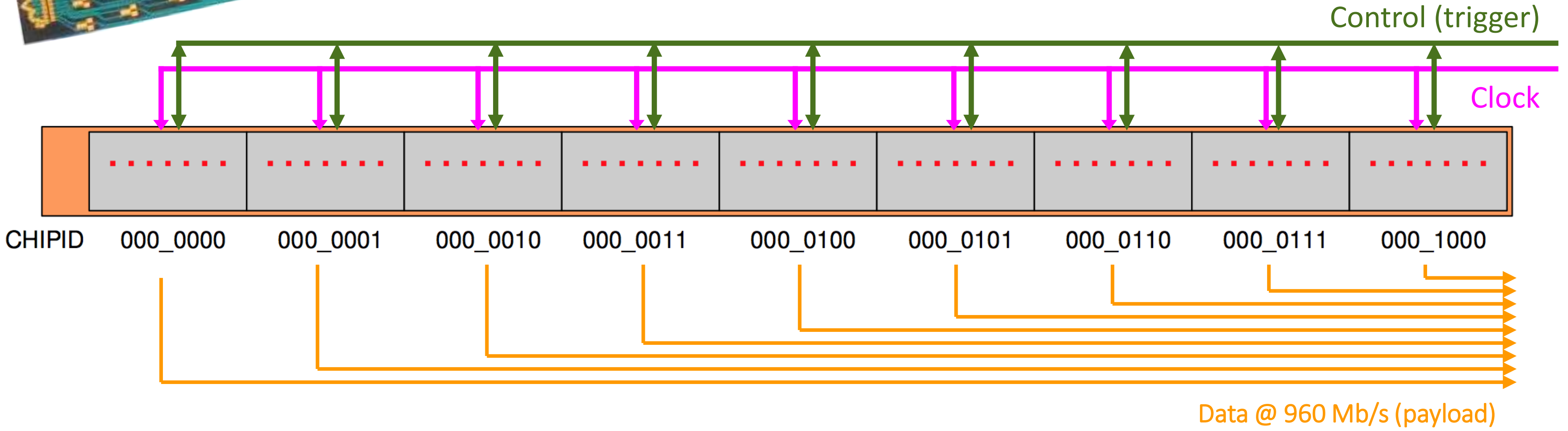



| Layout | | | Readout Units | | GBT Versatile link | | | | Fibers | | | Power | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Layer | Staves | Copper assembly | RUs × stave | RUs × layer | GBTx × layer | SCA × layer | VTRx × layer | VTTx × layer | TRG × layer | Data × layer | Ctrl × layer | Board | Unit |
| 0 | 12 | 12 | 1 | 12 | 36 | 12 | 24 | 12 | 12 | 36 | 12 | 6 | 12 |
| 1 | 16 | 16 | 1 | 16 | 48 | 16 | 32 | 16 | 16 | 48 | 16 | 8 | 16 |
| 2 | 20 | 20 | 1 | 20 | 60 | 20 | 40 | 20 | 20 | 60 | 20 | 10 | 20 |
| 3 | 24 | 96 | 1 | 24 | 72 | 24 | 48 | 24 | 24 | 72 | 24 | 12 | 24 |
| 4 | 30 | 120 | 1 | 30 | 90 | 30 | 60 | 30 | 30 | 90 | 30 | 15 | 30 |
| 5 | 42 | 168 | 1 | 42 | 126 | 42 | 84 | 42 | 42 | 126 | 42 | 42 | 84 |
| 6 | 48 | 192 | 1 | 48 | 144 | 48 | 96 | 48 | 48 | 144 | 48 | 48 | 96 |
| Total | | 624 | | 192 | 576 | 192 | 384 | 192 | 192 | 576 | 192 | 141 | |

# Sensors Connections

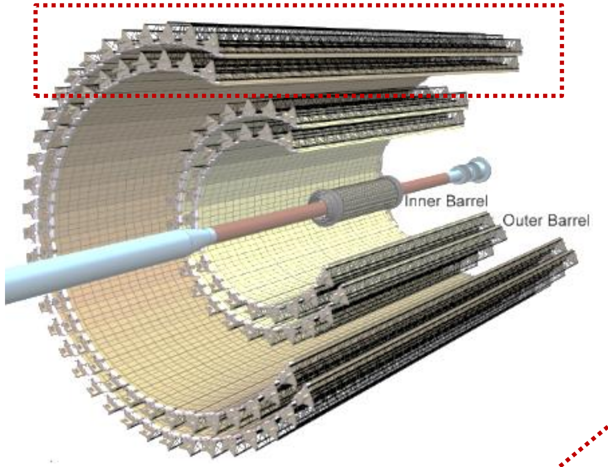
# Sensors – inner layers staves connections

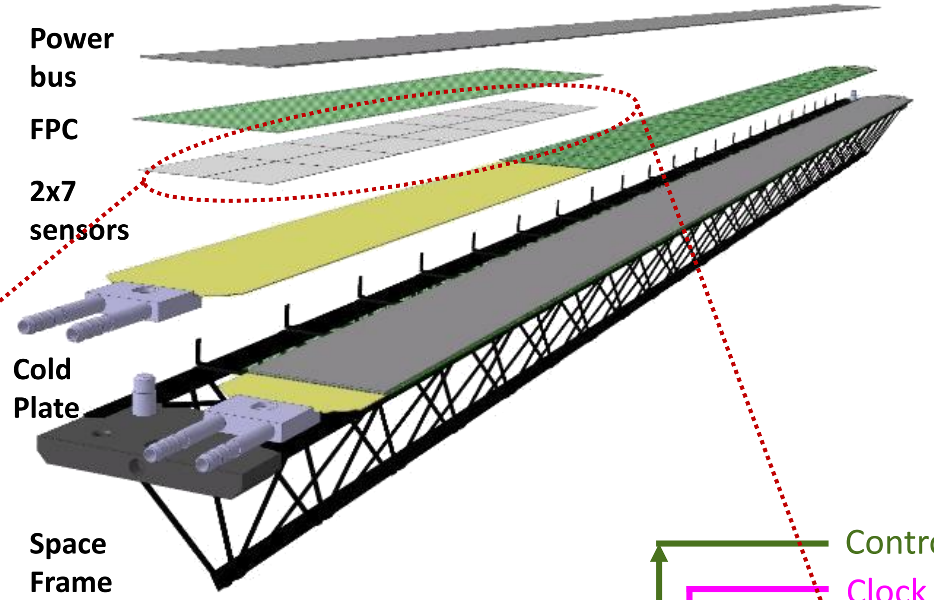
Inner layers stave, 9 master sensors (each read/drives its own control and data lines) to maximize.available bandwidth (960 Mb/s payload)’

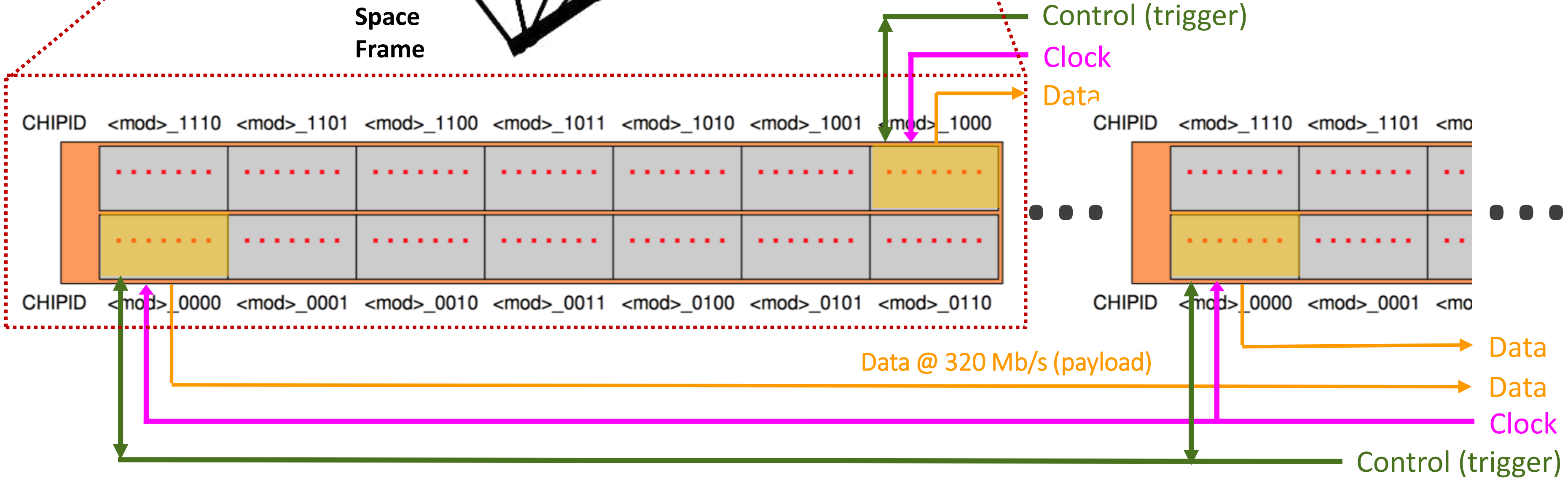



# Sensors – middle and outer layer staves and modules connections

**Mid/Outer layers module**: 2 symmetric group of <u>1 master</u> and <u>6 slave</u> chips. Only the master accesses the data/control lines toward/from the outer world. Bandwith (per master) is 320 Mb/s payload.

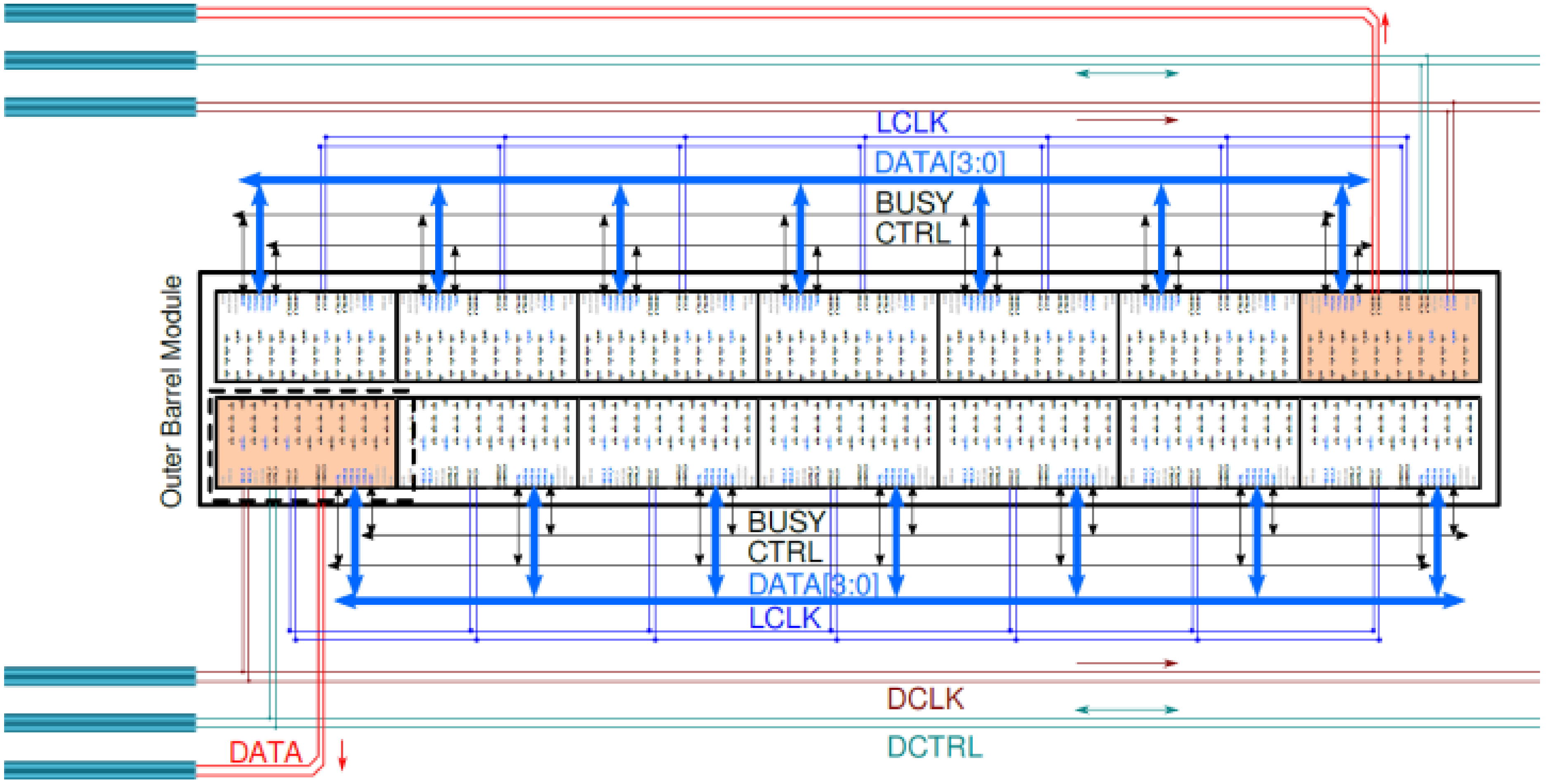


# Sensors – module sensor master/slave connections

**In the middle and outer layers modules,** the master sensor is connected with the 6 slaves through a local 4 bit bus (CMOS, single ended) which runs at 80 Mb/s. Special lines are provided to transmit the clock, the control and the busy status.

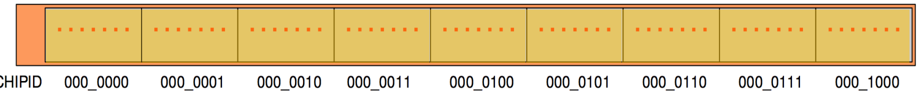


# Sensors – copper connections details

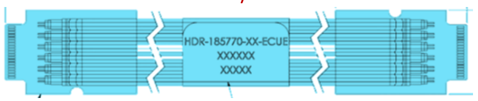
Each readout unit is connected to a stave through copper cables (5m long), which carry both bidirectional control lines and unidirectional clock and data lines.

## Inner Layers

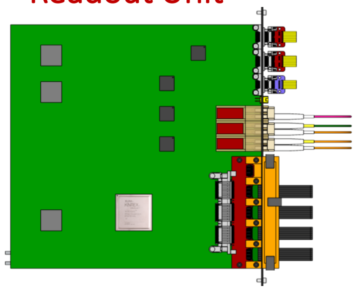
9 data lines, 1 clock, 1 control




9 data pairs,
1.2 Gb/s each

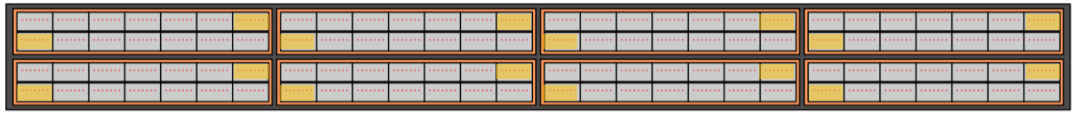



Readout Unit

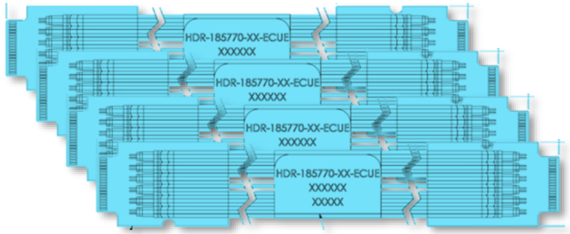


## Middle Layers

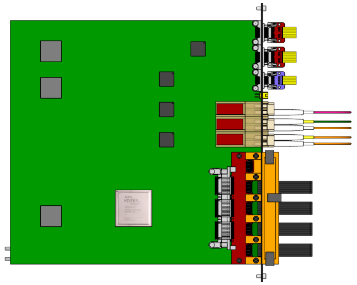
(4+4+4+4) data, (1+1+1+1) clock, (1+1+1+1) control




16 data pairs,
400 Mb/s each



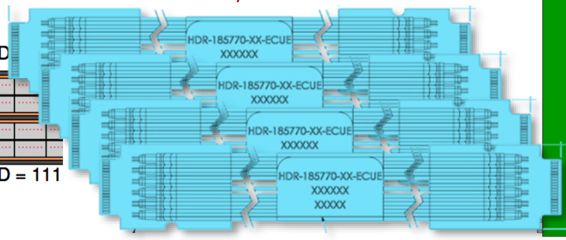

Readout Unit



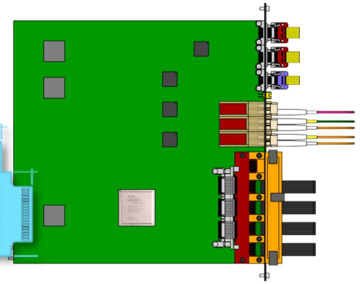
## Outer Layers

(7+7+7+7) data, (1+1+1+1) clock, (1+1+1+1) control


28 data pairs,
400 Mb/s each



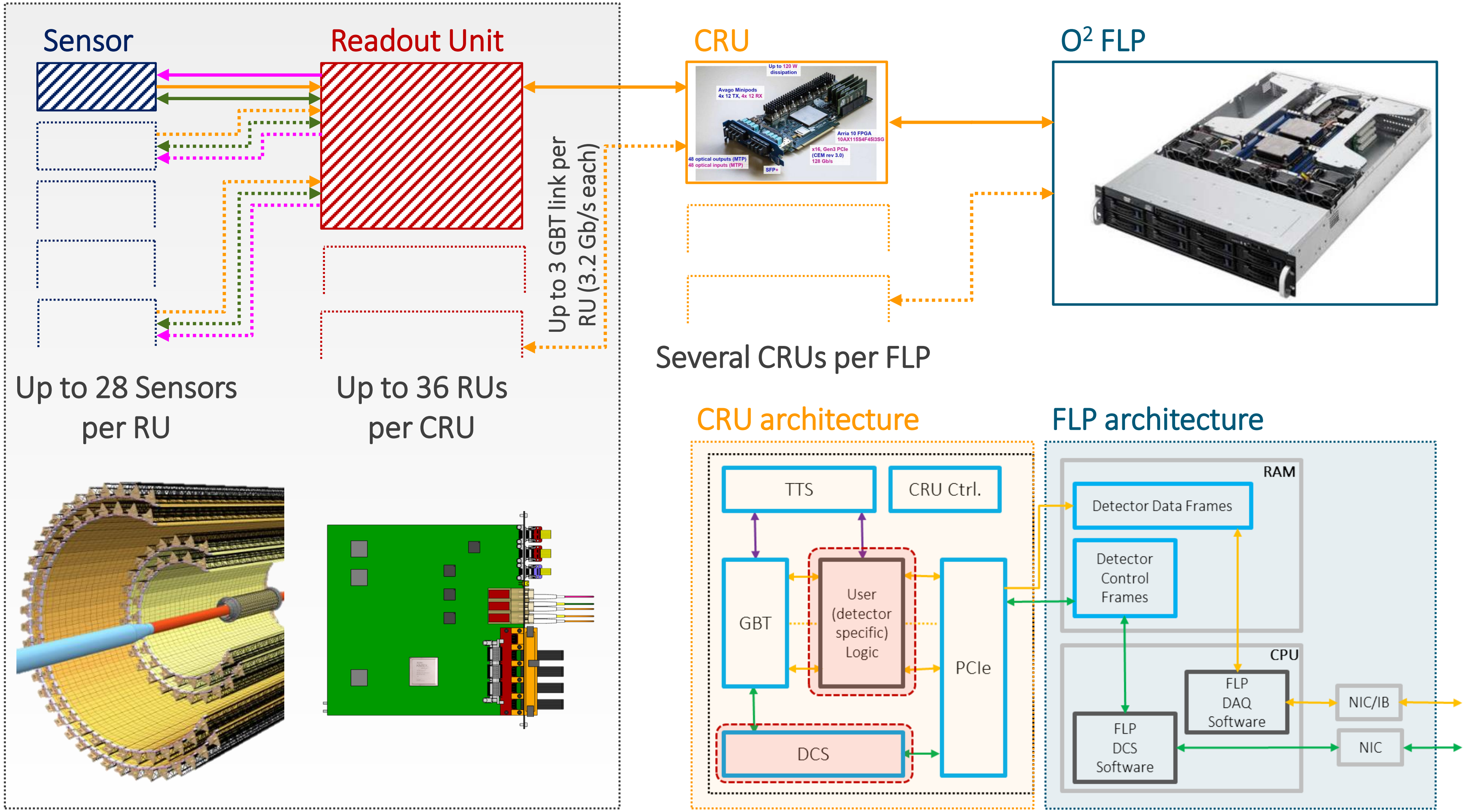

Readout Unit



# $O^2$ and Common Readout Unit

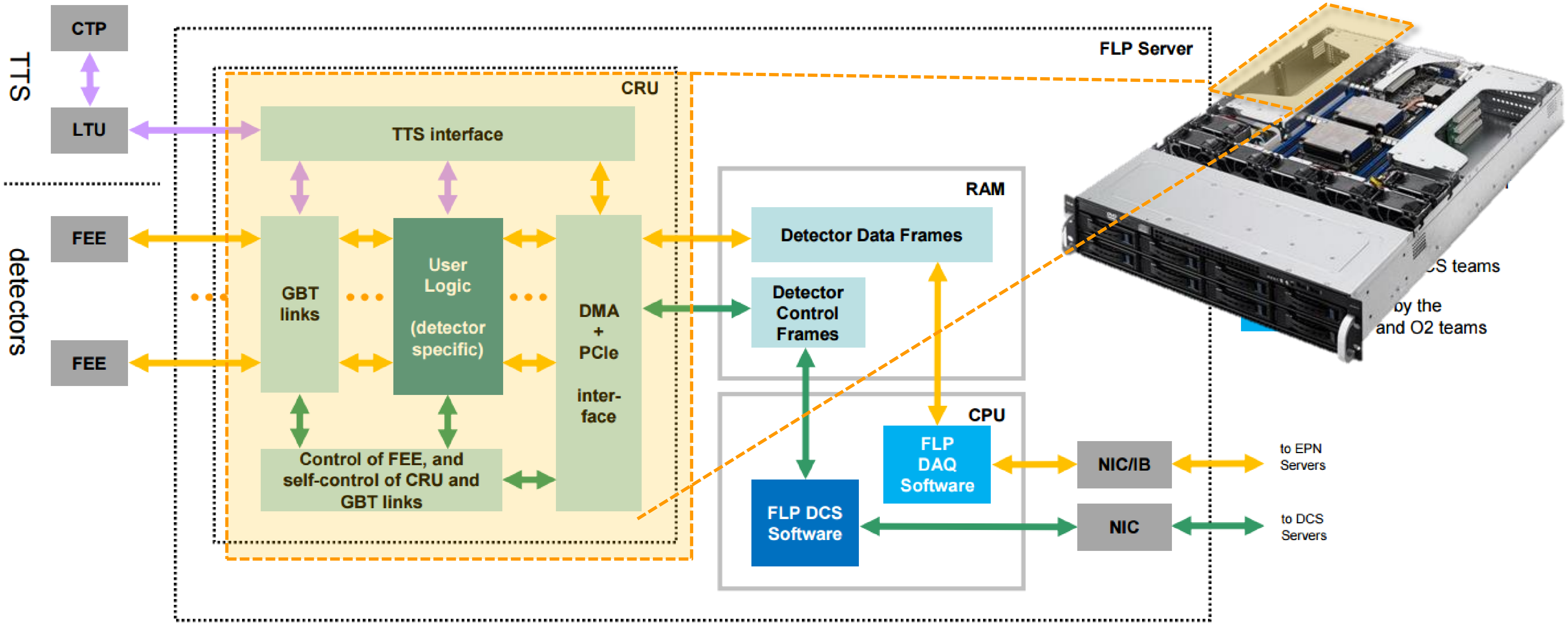
# $O^2$-CRU – Connections to/from the ITS

The O2 First Level Processors (**FLP**s) manage the detectors and collect/aggregate the data streams before storage. Each FLP hosts several Common Readout Units (**CRU**), which are optically interfaced with the ITS front-end electronics (Readout Units).



# O²-CRU – CRU within the FLP

Several CRU can be (logically and physically) hosted within a First Level Processor (FLP). Each CRU optically communicates with the detector front end electronics and with the Central Trigger processor.




- CTP sends the trigger info to the CRU, the CRU acknowledges success or failure to process, forward detector data.
- CTP sends a HB accept or HB reject to inform the CRU whether to process or flush the corresponding data frame.

# O²-CRU – data protocol from the detector

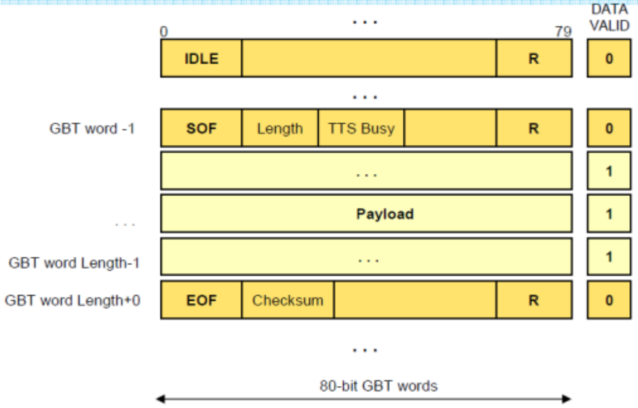
The CRU uses a specific protocol to exchange data with the detector Front End Electronics, which depends on the ALICE DAQ operating mode (continuous or triggered, see timing presentation).

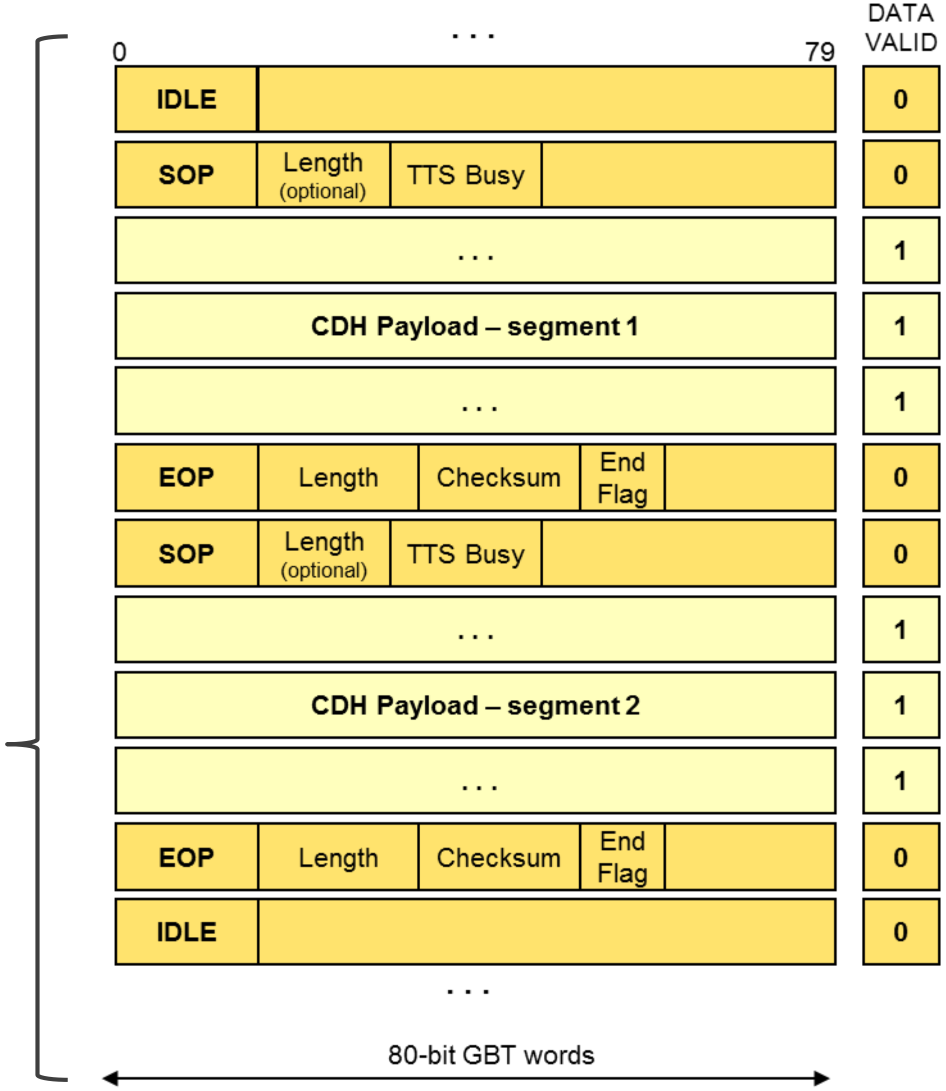
**With packets protocol**
(e.g. TOF, ITS, etc.):

• For every trigger (physics or heart beat) the detector generate a packet:

- ***SOP*** (Start of Packet)
- **PAYLOAD**
- ***EOP*** (End Of Packet)

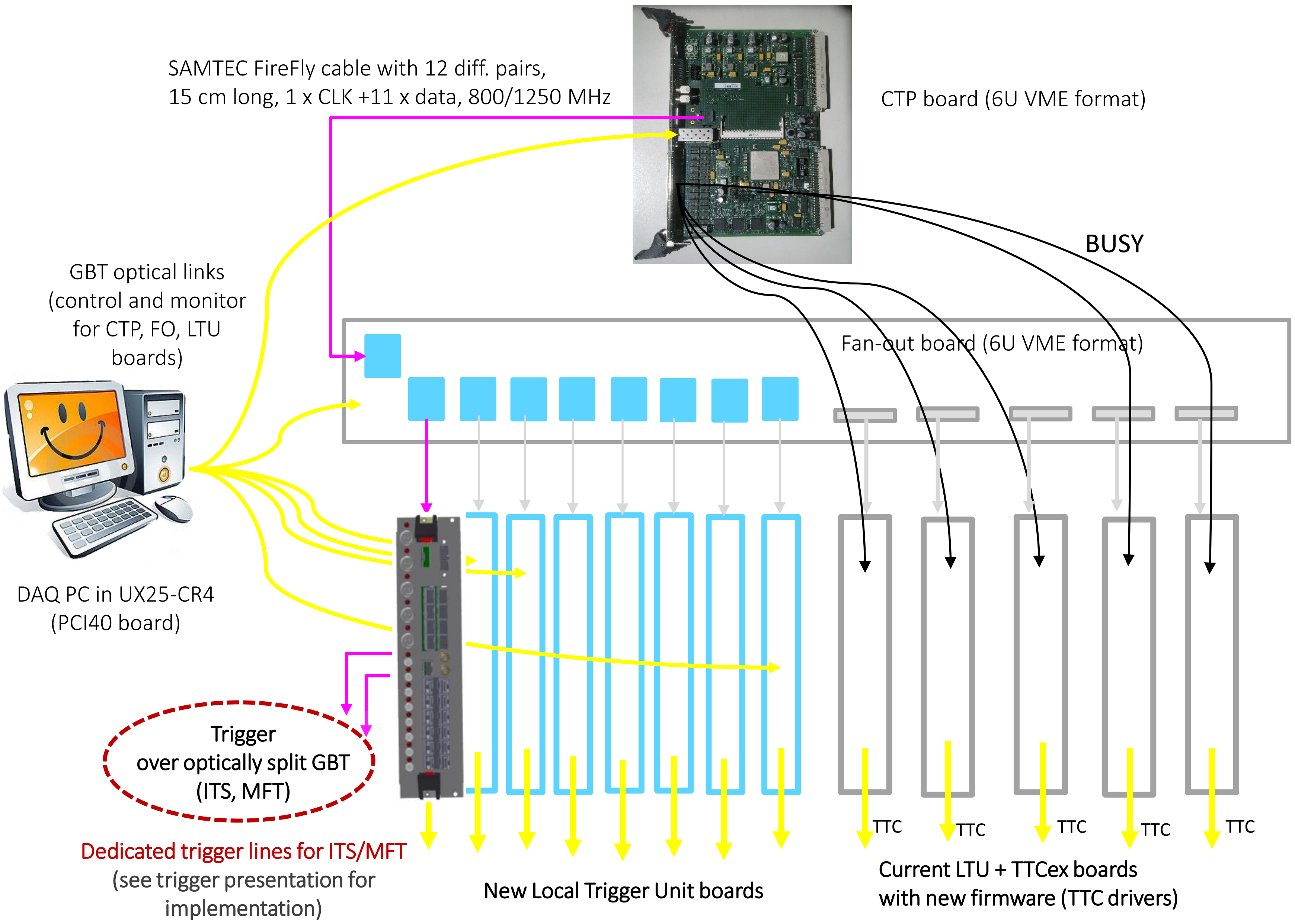
• Within the packet the data is tagged with event identification



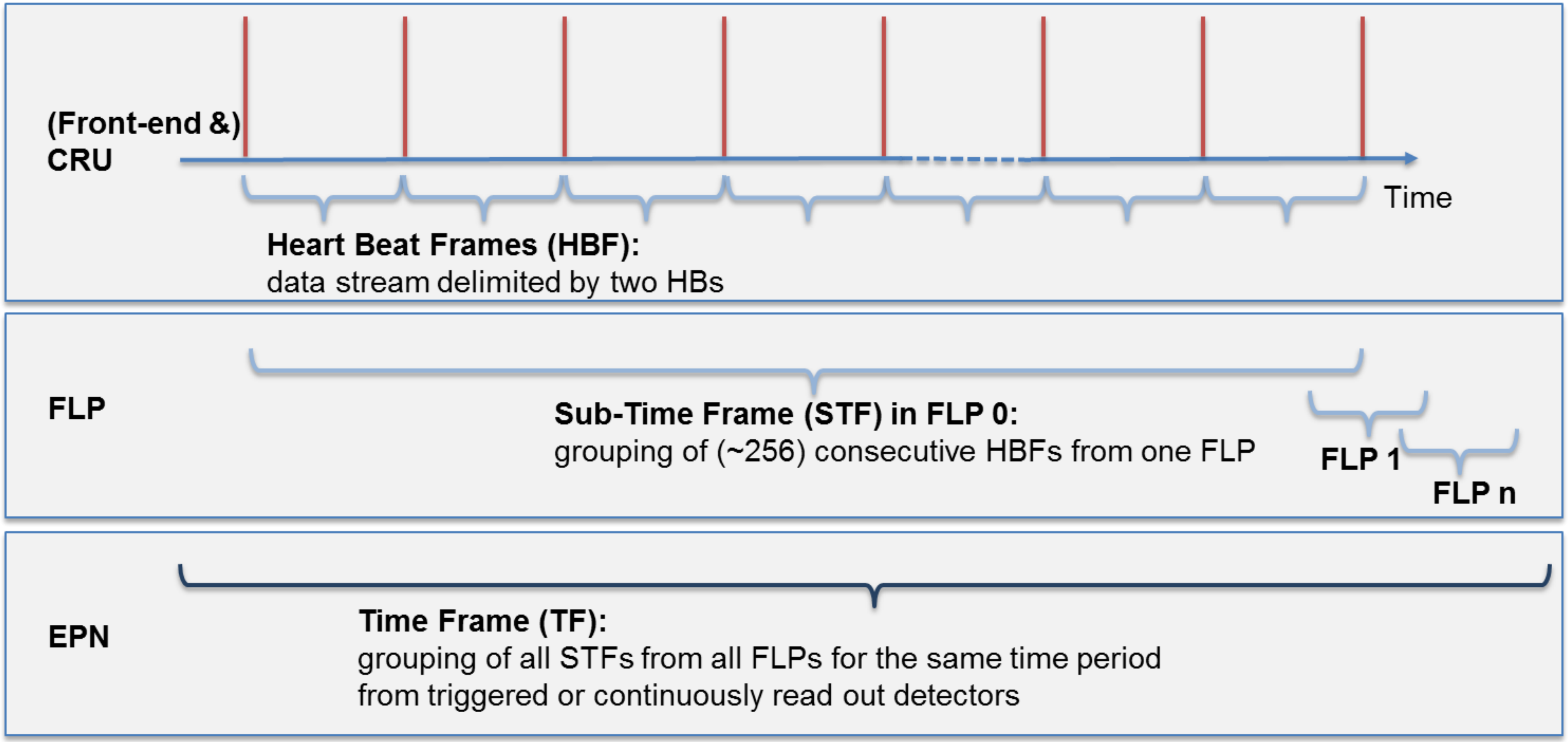
# Trigger and timing

# Trigger – Central Trigger Processor interface



# Trigger – Continuous mode

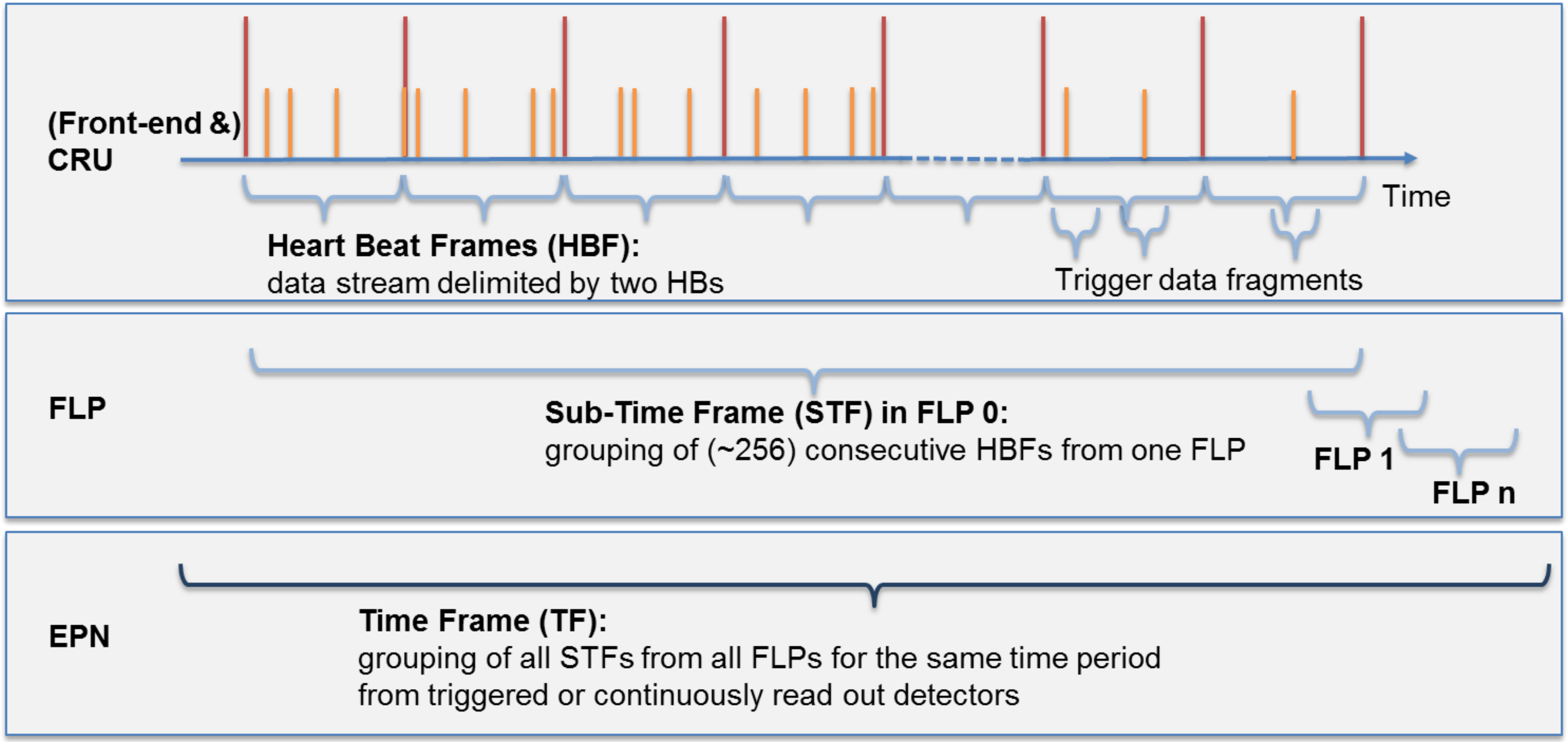
The Central Trigger Processor (**CTP**) issues a Heart Beat (HB) trigger every **89.4** μs. Data from the detector are packed into the Heart Beat Frame (**HBF**) they belong to. 256 HBFs form a Time Frame (**TF**).




- Sub-Time Frames (STF) are composed of 256 HBF aggregated within a single FLP.
- Aggregating all STFs from all FLPs form a **Time Frame**, which contains all events from all detectors for a given time interval. **Look at next section for FLP description.**

# **Trigger** – Triggered mode

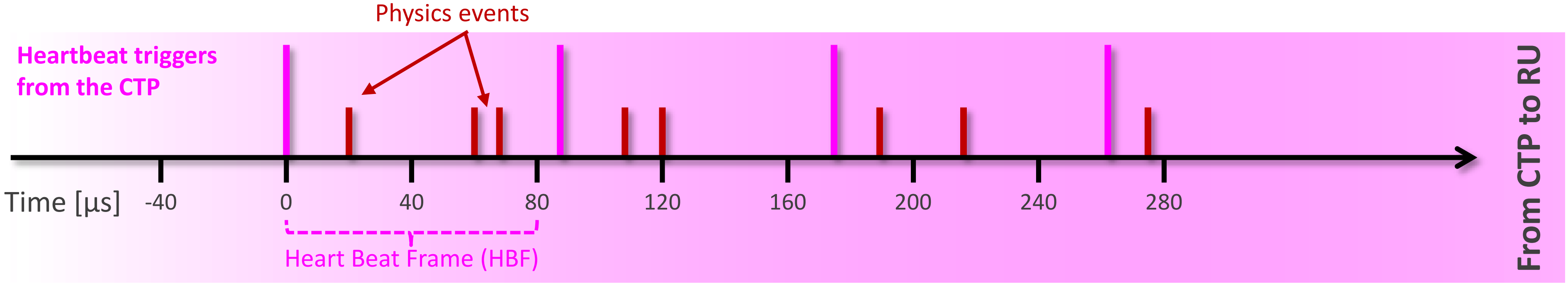
Almost identical to the continuous mode, but physical event triggers will be sent together with the Heart Beat Trigger to capable detectors (ITS is designed to accept triggers) and only data corresponding to the triggers are sent and collected in HBFs.



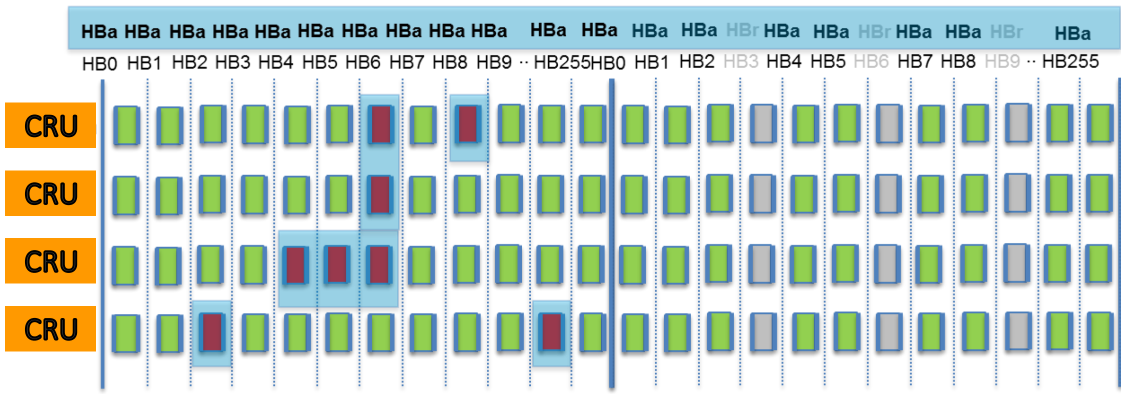

- Sub-Time Frames (STF) are composed of 256 HBFs aggregated within a <u>single FLP</u>.
- Aggregating all STFs from <u>all FLPs</u> forms a **Time Frame**, which therefore contains all events from all detectors for a given time interval.

# Trigger – Heart Beat and Throttling in continuous mode

In continuous mode the **CTP** will issue a Heart Beat trigger every **89.4** μs. Data are packed into the Heart Beat Frame (**HBF**) they belong to. 256 HBFs form a Time Frame (**TF**) across the detector.



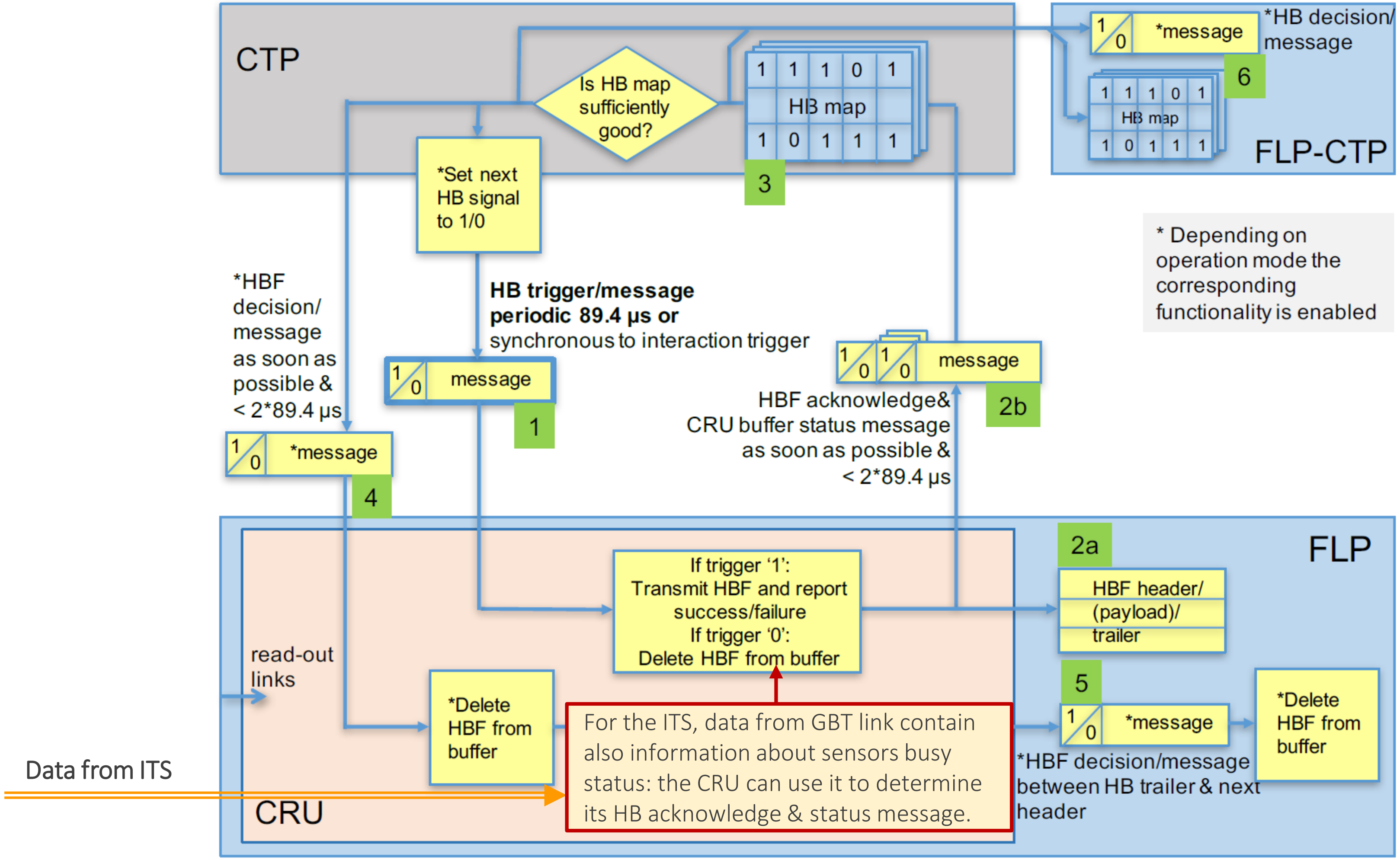

The CTP collects a HB acknowledge from each Common Readout Unit for each HBF, indicating success/failure of passing a complete HBF to its FLP. In case of excessive **negative** HB acknowledge in one or more detectors, the CTP is able to throttle down the overall acquisition speed by sending a special "Frame Suppression" trigger (HB reject, "HBr").




By sending some **HeartBeat reject** triggers (resulting in empty HBFs, grey rectangles) the CTP can effectively throttle down the acquisition bandwidth, improving the likeliness of having aligned data frames.

Each CRU decides on its own capability to pass a complete HBF to the FLP based on its internal resource status and (if provided) additional busy information from the detector front-end electronics, and indicates this to the CTP in its HB acknowledge.

# Trigger – ALICE readout detailed throttling scheme

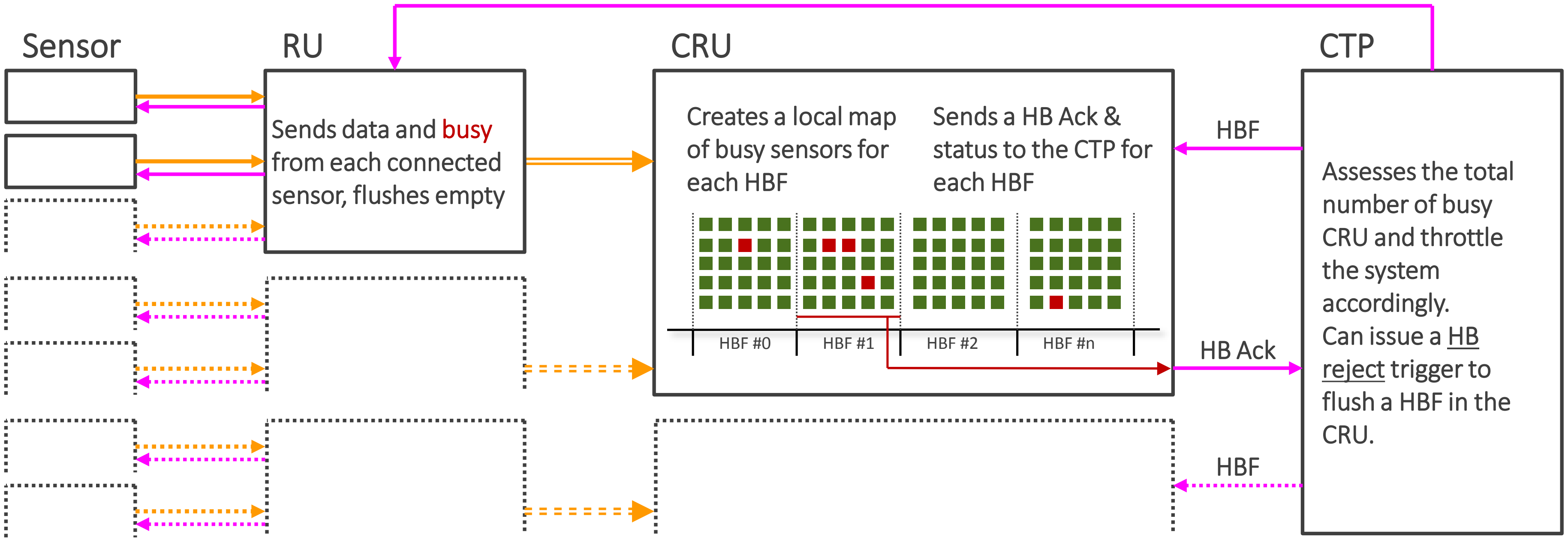



ITS will send additional busy information to the CRU, which could use it to determine its HB acknowledge & status message. Remember that each CRU collects data from as many as 36 Readout Units.

# Trigger – Busy reconstruction at CRU level

A sensor can answer to a trigger from the RU in three different ways:

- Good data packet(s)
- Empty sensor packet (no data at all in that sensor)
- Busy flag (by itself or within data packets, delivery prioritized over data): empty packets will be flushed, while data and busy info will be transmitted to the CRU

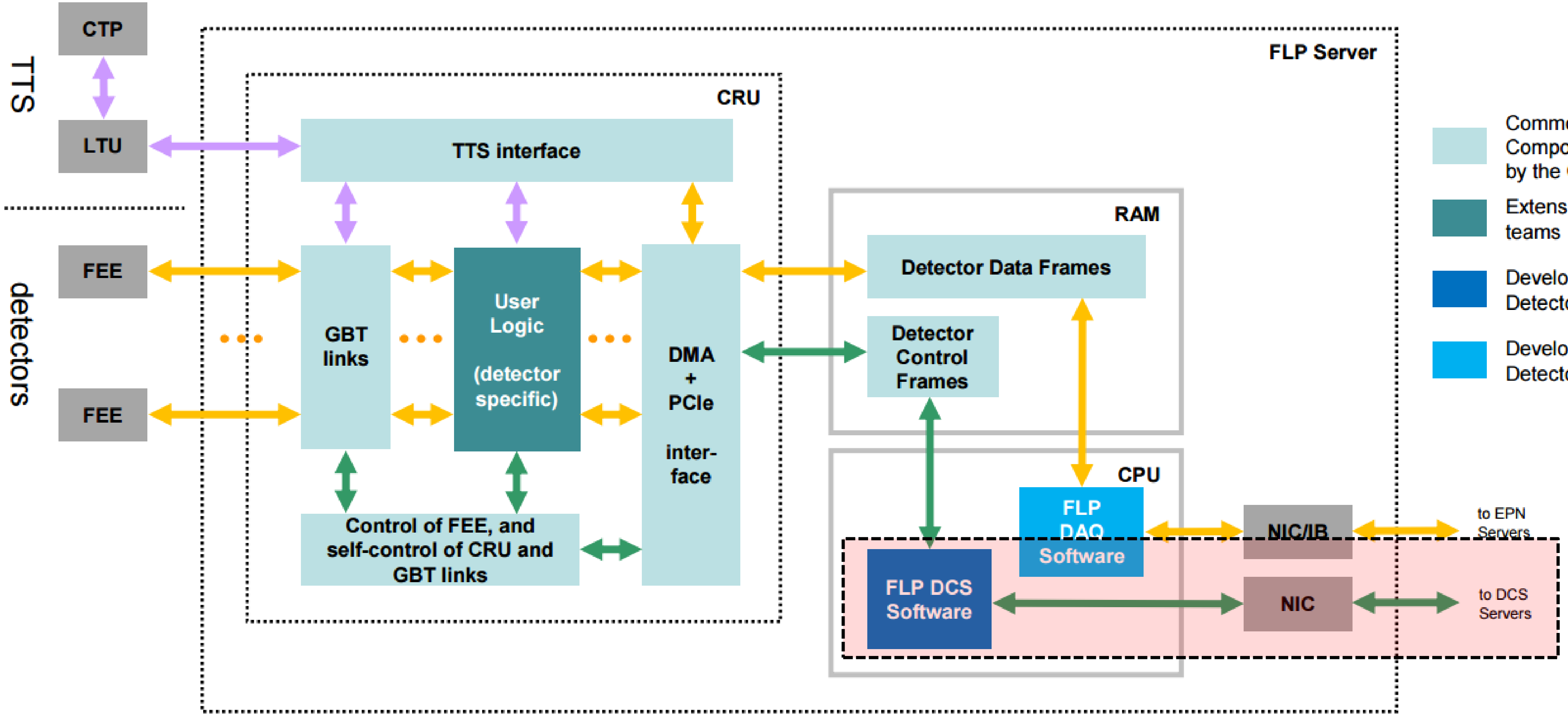



The CRU has therefore all the information to internally compute a "busy map" of all the sensors it is connected with. It can then decide on what kind of HB Acknowledge to provide to the CTP according to its own local busy map.

# Detector Control System

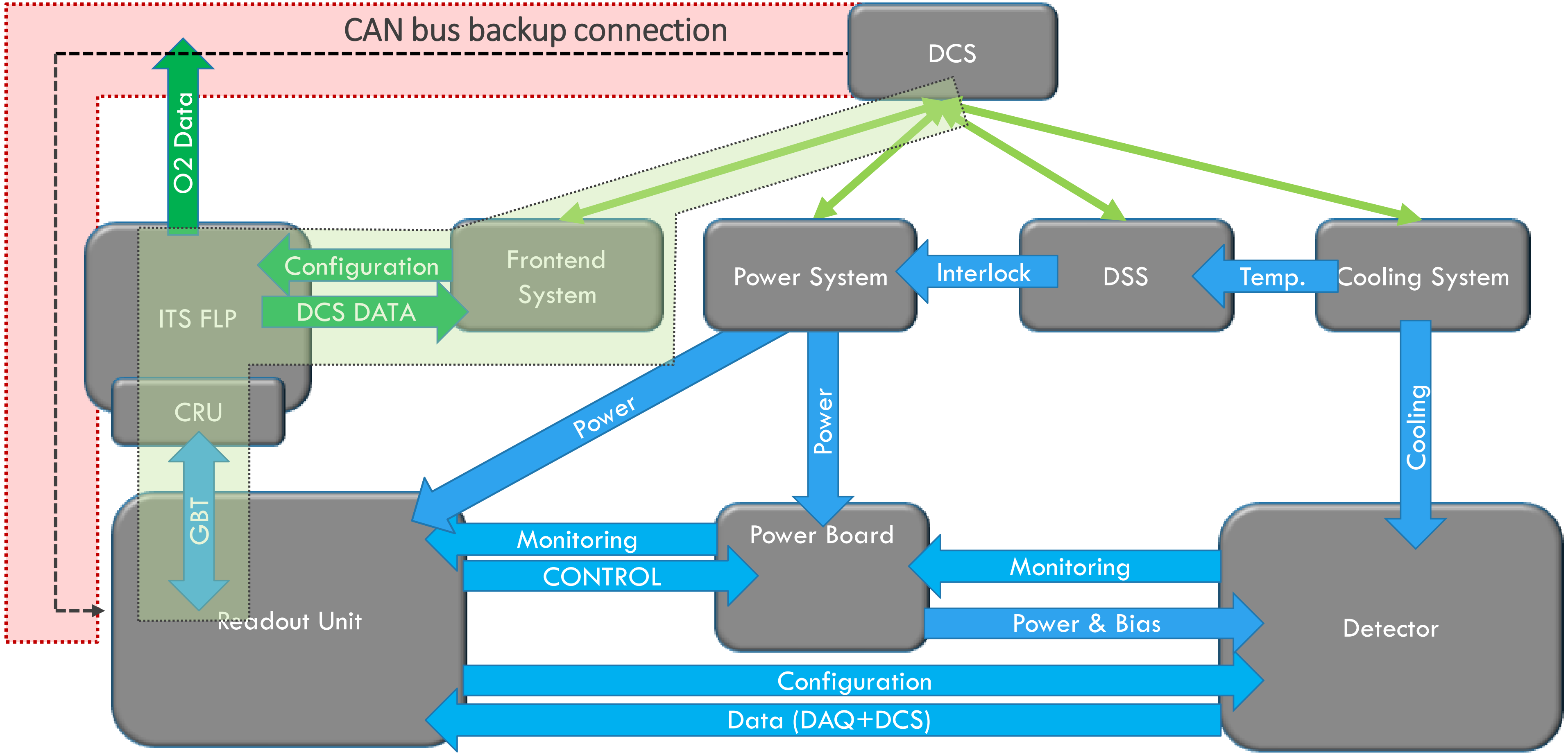
# DCS – Detector Control System (DCS)within the $O^2$

The Detector Control System has a priority path within the $O^2$ system to send DCS command to the detector through the same GBT optical lines used for the detector control.



# DCS – DCS-centric view of the ITS

- Standard DCS commands go through the CRU-GBT-Readout Unit connection.
- In case of shut-down of the CRUs (e.g. for maintenance or problems ), <u>DCS can alternatively control/monitor the Power Boards and the Readout Unit through a CANbus dedicated back-ip connection</u>.

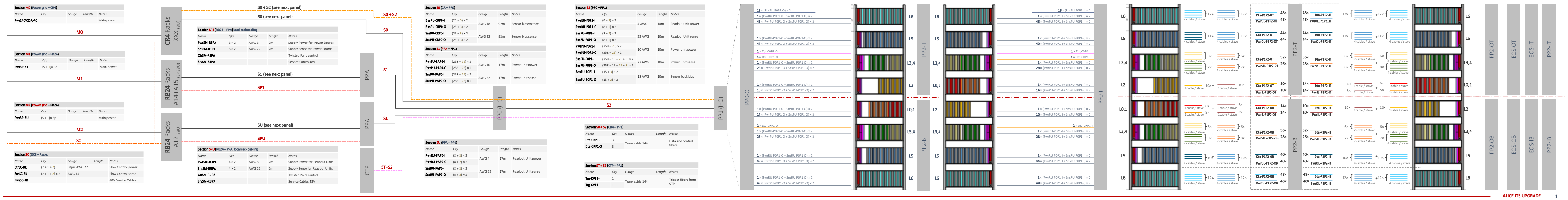


# System Integration

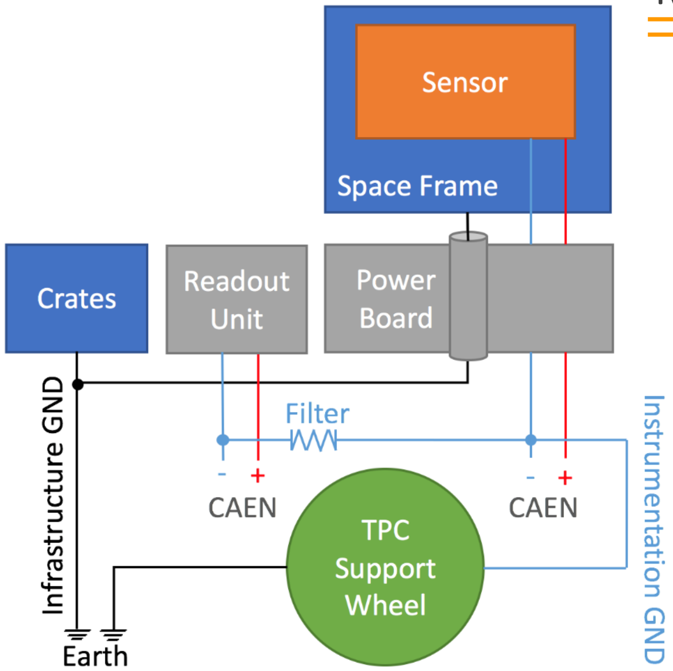
# Integration – General system layout, including Power Units

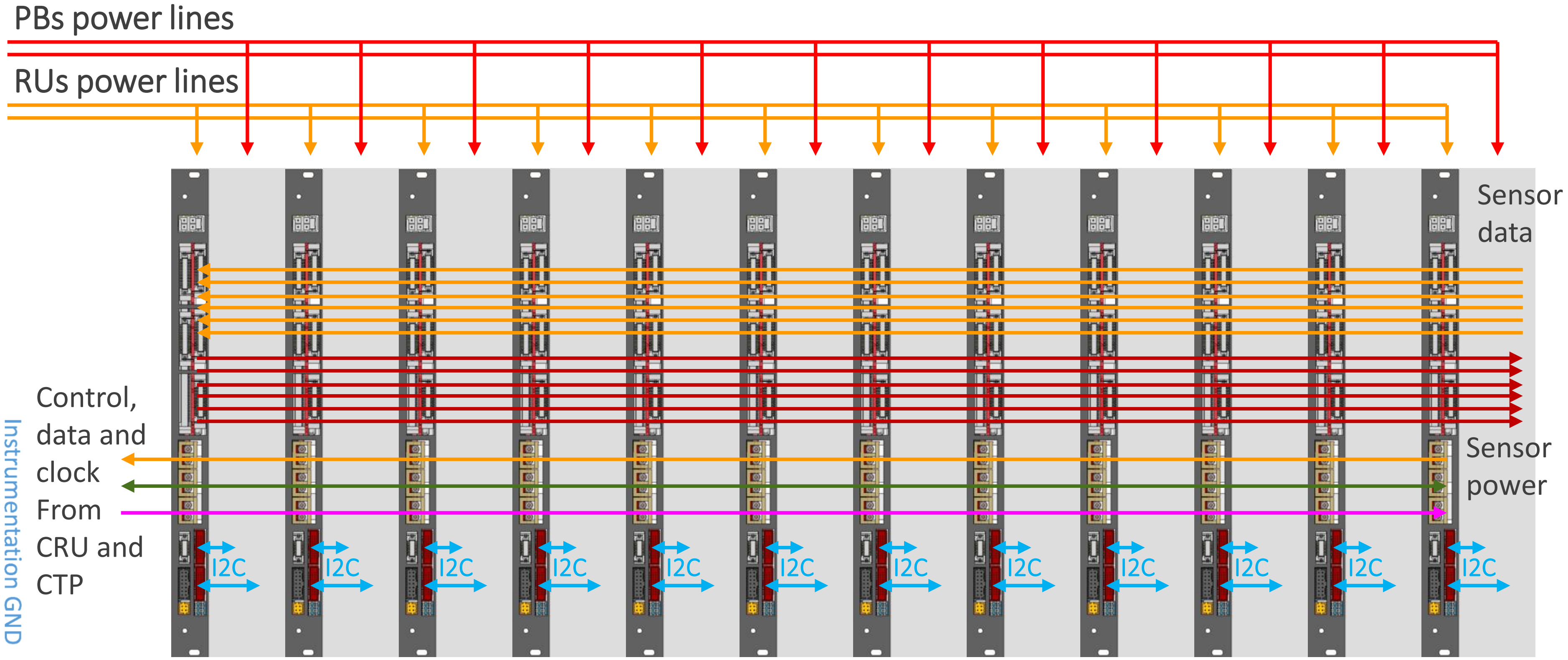
## Connections (power, bias, data, sense) layout from cavern racks to ITS end wheels **defined**.

ITS Connections Cartoon – 2017 Sep 15



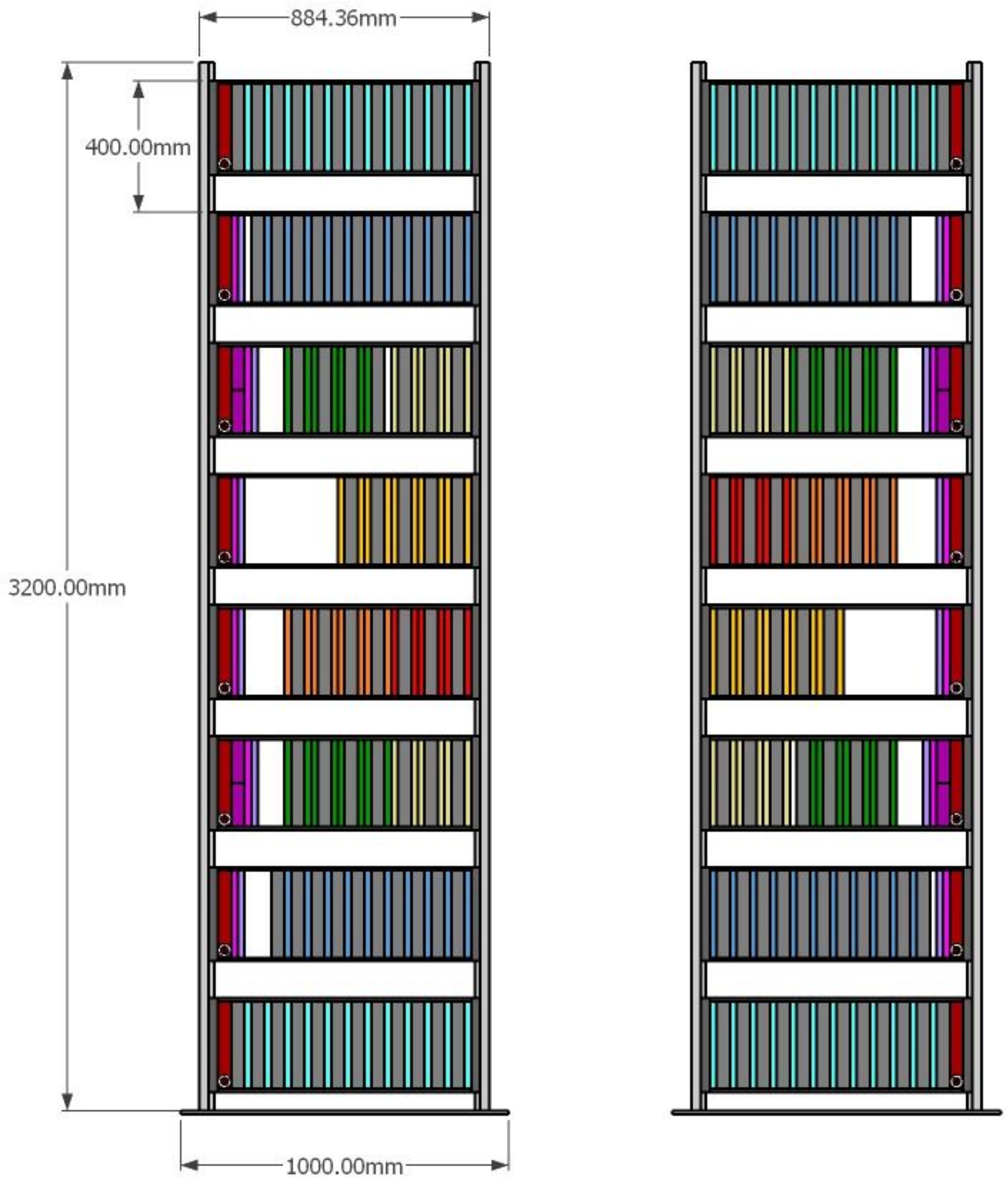
## Grounding scheme fixed.




Missing for clarity bias lines and CAN bus lines

# Integration – RU and PB layout in crates, 16 Crates in total, 3.2 m high and 0.9 m wide




- Layer 0 RUs
- Layer 1 RUs
- Layer 2 RUs
- Layer 3 RUs
- Layer 4 RUs
- Layer 5 RUs
- Layer 6 RUs
- Power Boards (2PU each)
- Trigger splitters
- Busy Units
- ~~Trunk Cables routing patches~~

In this drawing:

- RUs are **6U VME** board (actual PCB **233 mm** tall, front panel **266 mm** tall and **20 mm** wide).
- PUs are grouped by two into Power Boards, fitting TWO TIMES the volume of a RU 6U module.
- RU boards pitch is **4×HP** (4×5.08mm = **20.32mm**), the standard VME bus.
- Crates are **39** modules wide: total rack width about **88 cm.**
- Total height of a rack is 320 cm.
- Update from the infrastructure: Trunk cables routing made ABOVE the crates in common TPC space.

# **Integration** – Connections from **PP1** to **PP2** (racks toward detector patch panel)