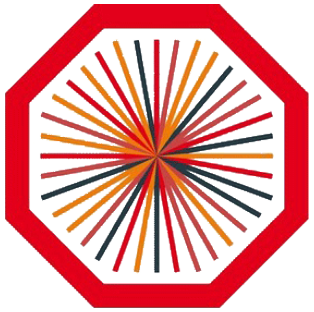
ALICE

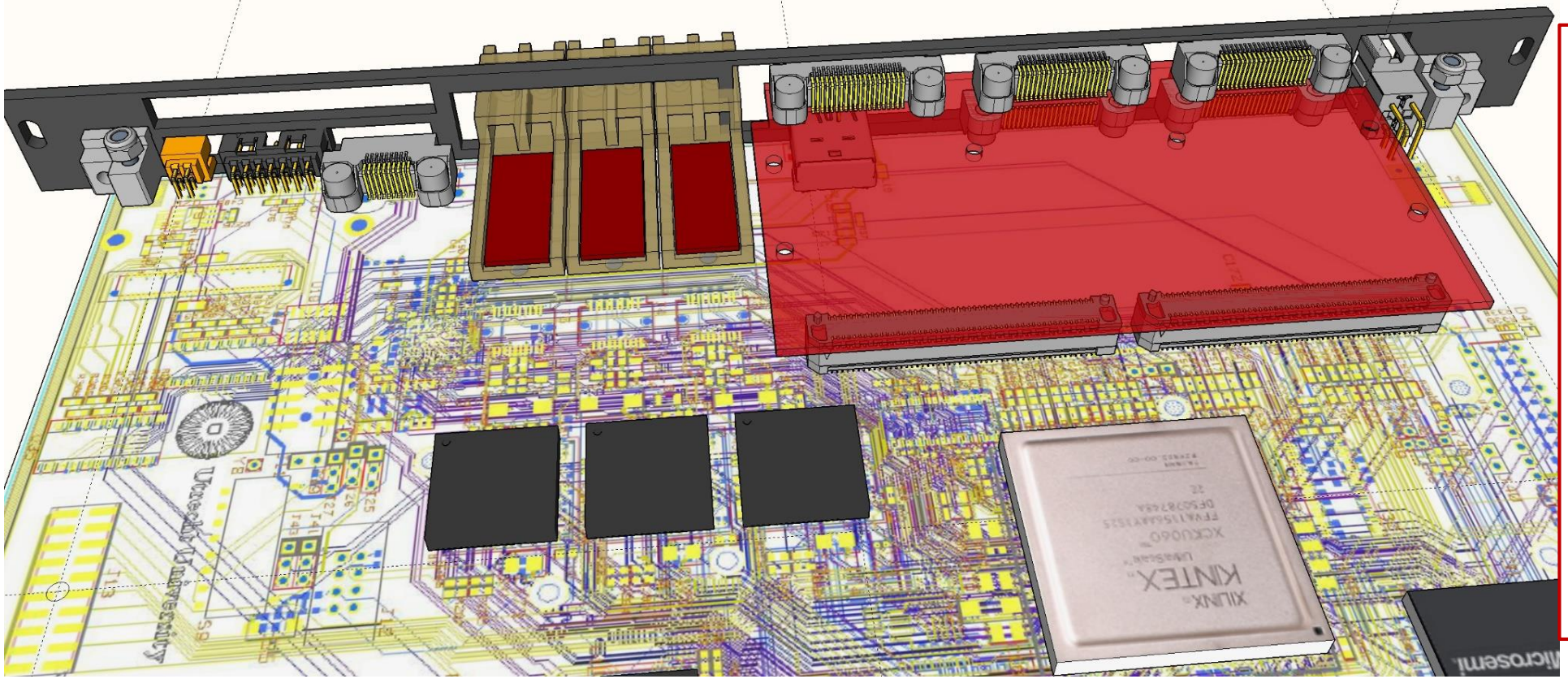


RUv2 overview

RUv2 – Overview

Readout Unit v2 will be production version and is almost identical to RUv1 (the logic part is actually identical), the major differences being about the system integration:

- Change in size to match the Power Board (220mm depth, same height).
- Change of the power connector, now available on the front panel to improve system integration (still compatible with VME powering through J1 backplane to ensure lab and MFT compatibility).
- Simplified/standardized cold plate (thanks to the bigger space available in the new board).

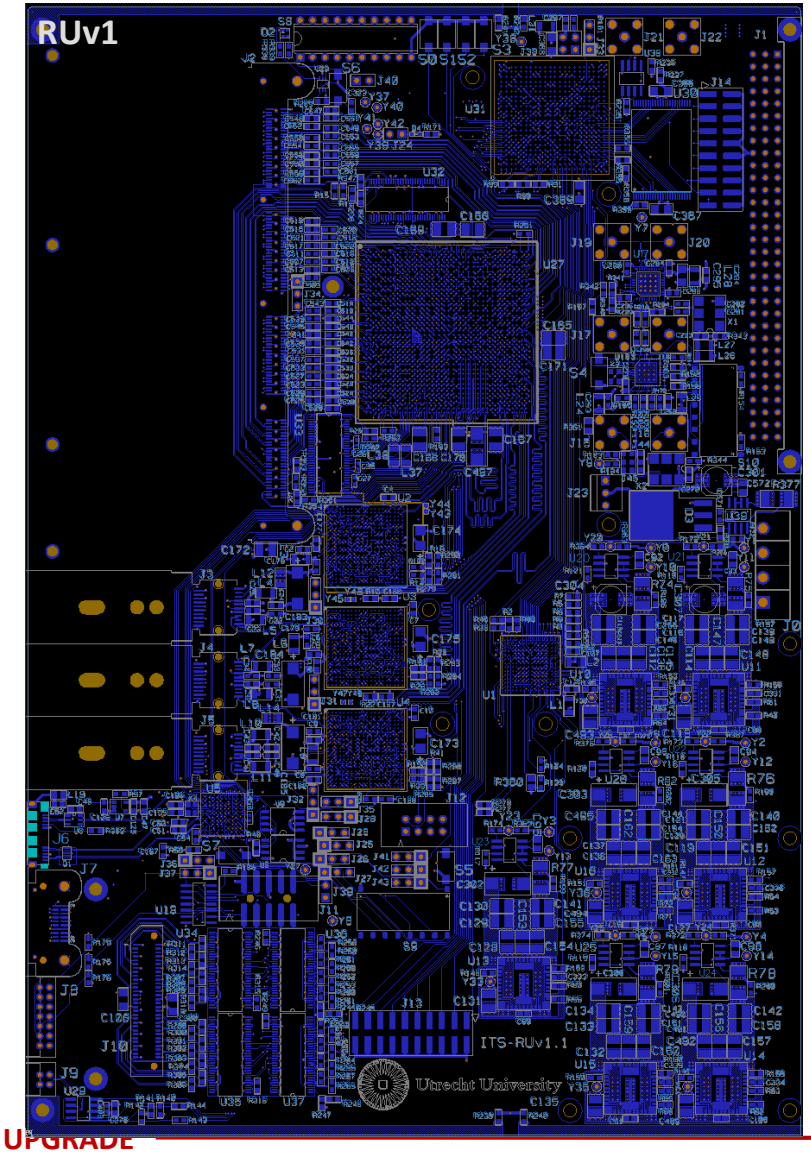


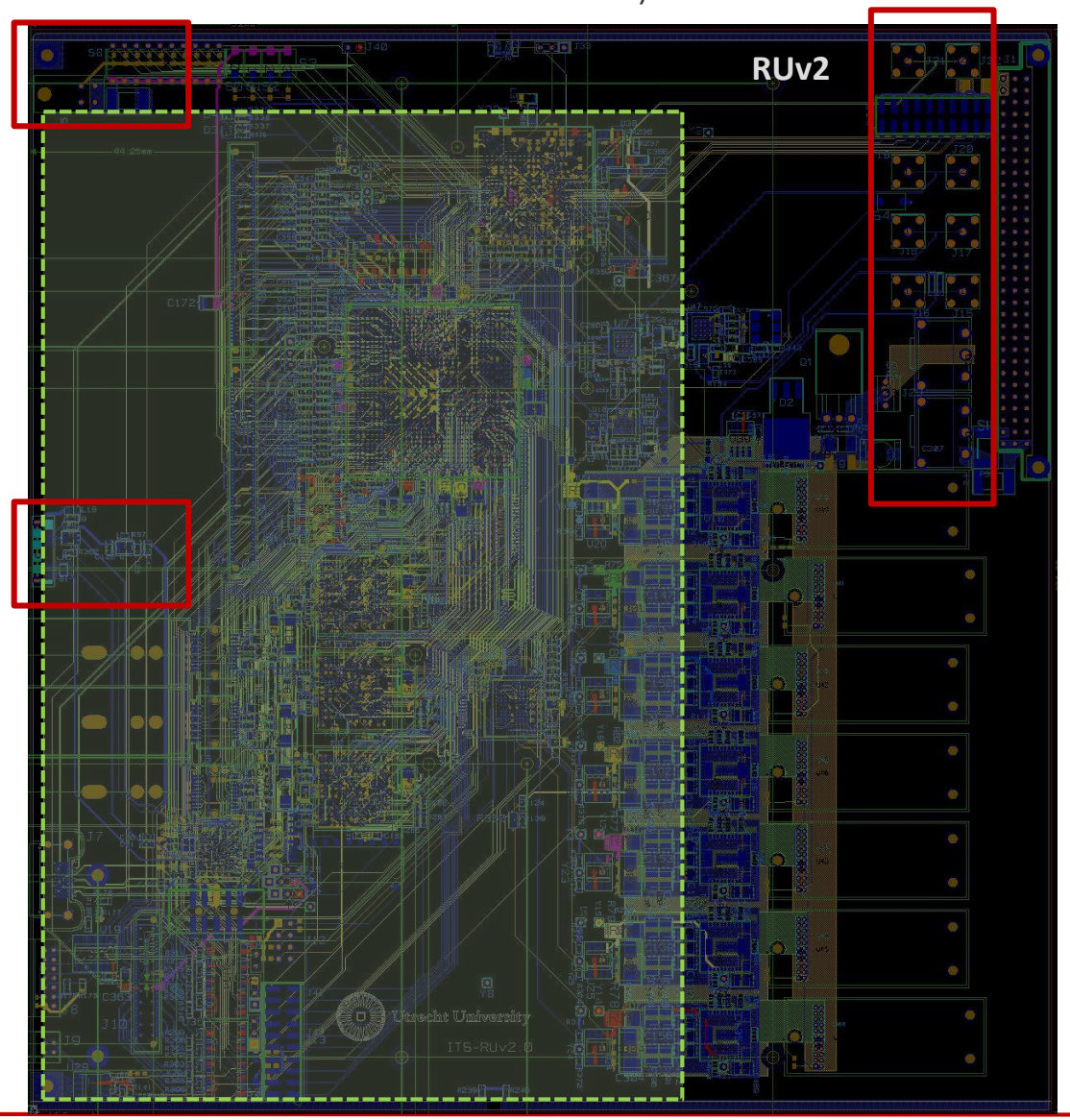
Note: both schematic and layout are 95% identical to RUv1, most changes are:

- improved power supply components placement
- placement and improved front panel connectors layout
- Improved transition board connectors

RUv2 – Form factor changed re-using 90% of RUv1.x tested layout

Layout completed, logic section mostly unchanged, effort went to optimize the power supplies layout and the compatibility with Power Board cold plate. (possibility to install FEASTAMP maintained).

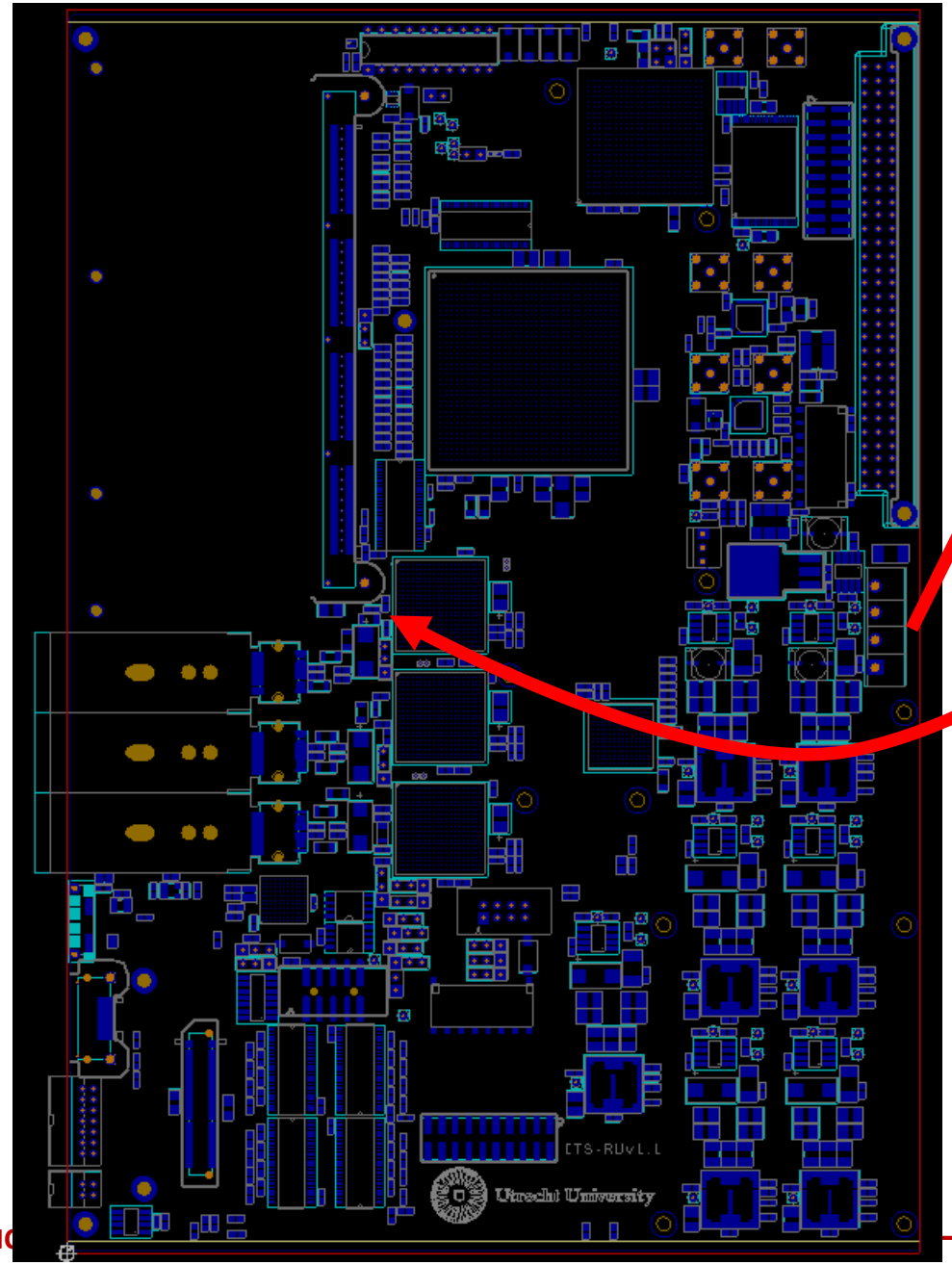




RUv2 – Main differences respect RUv1.x

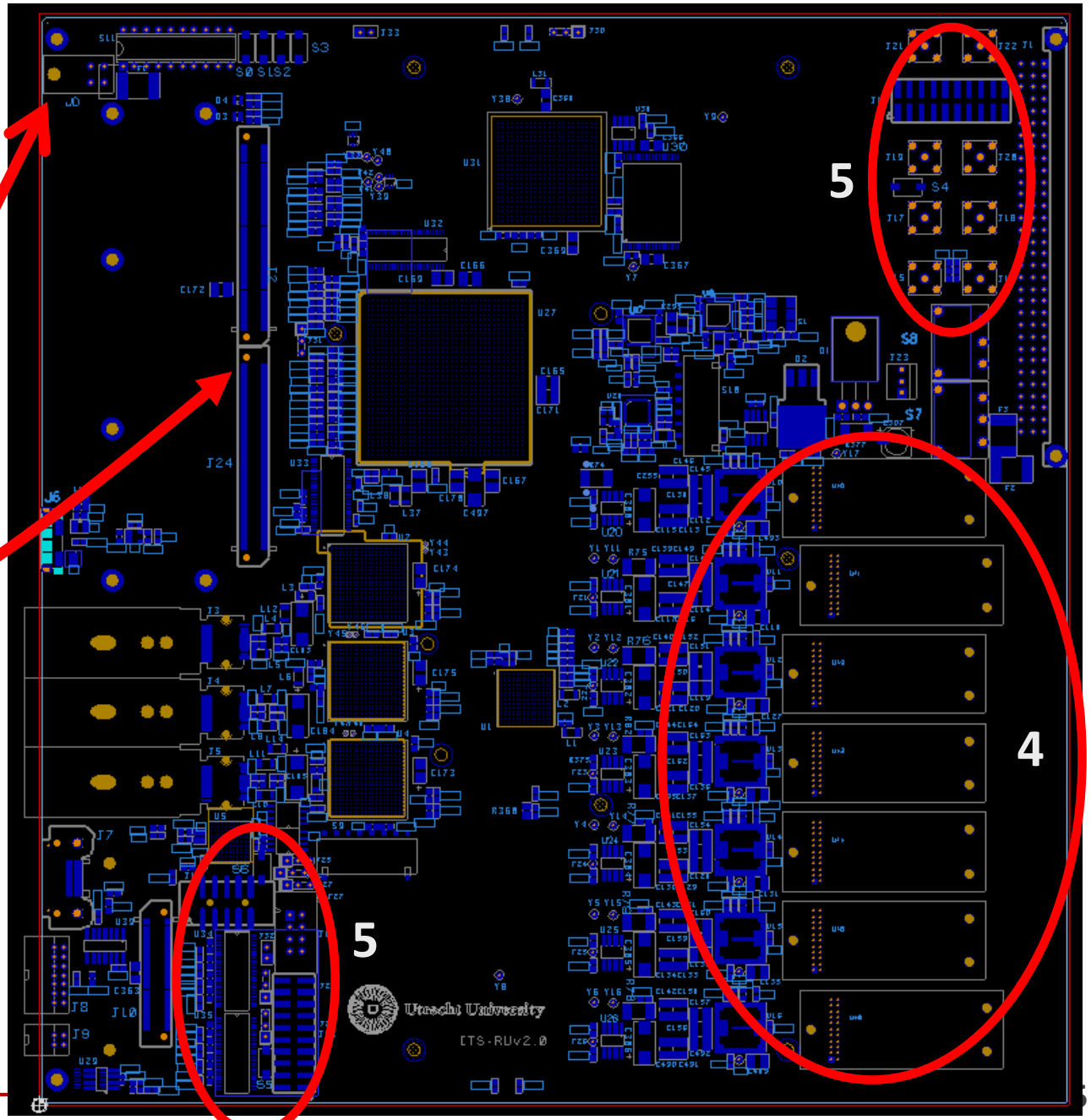
		RUv1_x	RUv2
1	Dimensions	160x233 mm	220x233 mm
2	Power connector	J0 (Weidmuller BL/SL 5.08) on back	J0 (MOLEX 172316) to front (J1 stays as it is + switch to select between J0 & J1)
3	Transistion board connector	Samtec QFS/QMS type	2 * Samtec ERF8-50... (USB3 connector also moved)
4	Power ICs	Only COTS DCDC	Updated DCDC placement for improved PI Use of blind via's to further improve PI
5	Removal high compements from the cold plate area, aiming for same cold plate of power board		
6	Change Clock distribution with PA3 clock independent from jitter cleaner		
7	Remove secondary JTAG chain		
8	Added reverse powerering protection (bypasseble with a switch) based on P-FET		

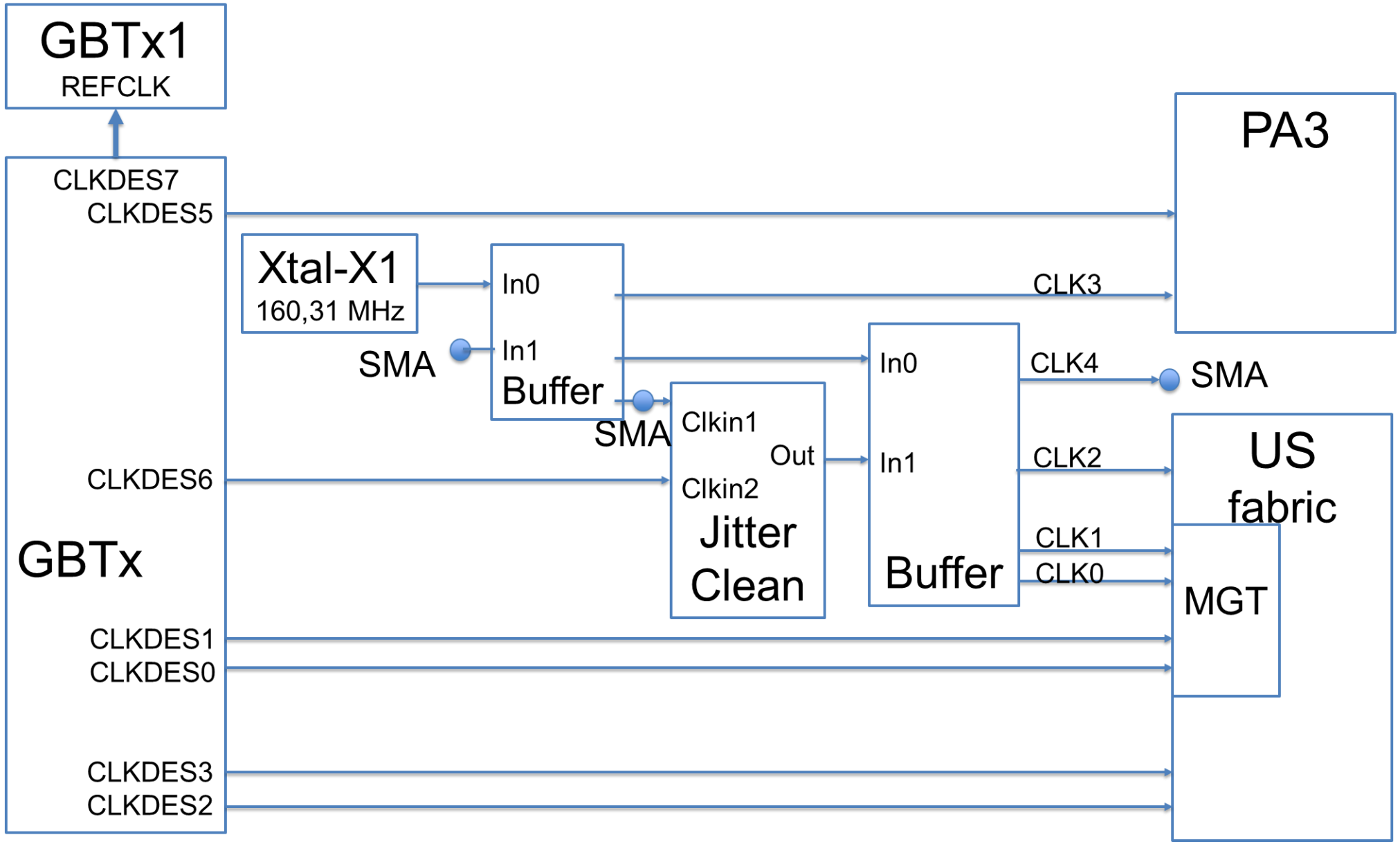
RUv2 – Main differences in layout respect RUv1.x



2

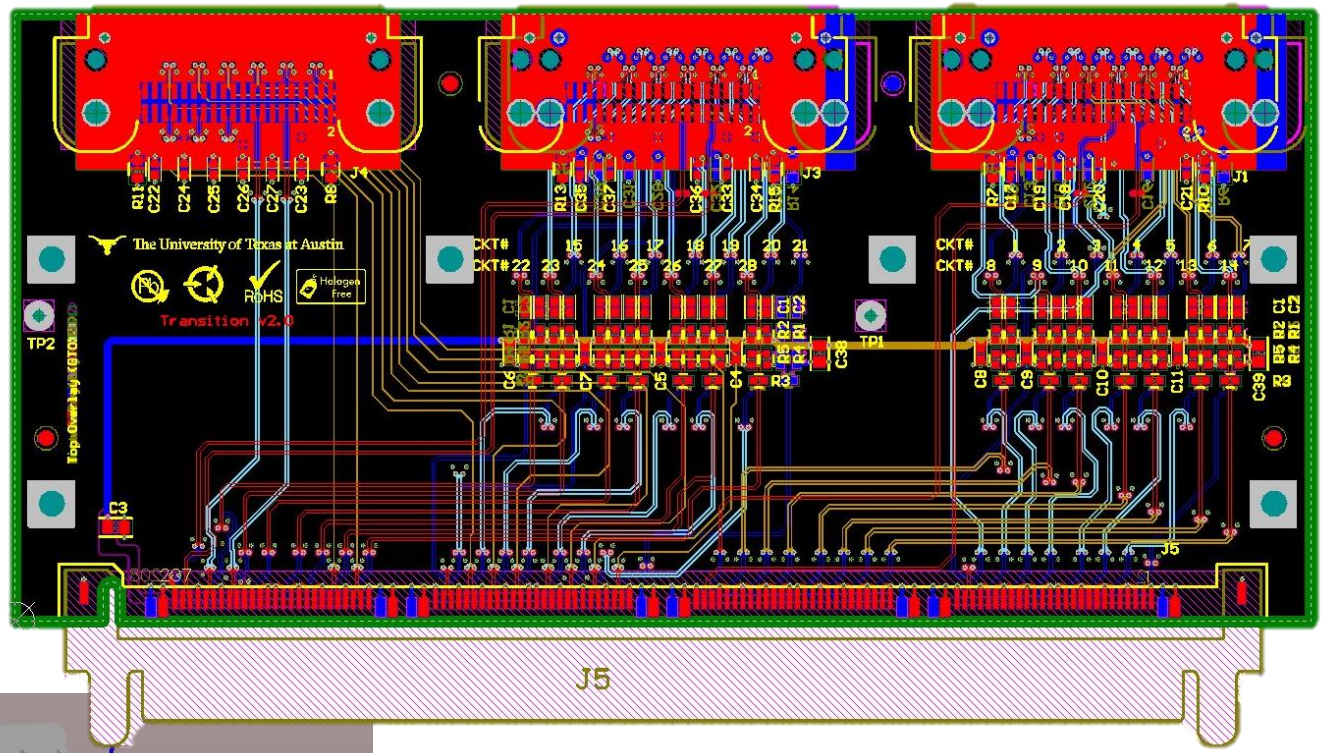
3

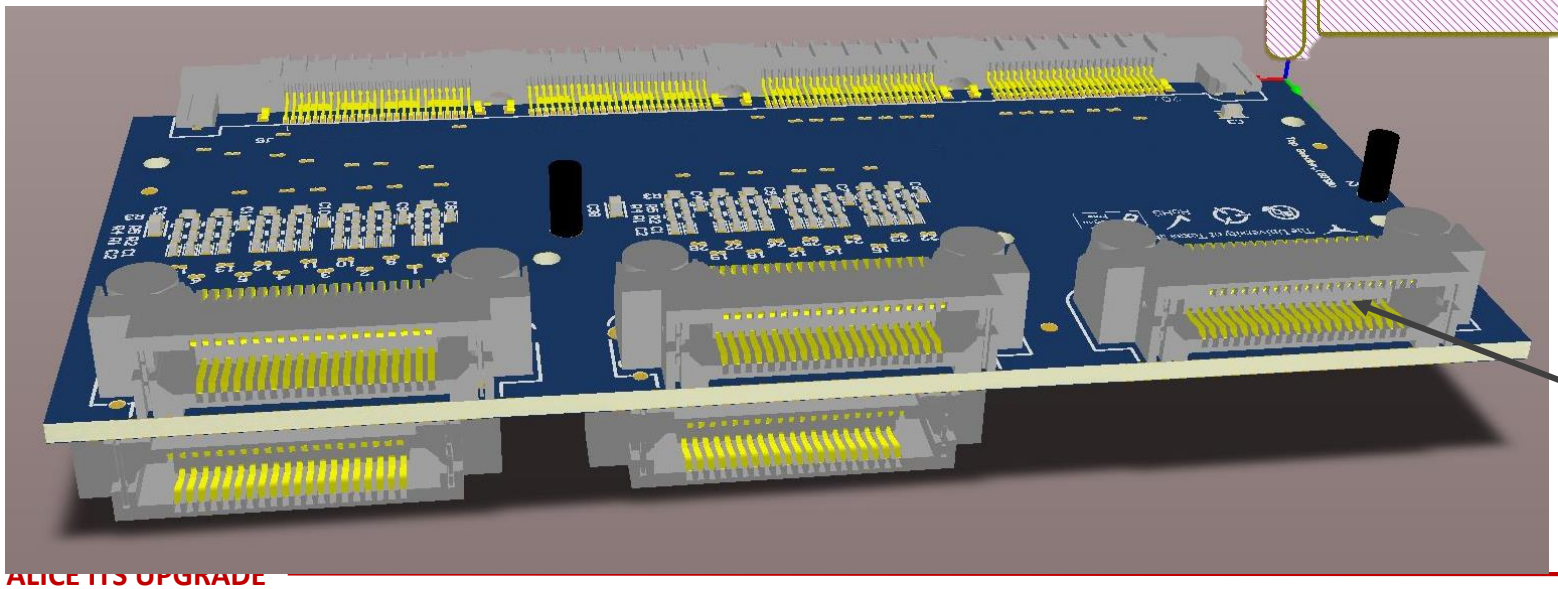



GBTx1
REFCLK
CLKDES7
CLKDES5
CLKDES6
GBTx
CLKDES1
CLKDES0
CLKDES3
CLKDES2
PA3
Xtal-X1
160,31 MHz
SMA
In0
In1
Buffer
SMA
CLK3
Clkin1
Clkin2
Out
Jitter
Clean
In0
In1
Buffer
CLK4
SMA
CLK2
CLK1
CLK0
US
fabric
MGT

RUv2 – Transition board for new cables with commercial RU-side connectors

- An updated version of the transition board has been designed (just launched production). It will be used to verify signal integrity with the commercial ERF connectors, foreseen to be employed for final version of the data cables.
- The final version will likely use an easier to assemble and more readily available connector (ERM series) for the back-connection to RUV2.

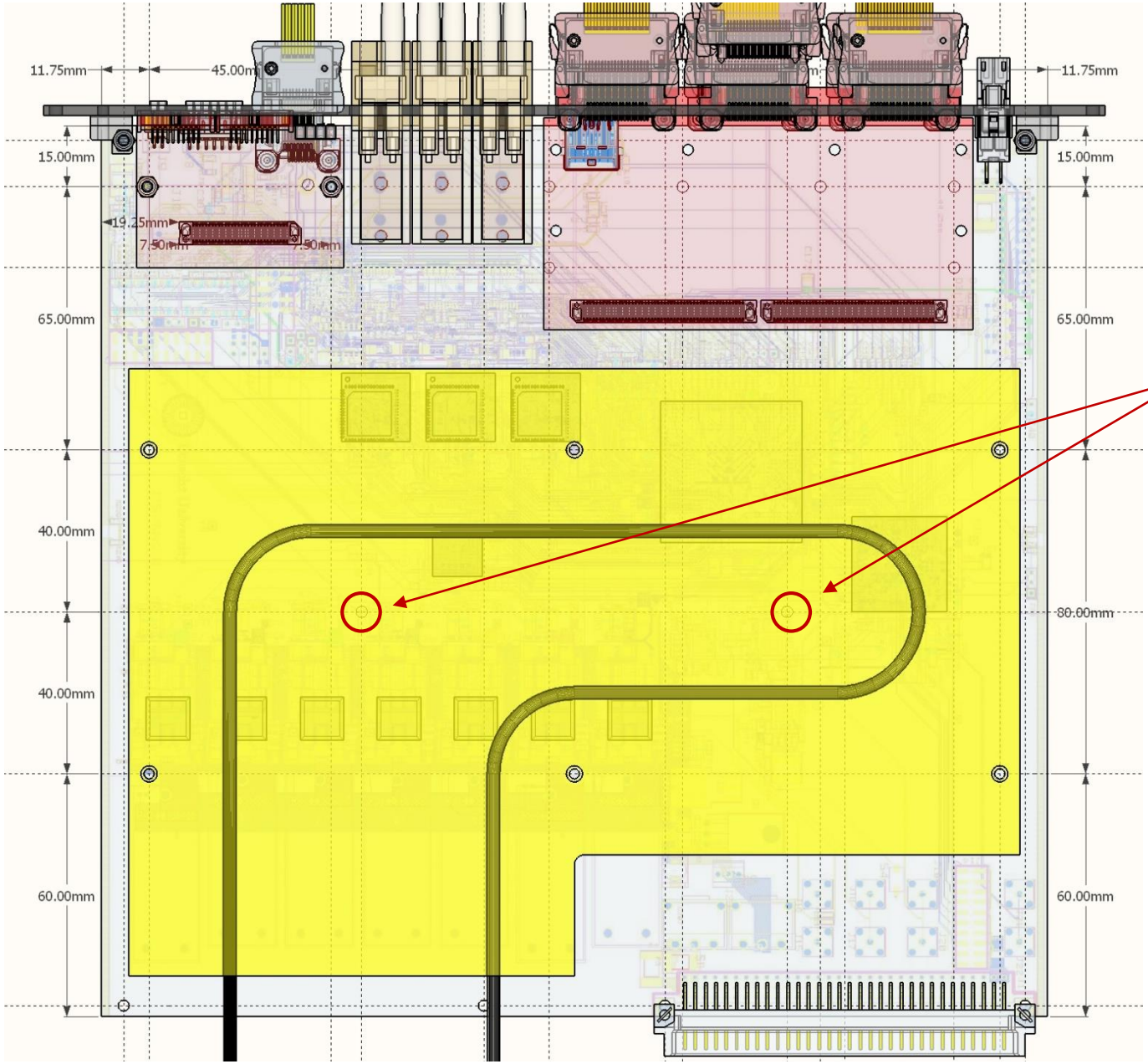




QMS connector compatible with RUv1 for testing, final one will be compatible with RUv2

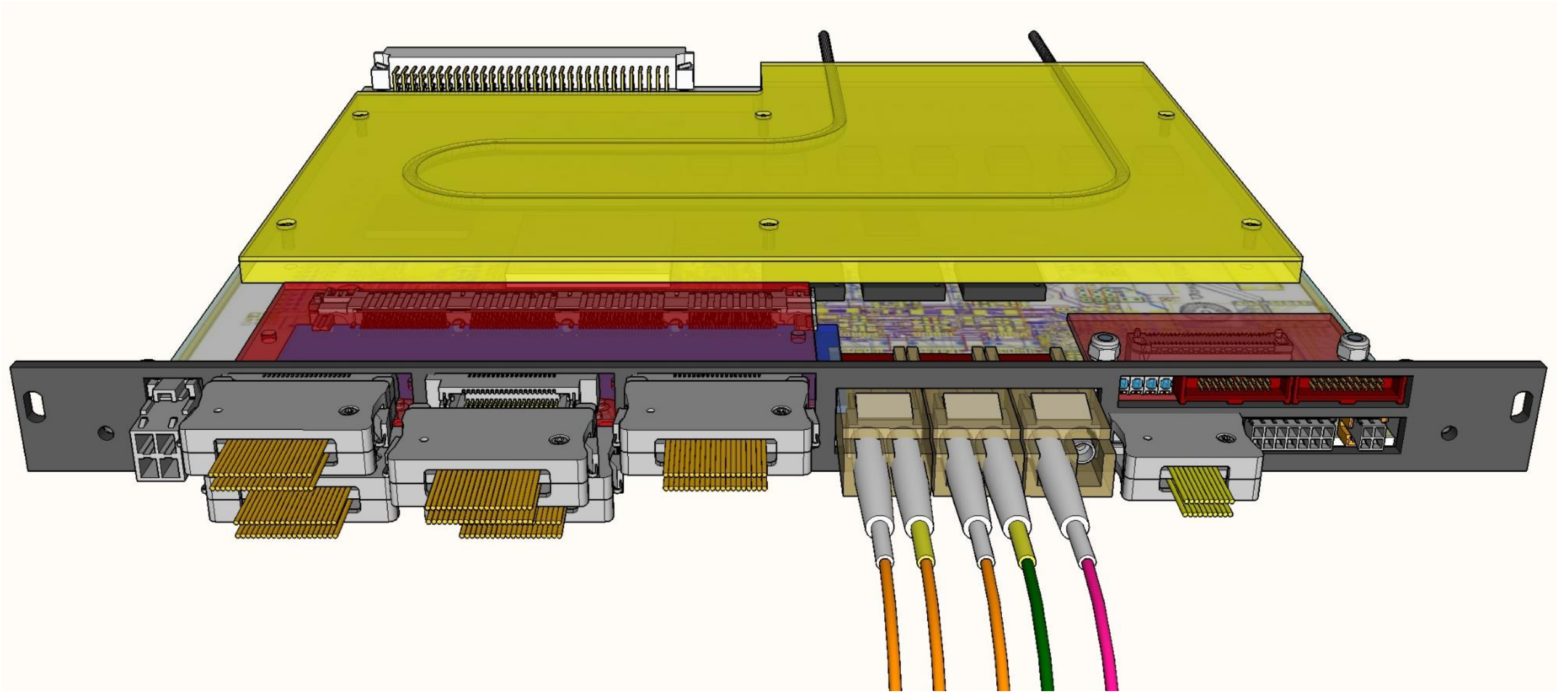
Commercial ERF connectors, dual sourced by Samtec and Hirose

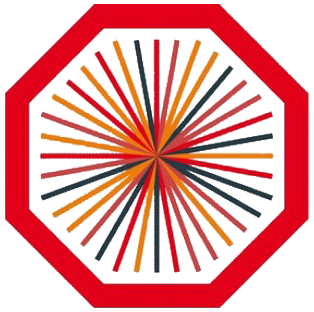
RUv2 – Made compatible with the same cold plate of the Power Board



- Two extra holes (not used by the power board) necessary to optimize coupling
- They will not interfere with pipe routing

RUv2 – Overall view

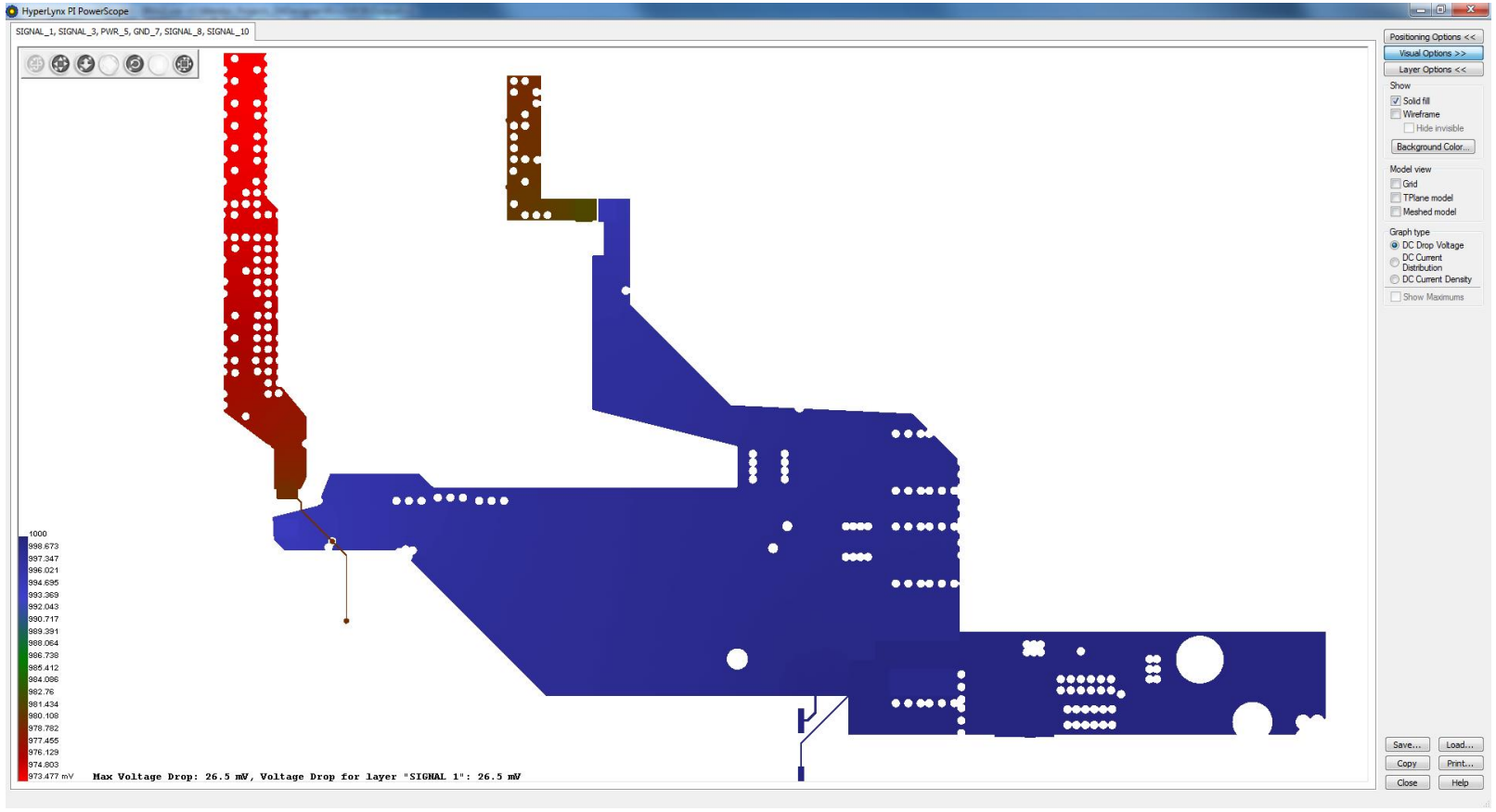


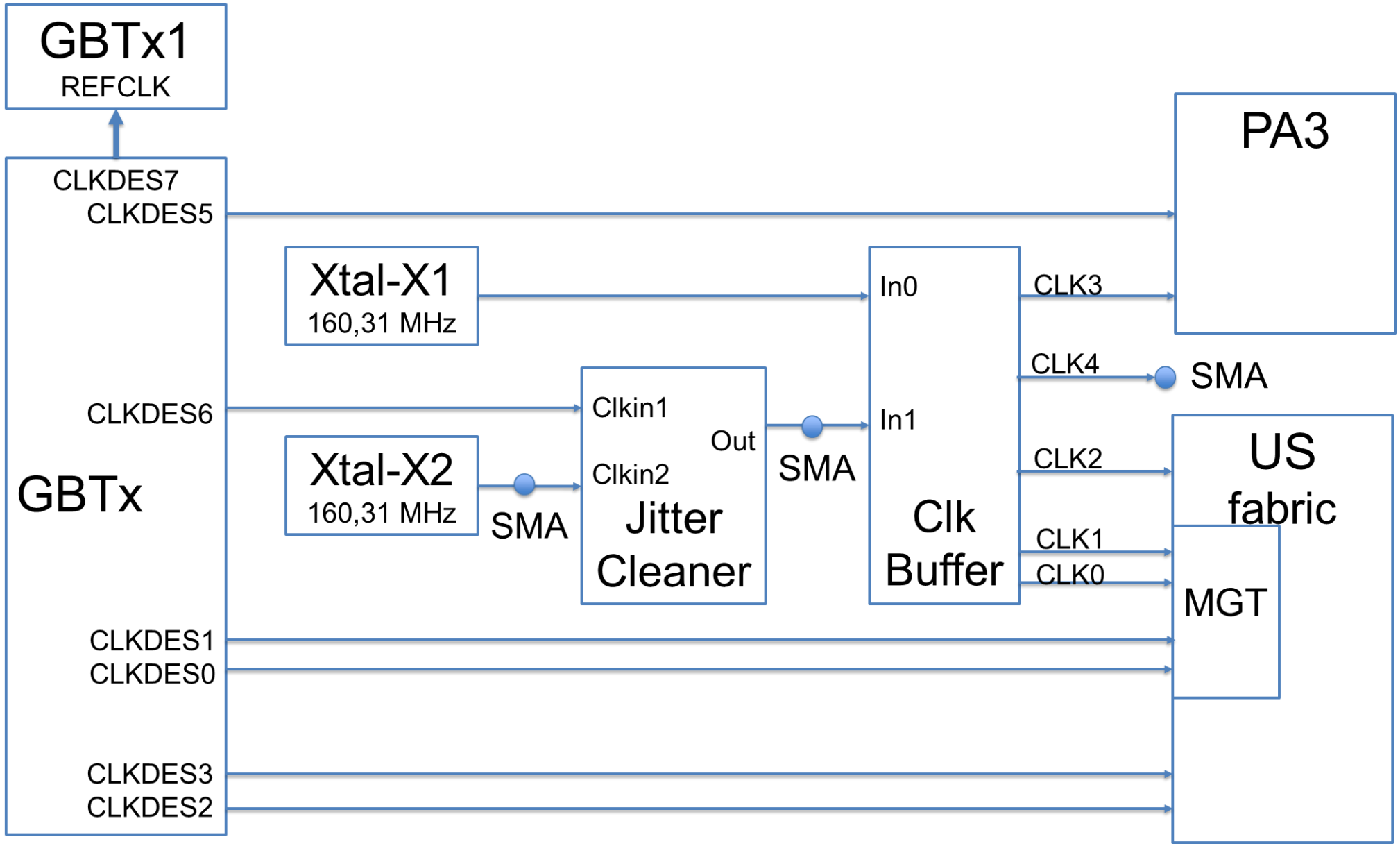


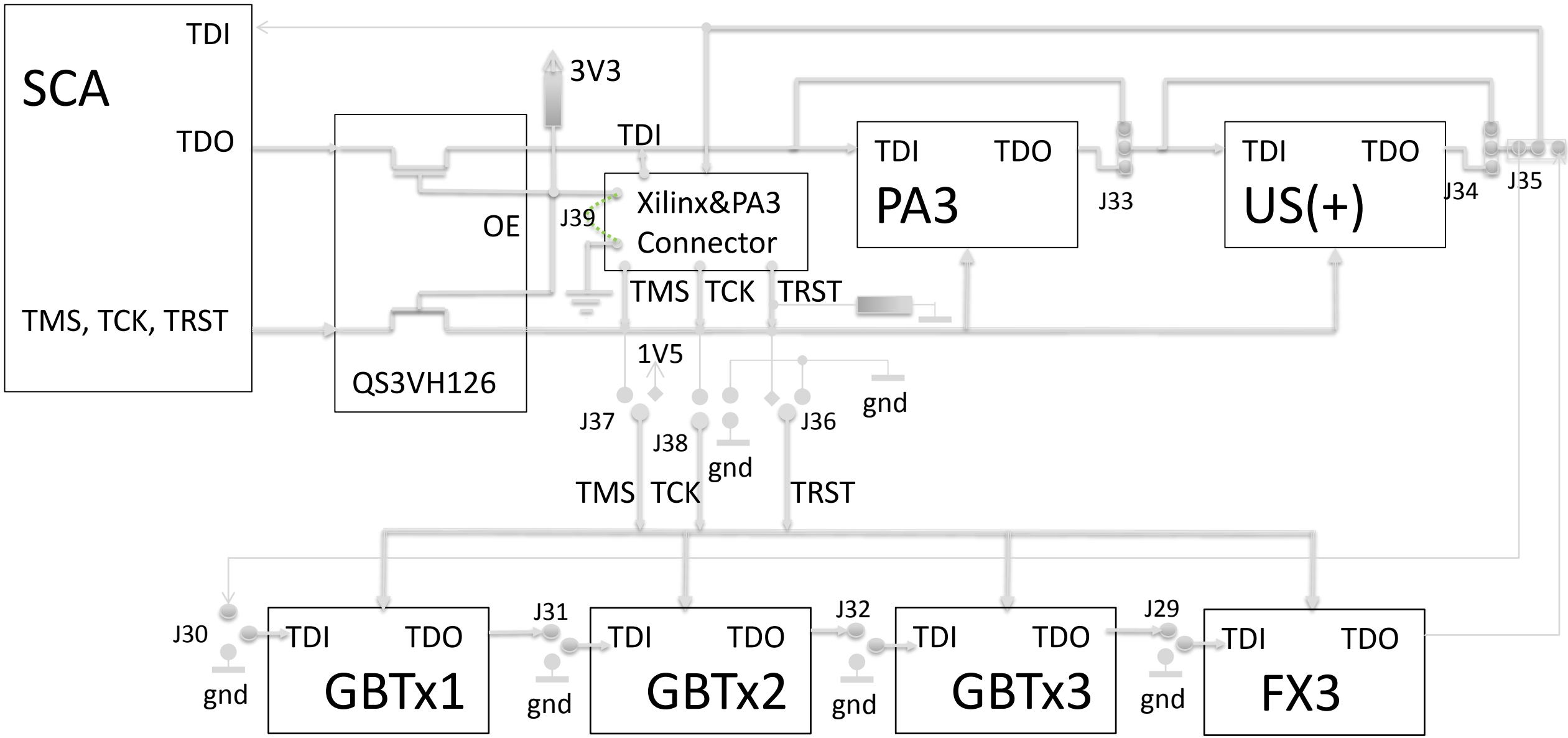
Technical details

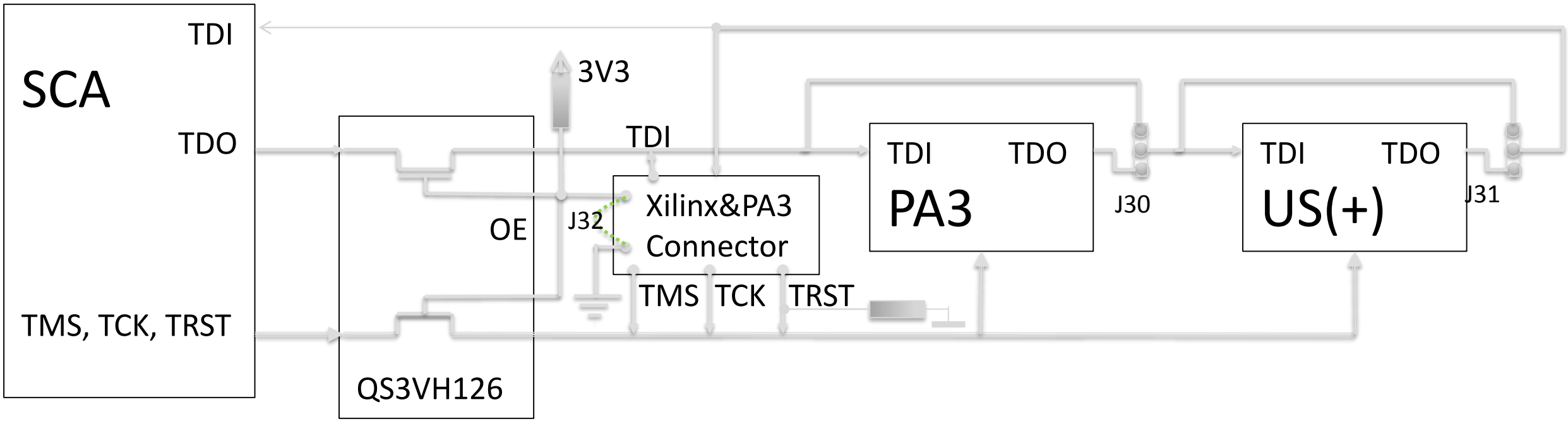
RUv2 – Improved power distribution layers

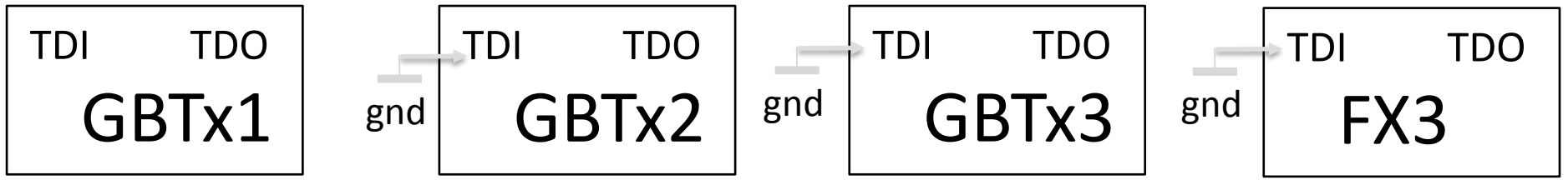
Rail	V	RUv1.x (mV)	RUv2 (mV) New DCDC placement	RUv2 (mV) Adding blind via's
VCCINT	0,95	19,5	13,5	11,3
MGTAVCC	1	32,1	26,8	26,5
MGTAVTT	1,2	30,8	25,2	24,4




GBTx1
REFCLK
CLKDES7
CLKDES5
CLKDES6
GBTx
CLKDES1
CLKDES0
CLKDES3
CLKDES2
Xtal-X1
160,31 MHz
Xtal-X2
160,31 MHz
SMA
Clkin1
Clkin2
Out
Jitter
Cleaner
SMA
In0
In1
Clk
Buffer
CLK3
CLK4
CLK2
CLK1
CLK0
PA3
SMA
US
fabric
MGT


SCA
TDI
TDO
TMS, TCK, TRST
3V3
OE
QS3VH126
TDI
J39
Xilinx&PA3
Connector
TMS
TCK
TRST
1V5
J37
J38
J36
gnd
gnd
TMS
TCK
TRST
TDI
TDO
PA3
J33
TDI
TDO
US(+)
J34
J35
J30
gnd
TDI
TDO
GBTx1
J31
gnd
TDI
TDO
GBTx2
J32
gnd
TDI
TDO
GBTx3
J29
gnd
TDI
TDO
FX3


SCA
TDI
TDO
TMS, TCK, TRST
3V3
TDI
OE
J32
Xilinx&PA3
Connector
TMS
TCK
TRST
QS3VH126
TDI
TDO
PA3
J30
TDI
TDO
US(+)
J31


TDI
TDO
GBTx1
gnd
TDI
TDO
GBTx2
gnd
TDI
TDO
GBTx3
gnd
TDI
TDO
FX3

RUv2 – Main differences

		RUv1_x	RUv2
1	Dimensions	160x233 mm	220x233 mm
2	Power connector	J0 (Weidmuller BL/SL 5.08) on back	J0 (MOLEX 172316) to front (J1 stays as it is + switch to select between J0 & J1)
3	Transistion board connector	Samtec QFS/QMS type	2 * Samtec ERF8-50... (USB3 connector also moved)
4	FEASTMP	Only COTS DCDC	Besides COTS also FEASTMP_CLP placeholder Updated DCDC placement for improved PI Use of blind via's to further improve PI
5	Removal high compements from the cold plate area, aiming for same cold plate power board		
6	Change Clock distribution with PA3 clock independent from jitter cleaner		
7	Remove secondary JTAG chain		
8	Added reverse powerering protection (bypasseble with a switch) based on P-FET		

And many more smaller changes that can be found in:
ITS_RUv2_changes

RUv2 – Component qualification

REFDES	Device	Reference	TID (krad)
U1	SCA	Qualified by GBTx team	Ok
U2-U4	GBTx		
U5	CYUSB3014-BZXC	Qualification not needed. USB3 components will be unpowered during experiment/radiation	Ok
U6	USB82400102		
U7	NCP361SNT1G		
U8,U9	24FC1025-I/SM		
X4	CX2520DB19200D0FLJC2		
U10-U16	LMZ31710RVQ	https://twiki.cern.ch/twiki/pub/ALICE/BASE20testing/2016_06_08_TID_testbeam_report_lg.docx (LMZ31503)	30
		https://indico.cern.ch/event/693890/contributions/2846941/attachments/1583662/2503678/20180116_WP10_plenary_JS.pdf	>10
		https://indico.cern.ch/event/626954/contributions/2532813/attachments/1435381/2206935/DCDC_tests_under_magnetic_field_28_03_17.pdf https://indico.cern.ch/event/625131/contributions/2524193/attachments/1431330/2198807/DCDC_tests_under_magnetic_field_21_03_17.pdf	NA
U17-U18	CDCLVD1212	https://indico.cern.ch/event/299180/contributions/1659565/attachments/563051/775695/Poster_ClockDemo_TWEPP14.pdf	1130
U28	Si5316	Not Qualified, probably not needed	?
X3	ABM8-166-114.285		
U39	QS3VH126S1G	https://radwg.web.cern.ch/radwg/Pages/Documents/TulliosPartList.pdf (QS3VH125S1G)	42
U19-U26	AD8418WBRZ	https://twiki.cern.ch/twiki/pub/ALICE/BASE20testing/TID_second_testbeam_report_ac.docx	30
U27	XCKU060FFVA1156	WP10	TBD
U36-U37	SN74AVC1T45DCKR	Qualification not needed. LEDs unpowered during experiment/radiation	Ok
D2	598-8410-207CF		
D4	SML-310PT		
U29	SN65HVD233-EP	Unqualified, looks like space part: SN65HVD233-SP => Include replacement option for ISL71026MVZ https://www.intersil.com/content/dam/Intersil/documents/isl7/isl71026m.pdf	30
U30	K9WBG08U1M-PIB0	https://escies.org/download/webDocumentFile?id=63077 https://escies.org/download/webDocumentFile?id=62803 https://escies.org/download/webDocumentFile?id=62852	70
U31	A3PExx00L	http://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/rt-proasic3	40
U32-U35	SN65MLVD080DGG	https://twiki.cern.ch/twiki/pub/ALICE/BASE20testing/TID_second_testbeam_report_ac.docx	30
U38	TPS3306-15D	Used in Alice TPC (Johan Alme)	Ok
X1, X2	IQXO-661	https://edms.cern.ch/document/1327311/1 (CFPS-73)	50
D3	STPSC806G-TR	https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20110015251.pdf (STPSC806D)	9000
Q1	NDP6020P	http://villaolmo.mib.infn.it/talks/M_Menichelli.pdf	30