ALICE

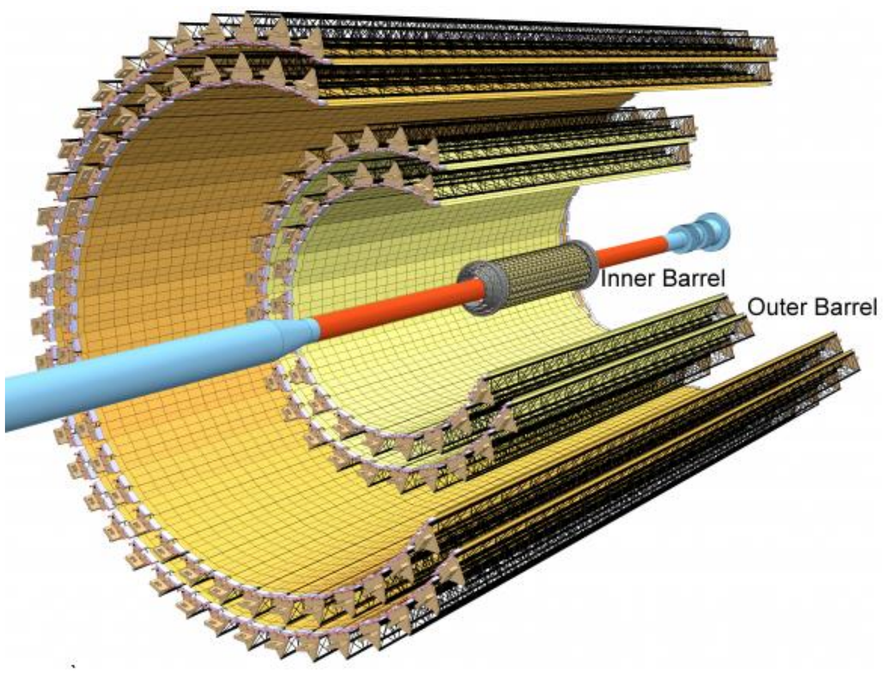
Readout Unit Overview

ITS Readout Electronic – **Production Readiness Review** – 13 Apr 2018 – CERN

Specifications

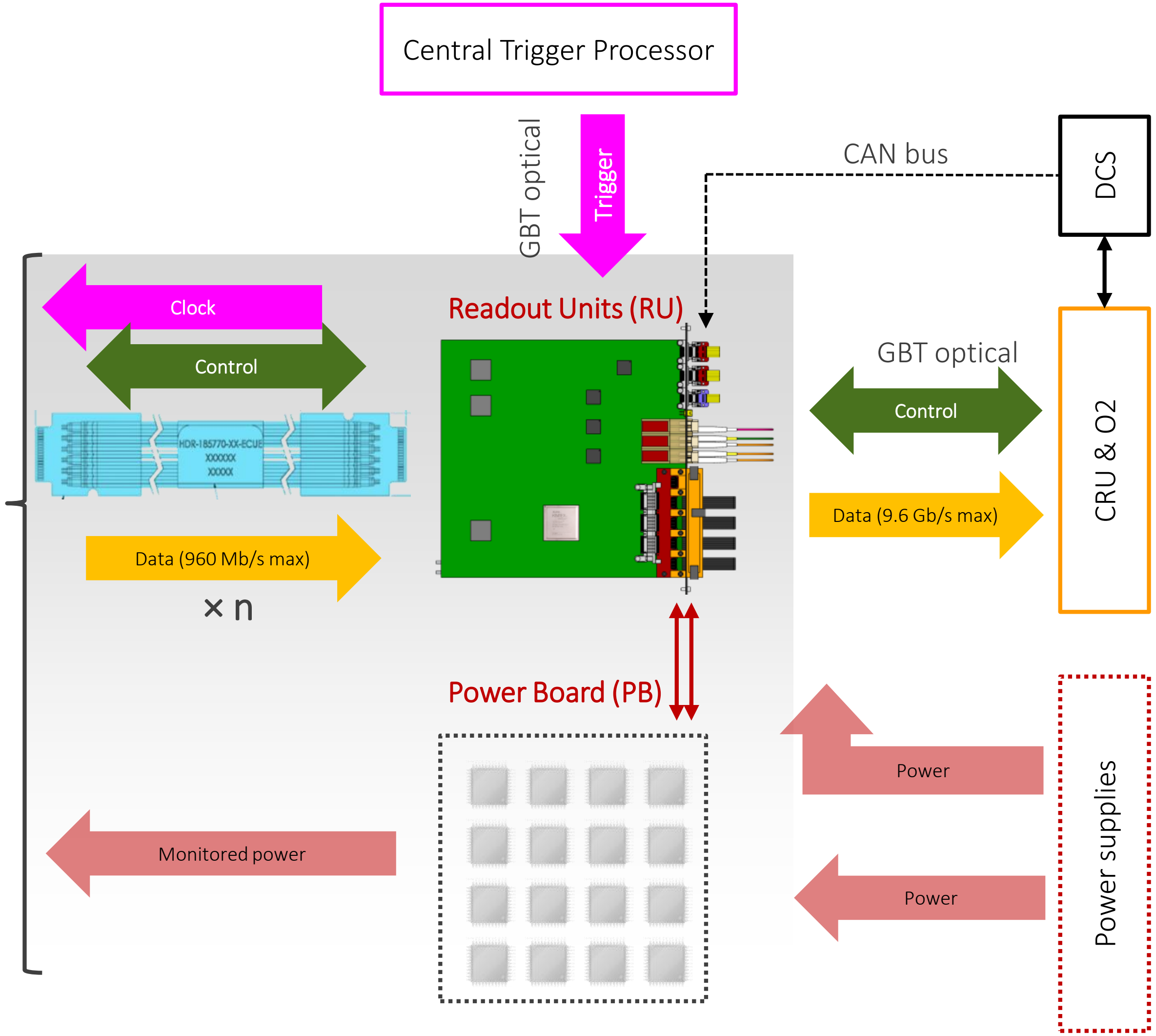
Specifications – ITS Readout Electronics is organized in Readout Units (RU)

The ITS front-end electronics are divided into **192** modular **Readout Units**, each connected to one ITS stave, and optically interfaced with both the Common Readout Unit (CRU) and the Central Trigger Processor (CTP).



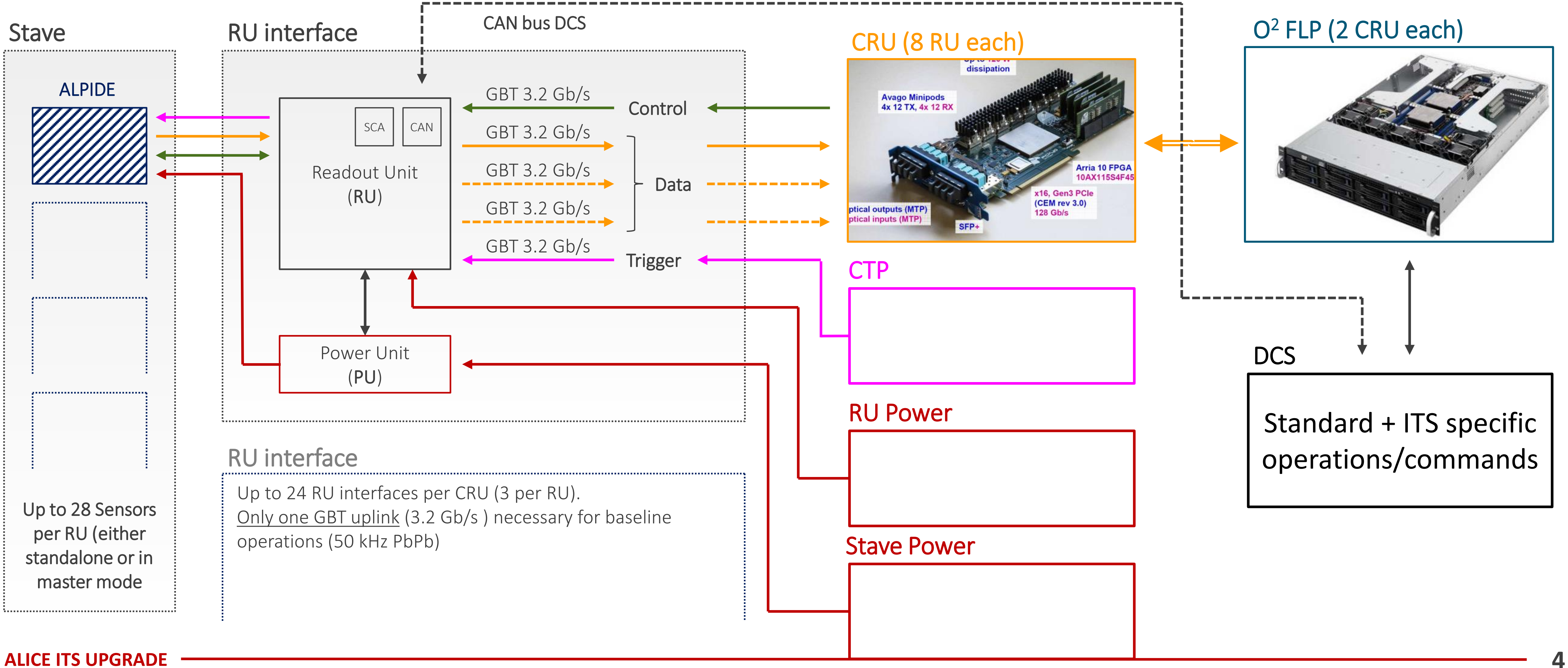
Each Readout Unit is connected to one stave, both for Inner and Outer Barrels

× 192 staves



Specifications – Connections to the other components of the ALICE readout & control system

- The ITS front-end electronic is divided into modular Readout Units (RU), identical for each layer.
- Each readout unit controls an entire stave, including power to the sensors (through custom-made powe units).
- The CRU interfaces with the Readout Unit only, which in turn manages the trigger and the power for the stave.

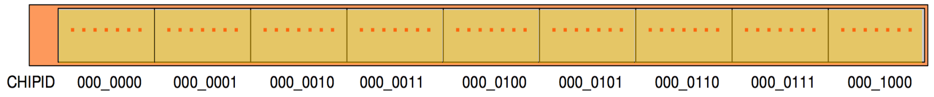


Specifications – Connections toward the sensors

- Each RU is connected to a stave through copper cables (8m long), for control lines, clock, and data lines.
- For the Inner Layers the RU must read **9** 1.2 Gb/s lines, and drive 1 clock and 1 control line.
- For the Outer Layers the RU must read **28** 400 Mb/s lines, and drive 4 clocks and 4 control line.

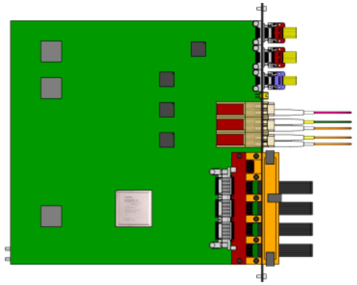
Inner Layers

9 data lines, 1 clock, 1 control



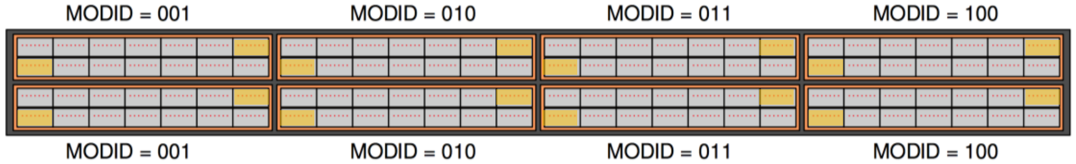
9 data pairs,
1.2 Gb/s each

Readout Unit

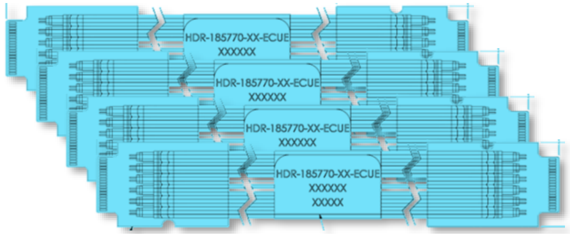


Middle Layers

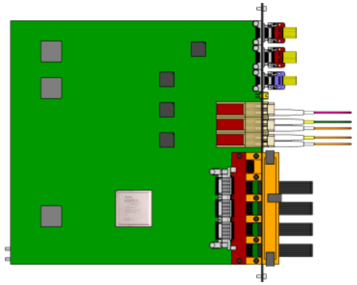
(4+4+4+4) data, (1+1+1+1) clock, (1+1+1+1) control



16 data pairs,
400 Mb/s each

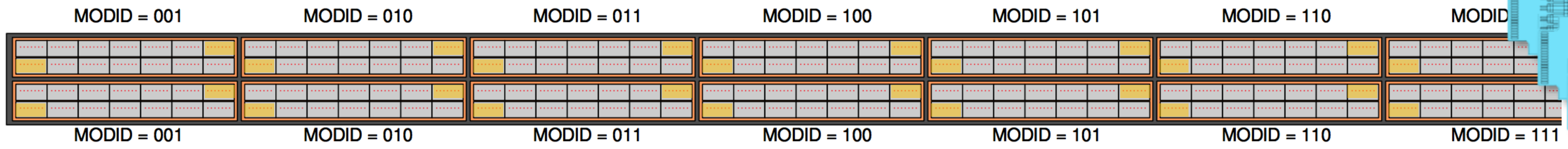


Readout Unit

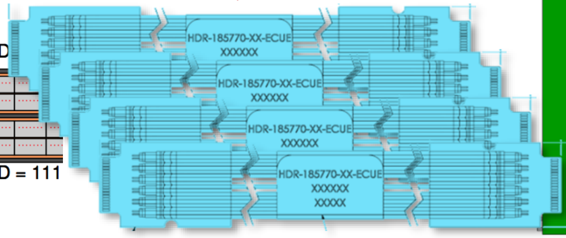


Outer Layers

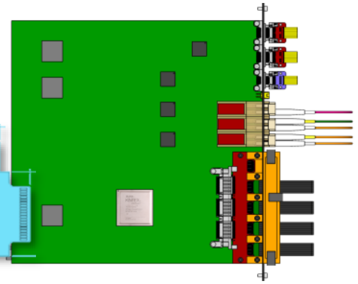
(7+7+7+7) data, (1+1+1+1) clock, (1+1+1+1) control



28 data pairs,
400 Mb/s each

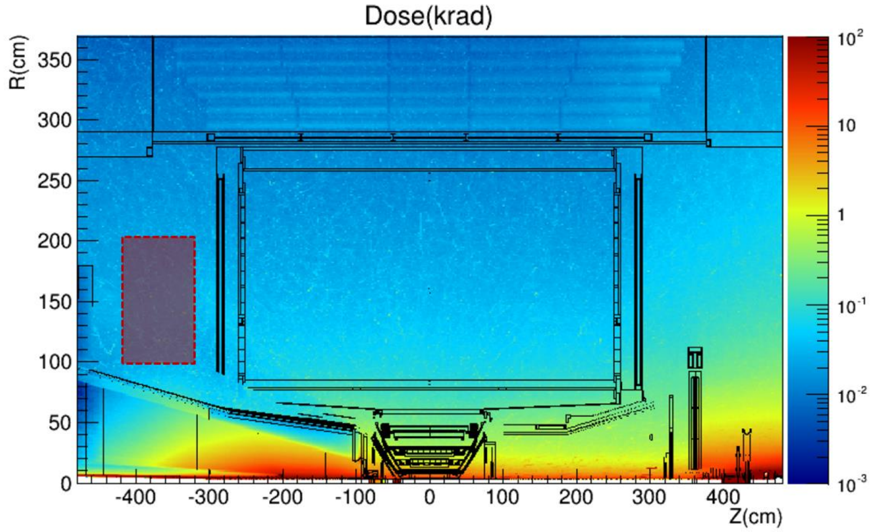


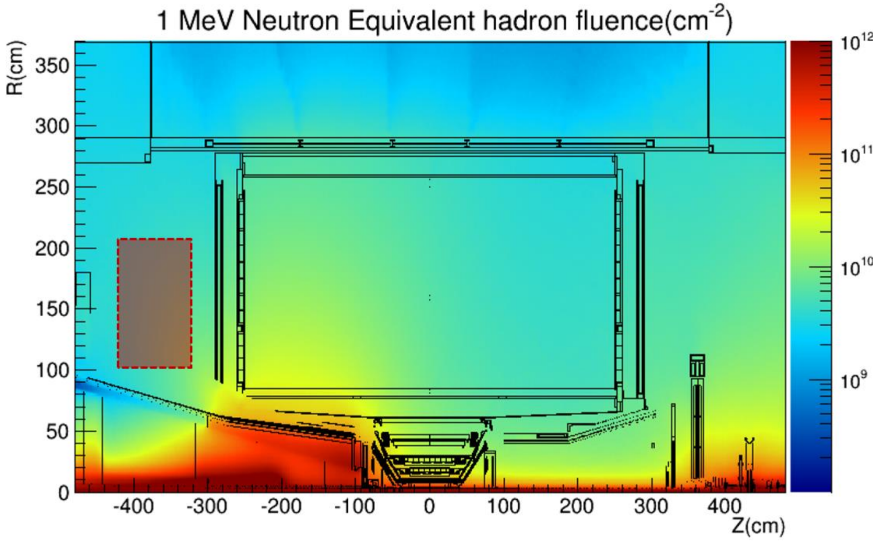
Readout Unit

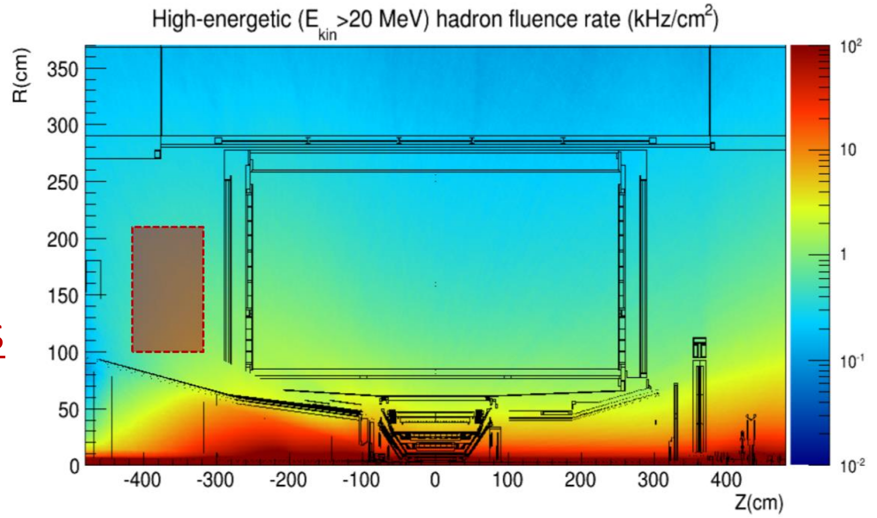


Specifications – Expected radiation levels summary

- **TID levels** (10k considering 10× safety factor) are of no practical concern for modern microelectronic devices.
- **NEF levels** (10^{11} including 10× safety factor) are not a concern for material degradation and component reliability.
- **High energy* hadrons** are the real concern, as the can cause latch-ups in electronic components and SEU on logic devices. Testing did show that latch-ups will not be a problem, while proper design is required to mitigate the SEUs effects.







Position respect to beam			Radiation levels (total)		
r	z	Name	TID	1 MeV neq fluence	High energy hadron flux*
[cm]	[cm]		[krad]	[cm^{-2}]	[kHz cm^{-2}]
2.2	[±13.5]	ITS L0	2734	1.7×10^{13}	765 (770)
43	[±73.7]	ITS L6	20	8.1×10^{11}	3.4 (4.9)
79	[±260]	TPC In	5.6	7.0×10^{11}	1.35 (1.8)
100	330	RE	≈ 5	≈ 1.6×10^{11}	0.86
258	[±260]	TPC Out	0.86	1.4×10^{11}	0.27 (0.37)
290	[±290]	TRD	0.6	1.2×10^{11}	0.23 (0.31)

We assume 1 kHz cm^{-2} for baseline reference.

- TID & fluence = (table 1 × $1.3_{\text{data taking efficiency}}$ + Table 2 / $10_{\text{better vacuum}}$) × $10_{\text{safety factor}}$
- **Hadrons and charged particles as for 50 kHz Pb-Pb collisions** (worst case scenario).
- The average value within the z span is reported, in brackets the peak value.
- * Momentum > 20 MeV

Specifications – Summary

High Speed I/Os

- 9 × 1.2 Gb/s transceiver lanes for reading Inner Layers data (ITS).
- Up to 28 × 1.2 Gb/s transceiver lanes for reading data (MFT and ITS fall-back).
- 28 × 400 Mb/s fabric lanes for Middle and Outer Layer data.

GBT chipset (optical I/Os)

- 28 × GBTx chip: 1 for control and basic data, 1 for further transmission, one for receiving the trigger.
- 2 × VTRx modules (control, data and trigger).
- 1 × VTTx module (high data bandwidth, not used for baseline operation).
- 1 × SCA chip: board monitoring, firmware upload, FPGAs reset.

Other IOs

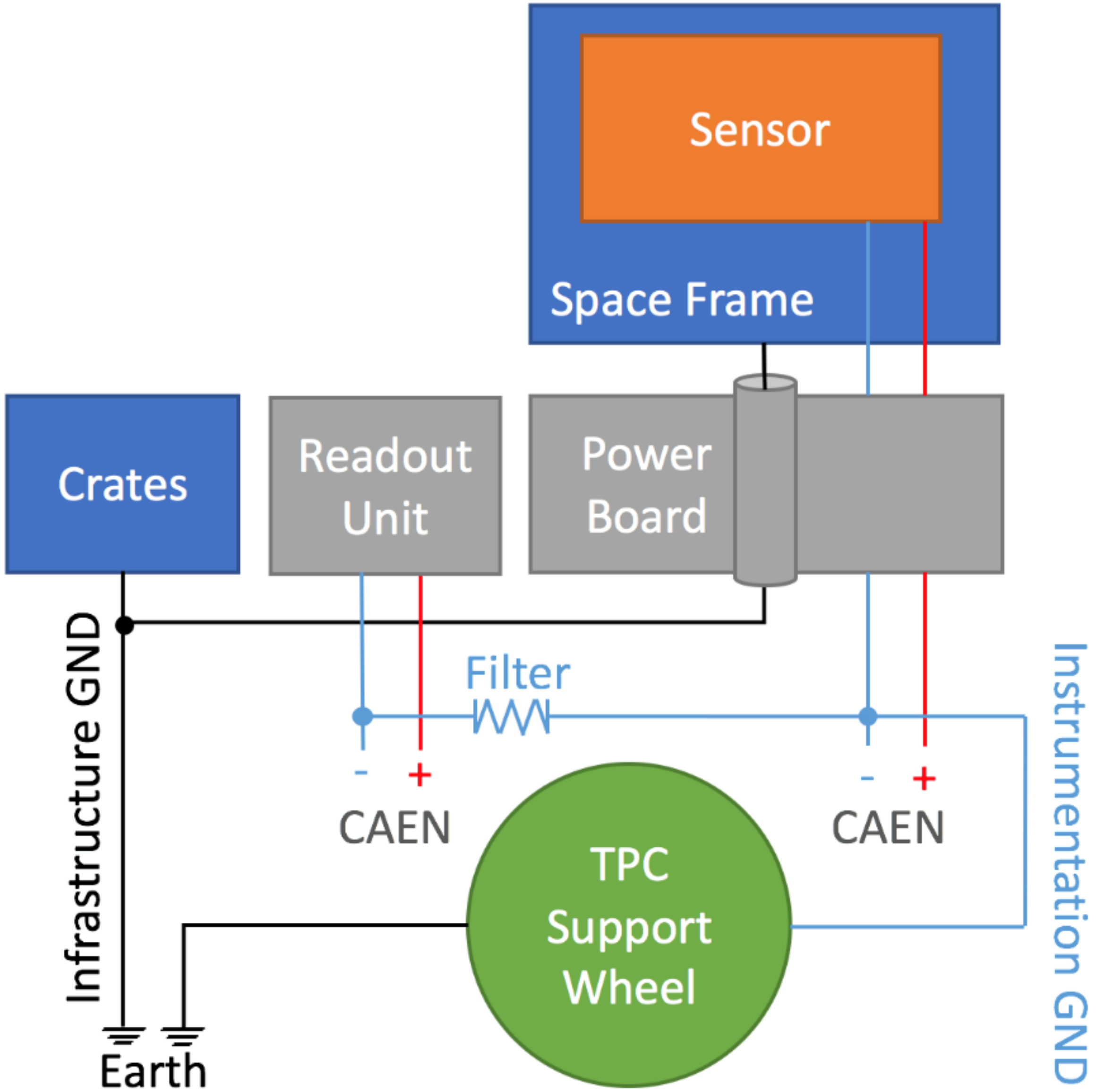
- 1 × CAN bus connection for backup slow control in case of optical link failure.
- 4 × I^2C bus for controlling the Power Board.
- 2 × High speed lanes for future implementation of busy/sync system across the RUs.
- 1 × USB 3.0 port for table-top and test-beam measurements and debugging.
- 1 × JTAG interface for table-top FPGA programming and debugging.

Operating conditions

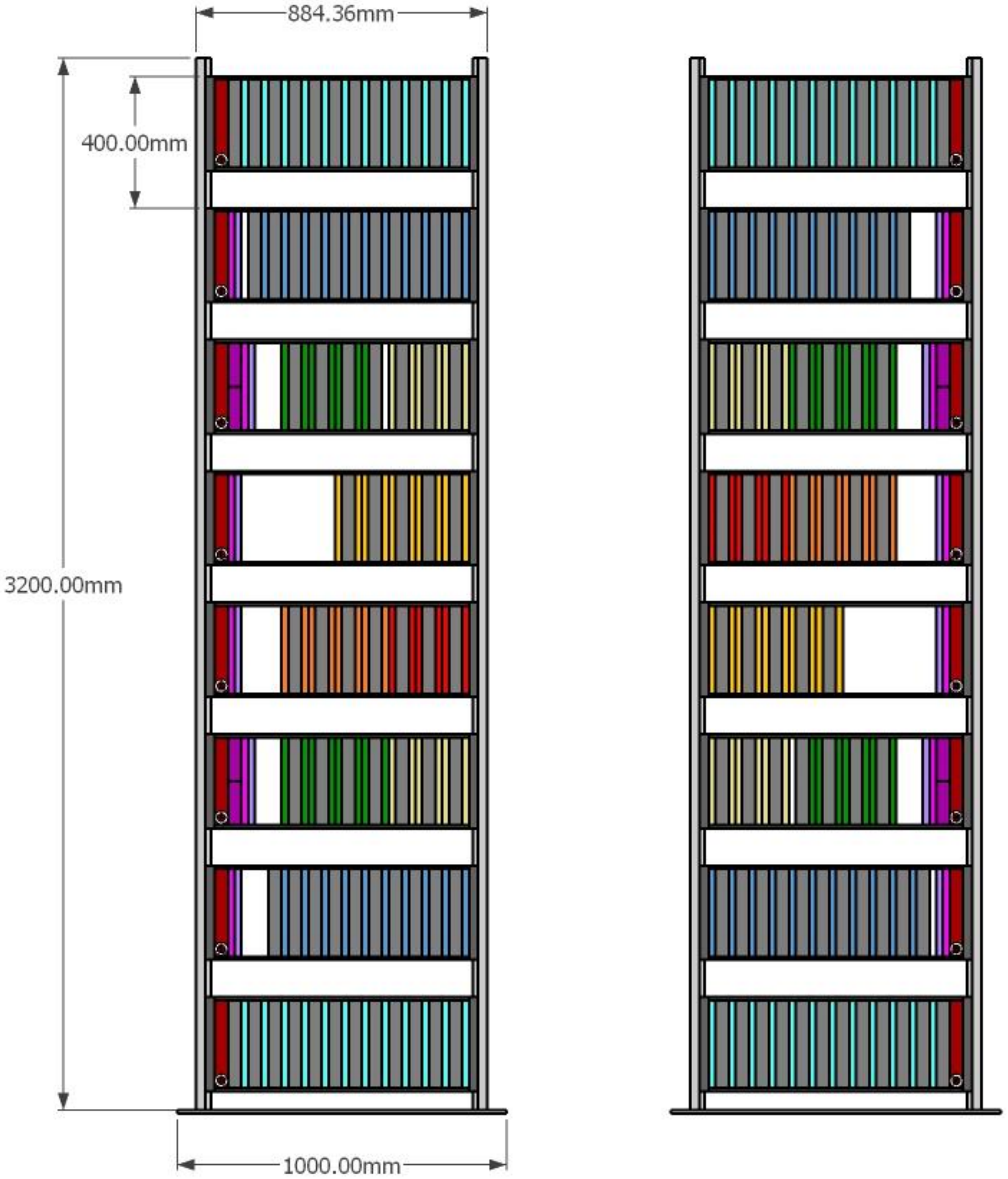
- 0.5T magnetic field
- 10 kRad TID, 1 KHz cm^{-2} high energy ionizing particle flux.

System Integration

Integration – Grounding scheme



Integration – RU and PB layout in crates, 16 Crates in total, 3.2 m high and 0.9 m wide

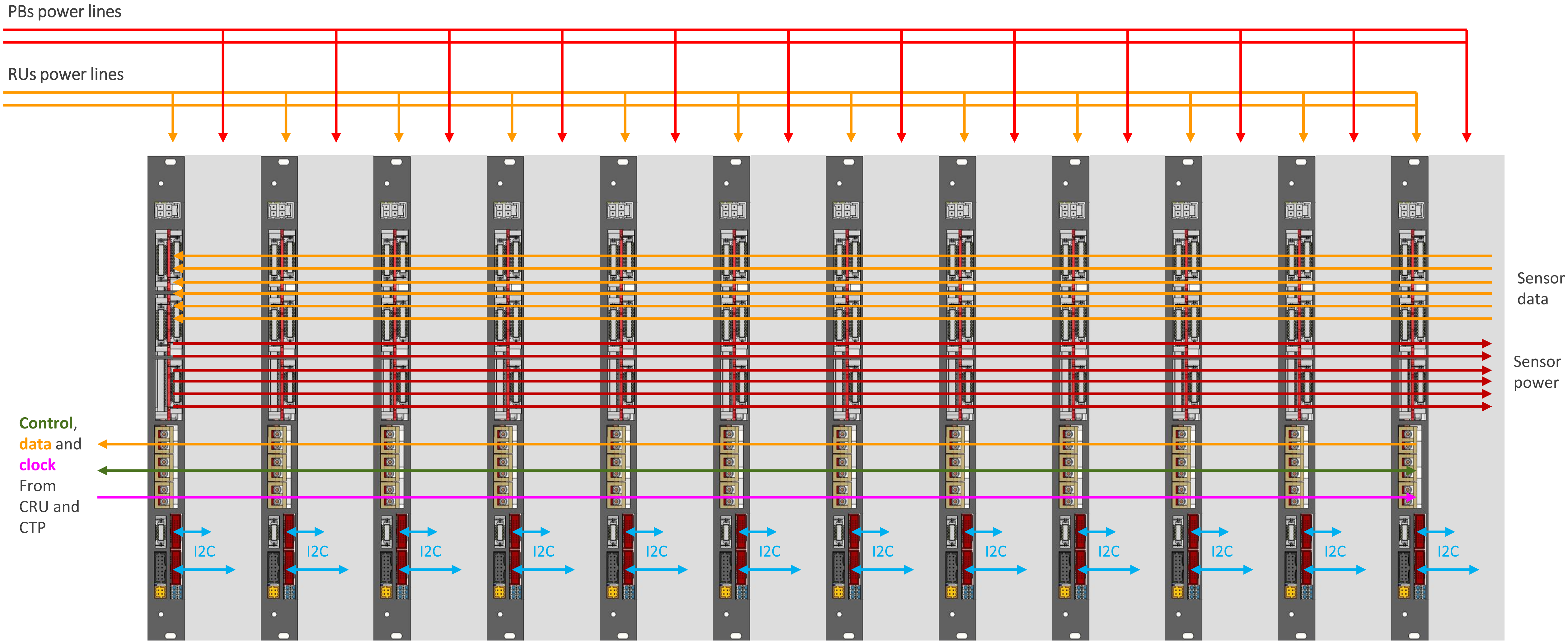


- Layer 0 RUs
- Layer 1 RUs
- Layer 2 RUs
- Layer 3 RUs
- Layer 4 RUs
- Layer 5 RUs
- Layer 6 RUs
- Power Boards (2PU each)
- Trigger splitters
- Busy Units
- Bias / CAN Bus breackout

In this drawing:

- RUs are **6U VME** board (actual PCB **233 mm** tall, front panel **266 mm** tall and **20 mm** wide).
- PUs are grouped by two into Power Boards, fitting TWO TIMES the volume of a RU 6U module.
- RU boards pitch is **4×HP** (4×5.08mm = **20.32mm**), the standard VME bus.
- Crates are **39** modules wide: total rack width about **88 cm.**
- Total height of a rack is 320 cm.

Integration – Crate connections overview

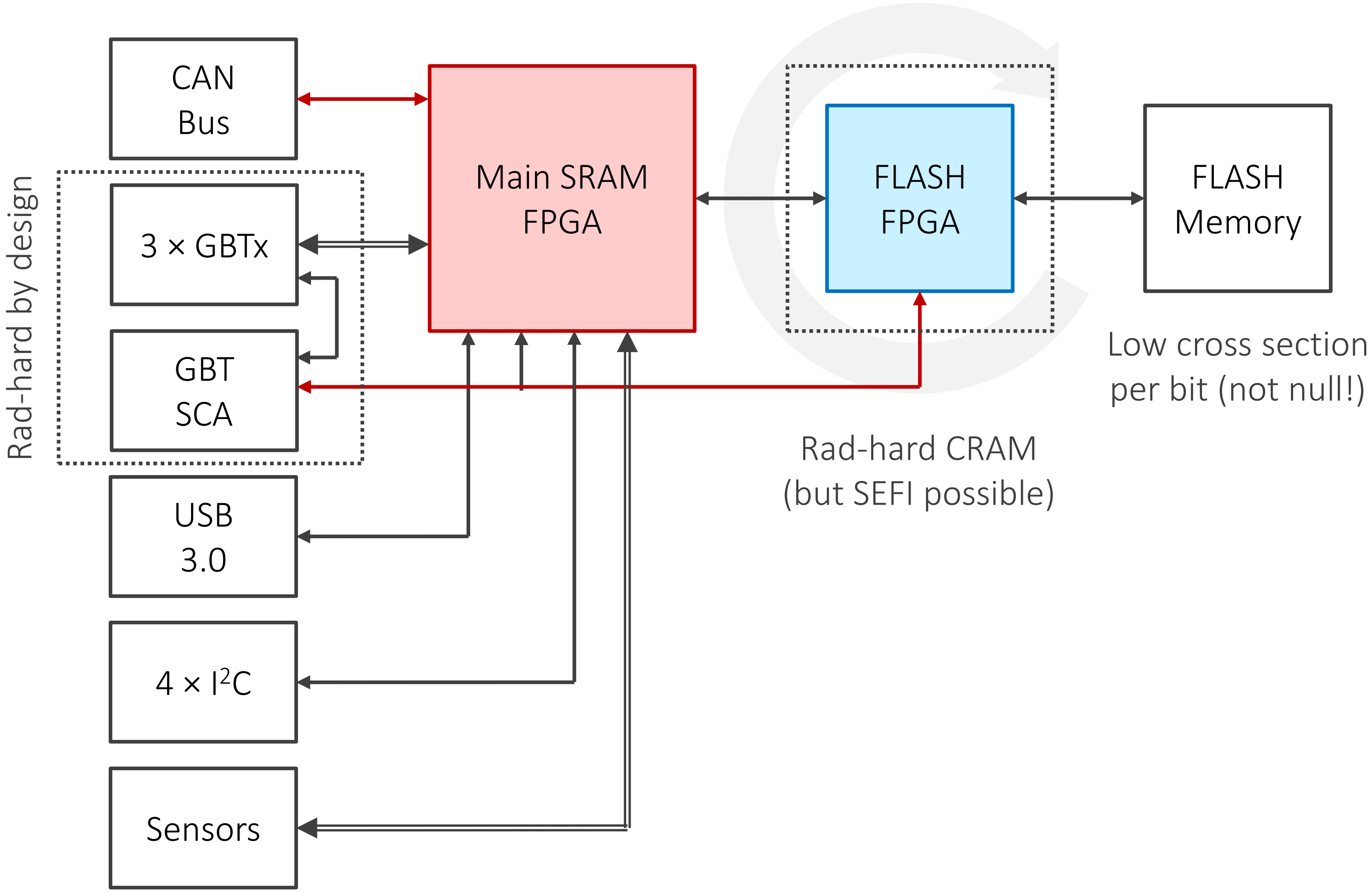


Missing for clarity bias lines and CAN bus lines. Light grey spaces represent power boards.

Design details

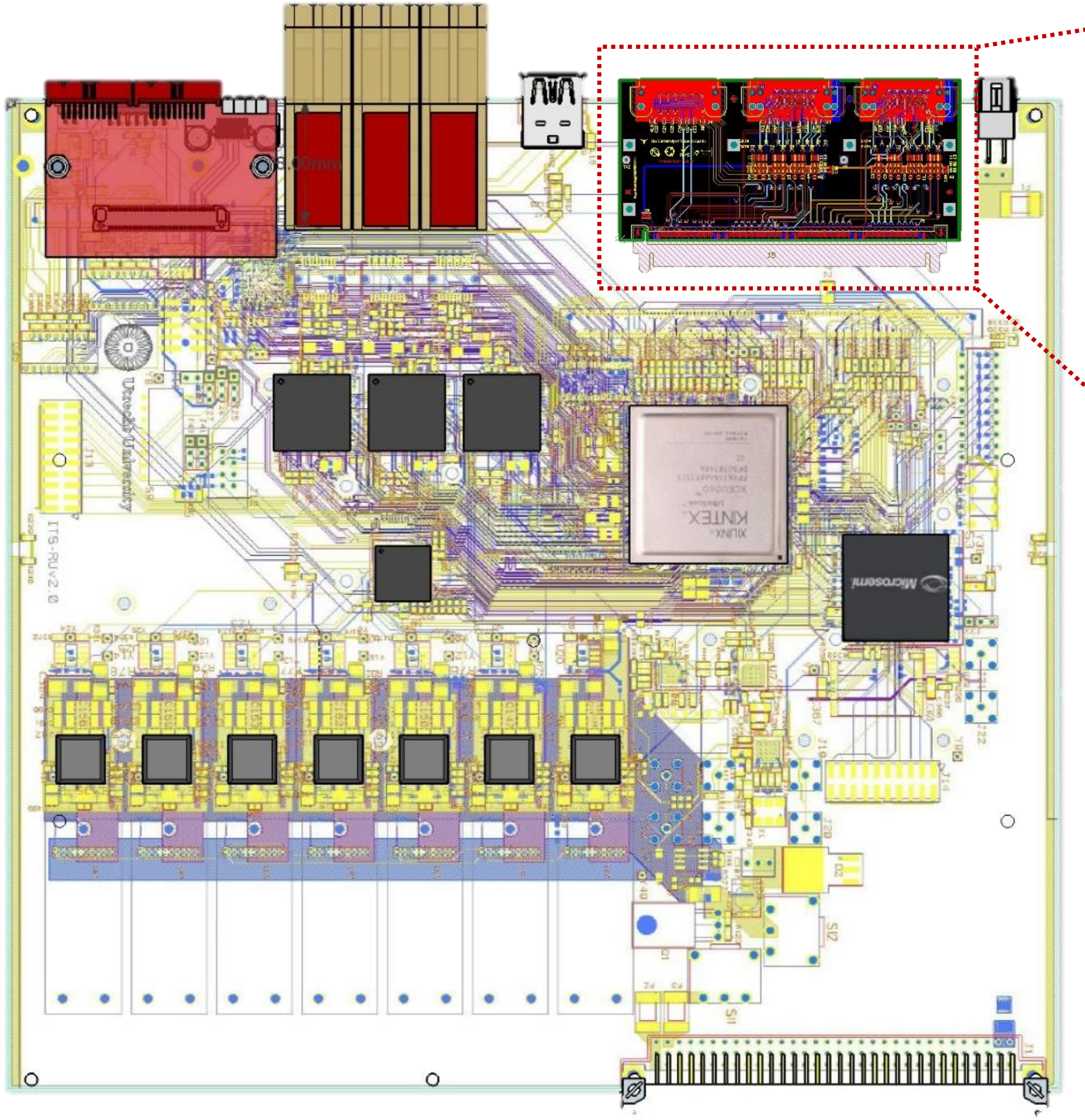
Design – Overview

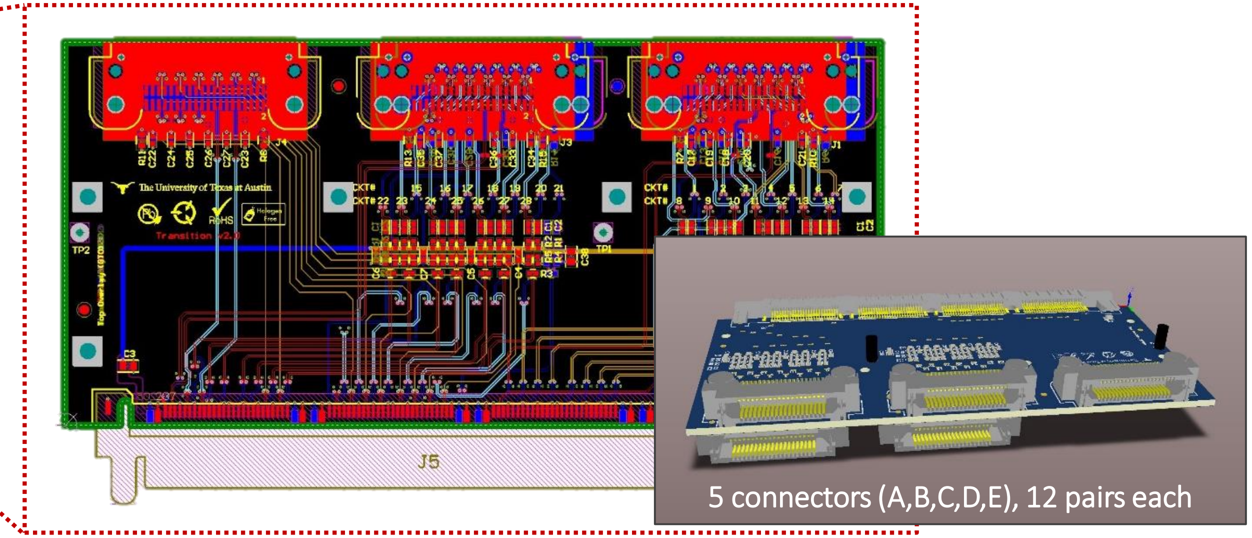
- Main FPGA (SRAM based) devoted to sensor management and data transfer.
- Secondary FPGA (FLASH) used to scrub the main one (on board FLASH memory with golden copy).
- GBT SCA chip used to monitor the board and communicate with both FPGAs.

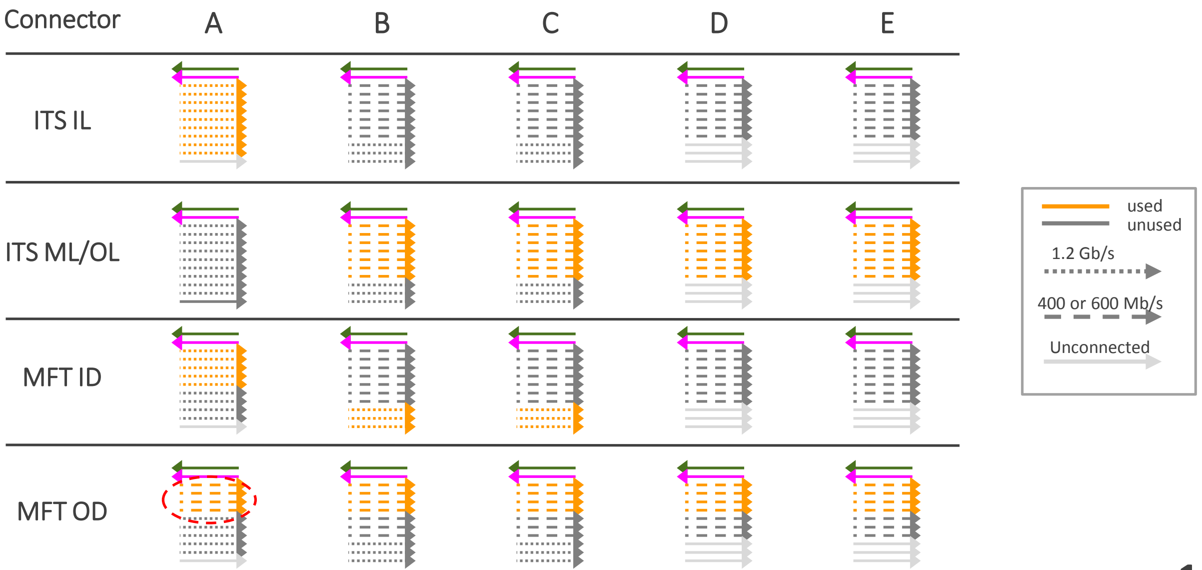


Design – Compatibility with MFT

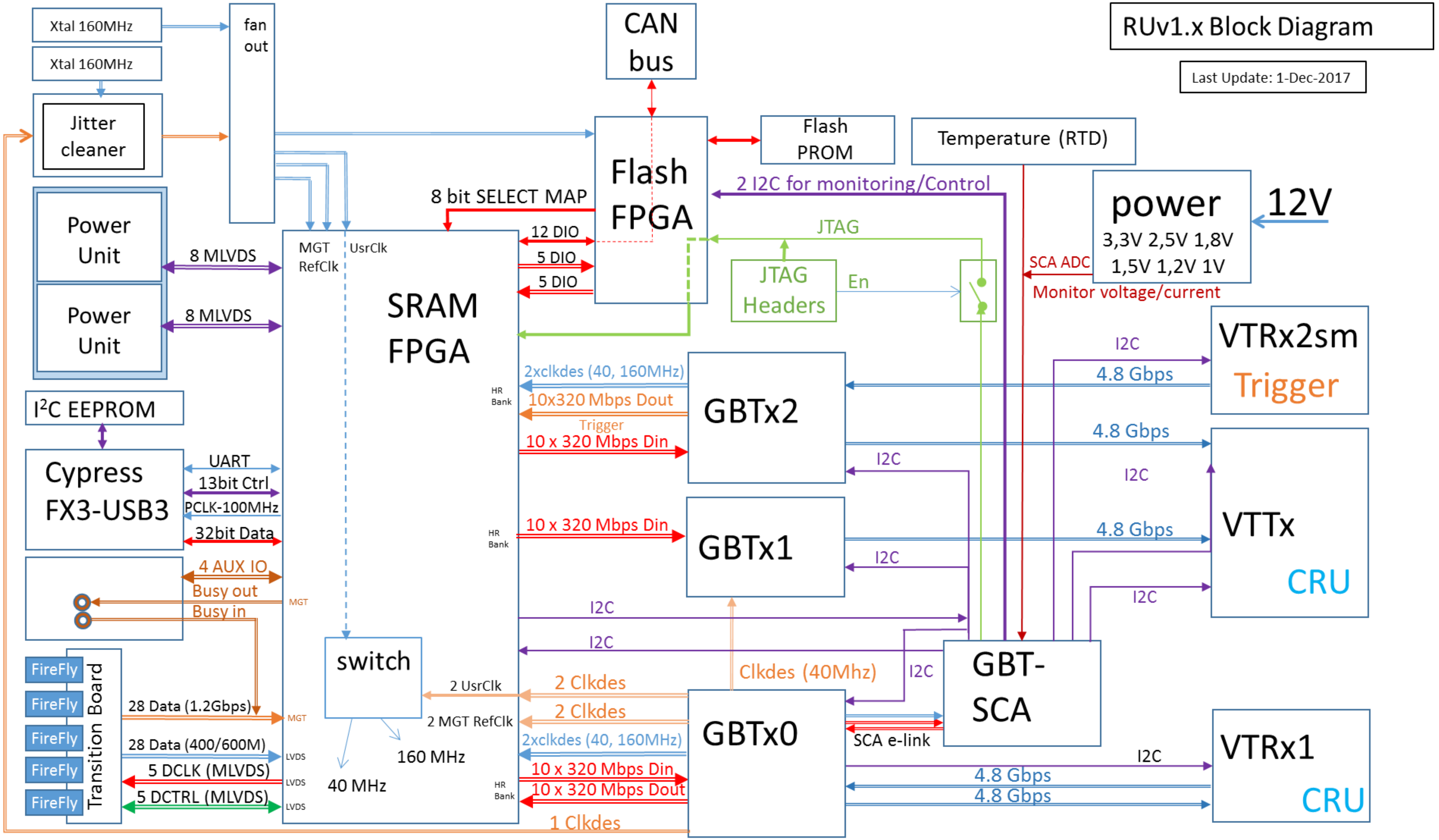
- The RU must comply with MFT specifications, which require using 25 GTX lanes for reading the sensors. To solve the routing, a changeable mezzanine card solution (**Transition Board**) has been adopted.



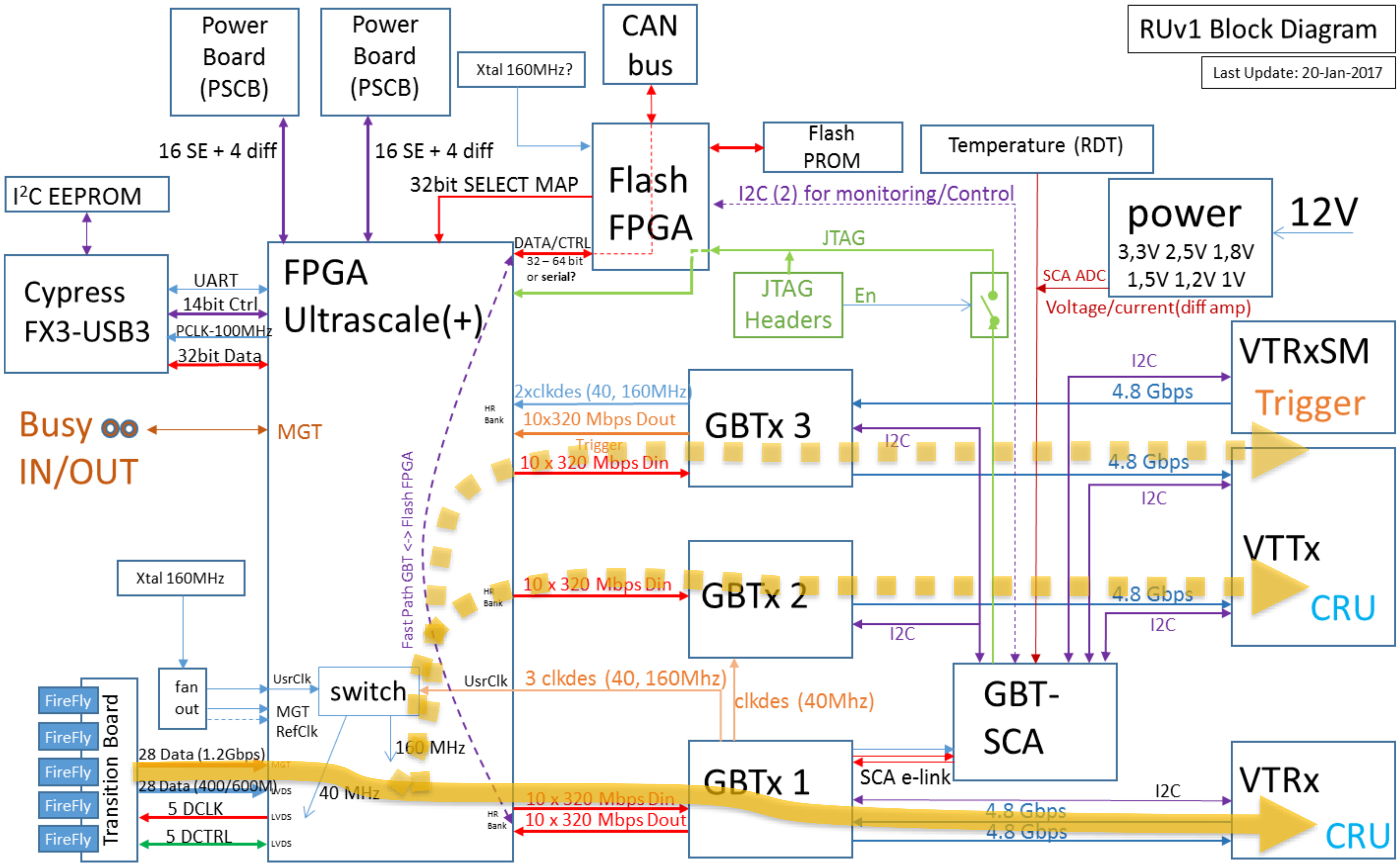




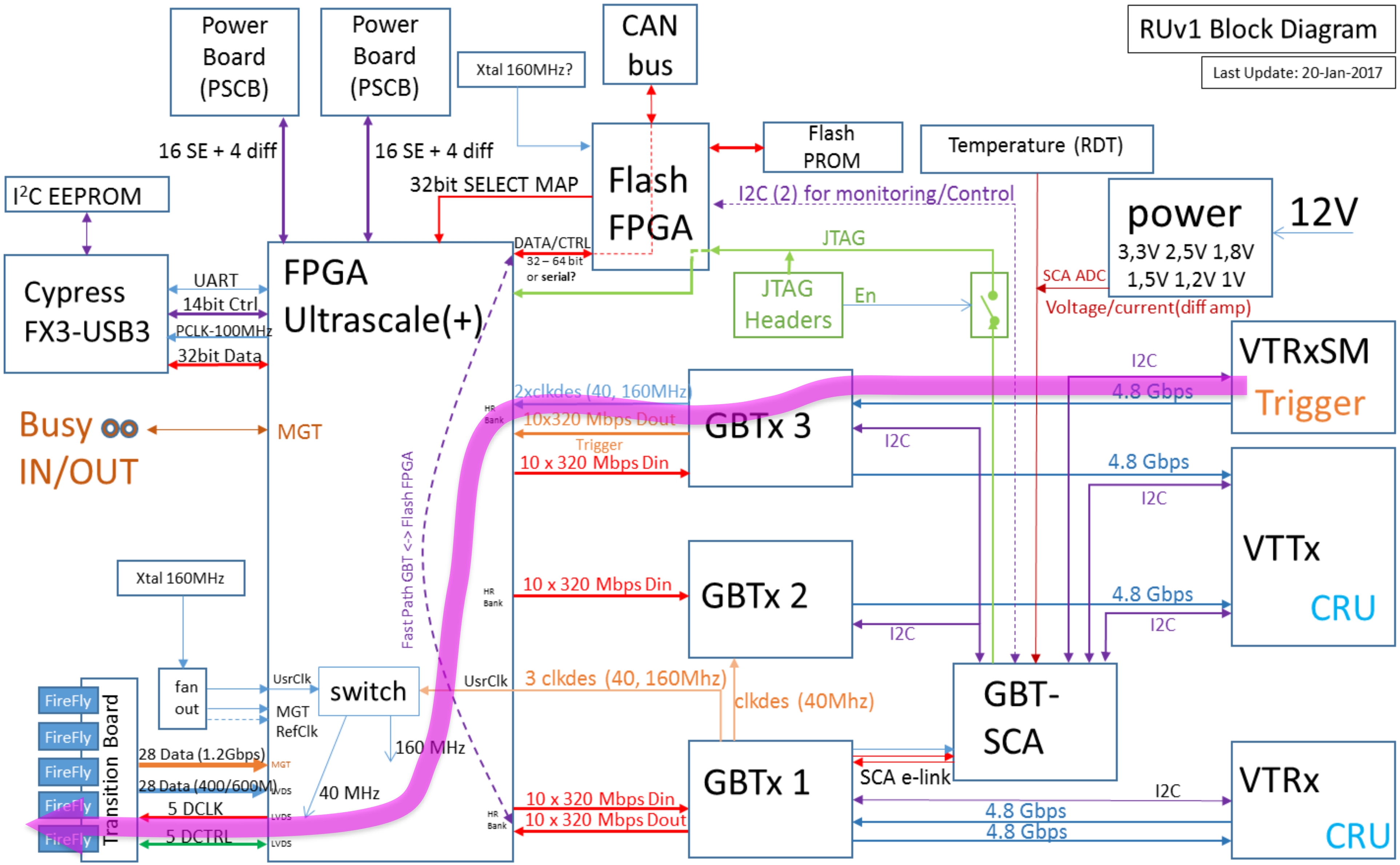
Design – Block diagram



Design – Block diagram sensor data path

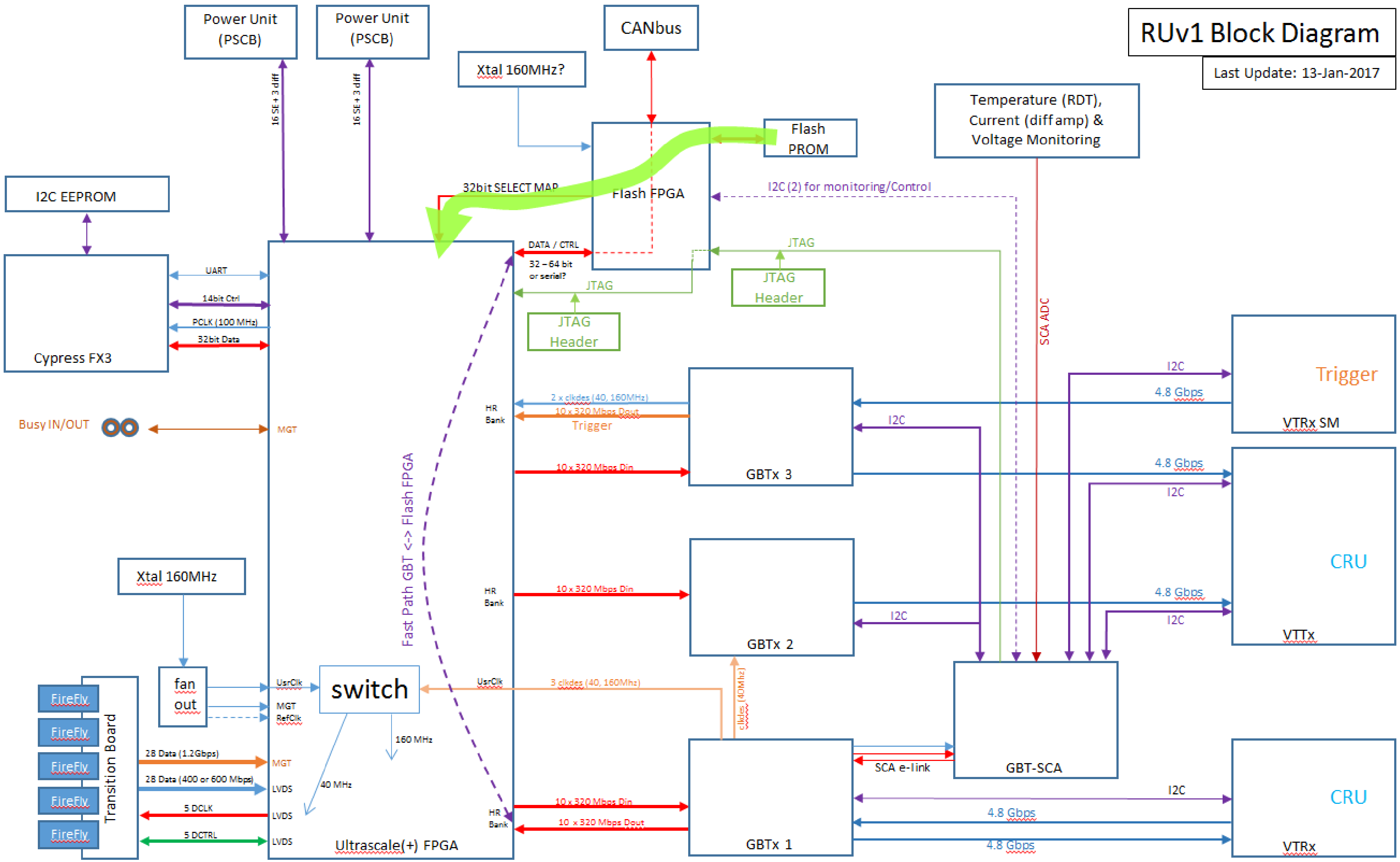


Design – Block diagram trigger path



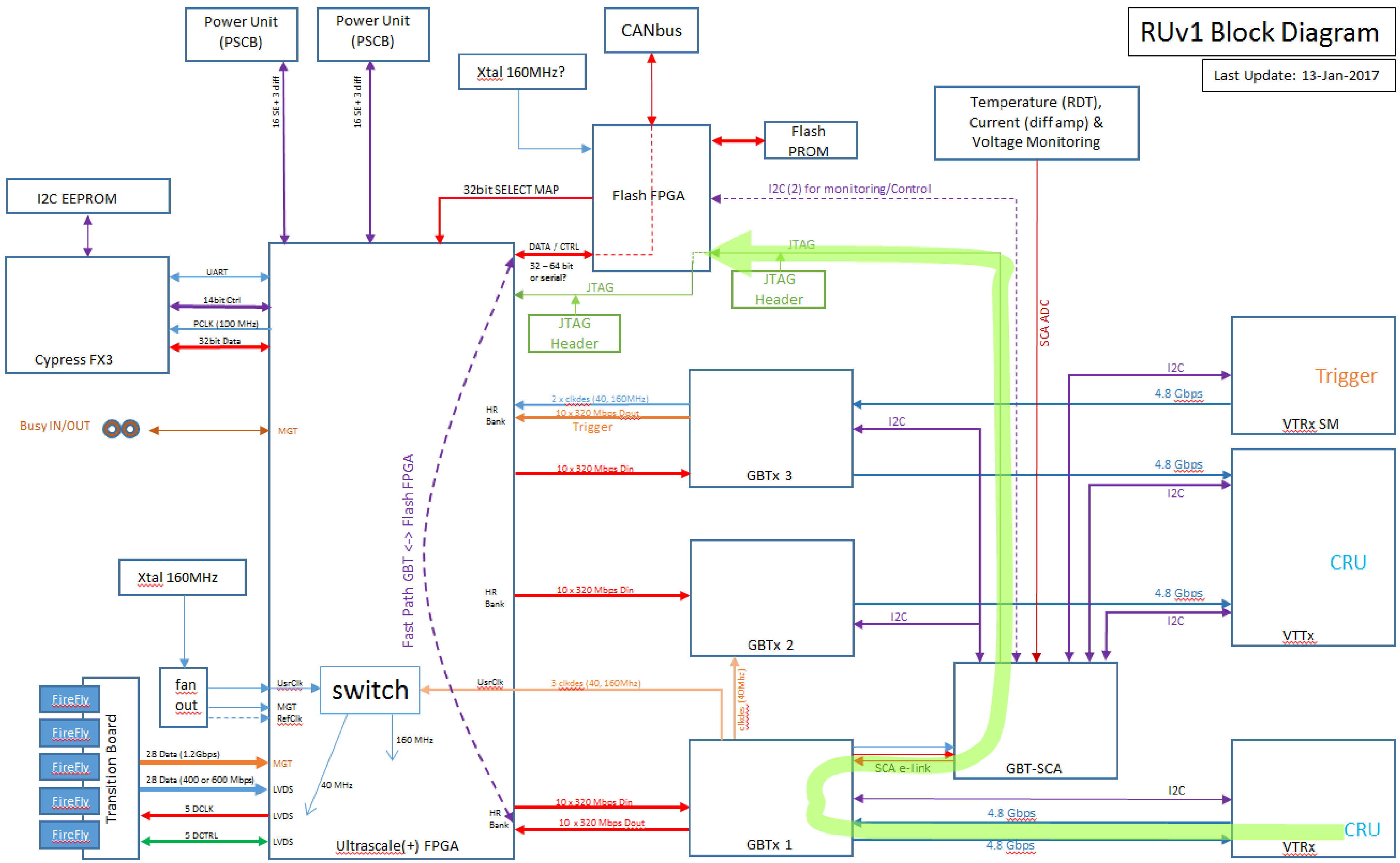
Design – Block diagram: SRAM FPGA configuration and scrubbing

Flash Prom=>PA3=>US(+)select map



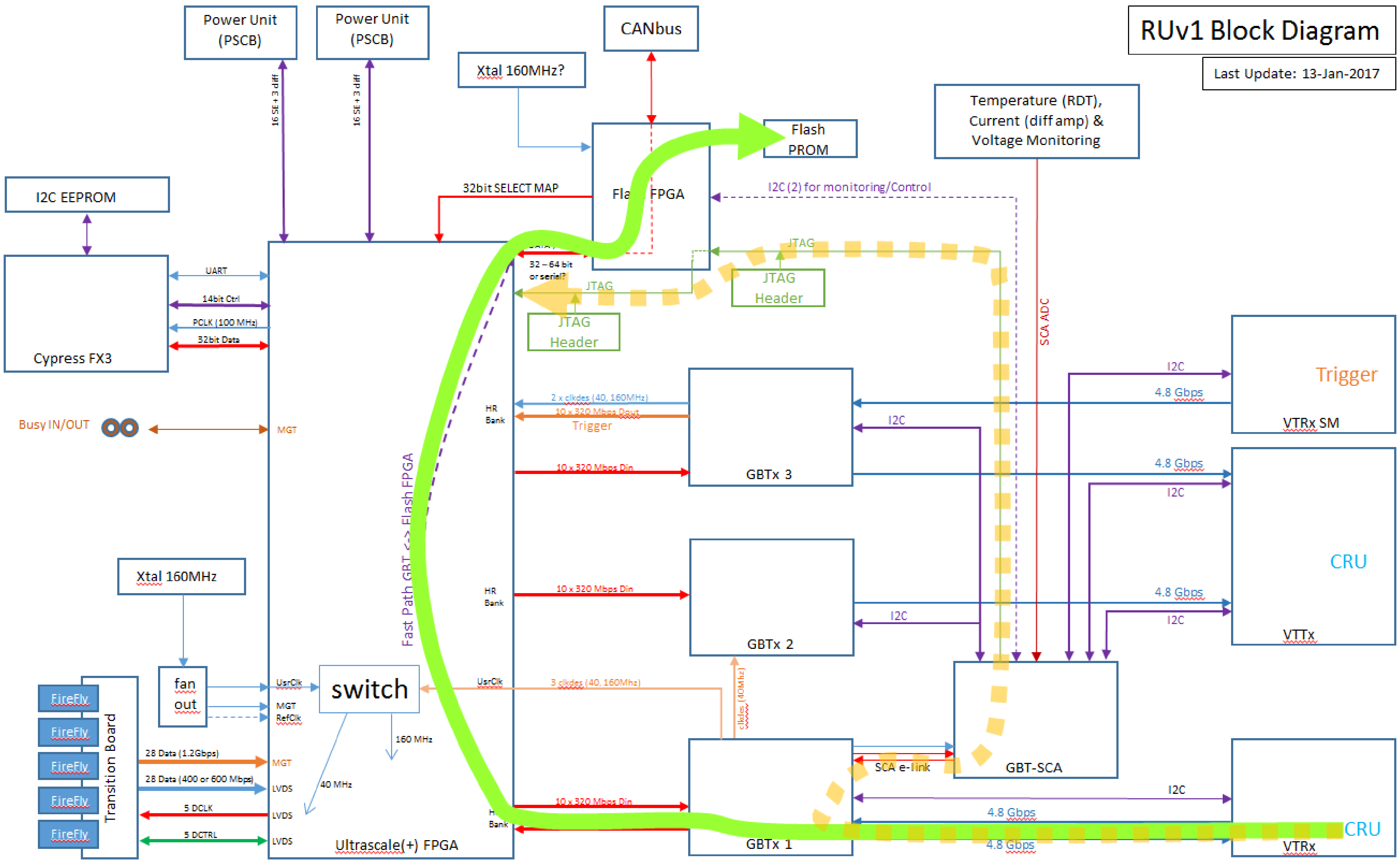
Design – Block diagram: FLASH FPGA programming

CRU=>GBT=>SCA=>PA3 JTAG



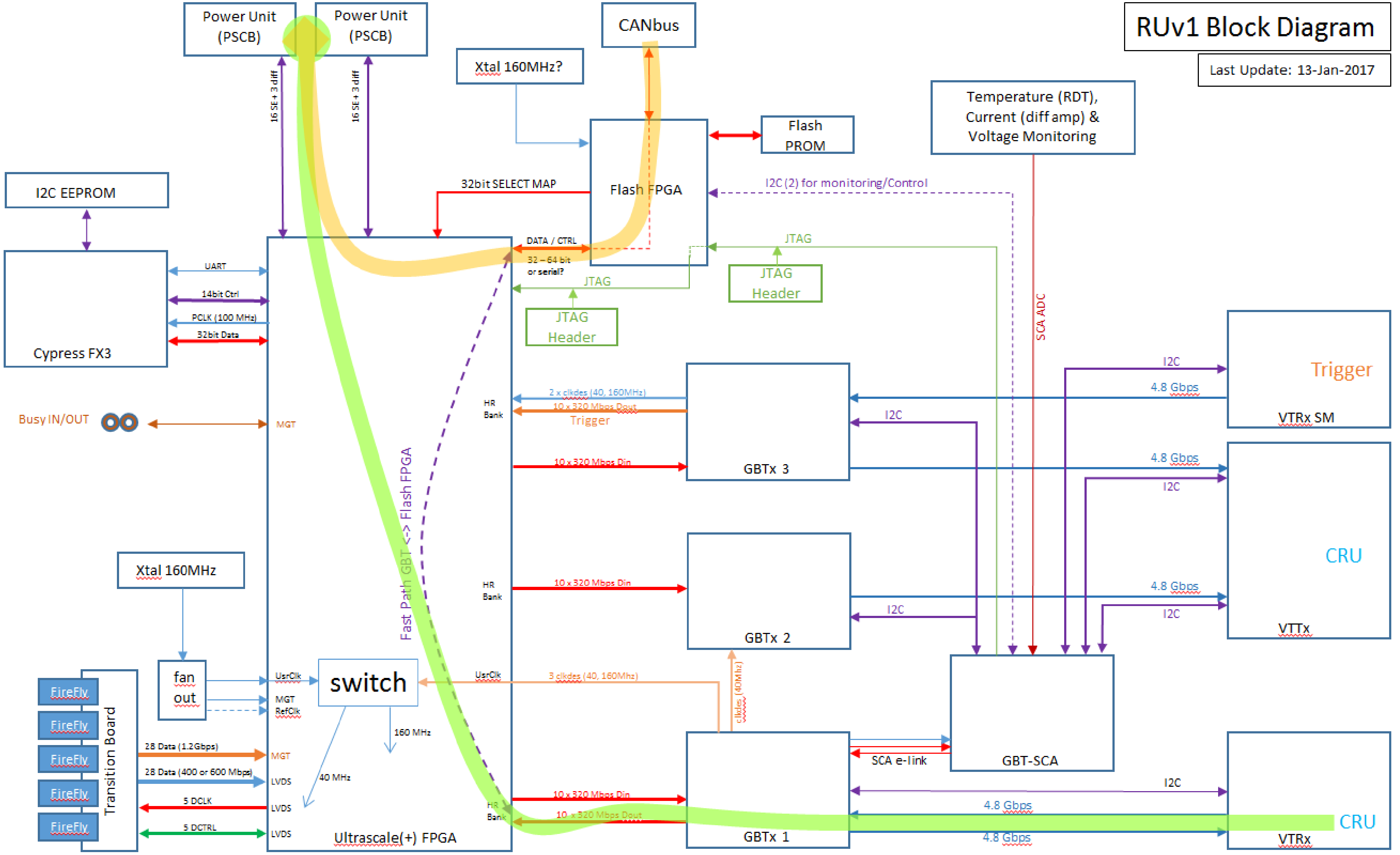
Design – Block diagram: FLASH PROM programming

CRU=>GBT=>US(+)=>PA3=>Flash Prom, (re-)configure US(+) via jtag: CRU=>GBT=>SCA=>US(+) JTAG



Design – Block diagram: Power Board(s) control path

- Main: CRU=>GBT=>US(+)=>Power Board (2*16SE+2*I2C)
- Alternative: CAN=>PA3=>US(+)=>Power Board (2*16SE+2*I2C)



Components selection

Components selection – FPGA general considerations

FPGA choice main reasons

- availability of high speed tranceivers to receive Alpide data
- enough resources to process up to 28 sensor data stream in parallel
- Xilinx device chosen (SRAM based => requires TMR & scrubbing)

Device	CRAM FIT/Mbit	Std. FF FIT/MFF
Kintex7 (used on RUv0)	1	1
UltraScale (US)	/3	/2
UltraScale+ (US+)	/50	/20

- One of the main reason is the pin-to-pin compatibility between various device of the Ultra Scale (**US**, 20nm) and Ultra Scale Plus (**US+**, 16nm FinFet), which allow to upgrade to a more powerful and more rad tolerant technology
  - Anyway, first irradiation of US+ devices did show latch-ups, therefore ruled out
- Smaller cross-section for transients in both fabric logic and transceiver respect to the Microsemi devices also an important factor.

Evaluated alternatives

- Microsemi (flash based, no scrubbing needed)
  - IGLOO2 (only TMR needed)
  - RTG4 (no TMR needed, RHDB=Radiation Hard By Design)

Components selection – IOs and Transceivers in baseline device

KU060 in Package FFVA1156 chosen to maximize compatibility with other devices of the same family, in particular the higher specs KU095

Table 4: **Kintex UltraScale Device-Package Combinations and Maximum I/Os**

Package [1][2][3]	Package Dimensions (mm)	KU025 HR, HP GTH	KU035 HR, HP GTH	KU040 HR, HP GTH	KU060 HR, HP GTH	KU085 HR, HP GTH	KU095 HR, HP GTH, GTY[4]	KU115 HR, HP GTH
SFVA784[5]	23x23		104, 364 8	104, 364 8				
FBVA676[5]	27x27		104, 208 16	104, 208 16				
FBVA900[5]	31x31		104, 364 16	104, 364 16				
FFVA1156	35x35	104, 208 12	104, 416 16	104, 416 20	104, 416 28		52, 468 20, 8	
FFVA1517	40x40				104, 520 32			
FLVA1517	40x40					104, 520 48		104, 520 48
FFVC1517	40x40						52, 468 20, 20	
FLVD1517	40x40							104, 234 64

KU060 baseline device

Components selection – FLASH FPGA selection

Scrubbing FPGA must operate reliable

⇒ Flash based FPGA as configuration is SEU immune

Microsemi PA3 series has good heritage

⇒ Preferred above new IGLOO2 due to TID issues

COTS version (same die/process) of space grade part

⇒ A3PE600L (3000L) corresponds to RT3PE600L (3000L)

Requirments:

- $>10^3$ IOs, 3 banks (1,5/2,5/3,3V)
- resources A3PE600L seems enough for scrubbing

Baseline: A3PE600L-FG484X53 upgradeble to A3PE3000L

As alternative, A3PEx is also pincompatible with A3PExL

Part	Price ($)
A3PE600L	200
A3PE3000L	310
A3PE600	60
A3PE1500	140
A3PE3000	280

PA3 FPGA function	#pins	IO standard
2 × I2C	4	LVCMOS1,5V
US(+) Select-map	40	LVCMOS1,5V
Flash interface	20	LVCMOS3,3V
US(+) comm.	35	LVCMOS/LVDS(2,5V)
Can Interface	4	LVCMOS3,3
Total IOs	103	

ProASIC3/EL Low Power Devices	A3PE600L		A3PE3000L	
ARM Cortex-M1 Devices			M1A3PE3000L	
Package	Single-Ended I/O[2]	Differential I/O Pairs	Single-Ended I/O[2]	Differential I/O Pairs
VQ100	–	–	–	–
PQ208	–	–	–	–
FG144	–	–	–	–
FG256	–	–	–	–
FG484	270	135	341	168
FG896	–	–	620	310

Components selection – power supplies general remarks

- How is RU powered
  - Voltage: 8 V
  - Power comes from the front or from the back
- (DC/DC) regulators need to operate in 0,5T
- Necessary to measure currents on each power rail
- US(+) desire power-on/off sequence

Components selections – selected power supplies by voltage rail

Maximum current drain has been calculated for each power rail, and adequate Dc-DC power supply selected (details on the backup slides). Two types of DCDC will cover the RU requirements

3V3	PA3_Vpump	FX3_Vbat		$I_{TOTAL\ MAX}$ (mA)	
3.3	1	60		61	LMZ31503

2V5	PA3_LVDS	VTT+2*VTRx		$I_{TOTAL\ MAX}$ (mA)	
2.5	14	900		914	LMZ31503

1V8	US_V_{CCaux}	US_V_{CCADC}	US_$V_{MGTVCCAUX}$	$I_{TOTAL\ MAX}$ (mA)	
1.8	1581	19		1600	LMZ31503

1V5	GB Tx +2 × Xx	SCA	PA3	$I_{TOTAL\ MAX}$ (mA)	
1.5	3046	64	336	3446	LMZ31506

1V2	US_V_{MGTx32}	FX3		$I_{TOTAL\ MAX}$ (mA)	
1.2	2400	200		2600	LMZ31503

V_{MGT}	V_{MGT}			$I_{TOTAL\ MAX}$ (mA)	
1 (US+ 0,9V)	2300			2300	LMZ31503

V_{CCINT}	V_{CCINT}			$I_{TOTAL\ MAX}$ (mA)	
0.95 (US+ 0.85V)	4200			4200	LMZ31506

Components selection – CAN interface

Both soft IP and hardware controller available for the CAN bus protocol

CAN controler	Type	Voltage	TID (krad)	Price
Atmel	AT7908E (CPU interface)	5V	300k	high
ESA greece	ETM ASIC (only inputs)	3,3	1M	5
COTS				
TI	TMS570 Hercules		Under NDA	
Microsemi	PA3 IP-core in fabric			IP
	SF2 + internal ECC CAN periperal			Free
Xilinx	Opencores whishbone CAN slave			Free

Selected controller: Opencores CAN slave on Xilinx

CAN transceiver	type	Voltage	TID(krad)	Price
Intersil	ISL72026/7/8SEH	3,3	75	$836
Cobham/ aeroflex	UT64CAN333x	3,3	100	high
TI	SN55HVD233-SP	3,3	50	Prelim
COTS				
TI	SN65HVD233M-EP		??	5,1

Selected Transceiver: SN65HVD233M-EP

Components selection – main ICs list and testing status

Brand	Part (main)	type	#	Max TID (krad)	Test
Xilinx	XCKU060-1FFVA1156C	FPGA	1	K7 TID OK, SEU by tmr & scrubbing	OK
Microsemi	A3PE600L-FG484MX53	FPGA	1	40 [1] (recent TID issue?)	OK
Samsung	SN74CB3T16210DGG	Flash mem.	2	70 [2]	OK
Cypress	CYUSB3014-BZXC	FX3 USB3	1	Not qualified. Unused in experiment	Ok
TI	LMZ31503RUQ	DC/DC	5/4	30 [3] (also mag. Field B>1T [7])	OK
	LMZ31506RUQ		2	Tested working up to 30 kRad	OK
	MIC29501	Lin. reg.	0/1	20 [3]	OK
Analog dev.	AD626AR	Diff-amp	7	45 [3]	OK
Silicon Labs	TBD	Jitter cleaner		Not mandatory component	Test
TI	CDCLVD1212	2:12 LVDS buf	1	1130 [4]	OK
On-semi	NB7L14	1:4 LVPECL		>20 [5]	OK
IQD	CFPS-73 (tr/tf=6ns)	Crystal	1	50 [6]	OK
GBT	GBTx	SERDES	3	OK	OK
	SCA	IO	1	OK	OK
	VTRx	E/O convers.	2	OK	OK
	VTTx	E/O convers.	1	OK	OK

Components – glue logic list and testing status

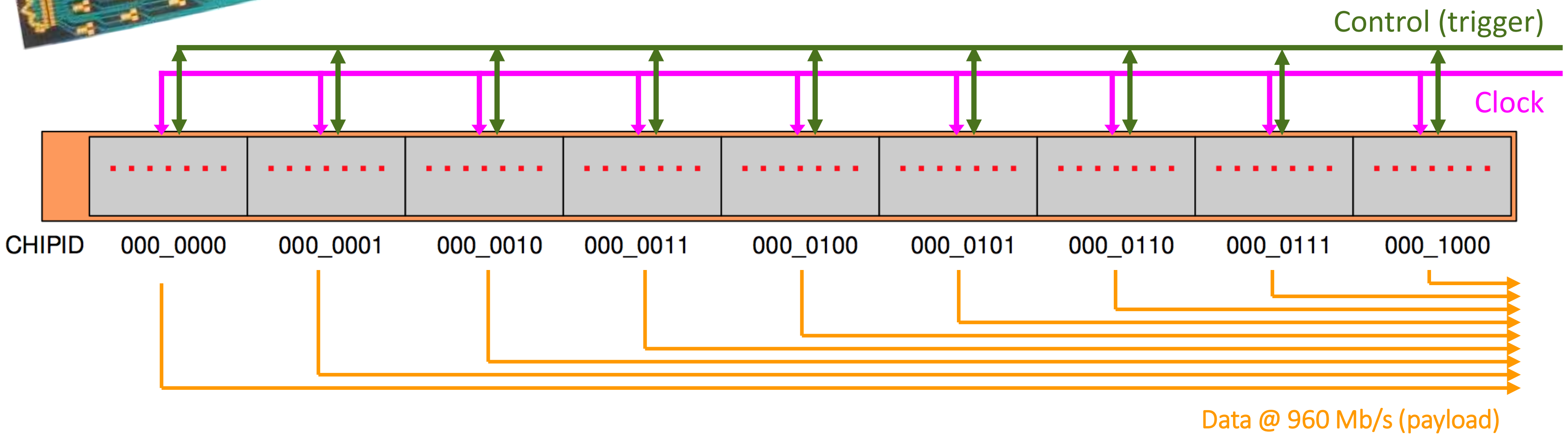
Brand	Part (Glue logic)	type	#	Max TID (krad)	Test
TI	SN65HVD233MDREP	Can-trans	1	Seems like space part: SN65HVD233-SP	Planned
	DS90LV047ATM	LVDS driver	1	70 [8]	OK
	DS90LV048ATM	LVDS receiver	1	70 [8]	OK

- http://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/rt-proasic3
- https://escies.org/download/webDocumentFile?id=63077
- https://twiki.cern.ch/twiki/pub/ALICE/BASE20testing/2016_06_08_TID_testbeam_report_lg.docx
- http://indico.cern.ch/event/299180/contributions/1659565
- https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20140017803.pdf
- https://edms.cern.ch/document/1327311/1
- ITS WP10 EDR: RUv0 presentation, Krzysztof Marek Sielewicz
- Gianluca Di Mattia, thesis, Univ. "La Sapienza" , 2003, Roma (TulliosPreferredPartList)

Backup

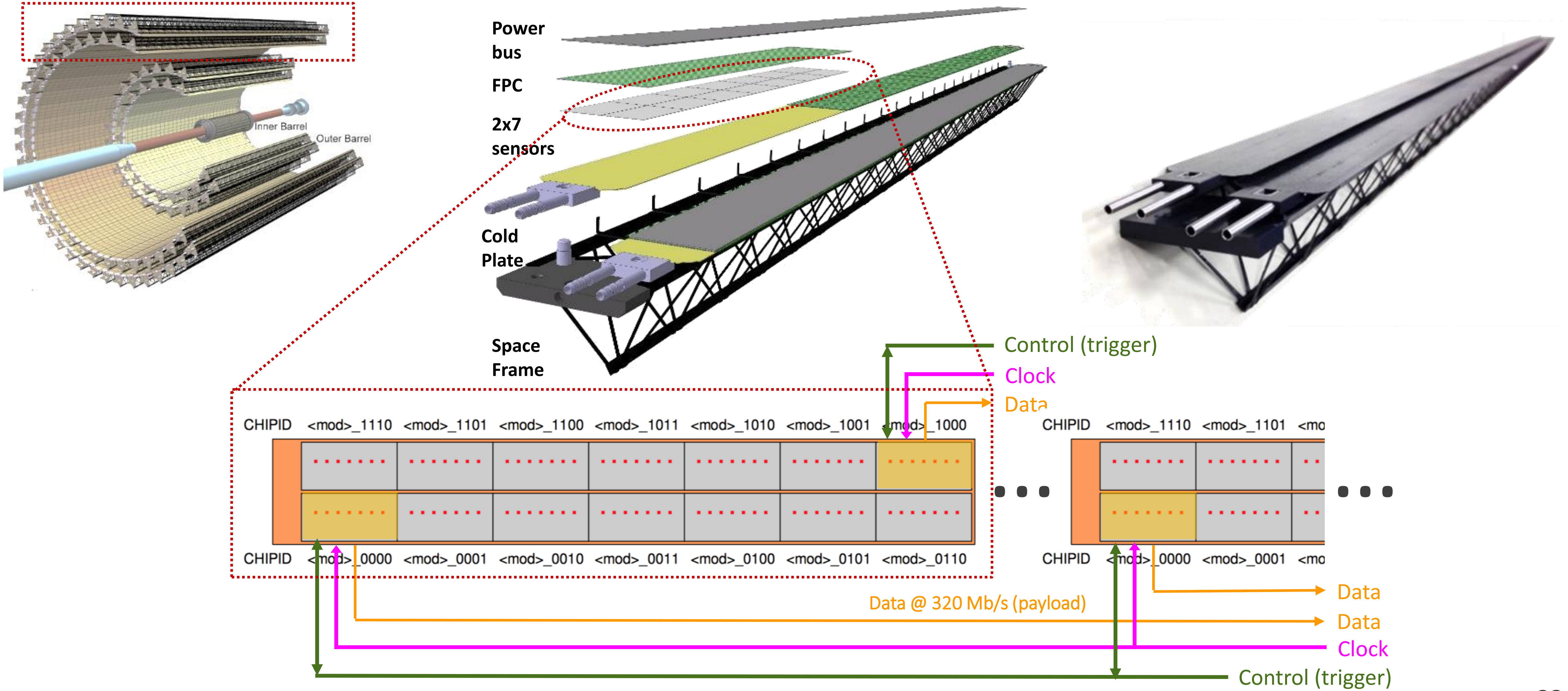
Sensors – inner layers staves connections

Inner layers stave, 9 master sensors (each read/drives its own control and data lines) to maximize.available bandwidth (960 Mb/s payload)’

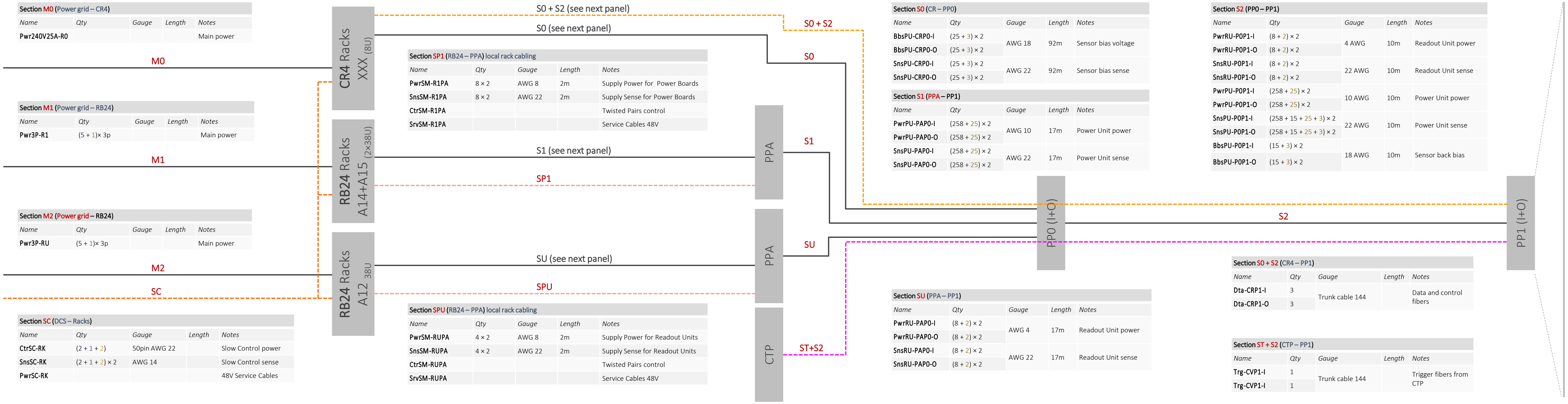


Sensors – middle and outer layer staves and modules connections

Mid/Outer layers module: 2 symmetric group of 1 master and 6 slave chips. Only the master accesses the data/control lines toward/from the outer world. Bandwith (per master) is 320 Mb/s payload.



Integration – Overall connections



Section M0 (Power grid – CR4)				
Name	Qty	Gauge	Length	Notes
Pwr240V25A-R0				Main power

Section M1 (Power grid – RB24)				
Name	Qty	Gauge	Length	Notes
Pwr3P-R1	(5 + 1)× 3p			Main power

Section M2 (Power grid – RB24)				
Name	Qty	Gauge	Length	Notes
Pwr3P-RU	(5 + 1)× 3p			Main power

Section SC (DCS – Racks)				
Name	Qty	Gauge	Length	Notes
CtrSC-RK	(2 + 1 + 2)	50pin AWG 22		Slow Control power
SnsSC-RK	(2 + 1 + 2) × 2	AWG 14		Slow Control sense
PwrSC-RK				48V Service Cables

Section SP1 (RB24 – PPA) local rack cabling				
Name	Qty	Gauge	Length	Notes
PwrSM-R1PA	8 × 2	AWG 8	2m	Supply Power for Power Boards
SnsSM-R1PA	8 × 2	AWG 22	2m	Supply Sense for Power Boards
CtrSM-R1PA				Twisted Pairs control
SrvSM-R1PA				Service Cables 48V

Section SPU (RB24 – PPA) local rack cabling				
Name	Qty	Gauge	Length	Notes
PwrSM-RUPA	4 × 2	AWG 8	2m	Supply Power for Readout Units
SnsSM-RUPA	4 × 2	AWG 22	2m	Supply Sense for Readout Units
CtrSM-RUPA				Twisted Pairs control
SrvSM-RUPA				Service Cables 48V

Section S0 (CR – PP0)				
Name	Qty	Gauge	Length	Notes
BbsPU-CRP0-I	(25 + 3) × 2	AWG 18	92m	Sensor bias voltage
BbsPU-CRP0-O	(25 + 3) × 2			
SnsPU-CRP0-I	(25 + 3) × 2	AWG 22	92m	Sensor bias sense
SnsPU-CRP0-O	(25 + 3) × 2			

Section S1 (PPA – PP1)				
Name	Qty	Gauge	Length	Notes
PwrPU-PAP0-I	(258 + 25) × 2	AWG 10	17m	Power Unit power
PwrPU-PAP0-O	(258 + 25) × 2			
SnsPU-PAP0-I	(258 + 25) × 2	AWG 22	17m	Power Unit sense
SnsPU-PAP0-O	(258 + 25) × 2			

Section SU (PPA – PP1)				
Name	Qty	Gauge	Length	Notes
PwrRU-PAP0-I	(8 + 2) × 2	AWG 4	17m	Readout Unit power
PwrRU-PAP0-O	(8 + 2) × 2			
SnsRU-PAP0-I	(8 + 2) × 2	AWG 22	17m	Readout Unit sense
SnsRU-PAP0-O	(8 + 2) × 2			

Section S2 (PP0 – PP1)				
Name	Qty	Gauge	Length	Notes
PwrRU-P0P1-I	(8 + 2) × 2	4 AWG	10m	Readout Unit power
PwrRU-P0P1-O	(8 + 2) × 2			
SnsRU-P0P1-I	(8 + 2) × 2	22 AWG	10m	Readout Unit sense
SnsRU-P0P1-O	(8 + 2) × 2			
PwrPU-P0P1-I	(258 + 25) × 2	10 AWG	10m	Power Unit power
PwrPU-P0P1-O	(258 + 25) × 2			
SnsPU-P0P1-I	(258 + 15 + 25 + 3) × 2	22 AWG	10m	Power Unit sense
SnsPU-P0P1-O	(258 + 15 + 25 + 3) × 2			
BbsPU-P0P1-I	(15 + 3) × 2	18 AWG	10m	Sensor back bias
BbsPU-P0P1-O	(15 + 3) × 2			

Section S0 + S2 (CR4 – PP1)				
Name	Qty	Gauge	Length	Notes
Dta-CRP1-I	3	Trunk cable 144		Data and control fibers
Dta-CRP1-O	3			

Section ST + S2 (CTP – PP1)				
Name	Qty	Gauge	Length	Notes
Trg-CVP1-I	1	Trunk cable 144		Trigger fibers from CTP
Trg-CVP1-I	1