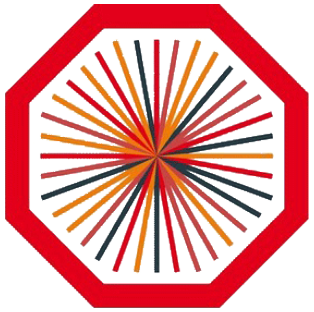
ALICE

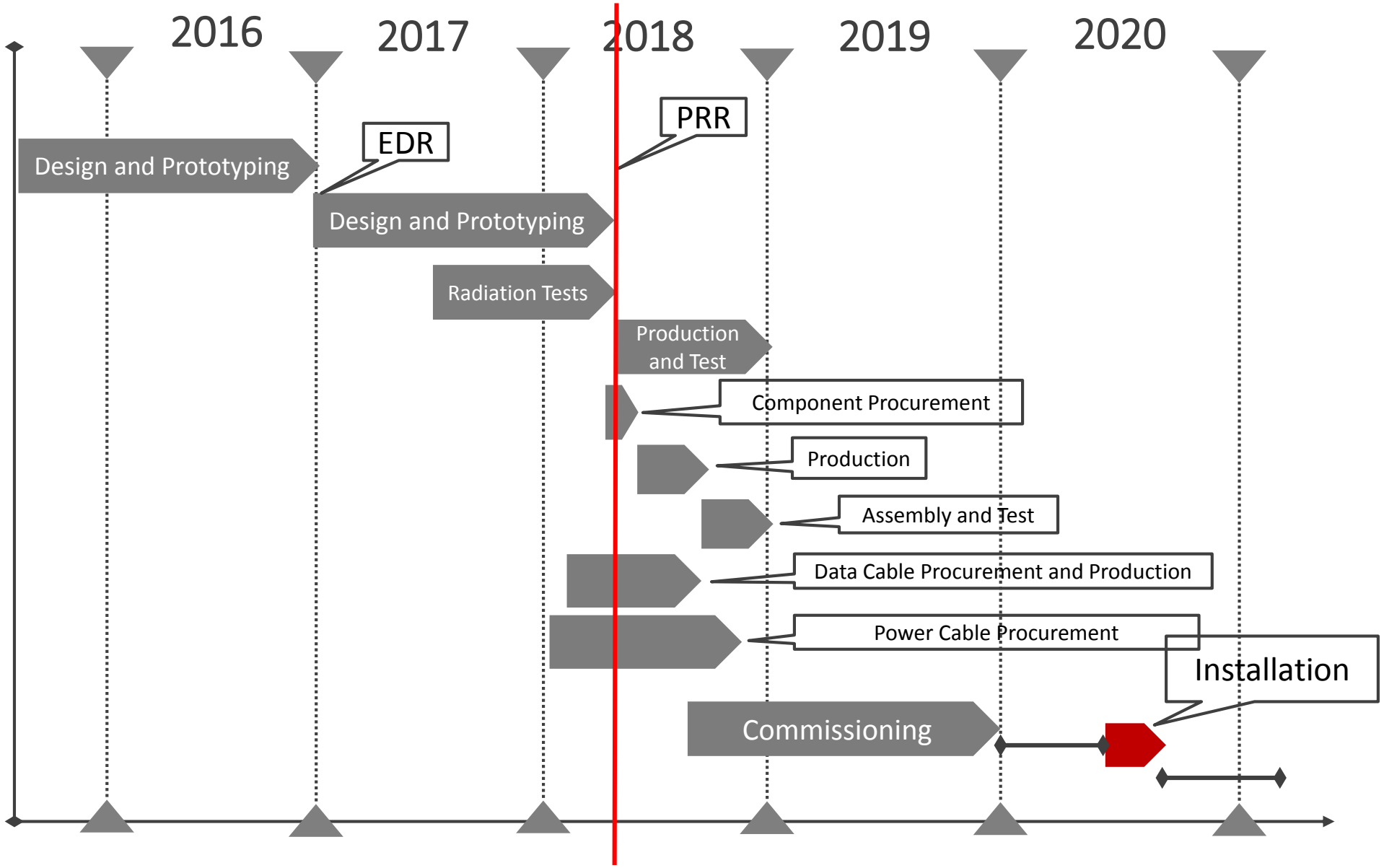


Planning

Planning – overview on Radiation Facilities Tests and Conditions

Facility	Type of Radiation	Energy	Flux [cm^{-2} s^{-1}]	Fluency / Max. Radiation Load	Device Tested	Test Objective
CHARM (CERN)	n, p, K, **π** (mixed field)	24 GeV/c on Cu target	1.4e11 per day (spill pulse length 300ms, 3 spill per min)	About 2×10^{11} (tbc) HEH/cms^2, 30 krad	Full System	Functional stability scrubbing
NPI Rez (Prague, CZ)(2 radiation campaigns)	p	30 MeV	O(1e7)	O(1×10^{12}) p/cm^2 (tbc)	RU	Scrubbing
ChipIr (RAL, UK)	n	0 – 800 MeV	3.5e6	5×10^{11} n/cm^2	RU+ IB Stave (not exposed to primary beam)	Functional stability scrubbing
NIF (UCL, Louvain-la-Neuve, BE)	n	0 – 50 MeV (20 MeV mean)	O(1e8)	1×10^{14} HEH/cm^2	DC-DC	SEE
GIF++ (CERN)	**γ**	^{137}Cs (662keV)	N/A	14.8 krad	Power board	TID Hardness

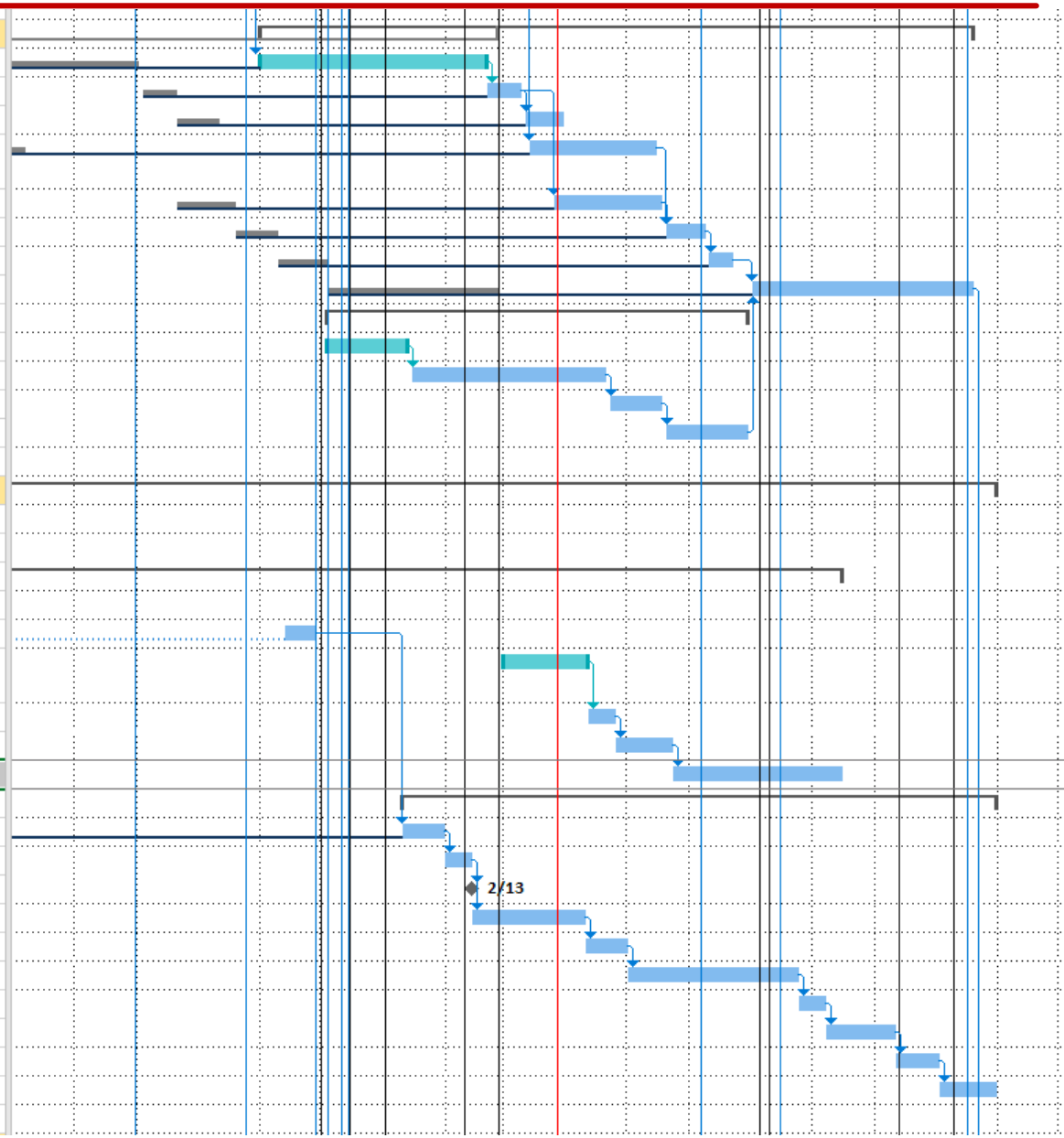
Planning – High level overview



Planning – Detailed Gantt chart

GANTT CHART

	Task Name	Duration	Start	Finish	Predecessors
560	**RUv2 (Final)**	**253 days?**	**Wed 11/1/17**	**Fri 10/19/18**	
561	Bug fix and design changes	80 days	Wed 11/1/17	Tue 2/20/18	555
562	Schematic review	13 days	Wed 2/21/18	Fri 3/9/18	561
563	Layout review	15 days	Mon 3/12/18	Fri 3/30/18	562
564	RUv2 Components procurements (FPGA, GBT, key components)	45 days	Wed 3/14/18	Tue 5/15/18	554
565	Tendering Board Production	40 days	Mon 3/26/18	Fri 5/18/18	562FS+10 days
566	Pre production	15 days	Mon 5/21/18	Fri 6/8/18	564,565
567	Power-up testing	10 days	Mon 6/11/18	Fri 6/22/18	566
568	Full production	80 days	Mon 7/2/18	Fri 10/19/18	567,573
569	**Ancillary Board for mass testing**	**150 days**	**Mon 12/4/17**	**Fri 6/29/18**	
570	Design	30 days	Mon 12/4/17	Fri 1/12/18	
571	Design review	70 days	Mon 1/15/18	Fri 4/20/18	570
572	Production	20 days	Mon 4/23/18	Fri 5/18/18	571
573	Review, Test and Finalisation	30 days	Mon 5/21/18	Fri 6/29/18	572
574					
575	**System integration**	**455 days**	**Wed 2/1/17**	**Tue 10/30/18**	
576	Cable PCB connector design	15 days	Wed 2/1/17	Tue 2/21/17	
577	General RPU system layout	15 days	Wed 3/1/17	Tue 3/21/17	
578	**Data Cable Procurement**	**401 days**	**Wed 2/1/17**	**Wed 8/15/18**	
579	Cable safety exception	30 days	Wed 2/1/17	Tue 3/14/17	
580	Cable finalization	30 days	Wed 3/22/17	Tue 11/28/17	576,577,579
581	Production version prototype procurement	30 days	Thu 3/1/18	Wed 4/11/18	
582	Prototype verification (incl mechanics)	10 days	Thu 4/12/18	Wed 4/25/18	581
583	Procurement final production	20 days	Thu 4/26/18	Wed 5/23/18	582
584	Production	60 days	Thu 5/24/18	Wed 8/15/18	583
585	**Power Cable Procurement**	**210 days**	**Wed 1/10/18**	**Tue 10/30/18**	
586	Cable tendering	15 days	Wed 1/10/18	Tue 1/30/18	580FS+30 days
587	Drawings	10 days	Wed 1/31/18	Tue 2/13/18	586
588	Material for Prototypes shipped	0 days	Tue 2/13/18	Tue 2/13/18	587
589	Prototype production	8 wks	Wed 2/14/18	Tue 4/10/18	587
590	Prototype Approval	3 wks	Wed 4/11/18	Tue 5/1/18	589
591	Production Batch 1	12 wks	Wed 5/2/18	Tue 7/24/18	590
592	Approval Batch 1	2 wks	Wed 7/25/18	Tue 8/7/18	591
593	Production Batch 2	24 days	Wed 8/8/18	Mon 9/10/18	592
594	Production Batch 3	16 days	Tue 9/11/18	Tue 10/2/18	593
595	Production Batch 4	20 days	Wed 10/3/18	Tue 10/30/18	594
596					



Planning – material/board procurement/production

Critical components procurement

Component	Due to	Status
ICs (FPGAs, memories)	Jun 2018	Ongoing
Fiberoptics	Sept 2018	Investigating
Crates	Sept 2019	Prototype ready

Boards production (and testing)

Commissioning	Due to	Readout Unit [cumulative]	Power Board [cumulative]	CRUs / FLP [cumulative]	Data cables [cumulative]
Layer 0	Sept 2018	12 [12]	6 [6]	2/1 [2/1]	12 [12]
Layer 1, 2	Feb 2018	16, 20 [48]	8, 10 [24]	4/2 [6/3]	16, 20 [48]
Layers 3, 4	Jun 2019	24, 30 [102]	12, 15 [51]	6/3 [12/6]	96, 120 [264]
Layers 5, 6	Sept 2019	42, 48 [192]	42, 48 [141]	12/6 [24/12]	168, 192 [624]
Total		**192**	**141**	**24/12**	**624**
Spares + R&D		28	16		26

Actual CRU number can be reduced by a factor 3 for commissioning