ALPIDE Chip Overview

ITS Upgrade Readout Electronics Production Readiness Review
13 April 2018

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TEXTUAL INTRODUCTION

Textual introduction copied from the manual (1)

The ALPIDE chip is a particle detector based on Monolithic Active Pixels and implemented in a 180 nm CMOS technology for Imaging Sensors. It has been designed for the Upgrade of the Inner Tracking System of the ALICE experiment at the CERN Large Hadron Collider.

The ALPIDE chip measures 15 mm (Y) by 30 mm (X) and contains a matrix of 512 ×1024 (Y×X) sensitive pixels (Fig. 1.1). The pixels are 29.24 μm × 26.88 μm (X×Y). A periphery circuit region of 1.2 × 30 mm^2 including the readout and control functionalities is present. It is assumed that the chip is observed from the circuits side and oriented such that the periphery is at the bottom. The pixel columns are numbered from 0 to 1023 going from left to right. Pixel rows are numbered from 0 to 511 going from the matrix top side downwards to the bottom one immediately above the periphery.

Each pixel cell contains a sensing diode, a front-end amplifying and shaping stage, a discriminator and a digital section (Fig. 1.2). The digital section includes three hit storage registers (Multi Event Buffer), a pixel masking register and pulsing logic.

The front-end and the discriminator are continuously active. They feature a non-linear response and their transistors are biased in weak inversion. Their total power consumption is 40 nW. The output of the front-end has a peaking time of the order of 2 μs, while the discriminated pulse has a typical duration of 10 μs. The front-end and the discriminator act as an analogue delay line. This allows operating the chip in triggered mode when the latency of the incoming trigger is comparable with the peaking time of the front-end.

A common threshold level is applied to all the pixels. The latching of the discriminated hits in the storage registers is controlled by global STROBE signals. A pixel hit is latched into one of three in-pixel memory cells if a STROBE pulse is applied to the selected cell while the front-end output is above threshold. Three distinct STROBE signals are generated at the periphery and globally applied to all pixels, controlling the storage of the pixel hit information in the pixel event buffers. The generation of the internal STROBE signals can be triggered by an external command (TRIGGER), but it can optionally be initiated by an internal sequencer.

The duration of the STROBE pulses is programmable.

In every pixel there is a pulse injection capacitor for injection of test charge in the input of the front-end. A digital-only pulsing mode is also available, forcing the writing of a logic one in the pixel memory cells. The pulsing patterns are fully programmable.

The readout of pixel hit data from the matrix is based on a circuit named Priority Encoder. There are 512 instances of this circuit, one every two pixel columns. The Priority Encoder provides to the periphery the address of the first pixel with a hit in its double column, selecting it according to a hardwired topological priority. During one hit transfer cycle a pixel with a hit is selected, its address is generated and transmitted to the periphery and finally the in-pixel memory element is reset. The address of the next pixel with a hit in the double column is then calculated. This cycle is repeated until the addresses of all pixels initially presenting a valid hit at the inputs of a Priority Encoder have been transmitted to the periphery and all the pixel state registers have been reset. The transfer of the frame data from the matrix to the periphery is therefore zero-suppressed.

Each Priority Encoder is a fully combinatorial circuit and it is steered by sequential logic in the periphery during the readout of a matrix frame. It is implemented in a very narrow region between the pixels, extending vertically over the full height of the columns. There is no free running clock distributed in the matrix and there is no signaling activity if there are no hits to read out. The average energy needed to encode the address of a hit pixel is of

Textual introduction copied from the manual (2)

the order of 100 pJ. Power is consumed proportionally to the readout rate and to the frame occupancy. The Priority Encoders also implement the buffering and distribution of readout and configuration signals to the pixels.

The readout of the matrix is organized in 32 regions (512×32 pixels), each of them with 16 double columns being read out by 16 Priority Encoder circuits (Fig. 2.1). There are 32 corresponding readout modules (Region Readout Units) in the chip periphery, each one executing the readout of a submatrix. The sixteen Double Columns inside each region are read out sequentially, while the thirty-two submatrices are read out in parallel.

The Priority Encoders are driven by state machines in the Region Readout Units. These modules contain de-randomizing memories and perform additional data reduction and formatting. The data from the 32 region readout blocks are assembled and formatted by a Top Readout Unit module. Two major readout modes are supported, one in which the strobing and readout are triggered externally and a second one in which frames are continuously integrated and read out, with programmable duration of the strobe assertion intervals.

Hit data can be transmitted on two different data interfaces according to one of three alternative operating modes envisaged for the application in the Upgraded ALICE ITS: *Inner Barrel chip*, *Outer Barrel Master* and *Outer Barrel Slave*. A 1.2 Gb/s Serial Data port with differential signalling is the largest capacity data readout interface and the primary one for the Inner Barrel Module chips. The serial data are 8b/10b encoded, therefore the maximum data throughput is 960 Mb/s. The serial port can optionally operate at reduced line rates (600 Mb/s or 400 Mb/s).

The same interface is intended to be used for the transmission of data off-detector by the Outer Barrel Master chips, using a bit rate of 400 Mb/s (320 Mb/s payload). The Master chips also collect the data of a set of neighboring Outer Barrel Slave chips and forward their data off-detector on the differential link.

A bidirectional parallel data port with single-ended signaling is also present, with a capacity of 320 Mb/s. It enables the implementation of the data exchange between the Outer Barrel Slave chips and the corresponding Master. All the functionalities related to the communication between Master and Slave chips on the parallel bus are implemented in the module called Data Management Unit.

The ALPIDE chip has custom control interfaces. There is a differential control port (DCNTRL) supporting bi-directional (half duplex) serial signaling at 40 Mb/s on differential links. A second single ended control line (CNTRL) is also available. These interfaces and the related control logic enable the interconnection of multiple chips on a multi-point control bus with a hierarchical topology, with control transactions relayed by the Master chips to Slave chips. The Control Management Unit block implements the control layer and provides full access to the control and status registers of the chip as well as to the multi-event memories in the Region Readout Units. The control bus is also used to distribute commands to the chips, most notably the trigger messages.

All the analog signals required by the front-ends are generated by a set of on-chip 8 bit DACs. Analog monitoring pads (DACMONV, DACMONI) are available to monitor the outputs of the internal DACs. The DACMONV pad can be used to override any of the voltage DACs. The DACMONI pad can be used to override any of the current DACs or to override the internal reference current used by the current DACs.

The analog section of the periphery also contains an ADC with 10-bit dynamic range, a bandgap voltage reference and a temperature sensing circuit. The ADC can be used to monitor several quasi-static internal analog signals: the outputs of the DACs, the analog and digital supply voltages, the bandgap voltage and the temperature sensor.

Textual introduction copied from the manual (3)

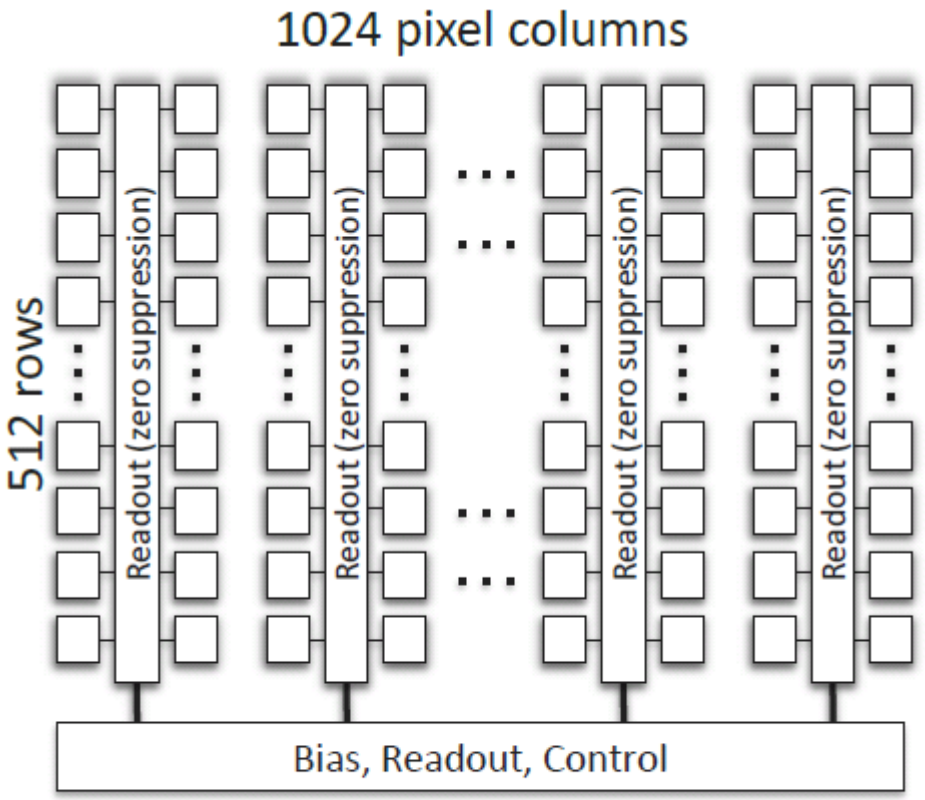


Figure 1.1: General architecture of the ALPIDE chip.

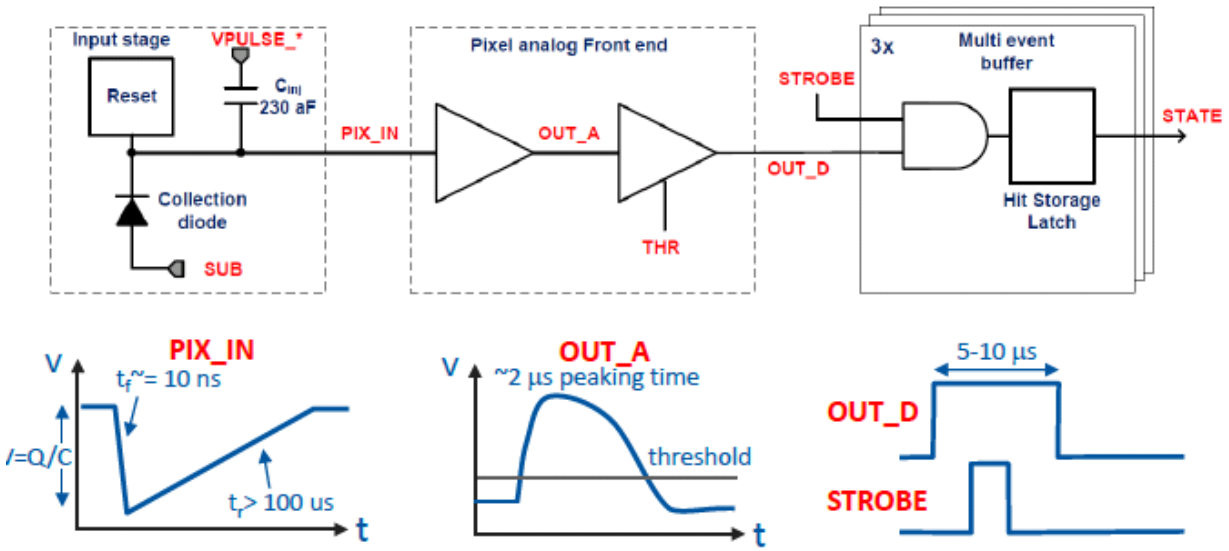
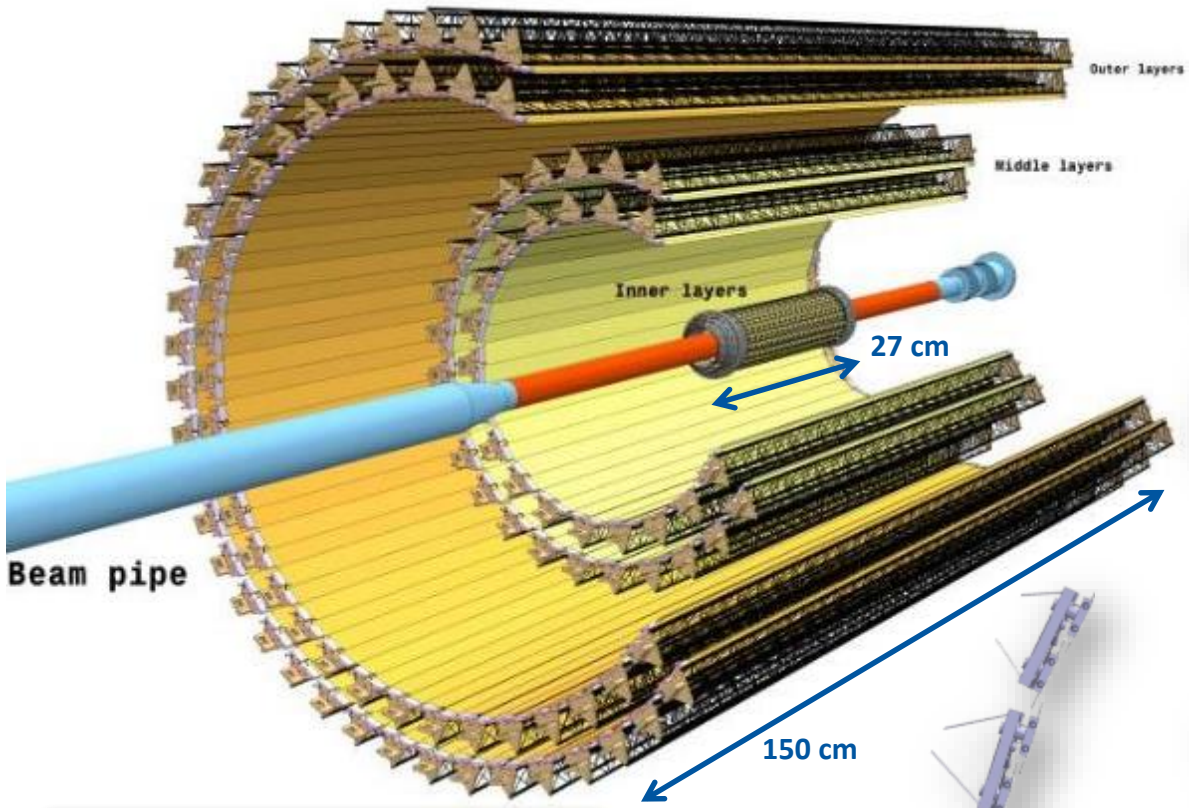


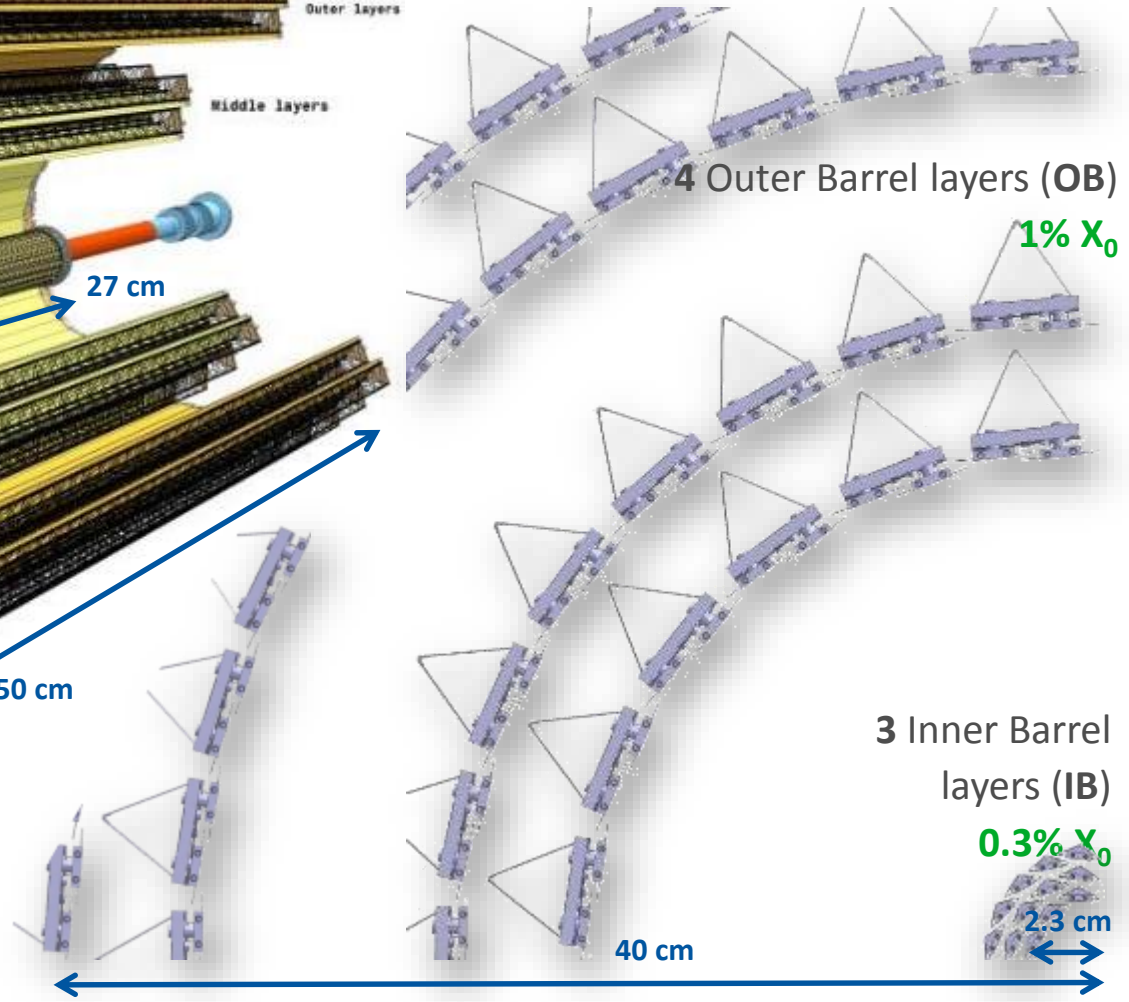
Figure 1.2: Block diagram of the ALPIDE pixel cell.

REQUIREMENTS

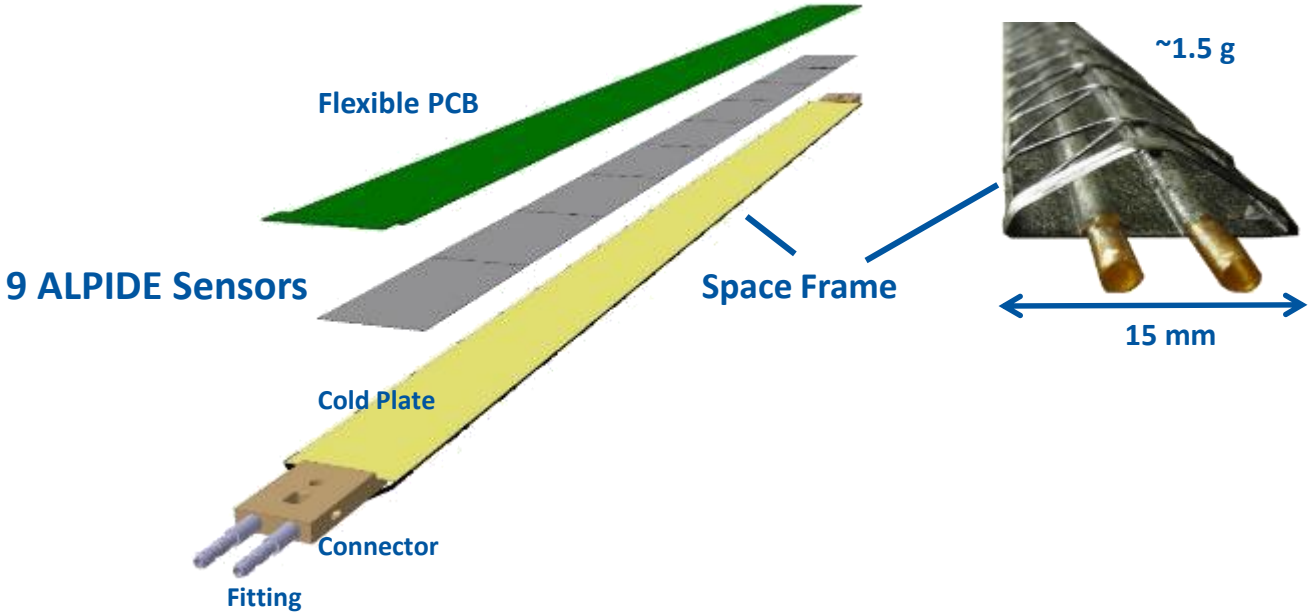
ALICE ITS Upgrade layout

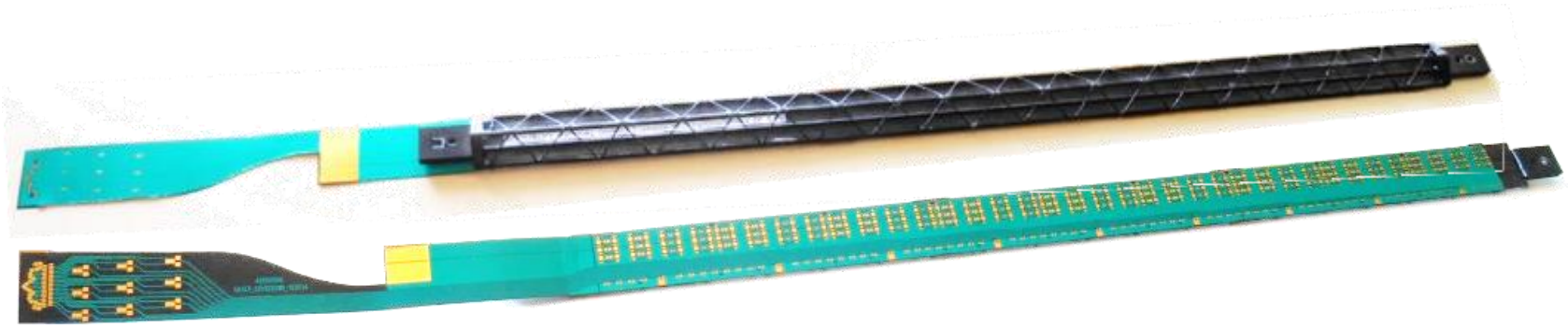


10 m² sensitive area
~24000 CMOS Pixel Sensors
12.5 Gpixels

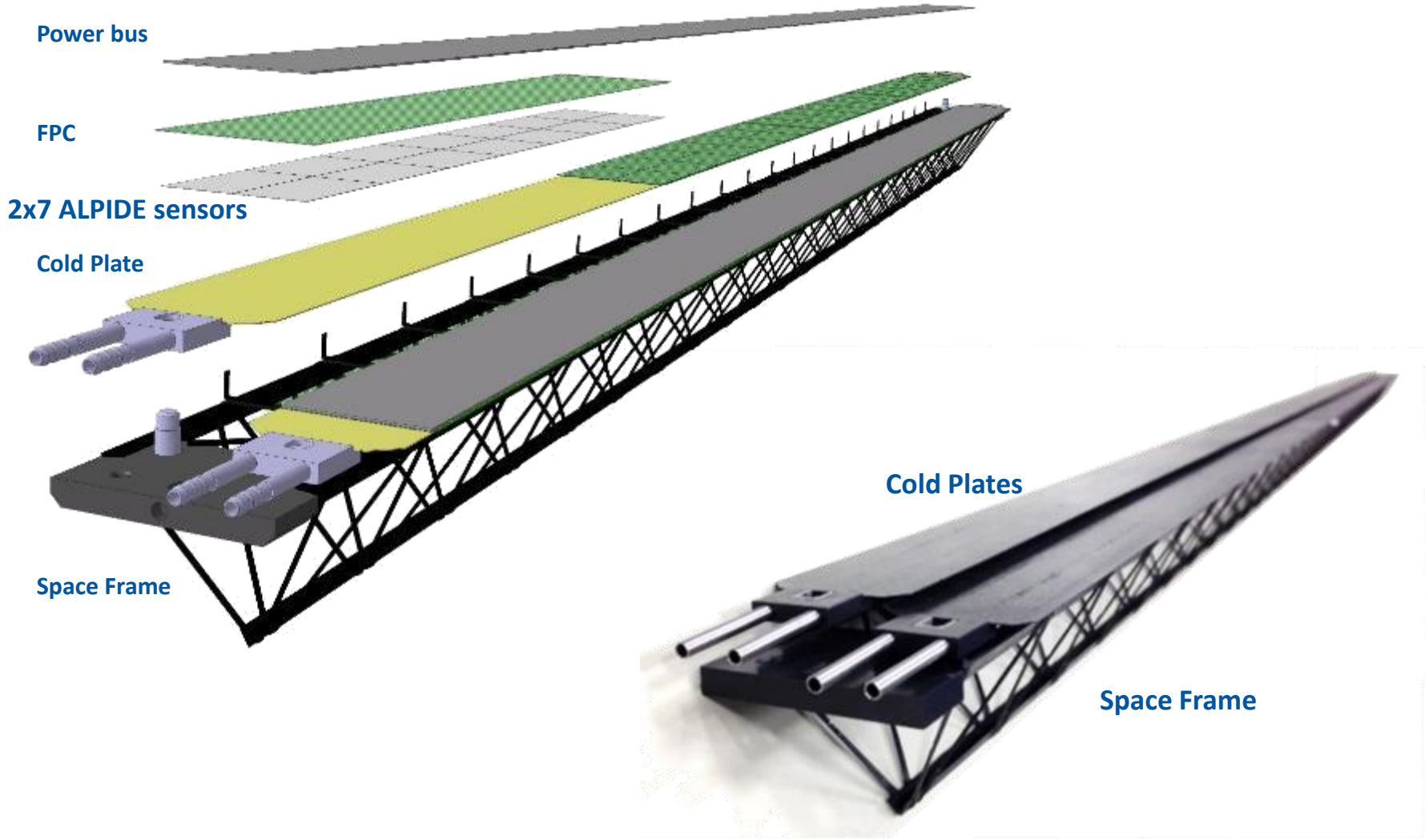


Inner Barrel Stave



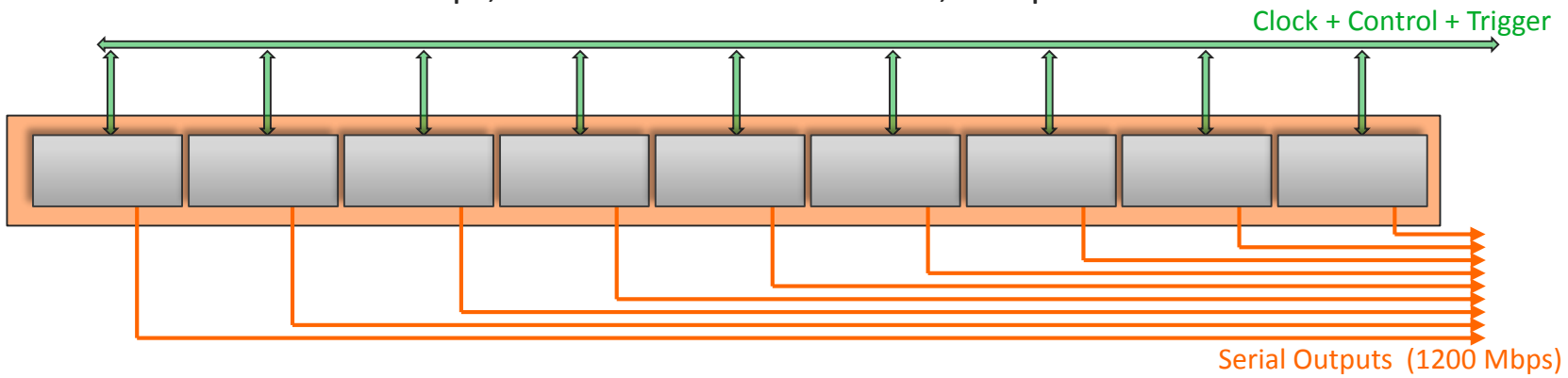


Outer Barrel Stave



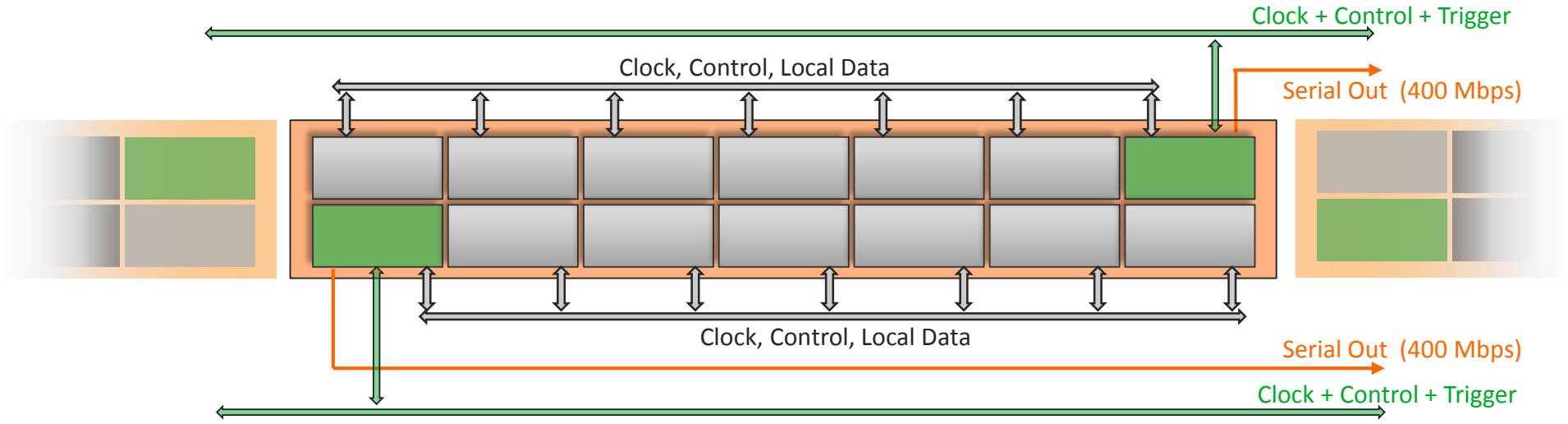
Modules (HICs) with ALPIDE Chips

ITS Inner Barrel Module – 9 chips, common clock and control, independent data lines



ITS Outer Barrel Module – 2 groups of chips, Master + 6 Slaves

Only the Master interfaces to the external world and bridges control and data transfer



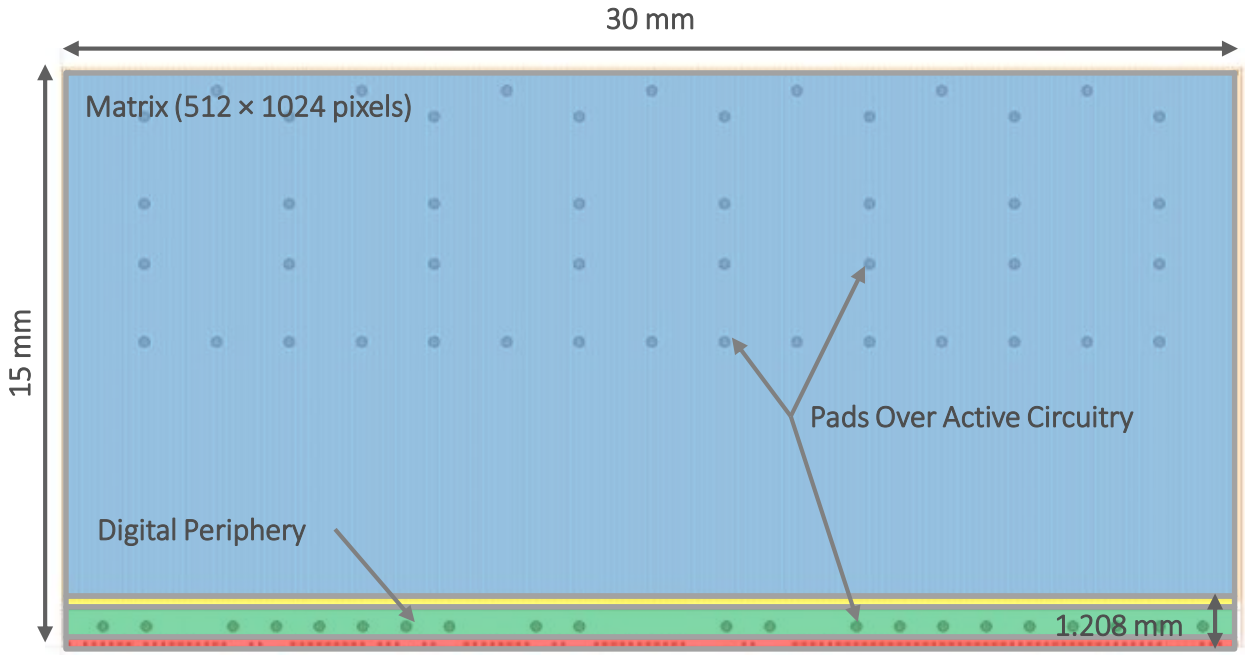
ITS Sensor General Requirements

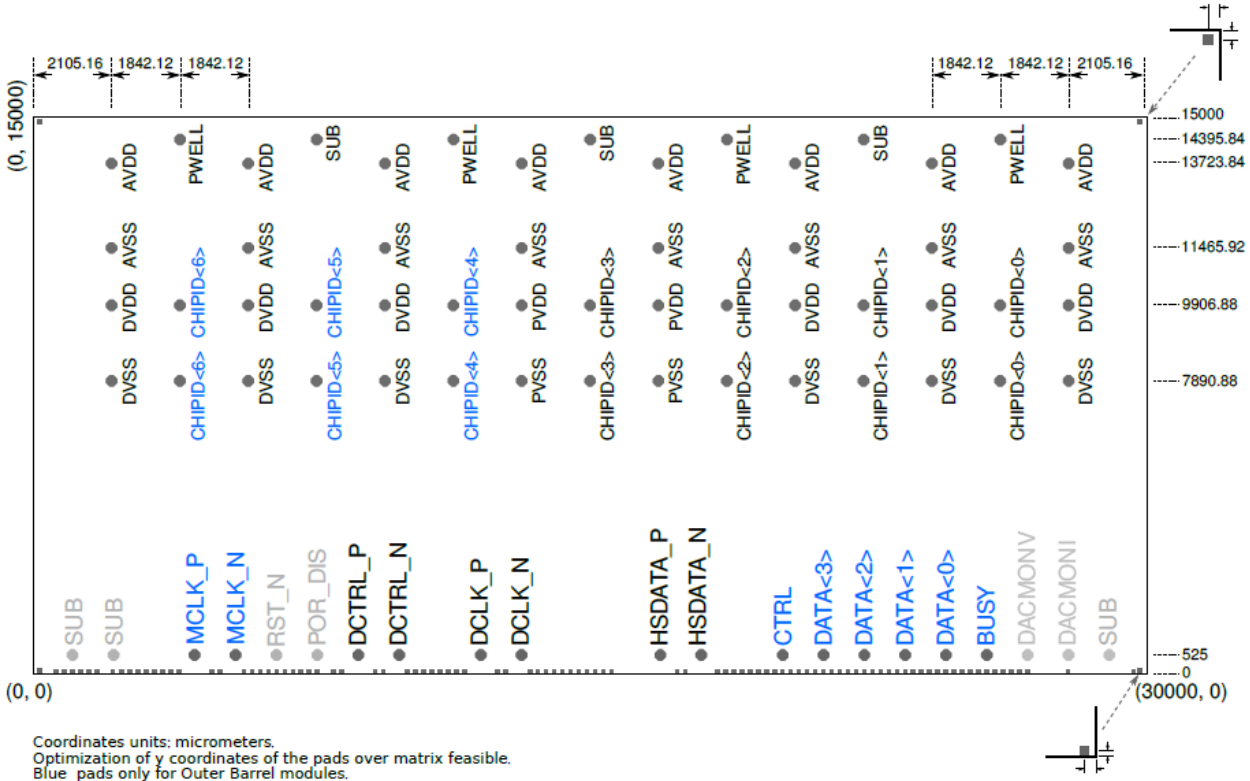
Parameter	Inner Barrel	Outer Barrel
Chip size (mm x mm)	15 x 30	
Chip thickness (μm)	50	100
Spatial resolution (μm)	5	10 (5)
Detection efficiency	> 99%	
Fake hit rate	$< 10^{-6}$ evt^{-1} pixel^{-1} (ALPIDE $<< 10^{-6}$)	
Integration time (μs)	< 30 (< 10)	
Power density (mW/cm^2)	< 300 (~40)	< 100 (~30)
TID radiation hardness (krad)	270	10
NIEL radiation hardness (1 MeV n_{eq}/cm^2)	1.7 x 10^{12}	1.7 x 10^{11}
Readout rate, Pb-Pb interactions (kHz)	100	
Readout rate, p-p interactions (kHz)	400	
Hit Density, Pb-Pb interactions (cm^{-2})	19	< 1

(*) In color: ALPIDE performance figure where above requirements

DESCRIPTION OF ALPIDE CHIP

ALPIDE Floorplan and Pinout



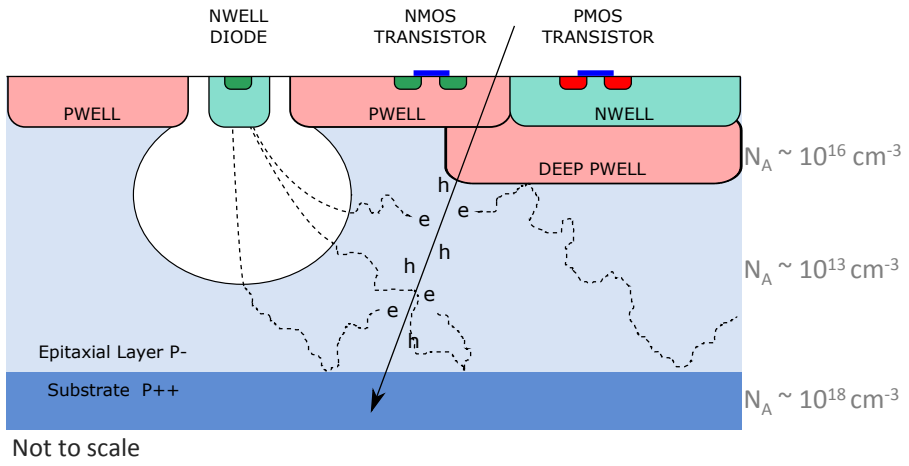


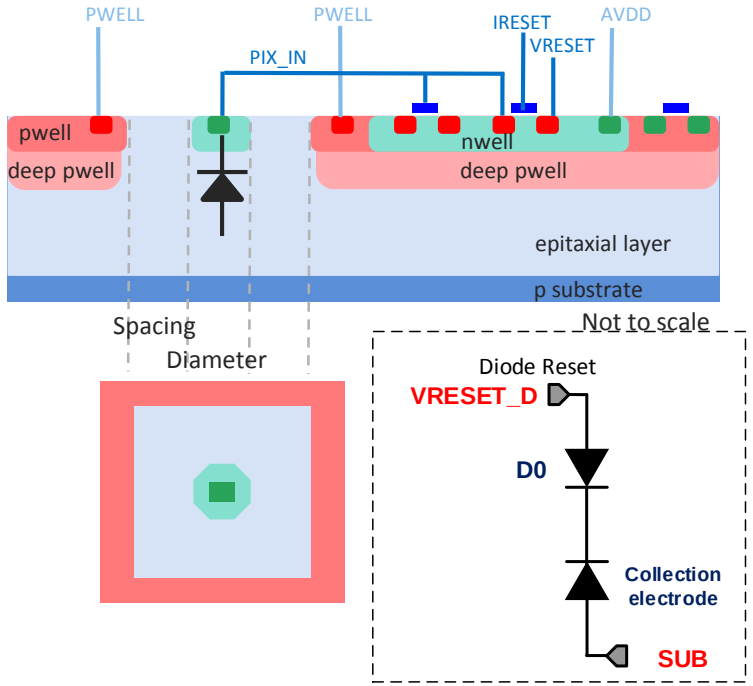
Coordinates units: micrometers.
Optimization of y coordinates of the pads over matrix feasible.
Blue pads only for Outer Barrel modules.
Light gray pads can be left unconnected and could disappear from the chip.

Technology

Pixel Sensor CMOS 180 nm Imaging Process (TowerJazz)

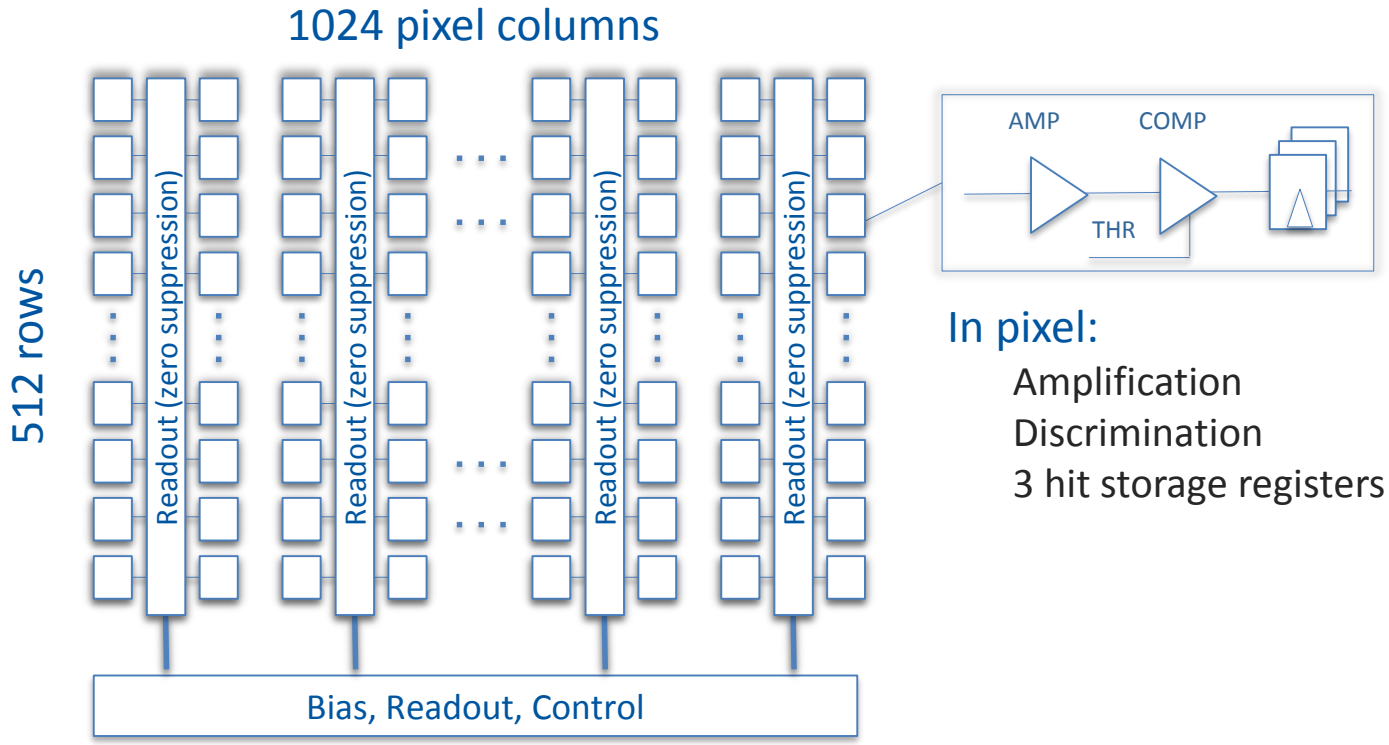
3 nm thin gate oxide, 6 metal layers





- High-resistivity (> 1kΩ cm) p-type epitaxial layer (18 μm to 30 μm) on p-type substrate
- Deep PWELL shielding NWELL allowing PMOS transistors (full CMOS within active area)
- Small n-well diode (2 μm diameter), ~100 times smaller than pixel => low capacitance => large S/N
- Reverse bias the substrate to increase the depletion volume around the NWELL collection diode

ALPIDE Architecture



In pixel:

- Amplification
- Discrimination
- 3 hit storage registers (MEB)

29 μm x 27 μm pixel pitch

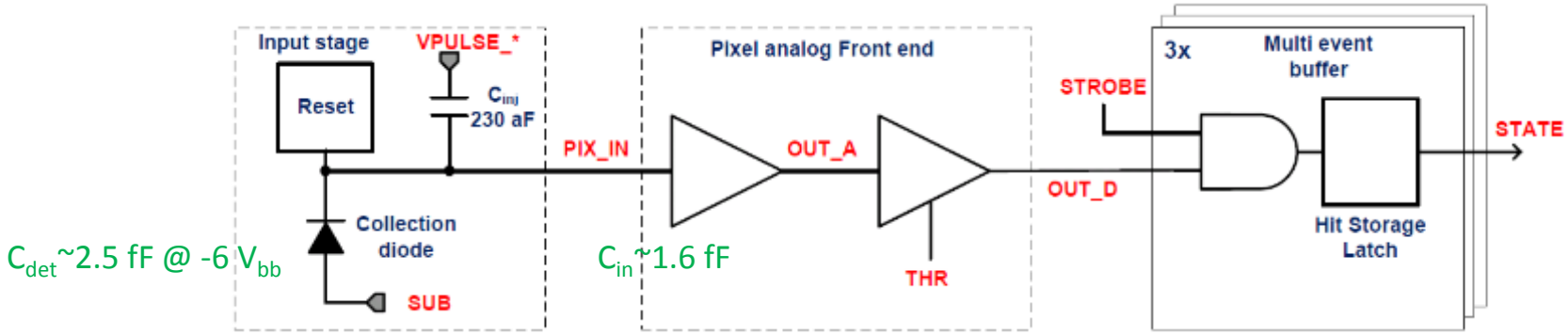
Continuously active front-end

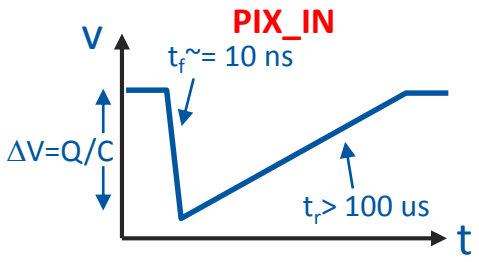
Global shutter

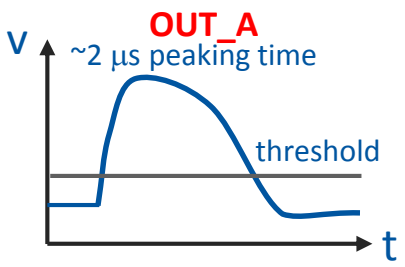
Zero-suppressed matrix readout

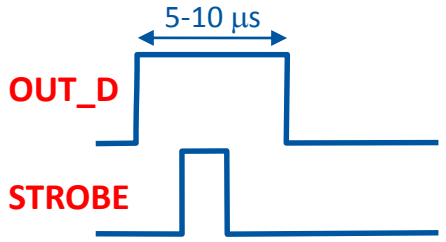
Triggered or continuous readout modes

Pixel









Analog front-end and discriminator continuously active

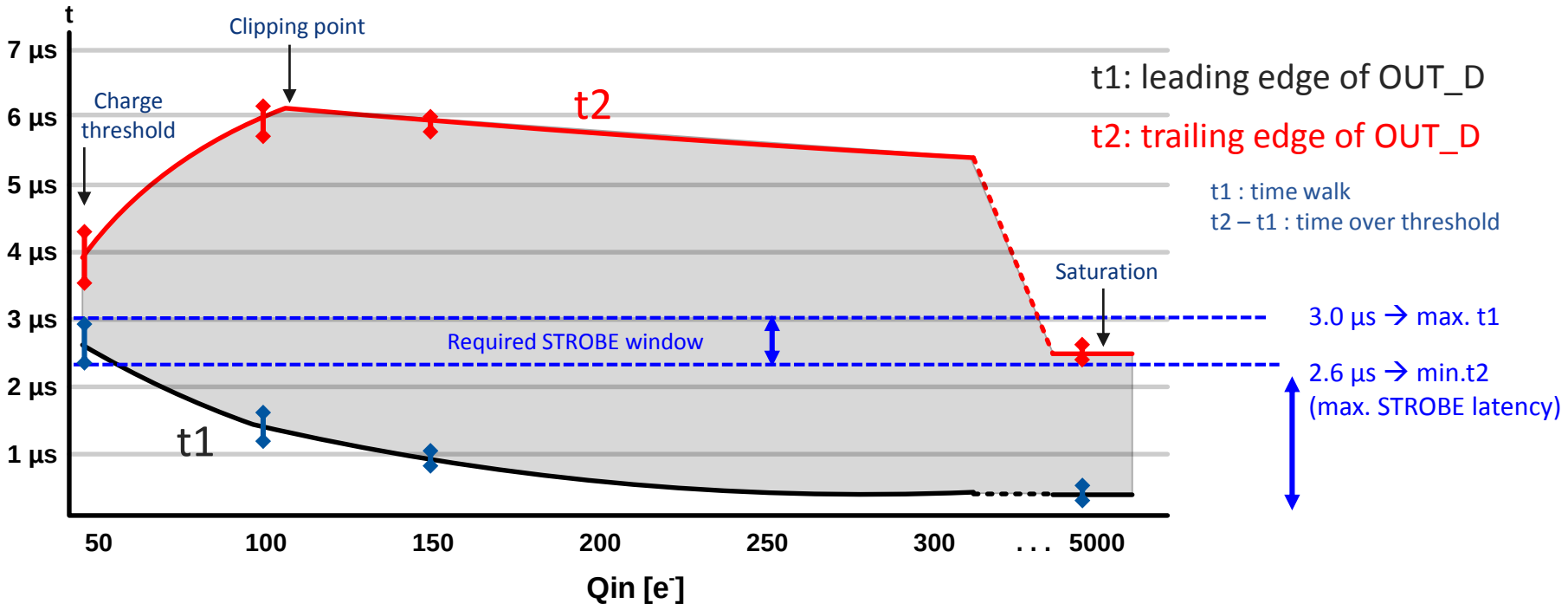
- Non-linear and operating in weak inversion. Ultra-low power: 40 nW/pixel
- The front-end acts as analogue delay line
- Test pulse charge injection circuitry
- Global threshold for discrimination -> binary pulse OUT_D

Digital pixel circuitry with three hit storage registers (multi event buffer)

- Global shutter (STROBE) latches the discriminated hits in next available register
- In-Pixel *masking* logic

Front End Characteristics (Simulated)	
Gain (small signal) [mV/e]	4
ENC [e]	3.9
Threshold [e]	92 ± 2

Timing of Discriminator Output



t1: leading edge of OUT_D

t2: trailing edge of OUT_D

t1 : time walk

t2 – t1 : time over threshold

3.0 µs → max. t1

2.6 µs → min.t2
(max. STROBE latency)

Q_{in}	t1 [us]	t2 [us]
50 e-	2.9 ±0.20	3.9 ±0.52
100 e-	1.5 ±0.16	5.9 ±0.24
150 e-	0.9 ±0.03	5.7 ±0.09
5 ke-	0.5 ±0.01	2.6 ±0.07

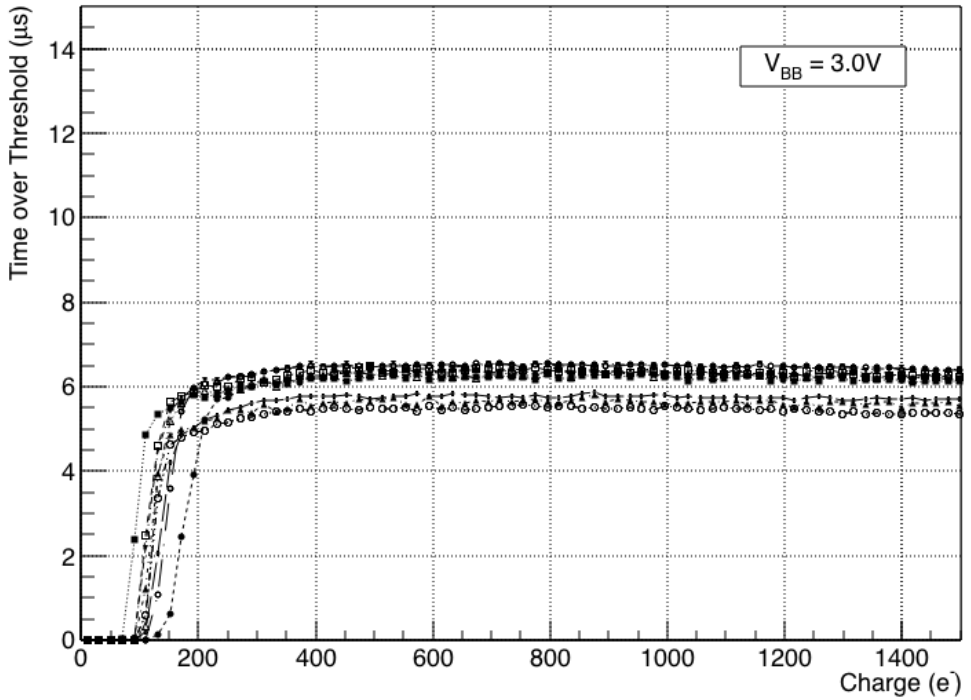
Simulation results

SOURCE: ALPIDE CHIP Production Readiness Review

Timing – Experimental Resutls

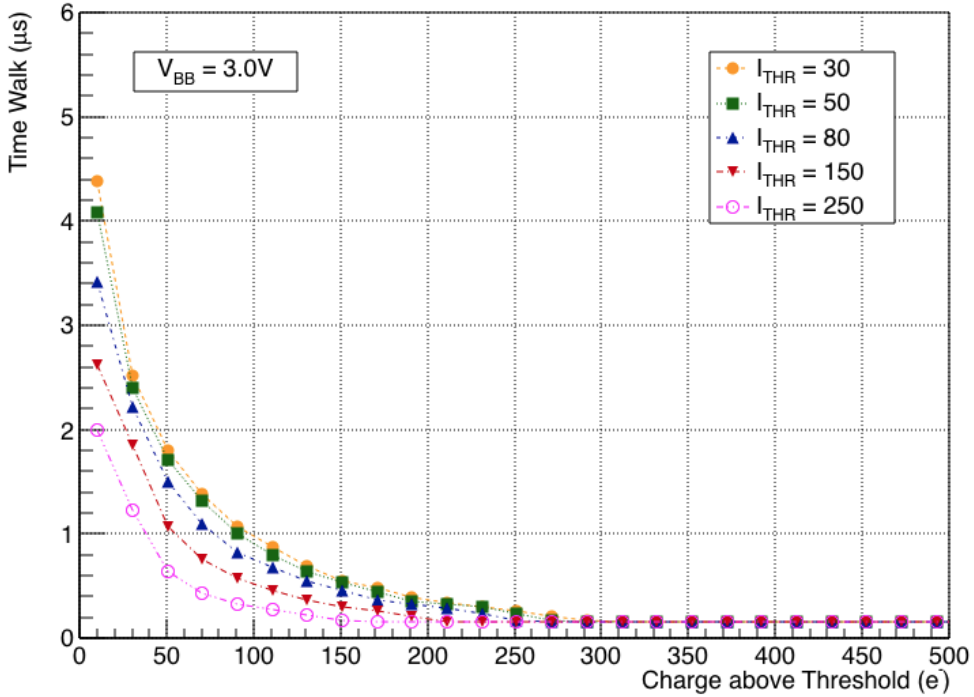
Measurement of Time over Threshold (t2-t1)

Plots show curves for sample of tested chips



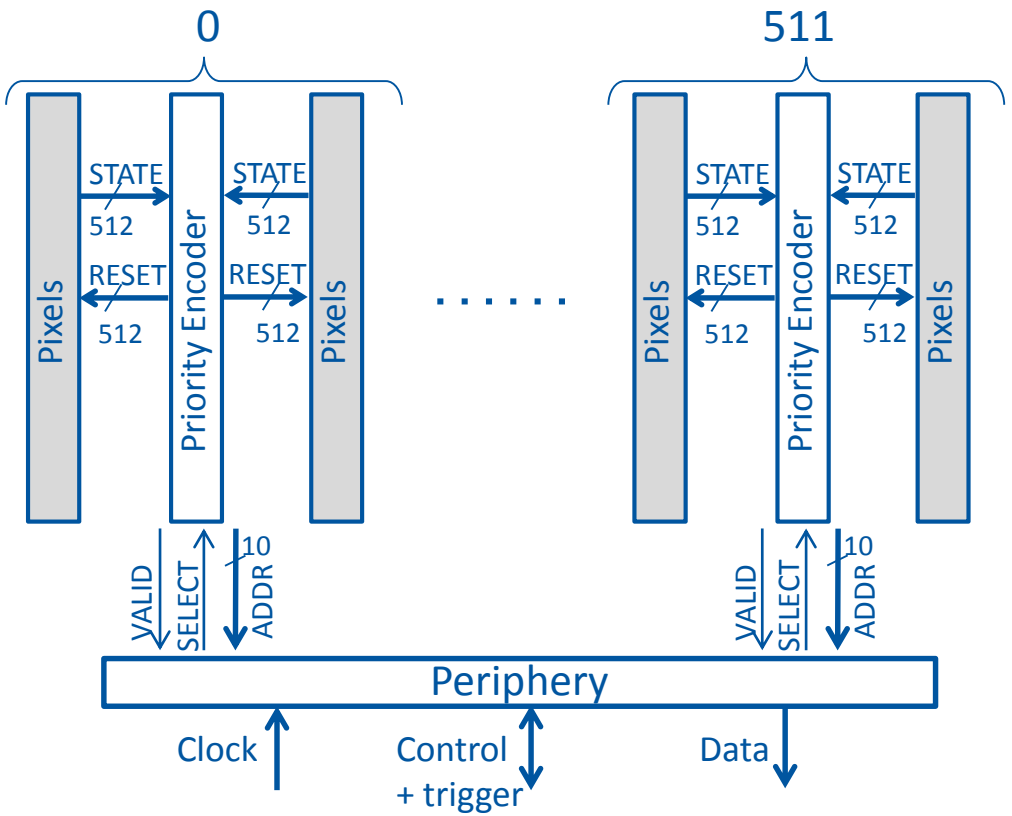
Measurement of Time Walk (t1)

Time walk as a function of charge above threshold for different settings of threshold (curves averaged over chips)



SOURCE: ALPIDE CHIP Production Readiness Review

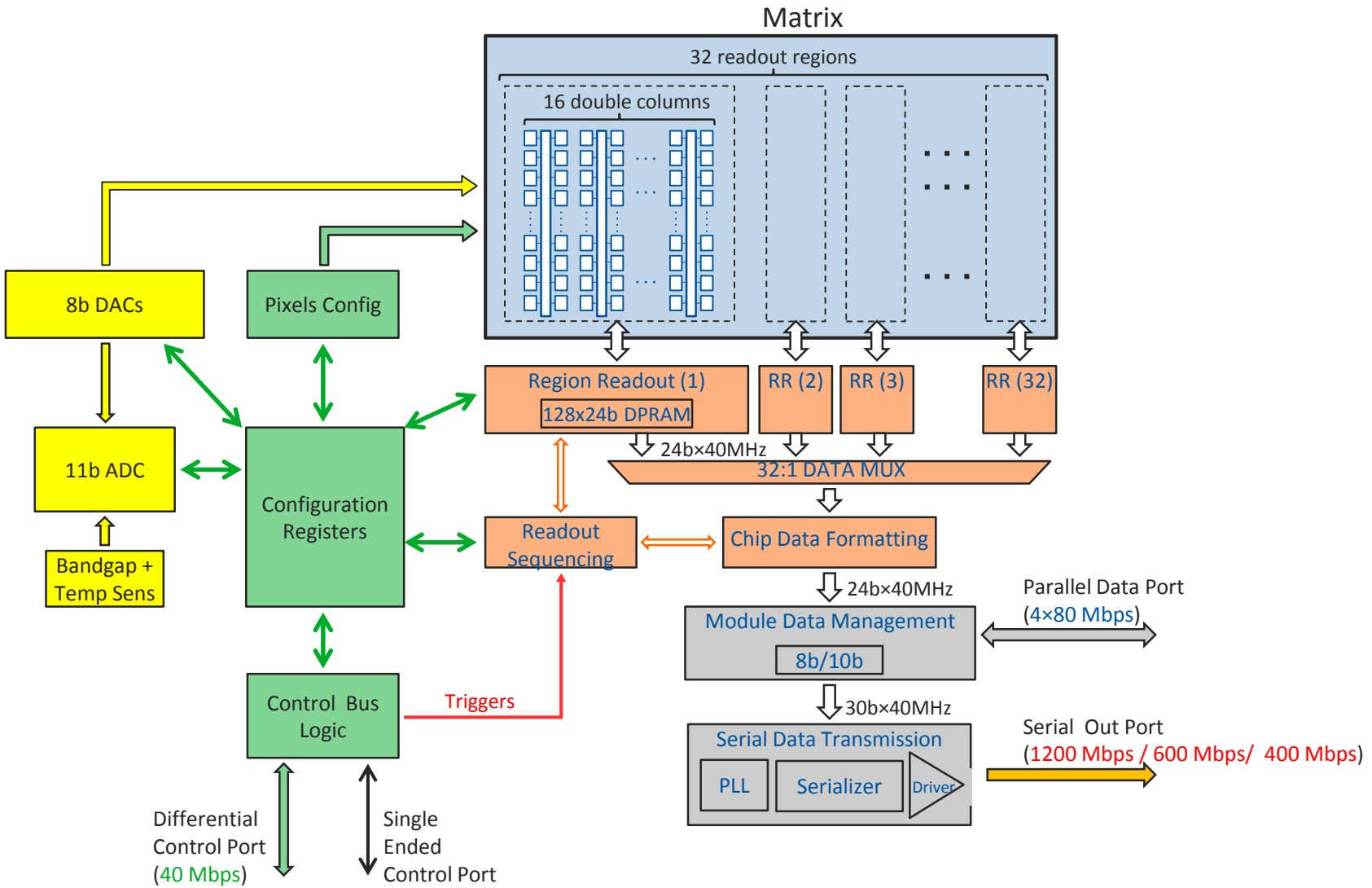
Matrix Readout



The Priority Encoder sequentially provides the addresses of all hit pixels in a double column

- Combinational digital circuit steered by peripheral sequential circuits during readout of a frame
- No free running clock over matrix. No activity if there are no hits
- Energy per hit: E_h ~= 100 pJ -> ~3 mW for nominal occupancy and readout rate
- Buffering and distribution of global signals (STROBE, MEMSEL, PIXEL RESET)

ALPIDE Readout and Control Features

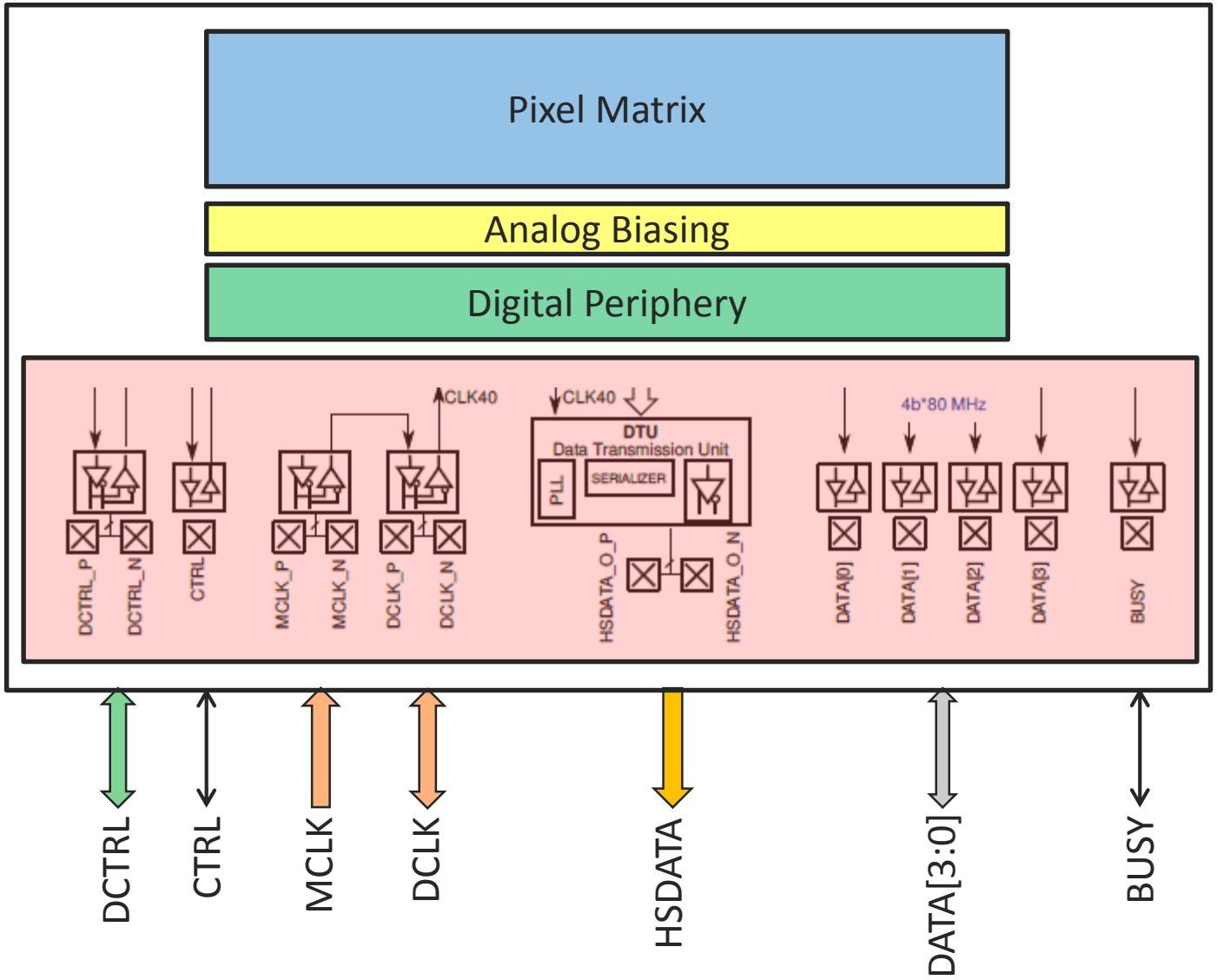


Main Interfaces

DCTRL	Bidirectional Control	Differential (MLVDS)
CTRL	Bidirectional Control	Single Ended
MCLK	Clock forwarding input	Differential (MLVDS)
DCLK	Ref. clock input (LHC BC freq.) and forwarded clock output	Differential (MLVDS)
HSDATA	Serial data output	Differential (sub-LVDS)
DATA	Parallel data bus (Input-Output)	Single Ended
BUSY	Busy flag IO	Open Drain and pull-up

MLVDS IOs
- Programmable drive current
- Configurable on-chip termination

CMOS IOs
- On-chip series termination
- Internal pull-up(-down)



Serial Data Output Port - HSDATA

Programmable Line Rate

1200 Mbps/600Mbps/400 Mbps

Implemented in the *DTU Logic* periphery module

PLL Phase Locked Loop

40 MHz -> 600 MHz

DTU Serializer

30 bits parallel input

2 Serial outputs (600 Mbps) to driver stage

1.2 Gbps serial stream made in Driver stage with fast muxes controlled by PLL clock

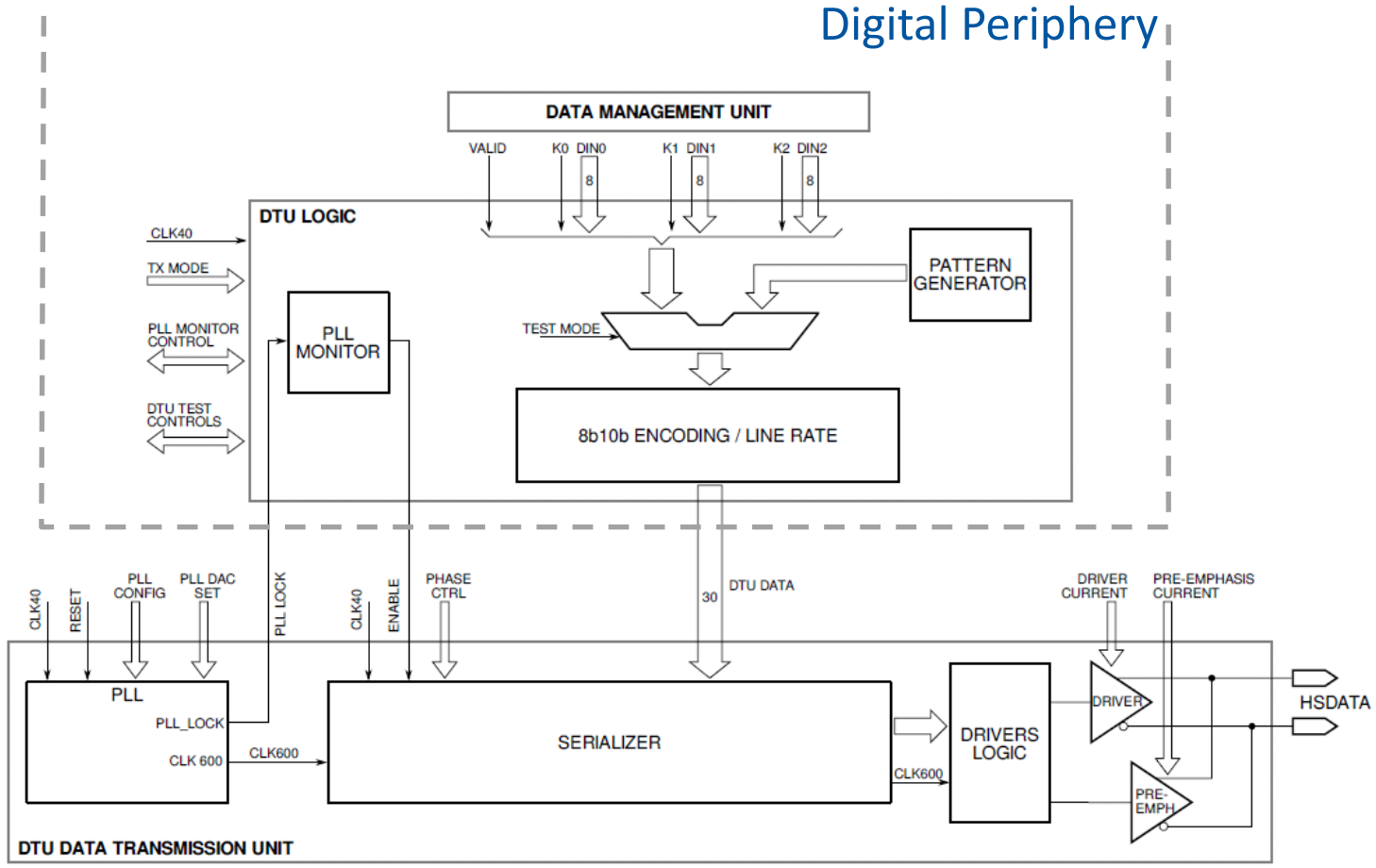
LVDS Driver

Programmable **drive current** and **pre-emphasis current**

Tailored to ITS application

1.2 Gb/s over 30 cm Al FPC + 5 m twinax cables

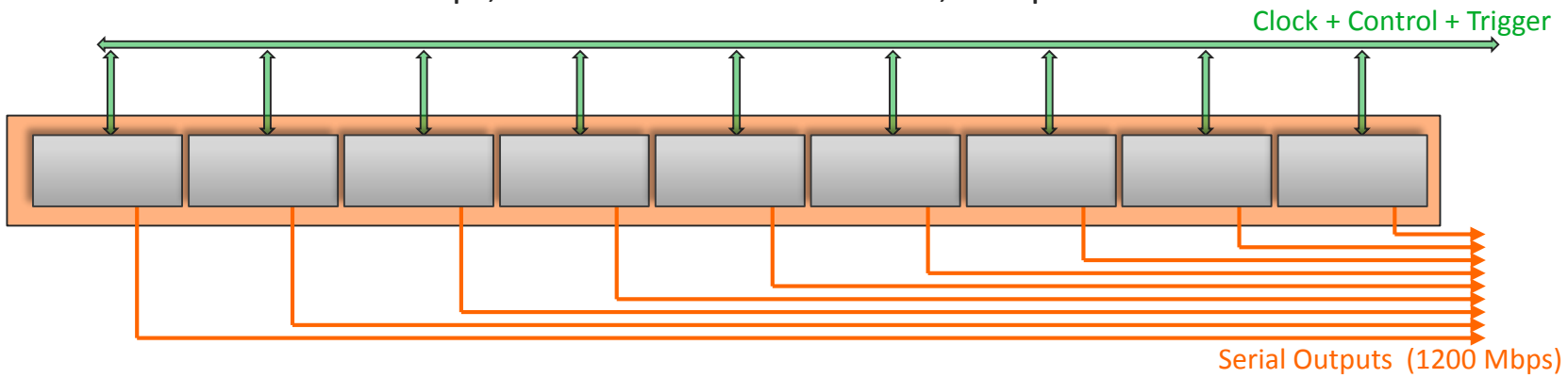
400 Mb/s over 1.5 m Cu FPCs + 5 m twinax cables



ALPIDE CHIP AND ITS MODULES

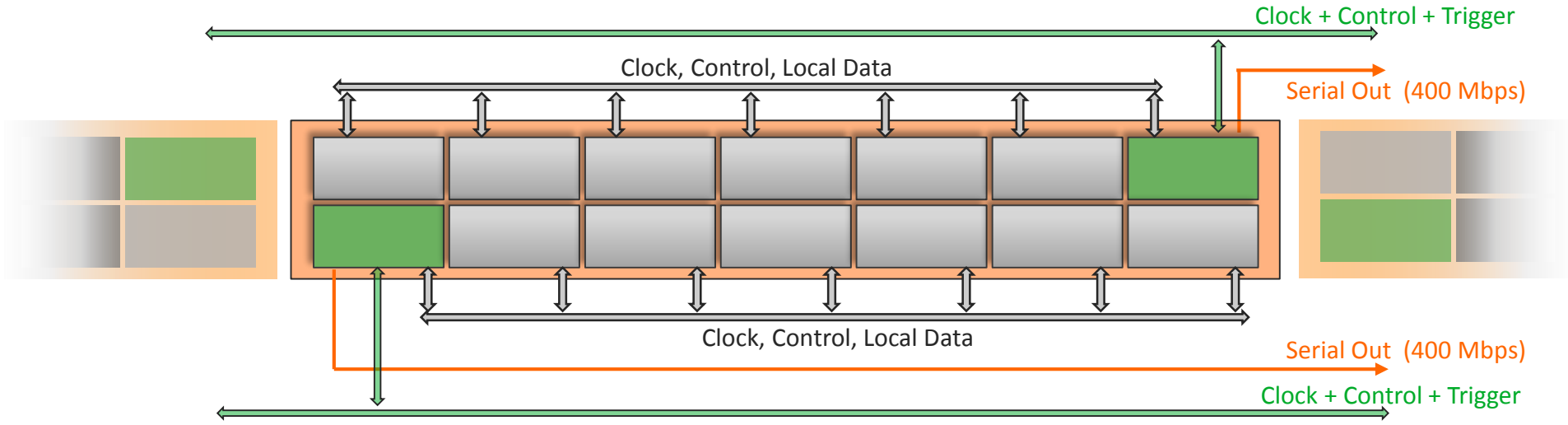
Modules (HICs) with ALPIDE Chips

ITS Inner Barrel Module – 9 chips, common clock and control, independent data lines

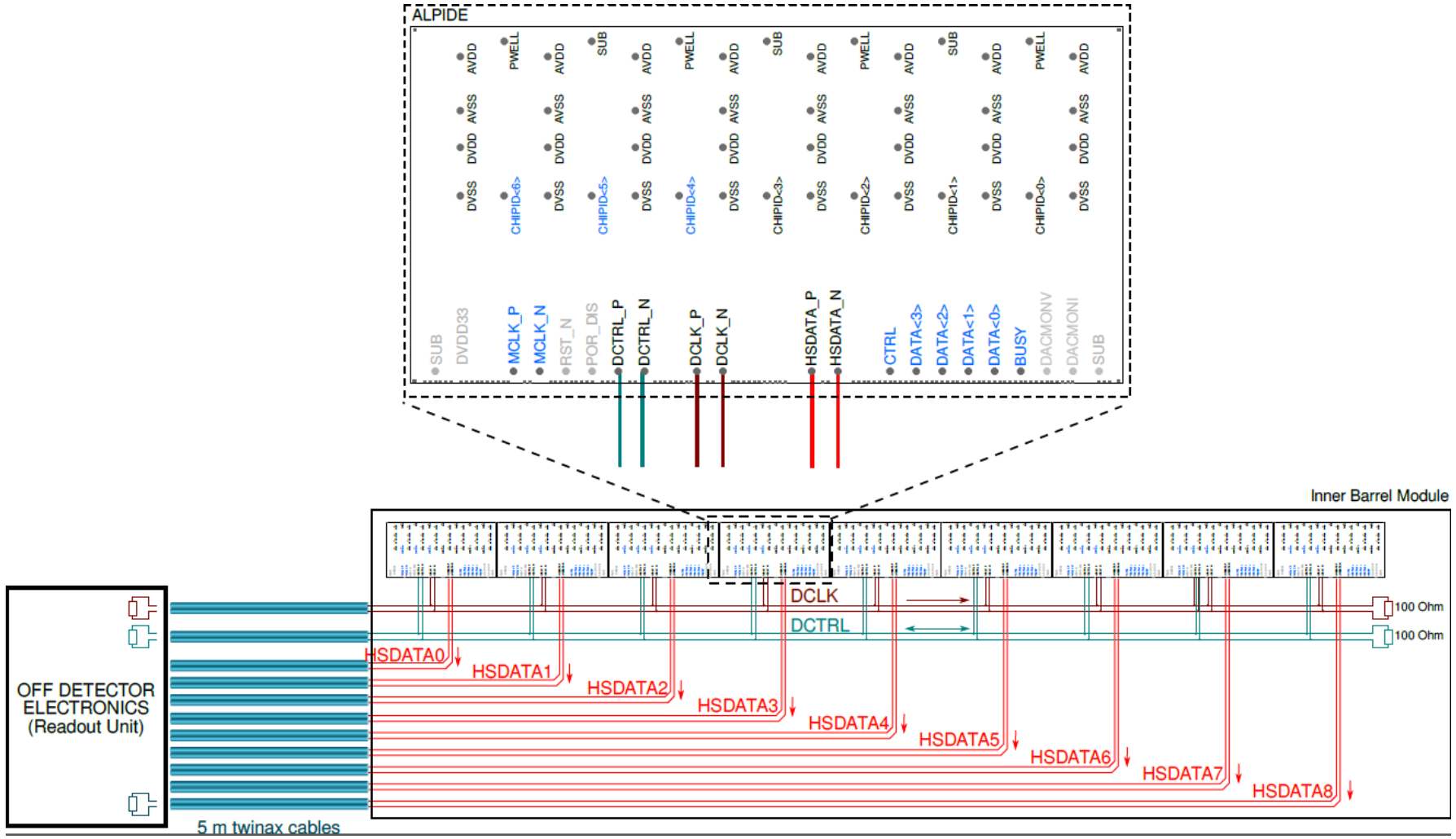


ITS Outer Barrel Module – 2 groups of chips, Master + 6 Slaves

Only the Master interfaces to the external world and bridges control and data transfer



Inner Barrel Module Wiring Scheme



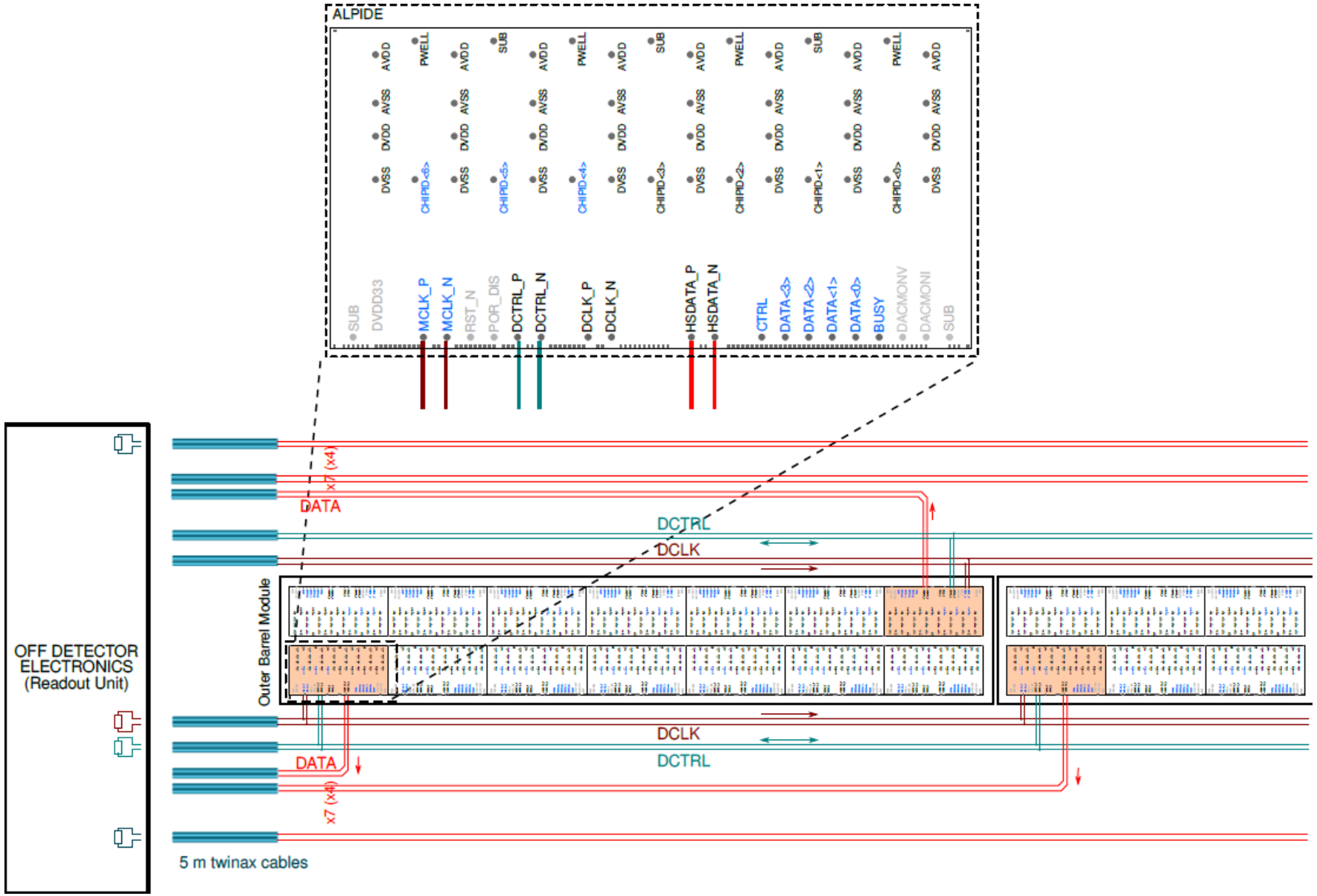
Inner Barrel Module

IB Module

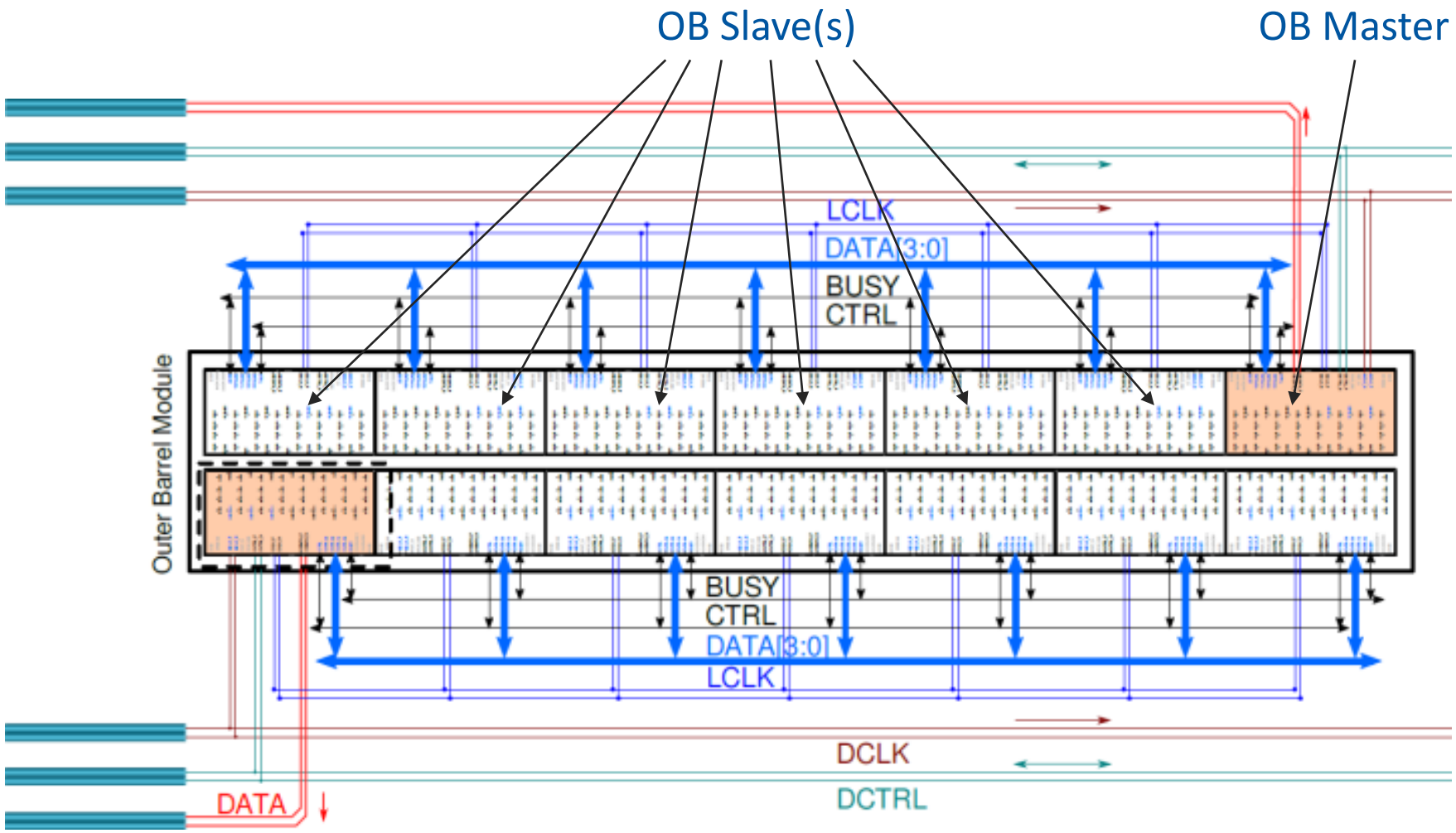
- 9 chips
- Indipendent point-to-point serial **data links** from Masters to Off-detector RU
  - **1200 Mb/s or 600 Mb/s or 400 Mb/s** line rate
  - **960 Mb/s or 480 Mb/s or 320 Mb/s** payload bit rate (8b/10b encoding)
  - 0.3 m differential lines on Al FPCs + 5 m twinax cables
- Shared *multi-drop* differential **clock bus**
- Shared *multi-poin*t differential **control bus**

Refer to Application Note Appendix B of ALPIDE Operations Manual

Outer Barrel Modules Wiring Diagram



Outer Barrel Module Local Wiring Diagram



Outer Barrel Module

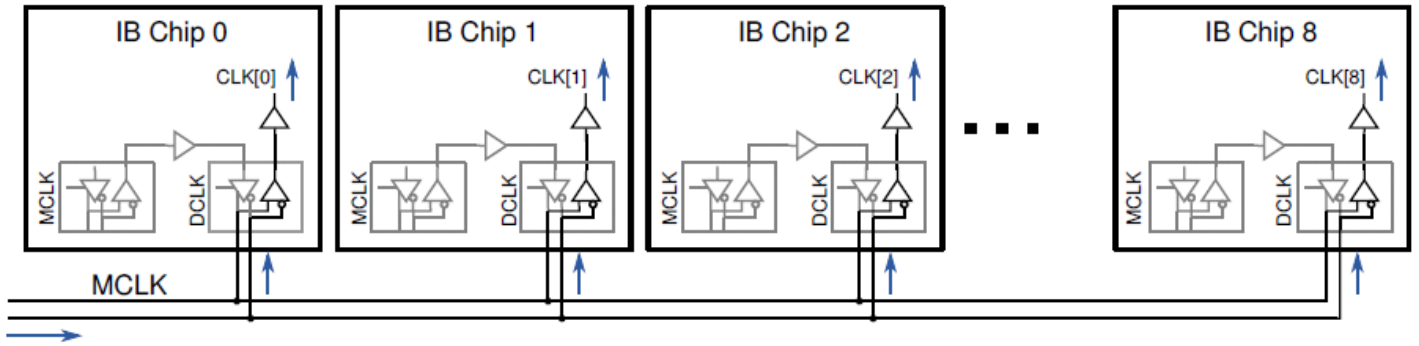
OB Module

- 2*7 chips
- 2 **Master** chips in a module
  - *Data aggregators* of adjacent 6 *Slave* chips
  - Point-to-point data links from Masters to Off-detector RU
    - **400 Mb/s** line rate (**320 Mb/s** data bandwidth)
  - 1.5 m (0.8 m) differential lines on FPCs + 5 m twinax cables
- **Local DATA bus** between slaves and masters
  - 4 lines synchronous parallel bus, Double Data Rate (**320 Mb/s**)
- **Clock and Control** forwarded by the OB Module Masters
  - Local clock and control re-distribution between *OB Module Masters* and *OB Module Slaves*
- Inter-chip BUSY signaling by dedicated shared line
  - Module “BUSY” state signaled by the OB Master Chip on data link

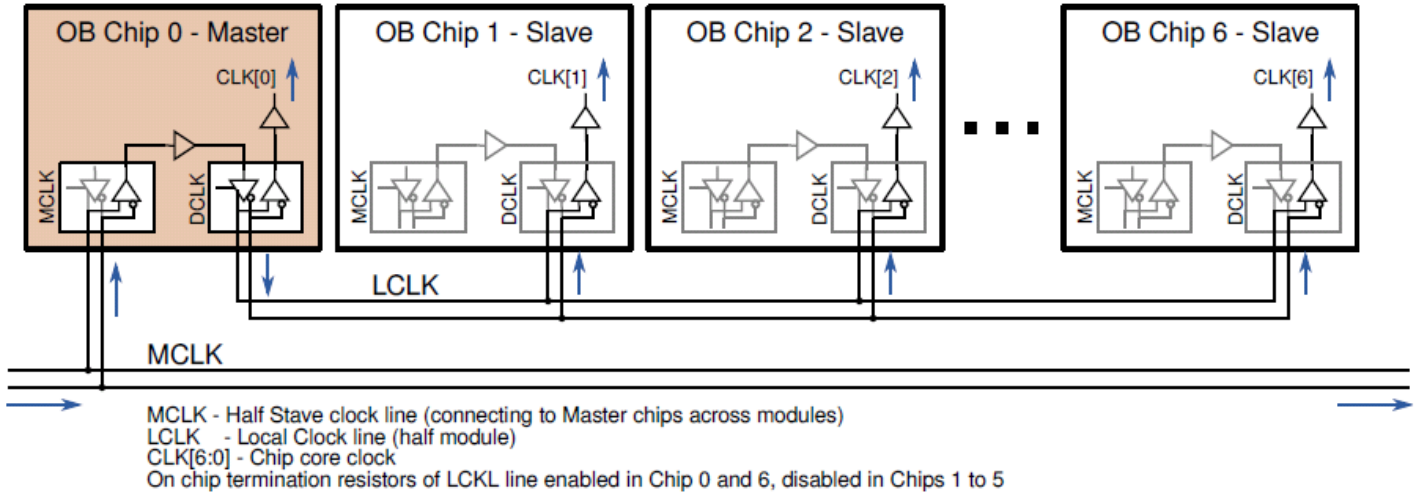
Refer to Application Note Appendix C of ALPIDE Operations Manual

Clock Distribution Diagrams

Inner Barrel Module



Outer Barrel Module



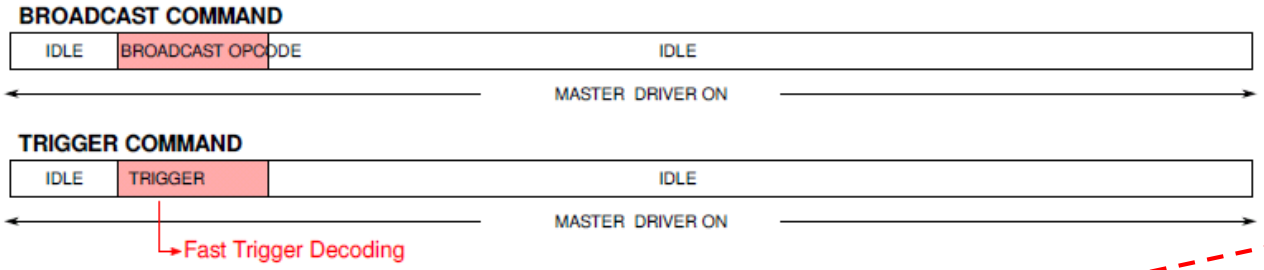
Refer to Application Note Appendix A of ALPIDE Operations Manual

CONTROL AND DATA READOUT

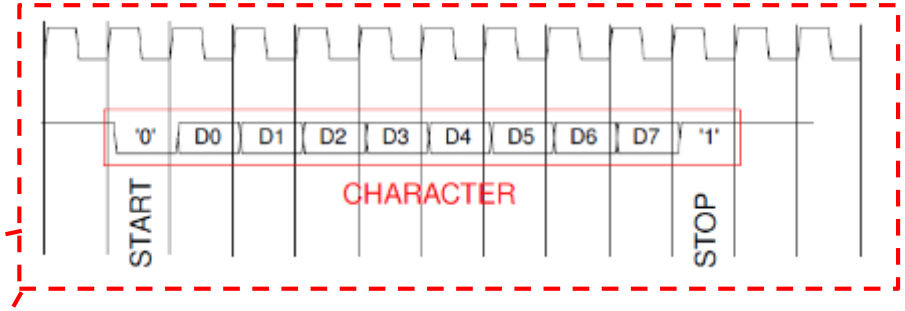
Control Transactions, Trigger, Broadcast Command

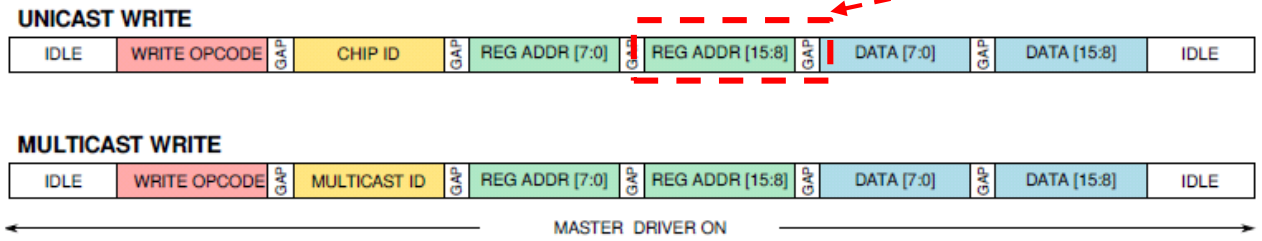
The slow control interface serves two purposes:

1. provide write and read access to internal registers, commands, configuration and memories (control and monitoring)
2. distribute trigger commands or other broadcast synchronization commands

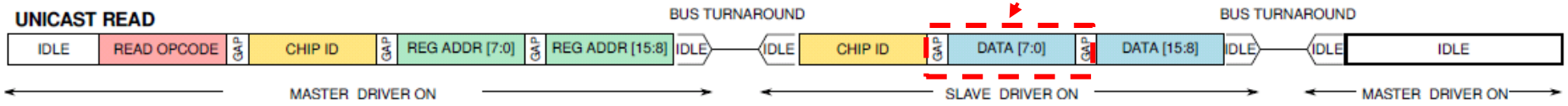


Transactions are composed of *characters*





(*) *Master* and *Slave* in these diagrams refer to the driver and the listener on the bus segment



Refer to User Guide section in ALPIDE Operations Manual for further details

Overview of the Slow Control Interface (read only)

The slow control interface serves two purposes:

1. provide write and read access to internal registers, commands, configuration and memories

2. distribute trigger commands or other broadcast synchronous signals

The ALPIDE chip has two ports to implement the slow control functionalities: a differential DCTRL port and a single-ended CTRL port. The port that is actually functional depends on the operating scenario. In Inner Barrel Chip role only the differential DCTRL port is used. In Outer Barrel Master role both ports are operated. In Outer Barrel Slave role only the single ended CTRL port is used.

The slow control interface and the ports have been designed to implement a **hierarchical control bus topology with multi-point connections of chips on the same electrical line**.

The nine (9) chips on **an Inner Barrel module** are directly connected to a shared control differential line using the DCTRL port. The Inner Barrel control bus is entirely based on differential signaling and it has multipoint topology.

On **Outer Barrel Staves**, the control bus is implemented with a hierarchical structure. Every Module *Master* chip is connected with other Master chips on the same half-stave by a differential shared bus with multi-point topology. The differential line crosses the module boundaries and can connect 4 (Middle Layer Stave) or 7 (Outer Layer Stave) Module Master on the same row along the z axis.

Each Outer Barrel Master chip acts as a **slow control hub and relays the control transactions to** six Outer Barrel *Slave* chips that are connected in a multi-point shared line topology with the Master. The bus segment local to the Outer Barrel Module operates with **single-ended signaling through the CTRL port**.

Inner Barrel modules and Outer Barrel modules present to the off-detector hardware fully equivalent control interfaces, physically appearing as a differential multi-point bus.

The control interface supports bi-directional, half-duplex communication: data are exchanged in both directions but not simultaneously.

The signaling on the control buses is serial and synchronous with the system clock (nominal 40.08 MHz, LHC clock) that is distributed through a hierarchical clock tree.

The slow control transactions are governed by the off-detector hardware initiating all type of messaging on the control bus. All chips have clocks derived from the same system clock and continuously sample the incoming serial control stream, decoding the transactions on the bus. The deserialization and the decoding of the control messages are executed at corresponding clock edges in all chips.

The ALPIDE control interface has been designed with support of DC balanced signaling on the DCTRL port for applications that require or can benefit of AC coupling of the DCTRL line. This is obtained using Manchester encoding for the serial characters transmitted by the chips, following the IEEE8 802.3 convention for the bi-phase symbols. The transmission of control responses on the DCTRL line using Manchester coding is enabled by default (post-reset value) but can be disabled in the chip configuration space. The off-detector electronics can also signal using Manchester encoding, this being transparent to on-chip circuits. The chips sample the control bus on the clock rising edges, therefore it is the electrical value seen on the bus at those sampling edges that is used by the logic of the chip control module.

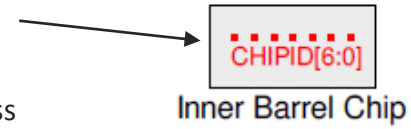
Refer to ALPIDE Operations Manual for further details

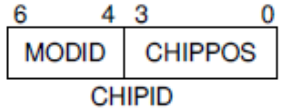
Chip Identification over Modules

CHIPID[6:0] input port

Sets Operating mode

Defines control address



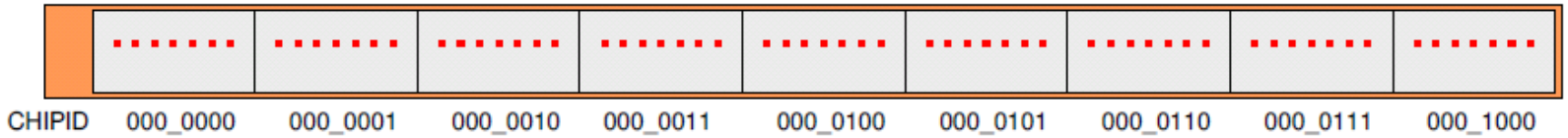


CHIPID[6:4] – Module identification field

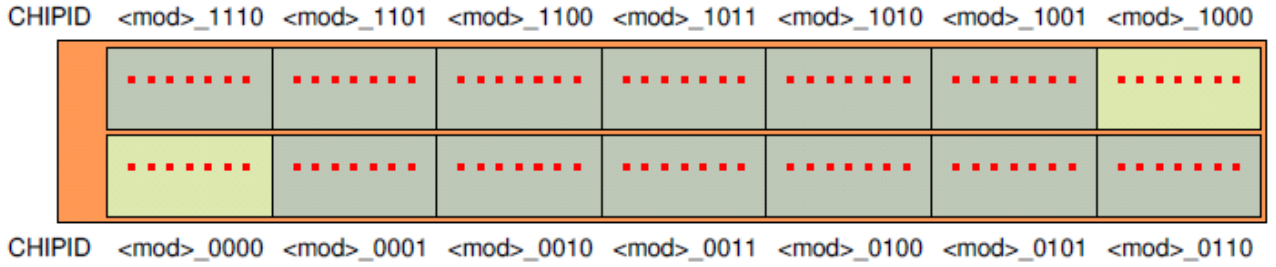
CHIPID[3:0] – Chip identification field

Default assignments of CHIPID values on one Inner Barrel Module and on a generic Outer Barrel Module.

INNER BARREL MODULE



OUTER BARREL MODULE



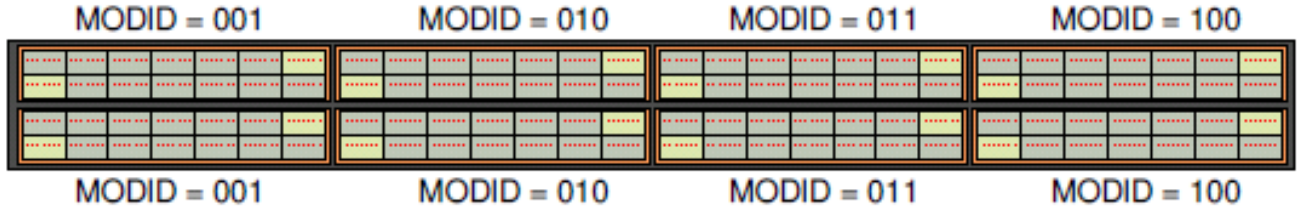
For ITS MIDDLE LAYERS <mod> is one of: {001, 010, 011, 100}

For ITS OUTER LAYERS <mod> is one of: {001, 010, 011, 100, 101, 110, 111}

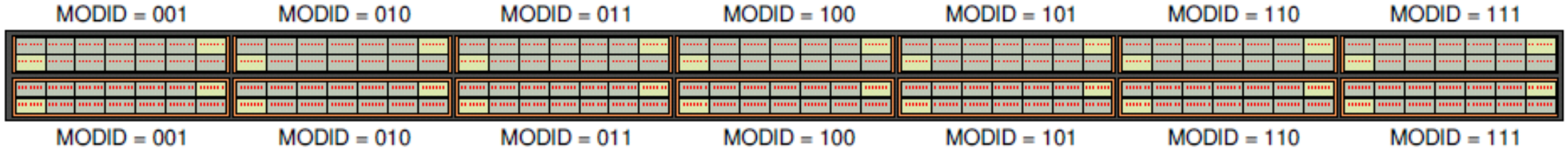
Chip Identification over Staves

Default assignments of Module Identifier fields for the Middle Layer Stave and Outer Layer Stave

MIDDLE LAYER STAVE



OUTER LAYER STAVE



Matrix Readout Sequences

Frame STROBE cycle

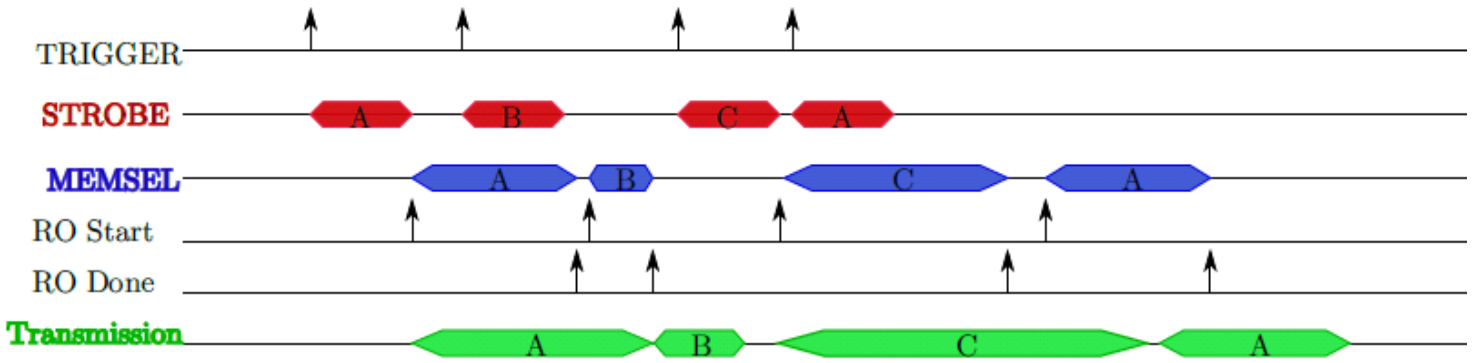
1. Trigger received
2. Assert STROBE to next available bank
3. Commit CHIP HEADER and event time-stamp when strobe de-asserted

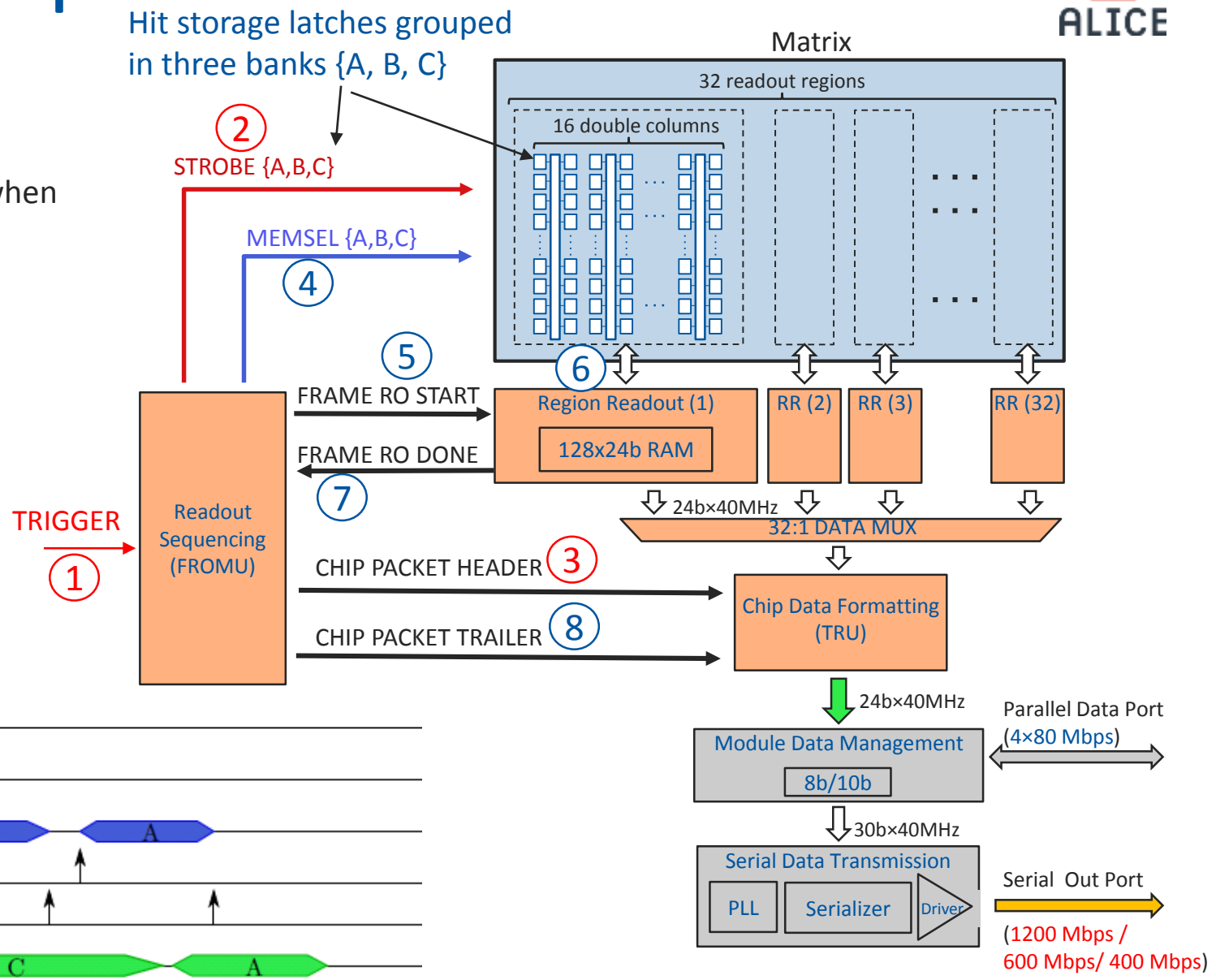
Rotate strobing pointer to following bank

Frame READOUT cycle

4. MEMSEL selects next bank to be read
5. Start Region Readout (FRAME_RO_START)
6. Matrix Frame Readout
7. FRAME_RO_DONE when finished
8. Commit CHIP TRAILER (with status flags)

Rotate reading pointer to following bank





Triggered and Continuous Readout Modes

Triggered Mode chip setting

- Short and randomly distributed strobing (integration) intervals
  - Typical scenario: external trigger commands and STROBE duration Θ(400 ns)
- Internal STROBE is not generated for new incoming triggers when MEB banks are full, need to wait for completion of matrix frame readout (priority to earliest events)
  - TRIGGER commands received while BUSY are still acknowledged queuing for transmission a Chip Empty Frame packet

Continuous Mode chip setting

- Longer and periodic strobing intervals
  - Duration Θ(1 us) or longer
- *Flush* oldest pending matrix frame when MEBs banks are becoming full and make space to start new STROBE interval (priority to latest framing interval)

Generation of internal STROBE

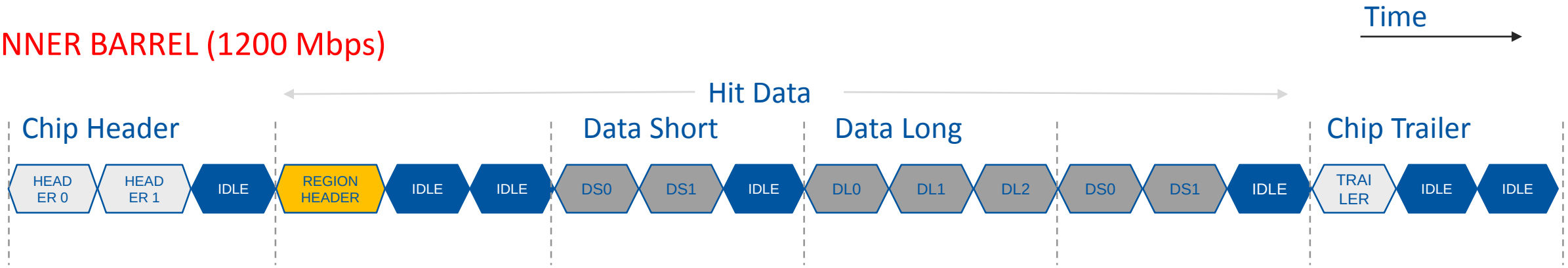
- Duration programmable 50 ns -> 1.6 ms *(for both chip readout settings)*
- External commands (trigger) or internal sequencer *(for both chip readout settings)*

BUSY condition

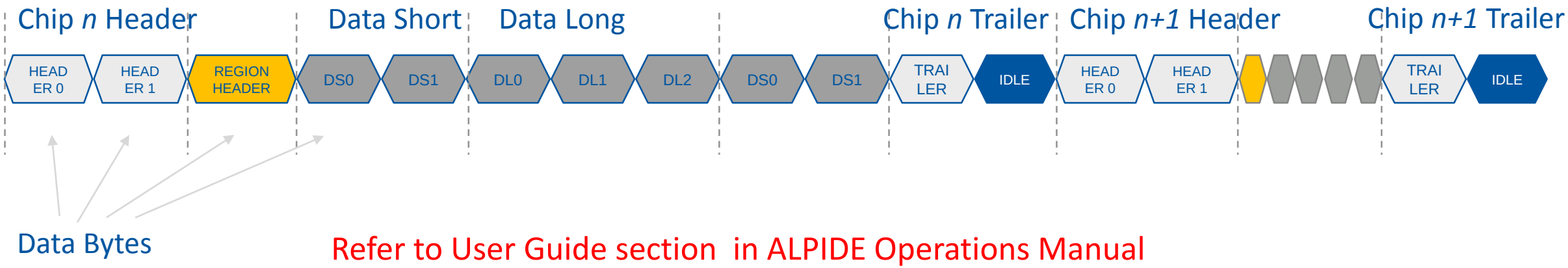
- Triggered Mode: *MEBs full* or *periphery FIFOs almost full*
- Continuous Mode: *MEBs almost full* or *periphery FIFOs almost full*

Output Data Streams

INNER BARREL (1200 Mbps)



OUTER BARREL (400 Mbps)



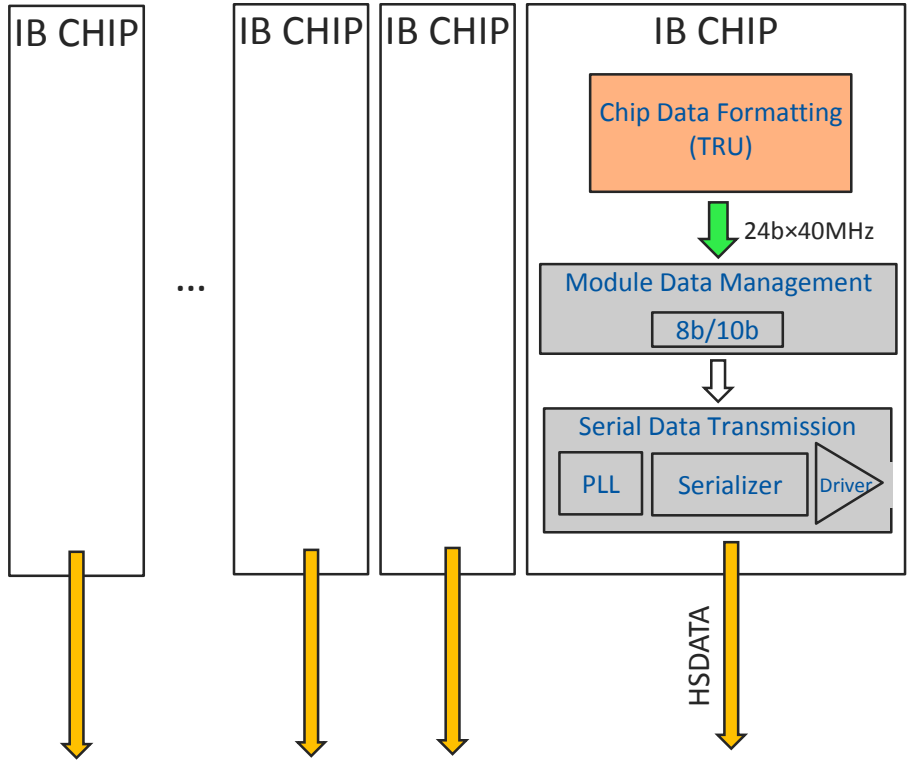
Refer to User Guide section in ALPIDE Operations Manual

Data Transmission Inner Barrel

INNER BARREL Chip

- Each chip has its own HSDATA serial link driven by the chip Data Transmission Unit
  - Programmable line rate: 1200 Mbps (default) or 600 Mbps or 400 Mbps
- Chip Data Packets are 8b/10b encoded and serially transmitted

Inner Barrel Module
Data Readout Scheme



Data Transmission Outer Barrel

OUTER BARREL Chips

OB Master and OB Slave chips send out their data, in turn, on the local shared DATA bus

- 320 Mbps throughput
- Time-division multiplexing with token exchange based on the protocol

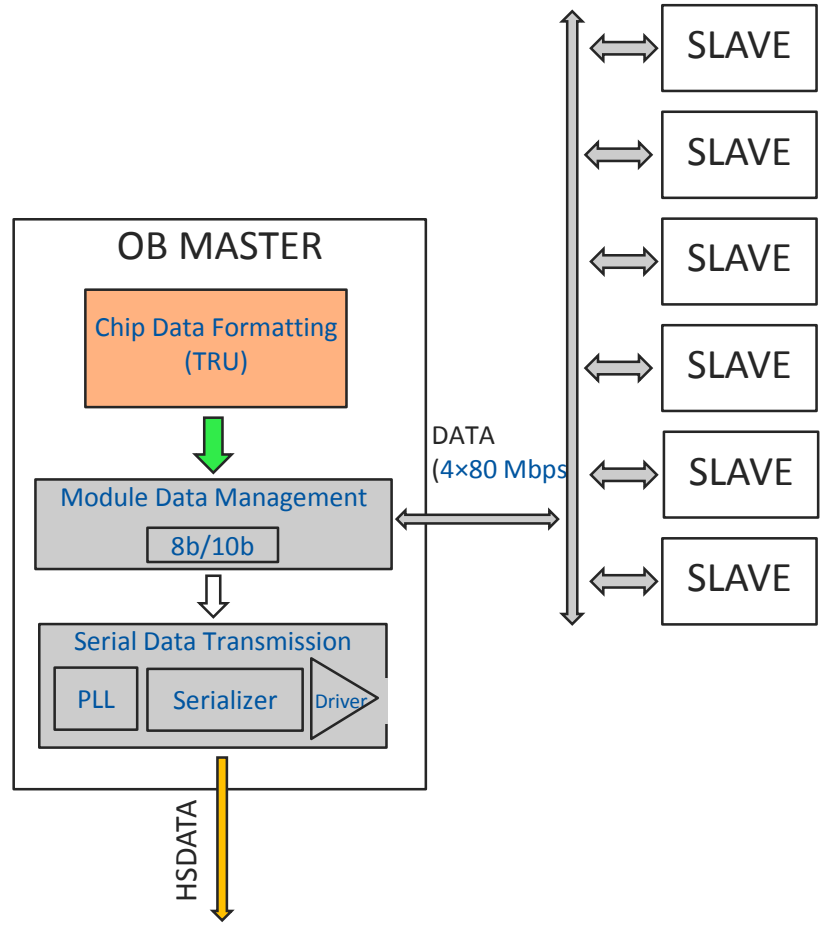
The Master chip continuously samples the local DATA bus and *forwards (*copies*)* the byte stream to the HSDATA serial output

The Data Transmission Unit of the Master retransmits with 400 Mbps line rate

- 8b/10b encoding is also executed in the Master

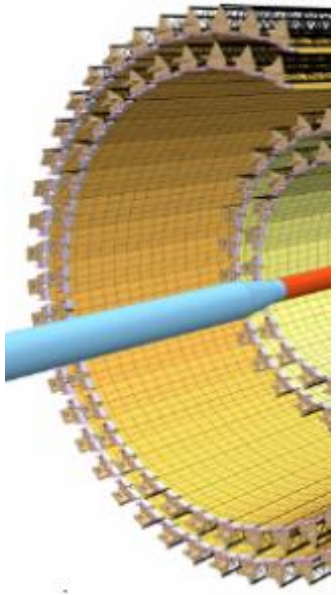
Slaves *do not* use the HSDATA serial output (DTU off)

Outer Barrel Module
Data Readout Scheme



ADDITIONAL REFERENCE MATERIAL

Readout System



Central Trigger Processor (CTP)

Trigger

Passive optical splitting, no busy back

Inner Layers

CLOCK (40 MHz)

CONTROL (80 Mb/s)

Data (9* 960 Mb/s)

FPGA

FPGA

CONTROL

Data (max 9.6 Gb/s)

x 192

Outer Layers

CLOCK (40 MHz)

CONTROL (80 Mb/s)

Data (28* 320 Mb/s)

FPGA

FPGA

CONTROL

Data (max 9.6 Gb/s)

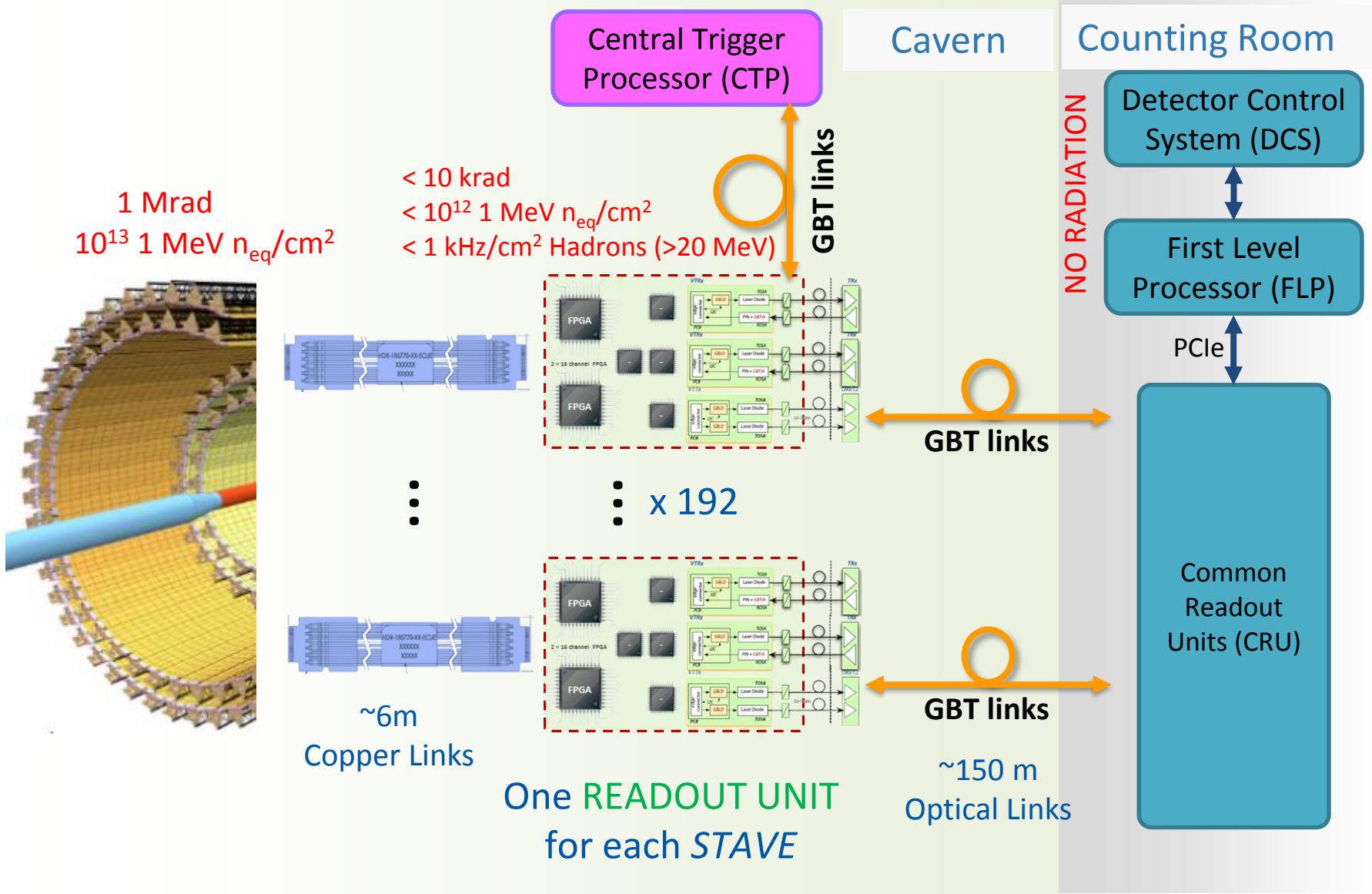
Common Readout Units (CRU)

One READOUT UNIT for each *STAVE*

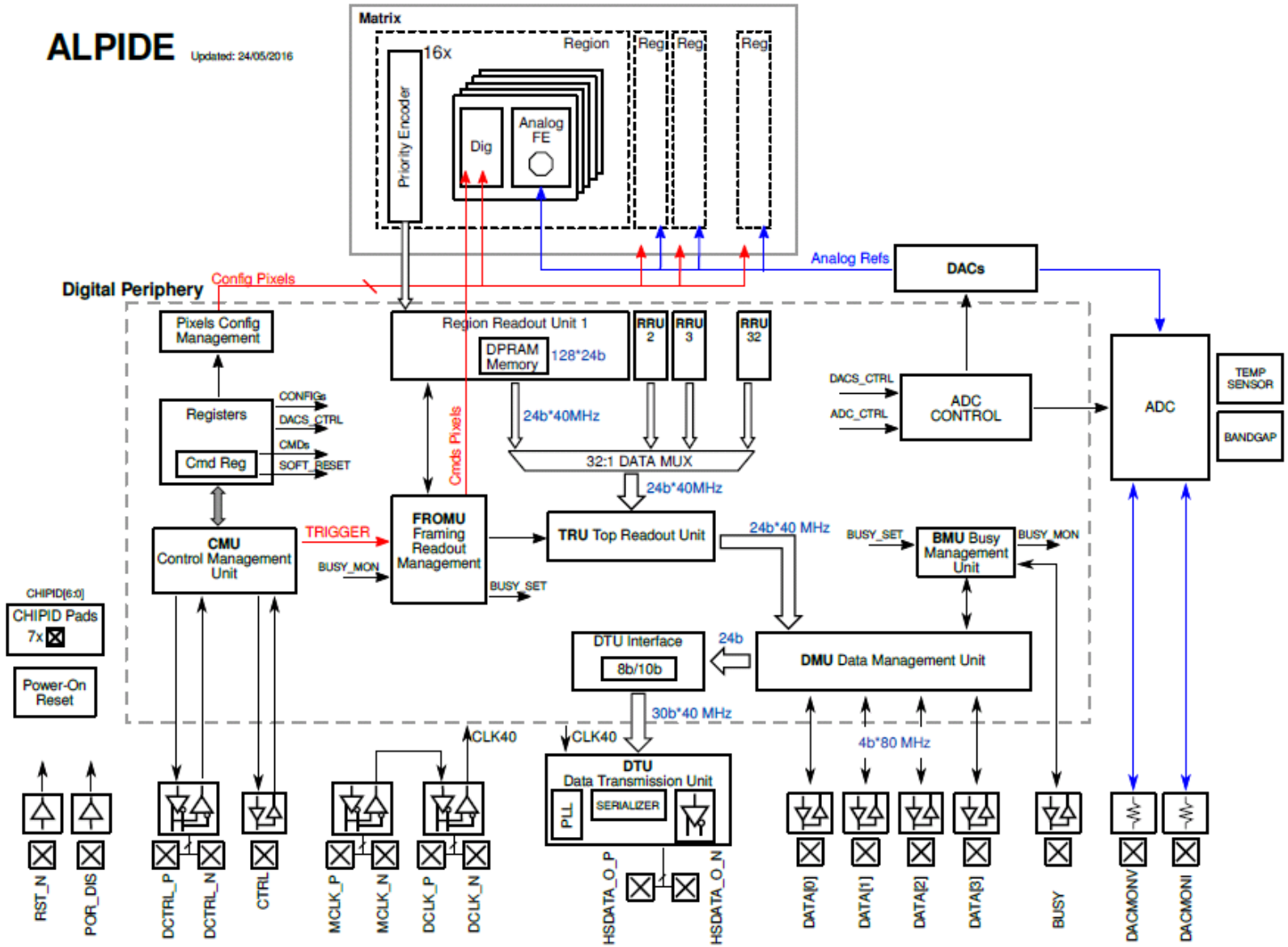
Cavern

Counting Room

Readout System



ALPIDE Block Diagram



Priority Encoder

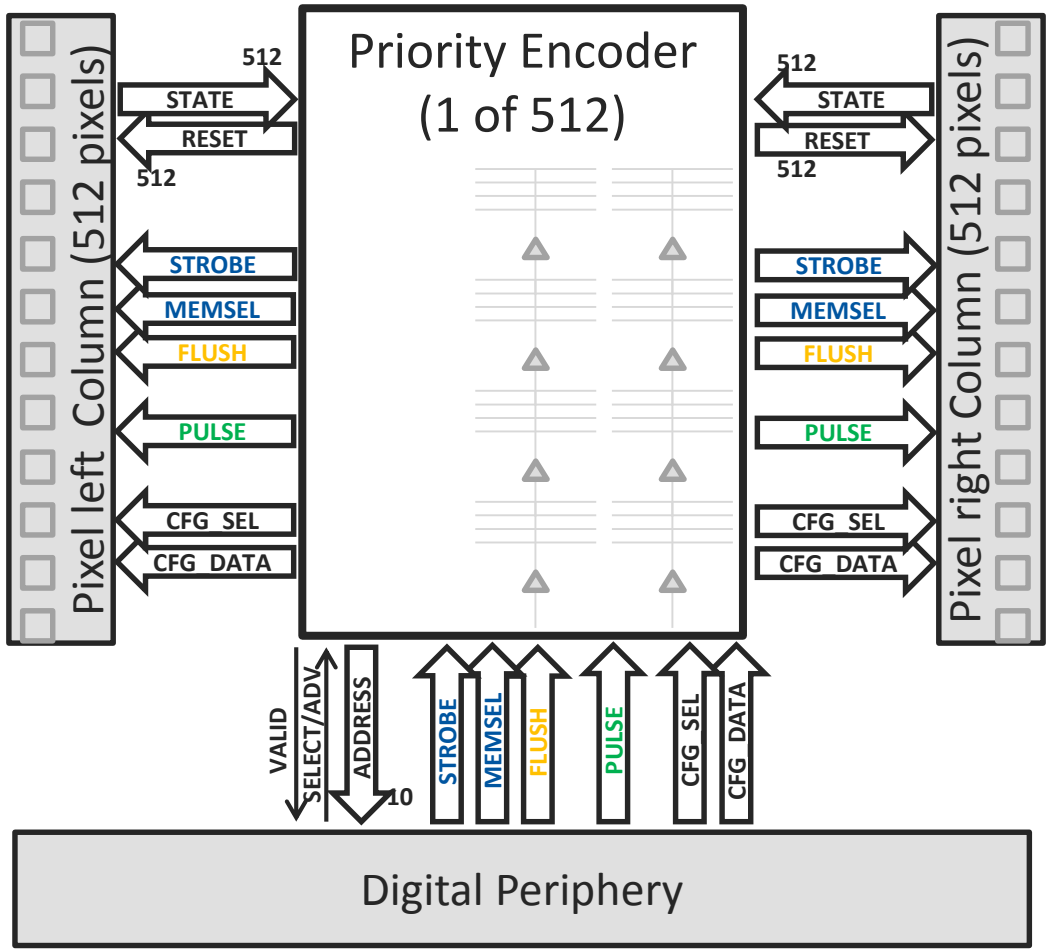
Encodes **ADDRESS** of first hit pixel of input **STATE** vector

Forwards **RESET** to hit pixel

Buffers global signals

STROBEs, MEMSELs, FLUSHs, PULSEs

Buffers **pixel configuration** signals



Digital Periphery Modules (1)

ALPIDE Updated: 24/05/2016

Pixels Configuration Management

Decoding and *Writing* into In-Pixel configuration registers

Top **Registers**

Configuration registers of all modules
Command register

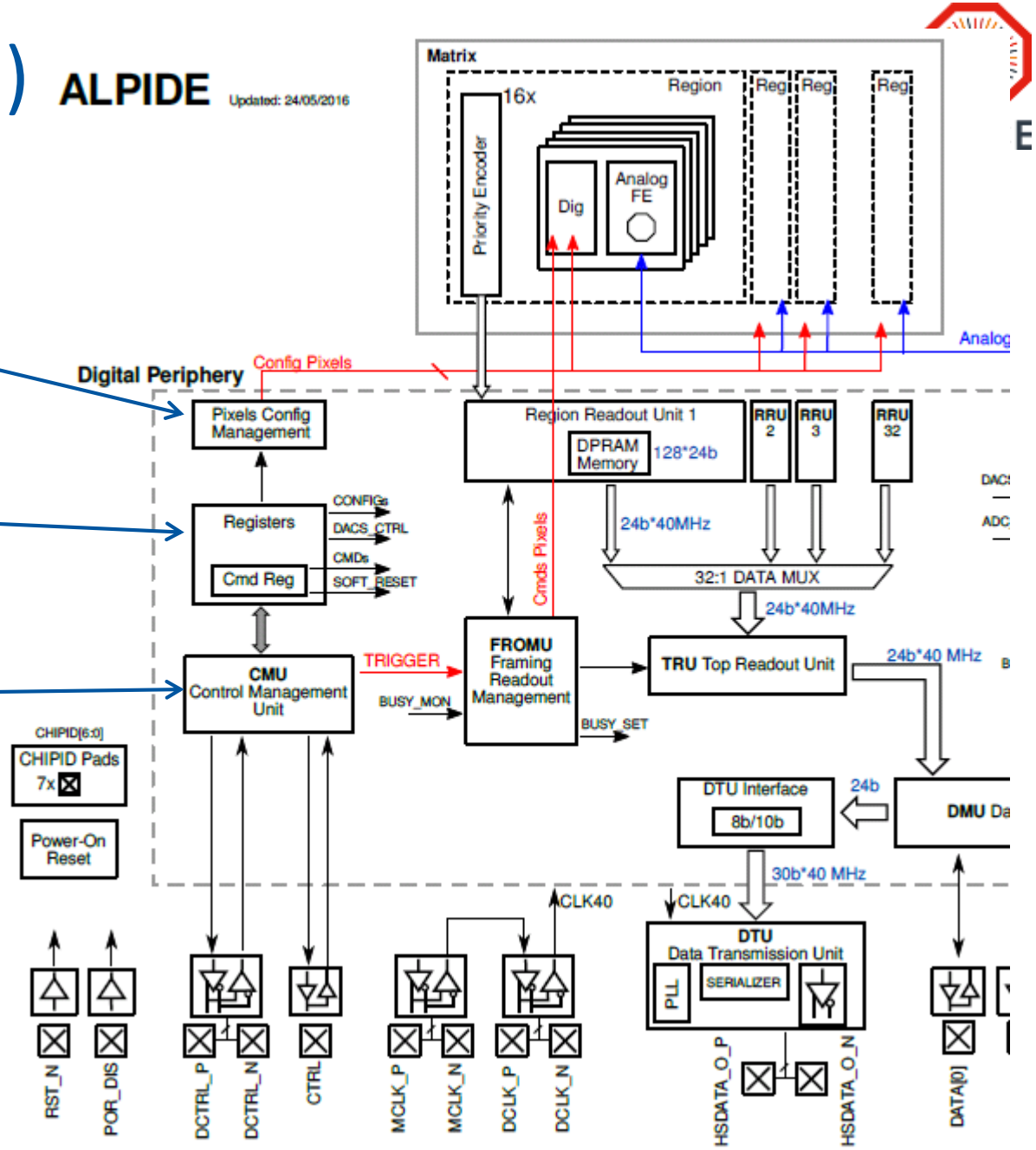
CMU Control Management Unit

Implementation of the control interface and protocol

Both on the link to the off-detector electronics and locally between OB Master and Slaves

Receiving of broadcast commands

Triggers, synchronize, resets



Digital Periphery Modules (2)

ALPIDE Updated: 24/05/2016

FROMU Framing and Read Out Management Unit

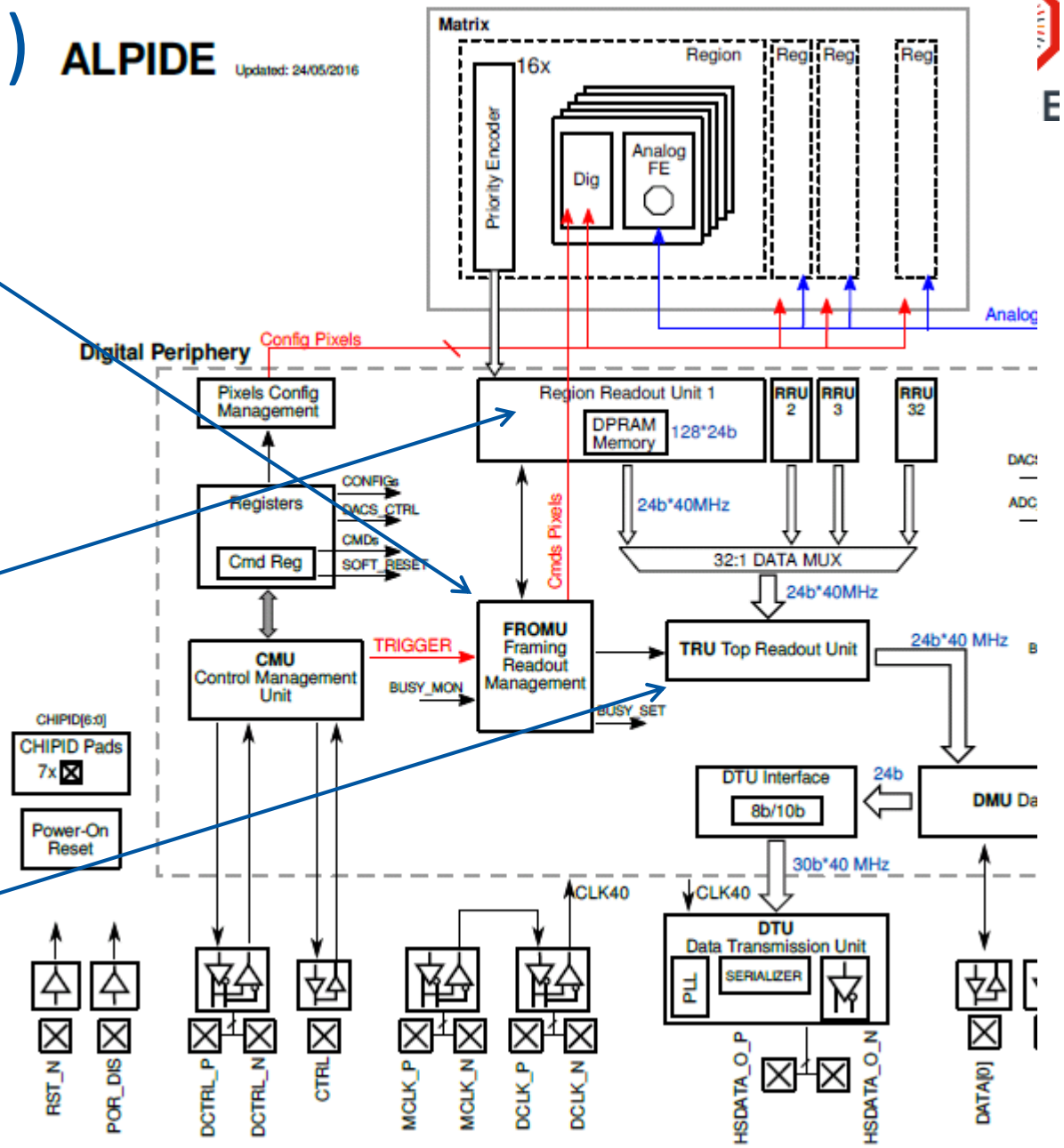
- Sequencing of frames *strobing* and readout phases
- Multi-event memory handling
- Programmable readout modes (*triggered*, *continuous*)
- Strobe duration control
- Time stamping of frames
- Flagging of anomalous conditions

RRU Region Readout Unit (32)

- Transfer of pixel hit data from in-pixel MEB memories to periphery memory
- Sequencing of Priority Encoders
- Data formatting and data reduction

TRU Top Readout Unit

- *Chip Data Frame* assembly and formatting
- Sequential reading of up to 32 Region Data Frames



Digital Periphery Modules (3)

BMU Busy Management Unit

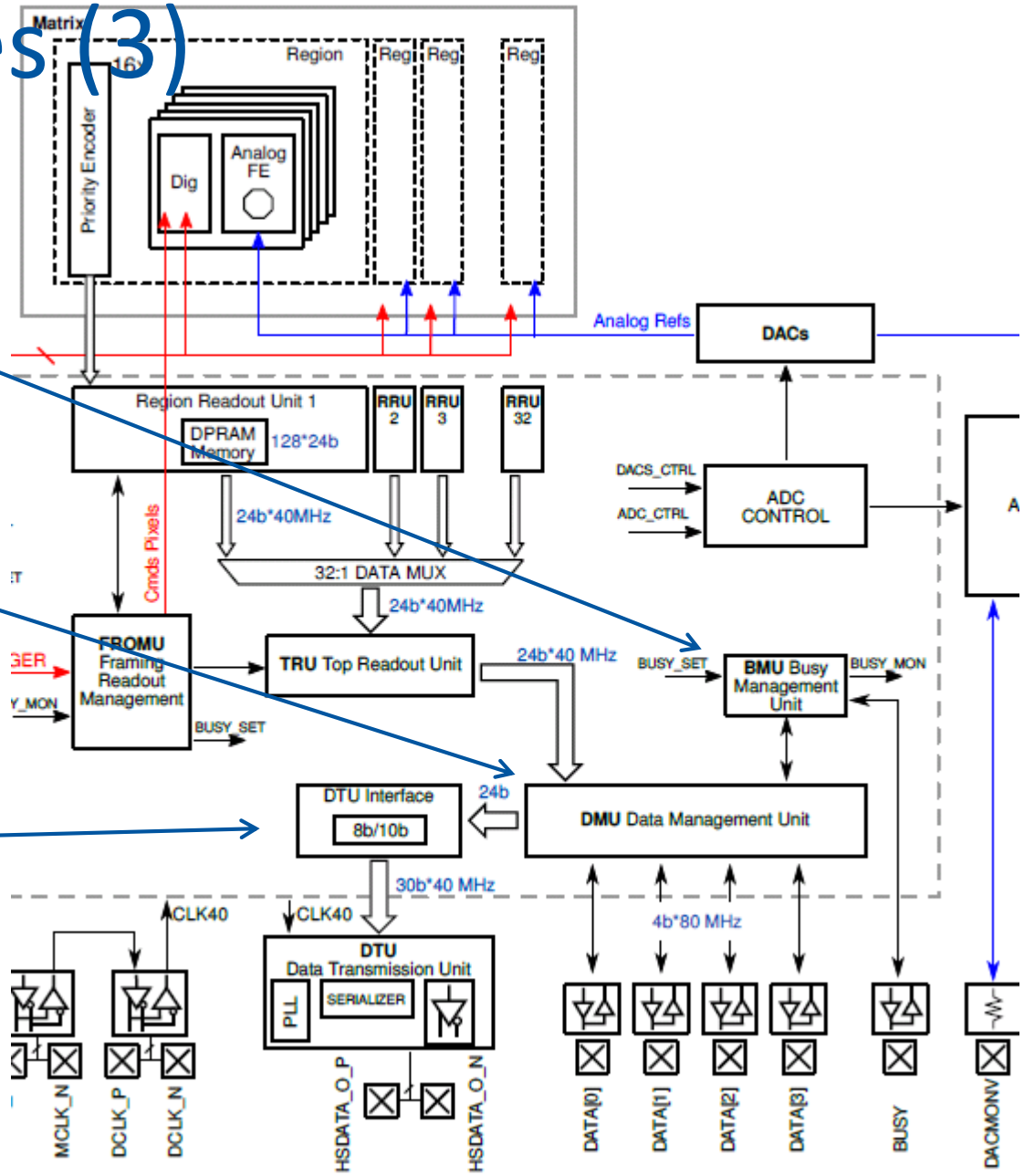
- Driving and sampling of BUSY line (configurable)
- Requests of transmission of BUSYON/BUSYOFF code words on the output data stream

DMU Data Management Unit

- Data exchange between OB Slaves and OB Master chips
- OB module local DATA bus sharing protocol (*token* passing)
- Double Data Rate logic

DTU Logic

- 8b/10b encoding
- Implementation of multi-rate serial transmission
- DTU monitoring functions
  - PLL monitoring and control
  - DTU test features



Full Custom Blocks

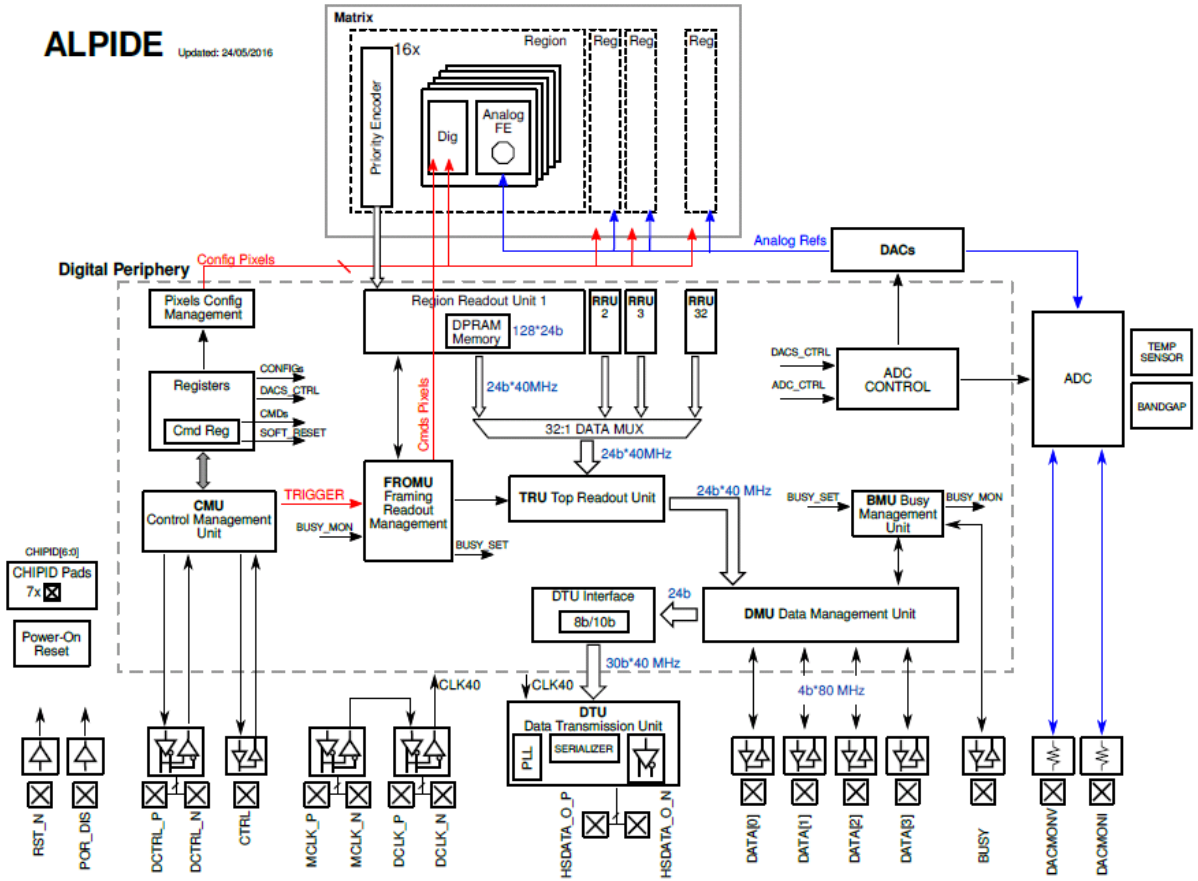
MLVDS Transceiver

- Differential ports (DCLK, MCLK, DCTRL)
- Fully controllable drive current

CMOS I/O pads

- Single ended CMOS bidirectional, tri-state
- ESD protections

Power On Reset



Analog **DACs**

- 11 internal DACs for the Analog Front-Ends
- Decoding inside digital periphery

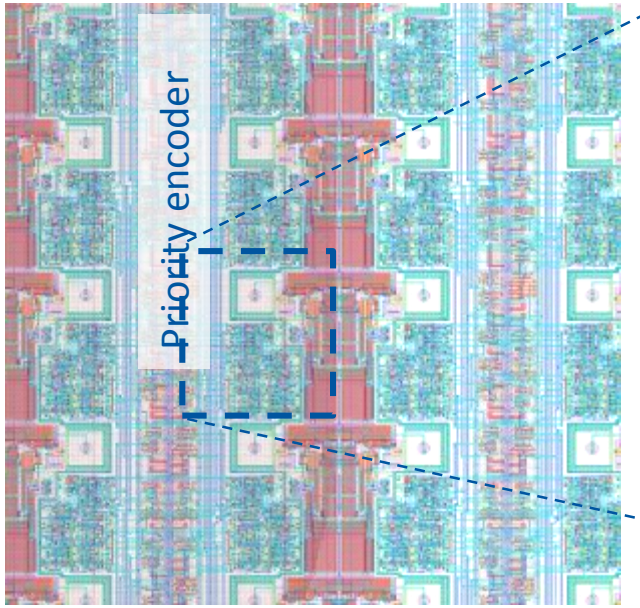
Bandgap Voltage Reference

ADC

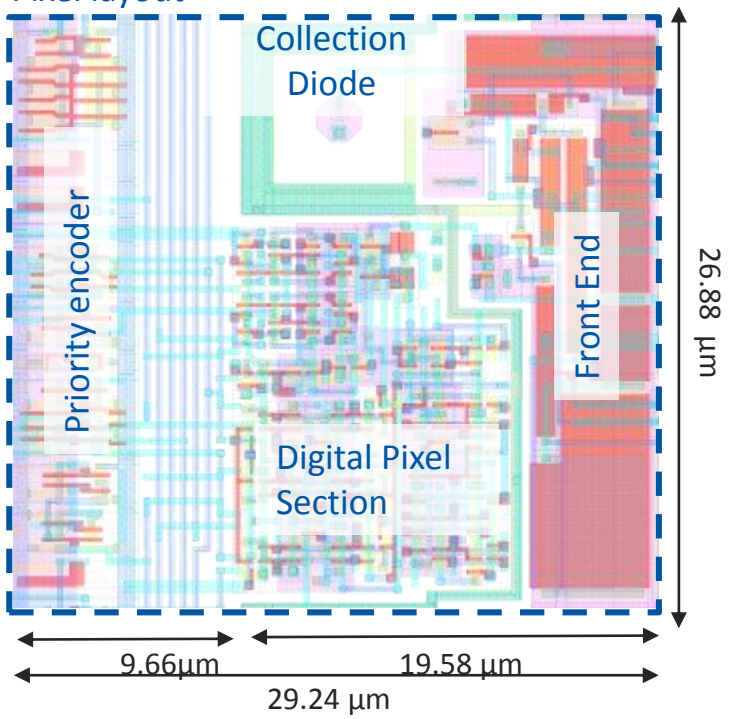
Temperature Sensing

Selected Layout Features

Matrix (detail)



Pixel layout



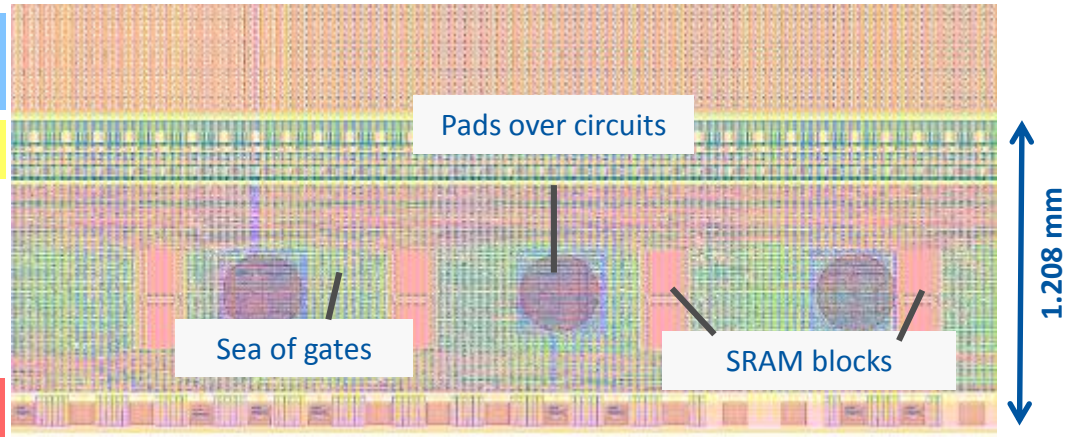
Periphery (detail)

Matrix - Pixels and Priority Encoders

Analog DACs

Digital Periphery

Regular pads + Custom blocks



Interface Signals

Table 2.1: ALPIDE interface signals.

Signal	Type	Direction	Purpose
MCLK_P	Differential (MLVDS)	INPUT	Forwarded clock input
MCLK_N	Differential (MLVDS)	INPUT	Forwarded clock input
RST_N	CMOS, internal pull-up	INPUT	Global chip reset
POR_DIS_N	CMOS, internal pull-up	INPUT	Power On Reset Disable
DCTRL_P	Differential (MLVDS)	BIDIR	Differential Control port
DCTRL_N	Differential (MLVDS)	BIDIR	Differential Control port
DCLK_P	Differential (MLVDS)	BIDIR	Main clock input and clock forwarding output
DCLK_N	Differential (MLVDS)	BIDIR	Main clock input and clock forwarding output
HSDATA_P	Differential (LVDS)	OUTPUT	Serial Data Output
HSDATA_N	Differential (LVDS)	OUTPUT	Serial Data Output
CTRL	CMOS, internal pull-up	BIDIR	Control port (OB local bus)
DATA[7]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
DATA[6]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
DATA[5]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
DATA[4]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
DATA[3]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
DATA[2]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
DATA[1]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
DATA[0]	CMOS, internal pull-up	BIDIR	Data port (OB local bus)
BUSY	CMOS, internal pull-up	BIDIR	Busy flag
DACMONV	ANALOG	OUTPUT	Voltage Monitoring Output
DACMONI	ANALOG	OUTPUT	Current Monitoring Output
CHIPID[6]	CMOS, internal pull-down	INPUT	Topological chip address
CHIPID[5]	CMOS, internal pull-down	INPUT	Topological chip address
CHIPID[4]	CMOS, internal pull-down	INPUT	Topological chip address
CHIPID[3]	CMOS, internal pull-down	INPUT	Topological chip address
CHIPID[2]	CMOS, internal pull-down	INPUT	Topological chip address
CHIPID[1]	CMOS, internal pull-down	INPUT	Topological chip address
CHIPID[0]	CMOS, internal pull-down	INPUT	Topological chip address

Clock ports (1)

DCLK_P, DCLK_N

Main clock *input* and forwarded clock *output*.

This is the chip internal clock source regardless of the operating mode and configuration scenario. In all configurations the receiver circuit at this port provides the clock to the chip core.

A chip configured as Outer Barrel Module Master sets the driver on this port *active* and forwards on it the signal received on the MCLK P, MCLK N port. On-chip line termination is provided by the Master and the furthermost Slave chip.

Characteristics

Nominal clock frequency: ~40.08 MHz (LHC BC)

Differential transceiver

- MLVDS receiver electrical specification

One differential line can distribute clock to a set of chips

- Multi-drop topology on the same IB module

Clock ports (2)

MCLK_P, MCLK_N

Clock forwarding *input* port

Used to implement the clock distribution in the Outer Barrel Module application scenario. This is a receiving only port, the driver behind it being disabled in all scenarios. The receiver is enabled when the chip is configured as Outer Barrel Module Master and the signal applied to this port is then forwarded to the DCLK_P, DCLK_N port. A chip configured as Inner Chip or Outer Barrel slave chip keeps the receiver on this port disabled

Characteristics

Frequency: ~40.08 MHz (LHC BC)

Differential input

- MLVDS receiver electrical specification

One differential line can distribute clock to a set of chips

- Multi-drop topology across OB modules

Control ports

RST_N

RST_N: Global active-low reset signal. This port can be left unconnected in applications not needing a dedicated reset pin. The ALPIDE chip includes a power-on-reset circuit. The chip can also be reset by commands issued by the control interface.

POR_DIS_N

POR_DIS_N: Disabling of the power-on-reset circuit, active low. Driving low this input masks the output of the internal power-on reset circuitry. If the internal power-on-reset is used this pin can be left unconnected since it is internally pulled-up.

CHIPID

CHIPID[6:0]: Chip topological address and mode selection. This port is intended to assign a binary coded address to each chip depending on its position on the ALICE ITS Modules. The address is used in the transactions via the control interface. The address value also selects if the chip behaves as a Inner Barrel Chip, an Outer Barrel Master chip or an Outer Barrel Slave chip. These pads have been designed to be directly wired to digital supply in order to set a binary '1' on intended lines. Leaving a pad unconnected effectively sets to '0' the corresponding input by the internal pull-down.

DCTRL

DCTRL_P, DCTRL_N: Differential bidirectional control port. Intended to implement the segments of the control bus between the Inner Barrel chips or the Outer Barrel Master chips and the off detector electronics. The DCTRL port is unused by a chip configured as Outer Barrel Slave Chip. The communication through this port is half-duplex. Signals are received or driven but not simultaneously.

CTRL

CTRL: Single ended, bidirectional control port. Intended to implement the local control bus segments between the Outer Barrel Master chip and the associated slaves. These chips shall have their CTRL ports directly connected by a single shared wire. The CTRL port is unused by a chip configured as Inner Barrel Chip. The communication through this port is half-duplex. Signals are received or driven but not simultaneously.

Data readout ports

HSDATA

HSDATA_P, HSDATA_N: Differential data output port. This port is used for the high speed serial transmission of data between chips and the off-detector electronics. It is used by chips configured as Inner Barrel Chip or Outer Barrel Master. The signaling rate on this port is programmable in the Inner Barrel Chip operating mode, selecting between 1.2 Gb/s (default), 600 Mb/s or 400 Mb/s. The signaling rate is 400 Mb/s in the Outer Barrel Master configuration. The serial stream is 8b/10b encoded.

DATA

DATA[7:0]: CMOS bidirectional data port. Intended to implement a shared parallel data bus between the Outer Barrel Slave chips and the associated Master chip. By default, the 4 lowermost lines of this port operate in Double Data Rate mode, with bits launched or sampled at both clock edges and one complete byte transfer completed at every clock cycle. Thus the uppermost 4 bits can be left unconnected and the bus can be implemented using 4 parallel wires shared by the chips. Optionally, the chips can be configured to revert to Single Data Rate signaling also on the lowermost 4 bits. In this case one byte is launched or sampled at every rising edge of the clock. This operating mode can be used for readout of chips through a 8 bit Single Data Rate parallel bus.

BUSY

BUSY: Single ended port. It is intended to implement the communication of the BUSY state between the Outer Barrel Slaves and the associated Master chip by wiring in parallel all their BUSY ports. This port is not used when the chip operates as an ITS Inner Barrel chip. This port can be in one of two states: actively driven low or high impedance, thus emulating an open-drain topology. The signaling is active low. The pad provides weak internal pull-up. An external strong pull-up resistor might be required to speed-up the rise-time of the de-assertion (rising) edge depending on the total capacitance of the line and the number of chips connected to it. The sampling of the input on this port is equipped with a sychronizer.

Analog Monitoring Ports

DACMONV

DACMONV: Analog pin with dual functionality. It can be used to monitor each of the voltages generated by the on-chip voltage DACs. It can also be used to override the internal voltage DACs. The overriding is possible for one user-selectable DAC at a given time.

DACMONI

DACMONI: Analog pin with triple functionality. (a) Monitoring of the currents generated by the on-chip current DACs. (b) Override of the internal current DACs. The overriding is possible for one user-selectable DAC at a given time. (c) Override of the chip internal current reference, thus changing the range of all current DACs simultaneously.

Supply, Ground and Bias Nets

Supply/Ground or Bias Domain	Purpose
AVDD/AVSS	Supply and ground nets of the analog domain. This includes the pixel front-end circuits, the analog biasing circuits (DACs), the ADC block.
DVDD/DVSS	Supply and ground nets of the digital domain. This includes the in-pixel configuration registers, the matrix readout circuits, the peripheral readout circuits and the chip input and output buffers and transceivers.
PVDD/PVSS	Supply and ground nets exclusively dedicated to the Phase Locked Loop of the Data Transmission Unit.
PWELL	Bias of the p-type wells in the pixel matrix region
SUB	Bias to the substrate contacts in the seal ring and in the periphery region.

Chip Data Format

	Length	Binary coding
IDLE	8 bits	**1111_1111**
CHIP HEADER	16 bits	**1010**_<chip_id[3:0]>_<time_stamp[7:0]>
CHIP TRAILER	8 bits	**1011**_<readout_flags[3:0]
CHIP EMPTY FRAME	16 bits	**1110**_<chip_id[3:0]>_<time_stamp[7:0]>
REGION_HEADER	8 bits	**110**_<region_id[4:0]>
DATA_SHORT	16 bits	**01**_<hit_position[13:0]>
DATA_LONG	24 bits	**00**_<hit_position[13:0]>_**0**_<hit_map[6:0]>
BUSY_OFF	8 bits	**1111_0000**
BUSY_ON	8 bits	**1111_0001**

chip_id[3:0]

Indexing of the chip in a module.

time_stamp[7:0]

BUNCH_COUNTER[10:3]

region_id[4:0]

Index of the region

readout_flags[3:0]

0	BUSY_TRANSITION
1	FATAL (panic mode)
2	FLUSHED_FRAME (in continuous mode)
3	BUSY_VIOLATION (in triggered mode)

hit_position[13:0]

Location of pixel hit in the matrix

hit_map[6:0]

Topoogical hit map when clustering is used

Refer to User Guide section in ALPIDE Operations Manual

Triggering and transmission rate upper limits

Abs Max triggering rate (external trigger)

4 MHz – Constrained by control interface

Inner Barrel Link Data Bandwidth

960 Mb/s = 120 MB/s

Abs Max Rate of output *Empty Frames*:

r_{ib} * 6 bytes <= 120 MB/s => **r_{ib} <= 20 MHz**

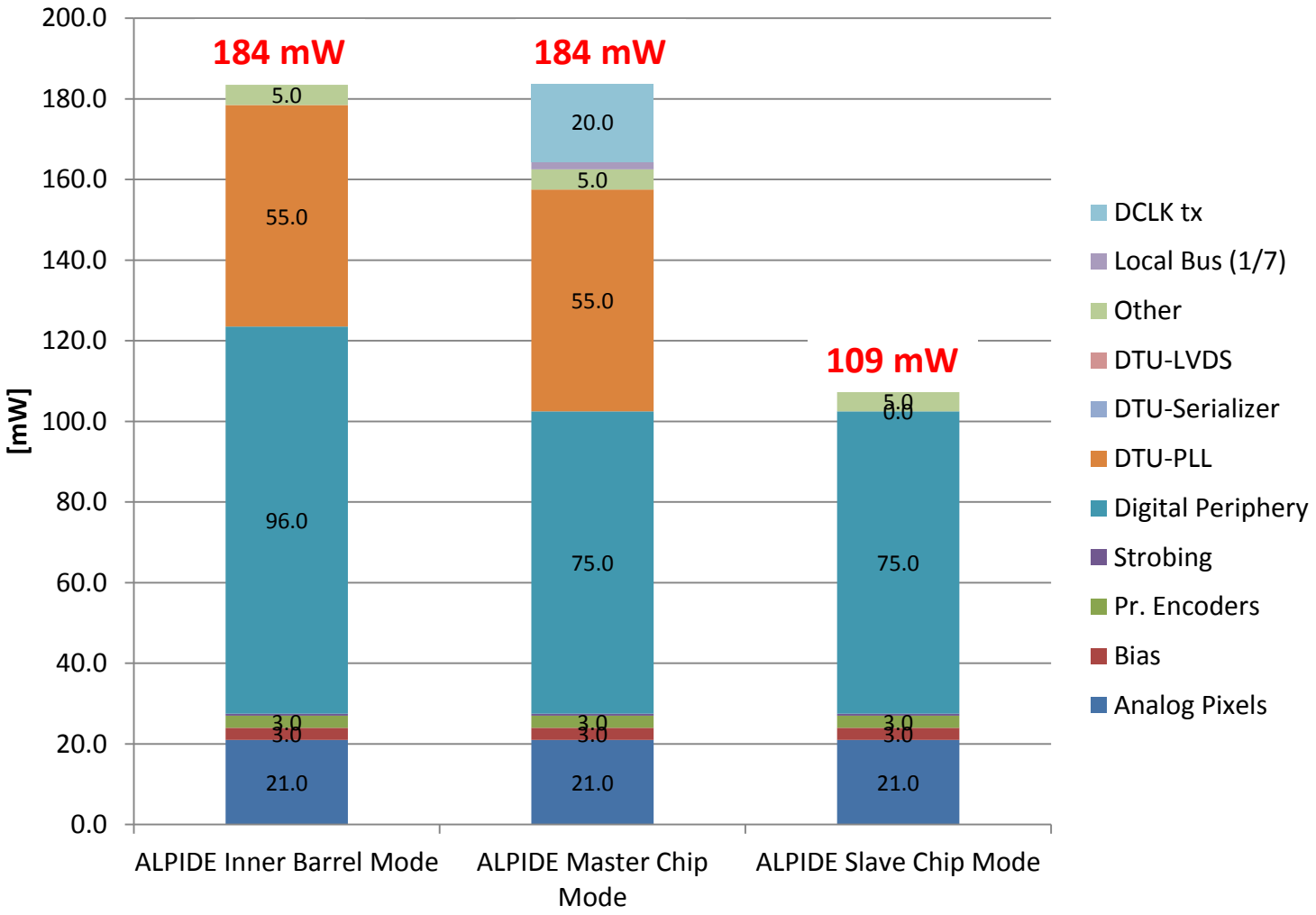
Outer Barrel Local Bus

320 Mb/s = 40 MB/s

Abs Max Rate of *Empty Frames*:

r_{ob} * 3 bytes * 7 chips <= 40 MB/s => **r_{ob} <= 1.9 MHz**

ALPIDE Power Consumption Breakdown



Inner Barrel: 41 mW/cm^2

Outer Barrel: 27 mW/cm^2

Data: combination of available measurements and simulations

Values scaled for readout at 100 kHz rates and max occupancies

Clock gating enabled