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Scientific Instrumentation

ITS upgrade

RUv2 changes

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Document History

Version	Date	Author	Section	Description
0.1	1-Dec-2017	M.J. Rossewij	-	First concept.

Contents

1 Introduction

This document contains a collection of possible changes and requirements to be applied on the RUv1 to come to the final RUv2 design.

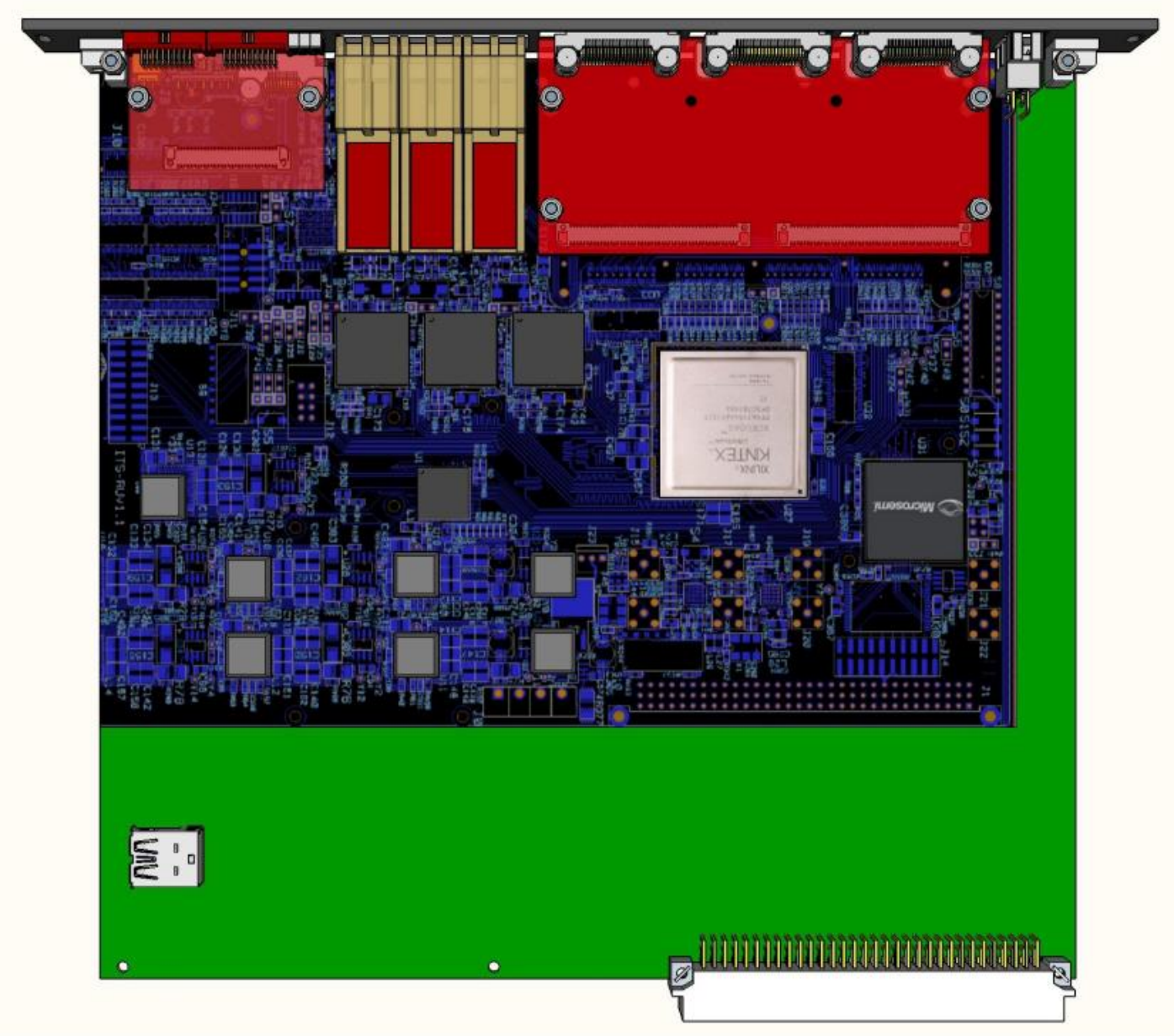
1.1 References

1. https://indico.cern.ch/event/693890/contributions/2846941/attachments/1583662/2503678/20180116_WP10_plenary_JS.pdf
2. http://project-dcdc.web.cern.ch/project-dcdc/public/DCDCmodulesDatasheets.html
3. https://indico.cern.ch/event/691944/contributions/2839653/attachments/1580297/2496998/WP10_2018_01_RUv1_VCCAUX.pdf
4. https://www.xilinx.com/support/documentation/user_guides/ug583-ultrascale-pcb-design.pdf
5. https://www.xilinx.com/support/documentation/data_sheets/ds892-kintex-ultrascale-data-sheet.pdf
6. https://twiki.cern.ch/twiki/bin/view/ALICE/FusingGBTx

2 Physical and connectors

2.1 Increase board width to 220mm

Proposal is to increase the RU PCB width from 160 mm to 220 mm (height remains 233.5 mm, VME 6U) to match Power Board.



2.2 RU board power input and move USB3 connector away from front pannel

Proposal is to introduce a Power plug on front panel, on "top" when used in standard VME crates, to match cabling layout in the crates/racks. It maintains ground and powering from back-side J1 connector, as in RUv1

To have sufficient space for above, this might imply that the USB3 connector is moved away from the front panel. Placing it under the transition-board can also be considered.

2.3 Change RU QFS <-> transition board QMS connector

The current transition board connector is a 208-pin samtec QFS/QMS-style connector. The mounting company indicated that they experienced difficulties to ensure all pins are properly soldered. Reducing the size of the transition-board connector (to e.g. 156 pins) improves manufacturability but does not provide sufficient space for the MFT.

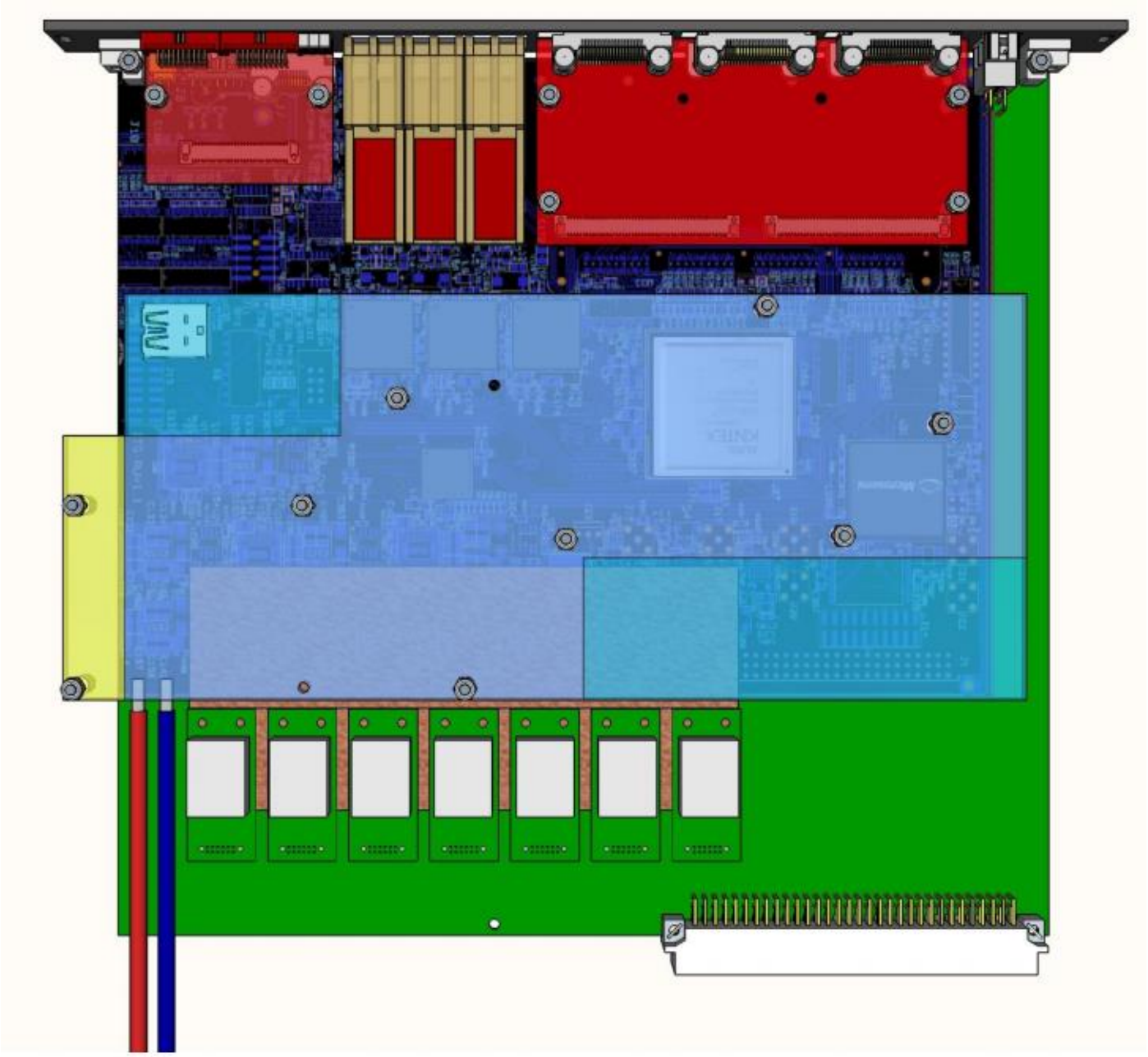
Below are the requirements for the different detectors:

		#clk/ctrl	#data	#pairs Clk+ctrl + MGT	#pairs Clk+ctrl+LVDS
ITS	IB	1	9	2 + 9 (conn1)	X
	MB	4	16	8 + 16 (conn1)	8 + 16 (conn2)
	OB	4	28	8 + 28 (conn1)	8 + 28 (conn2)
MFT	ID	3	11	6 + 11 (conn1)	X
	OD	5	25	10 + 25 (conn1+2)	10 + 25 (conn2)

The table below shows possible alternatives:

Pitch mm	RU	$	edgeConnector	$	#	# pins	Width mm	Hight	Speed Gbps
0,5			Not at Samtec						
0,635	QFS-104-01-SL-D-RA	20,19	QMS-104-01-SL-D-EM2	15,95	1	208	98	4,1	11
	QMS-104-01-SL-D-RA	19,94	QFS-104-01-SL-D-EM2	16,40			101		
	MEC6-150-02-X-D-RA1	6,08	PCB	0	2	200	78	3,5	14
	QFS-052-01-SL-D-RA	14,71	QMS-52-01-SL-D-EM2	11,62		208	111	4,1	11
	QMS-052-01-SL-D-RA	14,52	QFS-52-01-SL-D-EM2	11,95			116		
0,8	ERM8-049-01-S-D-RA	7,94	ERM8-049-01-L-D-EM2	4,1		196	105	3,1	15
	ERF8-049-01-L-D-RA	6,94	ERF8-049-01-L-D-EM2	4,27					
	ERM8-060-01-S-D-RA	8,98	ERM8-060-01-L-D-EM2	4,63		240	122		
	ERF8-060-01-L-D-RA	7,85	ERF8-060-01-L-D-EM2	4,83					
	HSEC8-149-01-L-RA	5,08	PCB	0		196	102	3	13

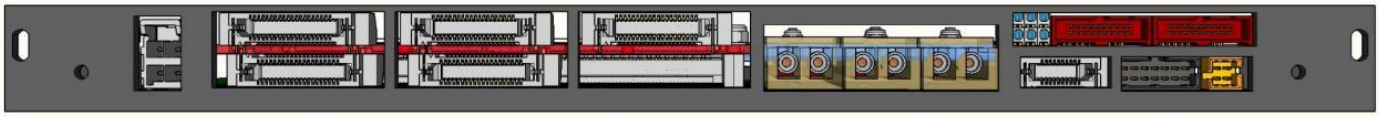
The ERF8/ERM8 are second sourced by Hirose.



It could be an opion to replace the single 208-pin samtec QFS/QMS-style connector with 2 ERF8/ERM8 connectors. T.B.I.

2.4 On transition board: Replace firefly with ERF8-style connectors

Possibility to modify the Transition Board to use latched, commercial connector. Awaiting offer from Samtec for completely commercial cable leg frm PP1 to PP2 (instead of custom-modified FireFly).



2.5 Default jumper positions

It is proposed to have all jumpers in the same position when installed in the experiment:

- 2-pin jumpers not placed
- 3-pin jumpers default 1-2

3 Power & current sense

3.1 Choice Power regulator (circuit)

The RUv1 employs 7 TI LMZ31710 DCDC regulators. These have been qualified for magnetic field and radiation [1, page 19]. After evaluating the test results it must be decided if:

1) Simply keep current regulator scheme.
2) Combine LMZ31710 DCDC with a LDO [1, page 21] to mitigate the most occurring SEU (i.e. power off glitches, once every 70 hours for the whole ITS).
3) Replace LMZ31710 with the low height (10mm) FEASTMP_CLP [2]: Vi=5…12, Vo=0,9…5, I_{CONT_MAX}=4A (ok, see Table 1).
4) Route both LMZ31710 and FEASTMP_CLP. Place only the regulator desired.

Rail	I (A) FPGA empty	I (A) FPGA loaded
V_{INT}=0,95	1,0	1,7
V_{MGT}=1	0,4	1,0
1V2	0,4	0,9
1V5	2,2	2,2
1V8	0,5	1,1
2V5	0,9	0,9
3V3	0,4	0,5

Table 1: Measured current requirements RUv1

For 2) and 4), the regulators from one rail (LDO+LMZ31710 or FEASTMP_CLP+LMX31710) should probably be kept together as crossing of planes is difficult considering that only 2 (5 & 6 from total of 10) layers are available for the planes. Board area is likely less of a problem.

3.2 Separate regulator for VCCAUX

Large jitter increase has been observed [1, page 24] on the DCLK output only during scrubbing and when using the MMCM. As the MMCM is powered by VCCAUX, this rail has been investigated more carefully. The RUv1 VCCAUX plane decoupling seems to follow the recommendations [3 page 3-12] and also simulations flags no problems. On RUv1, one 1V8 regulator is used for powering VCCAUX, VCCAUCMGT and the 1V8 IO banks. The XCU105 use 3 separate regulators for VCCAUX, VCCAUXMGT and the 1V8 IO banks. The KU040 powers VCCAUX and the IO banks from one regulator (allowed UG583 [4] page 219) and VCCAUXMGT from a separate regulator (following UG583 [4] page 103).

Later measurements [1 page 37] showed that also the KCU105 and KU040 have the similar large jitter increase, so the regulator sharing is probably not the cause of the "jitter issue". However, using a separate additional regulator for VCCAUX can still be considered. Likely a LDO going from 2.5V to VCCAUX gives least noise/ripple and power loss. The measured I_{CCAUX}=0,3…0,4A. Datasheet [5] states:
Typical quiescent supply current: ICCAUXQ+ICCAUX_IOQ=188+83=219mA
Power-on current=219+520=739mA

3.3 Functional added: remote (via GBT) repowering

It should be discussed if the RU should have an option to repower-up itself.

3.4 Remove AD8418 cap and replace 0-ohm resistor with permanent link

AD8418 now has a NP capacitor on its NC pin and a 0-ohm resistor to Vrefl. These components provide compatibility with the AD626 diff. amp. It can be considered to remove these parts completely.

3.5 Remove LMZ31710 inhibit resistors

The LMZ31710 inhibit input has resistors in series allowing them to enable/disable them individually. It can be considered to remove this functionality

4 PowerBoard interface, Xilinx, PA3 and Flash issues

4.1 Remove J1 PB interface and MLVDS buffers (U36/U37)

It is decided that the RU-PB connectivity goes via the front panel. So there is no need for a secondary path via J1. Proposal is to completely remove this path including U36 & U37. Also R315 and R316 can be removed by connecting U34/U35 RE directly to GND.

4.2 Functional change: PB I2C via SCA, PA3 or US

The Power boards I2C now comes from the Xilinx FPGA. It should be discussed if this is the best path or if SCA or PA3 are more suitable.

4.3 Replace ultrascale with kintex7 or ultrascale+

On RUv1 (and other boards with ultrascale devices), large jitter increase has been observed [1, page 24] on the DCLK output only during scrubbing. This effect was (nearly) not occurring with the Kintex 7. It could be considered to fall back to a Kintex7 device. Also checking jitter presence on a ultrascale+ device (using a dev board) could avoid redesigning RU for different FPGA family. For US+ compatibility, handle the signals on pins AM9, AK10, AJ10, AJ11.

4.4 Keep switch S6

Pressing switch S6 pulls ~programm signal low. As the Xilinx is configured in the slave select map mode (or JTAG), it does not result in a reconfiguration action. Should it be removed? No, It appears to be useful to bring FPGA in empty state.

4.5 Remove C323

Also C323 is not placed so the digital signals are not slowed down. Could be considered to be removed completely.

4.6 Remove inductors (@ FPGA)

The FPGA has decoupling ferrite beads close to the FPGA. It should be investigated whether these get saturated at 1T. If so, it could be considered to remove them as they it provide no noise reduction.

4.7 Fix: Done LED

The Done LED currently does not work because of the low (1,5V) Power supply. Add another switch like U28 (SN74AVC1T45DCKR).

4.8 Keep/Remove PA3 power on reset chip

Remove/Keep U38, PA3 power-on-reset chip? Used in TPC, so radiation testing not needed. => Keep. Change the PFI 2.5V divisions resistors to proper values.

4.9 Remove PA3 power on reset resistor

Remove/Keep R238. Johan reported that the single resistor power on reset does not work. Keep it?

4.10 Replace Flash PROM

Although also other parties have qualified the flash PROM for radiation, it can be considered to use another device for the following 2 reasons:

1) The Samsung Flash PROM is not in production anymore and could be difficult to obtain
2) These type of Flash PROMs require some mapping to exclude bad blocks. This complicates the PA3 design.

4.11 Replace CAN transceiver

The CAN transceiver has not been tested for radiation. Meanwhile, Intersil released a "low" cost radiation tolerant CAN transceiver (ISL71026MVZ). Depending on the price, it can be considered to change to this device.

5 Clocking scheme

5.1 Remove/keep jitter cleaner and independent clock to PA3

The question is if we really need the jitter cleaner. It should be tested first with the GBTx providing the machine clock to the RU.
If the cleaner is dropped, the PA3 automatically stays with a fixed local clock source.
If the jitter cleaner is required, the clock scheme might need to be reconsidered in order to provide the PA3 with a independent local clock source.
Also whether R342 should be placed must be evaluated.

5.2 Discuss crystal frequency

RUv1 now employs the IQD 160.3…MHz oscillator. Do we stay with this (high) frequency?

5.3 Remove L26 and/or L24

The 2.5V IQD 160.3…MHz oscillator seems to work properly. So there is no need for fallback solutions working on 3,3V. It can be considered to remove L26 and/or L24.

6 JTAG/configuration scheme and FX3

6.1 Remove secondary JTAG scheme

The RUv1 JTAG chain was designed to provide the following functionalities:

1) Programming the PA3 and/or Xilinx from SCA or JTAG-connector(s). In fact, the SCA-JTAG is the only path for (re)programming the PA3 remotely (e.g. after system installation).
2) Boundary scan: This could be helpful for testing connectivity during the production test. However, it became clear that the FX3 JTAG does not support boundary scan functionality (the FX3 JTAG is only intended as a debug interface for the FX3 internal processor). Also the GBTx JTAG is not supported by the GBTx development team. So it seems that the secondary JTAG chain does not provide any boundary scan functionality at all. So that leaves only the Xilinx <-> PA3 interconnectivity that can be tested by the primary boundary scan chain. So it can be considered to completely drop the secondary JTAG chain. This would also solve the voltage issue with the FX3 I2C PROMs:
    a. As the GBTx JTAG operate on 1,5V, it was decided operate all JTAG devices (Xilinx, PA3, GBTx/1/2 and FX3) on 1,5V. As the FX3 JTAG voltage bank is shared with the FX3 I2C PROMs (whose min. operation voltage is 1,8V), the bank is provided with a jumper for selecting the voltage (1V5 during boundary scan, 1V8 otherwise). In addition, the FX3 TDO has a series resistor limiting the fault current in case the jumper is in bad position.

6.2 Keep FX3/USB3 interface

Is it needed to keep the USB3 interface with the FX3 chip?

6.3 Replace FX3 dipswitch with single switch/slider

Dipswitch S9 provides too much flexibility in the FX3 setting. E.g. the FSL signals were intended to support different crystals-oscillators. In order to operate the FX3 properly with the oscillator installed, the 3 switches for the FSL signals need to be in the ground position. Moreover, the FSL signals are referenced CVVDQ which is now 3,3V whereas S9 switches to 1,8V (required for the mode signals). Proposal is to route the FSL signals directly to GND.

The FX3 power-up modes needed are:

PMODE[2:0]	Boot from
F11	USB
F1F	I2C, on failure USB

So by setting PMODE[2:1]="F1" and controlling PMODE[0] with a switch, all power-up modes can be set

So proposal is to replace FX3 dipswitch with single channel slider only for selecting proper boot mode

7 GBTX-SCA-VTXx

7.1 Remove GBTx fusing resistors

Investigate whether the resistors below really need to be removed for flashing the GBTx:

- Isolate SCA-I2C7 master: R277/R278
- Redirect 3V3 dongle power to GBTx involved: R279, R282 & R285

- Redirect programpulse to GBTx involved: R280, R283 & R286

The fusing procedure used so far is described on twiki [6].

Fusing was successfully without removing the SCA master. So it can be considered to have the SCA master permanently connected (so no R277/R278 positions at all).

It can also be tested if disconnecting fuse power and fuse pulse is really needed.

7.2 Discussion to hardwire the GBTx mode/I2C ID resistors

The GBTx mode and I2C ID are currently set by resistors. Does it stay like this or should it be hard wired?

7.3 Remove J42 (GBTx1 configuration selection I2C or EC)

As GBTx1 has no receiver connected, it can only be configured using I2C. So Remove/keep J42 (GBTx configuration selection I2C or EC) as no receiver is present?

7.4 Remove the VTRx/VTTx mod Abs resistors

As the RU is doing nothing with the module absence signals, it is proposed to completely remove the VTRx/VTTx mod Abs resistors.

7.5 Remove I2C3

Remove/Keep I2C3 to VTRx2 as VTRx–Tx is disconnected. On the other hand, it allows for reducing the power of the unused the laser diode. As alternative, the disable signal could be activated.

8 To be tested/qualified:

1) Configure PA3 via SCA JTAG => Johan
2) Employ GBTx/machine clock without using jitter cleaner
3) Saturation of ferrite beads in 1T
4) GBTx fusing: Removal fuse power/pulse resistors of non involved GBTx required?
5) Radiation tolerance:
    - U29: SN65HVD233-EP (CAN transceiver)?
    - U18: SI5316 (Jitter cleaner)

		Status	Status
2.1	Increase board width to 220mm	Do	Done
2.2	Front panel Power input	Do	Placed, waiting for approval pinassignment & exact location
	Remove J0 connector on the back	Do	Done
	Place jumper to disconnect power from J1	Use SPDT switch capable up to 5A	Done
	Location USB3 connector	Investigate under transition-board	Placed under transition board Should FX3 also be moved there?
2.3	Change RU QFS -> ERF8 transition board connector	Check assembly yield with loopback board & cable plug decision	ERF connectors placed MH still to be added
2.4	Replace firefly with ERF8-style connectors	Wait for input Piero/Samtec	Done (Solved on transition board)
2.5	Default jumper positions	Do	Done
		Enlarge pin1 identifier	Done
3.1	Choice Power regulator (circuit)	Investigate placement of both LMZ31710 and FEASTMP_CLP or maybe LDO	Baseline LMZ31710; Added placeholder for FEASTMP
3.2	Separate regulator for VCCAUX	Not possible from 2V5 rail as it comes later than 1V8 during the power up sequence. Keep as it is.	Keep as it is.
3.3	remote (via GBT) repowering	Not for ITS, maybe for MFT. TBI	Not Done. TBI
3.4	Remove AD8418 cap and 0-ohm resistor	Do	0-ohm removed, cap removed
3.5	Remove LMZ31710 inhibit resistors	Keep	Done
4.1	Remove J1 PB interface and MLVDS buffers	Remove (U36/U37)	Done
		Remove R315 & R316	Done
4.2	Functional change: PB I2C via SCA, PA3 or US	Keep as it is	Done
4.3	Replace ultrascale with kintex7 or ultrascale+	No, keep ultrascale device	Done
	Check ultrascale+ compatibility	Ignore US+ incompatibility (AM9, AK10, AJ10, AJ11)	Done
4.4	Keep switch S6	Remove	Done
4.5	Remove C323	Remove	Done
4.6	Remove inductors (@ FPGA)	Keep	Done
4.7	Fix: Done LED	Fix	Done
4.8	Keep/Remove PA3 power on reset chip U38/TPS3306	Keep	Done
	Change PFI input resistors to proper values	Do	Done. Used 487kΩ & 511kΩ
4.9	Remove PA3 power on reset resistor	Remove or Keep	Kept
4.10	Replace Flash PROM	1) Check availability => Available	Available ($10 @ 500 parts) Baseline: Keep Samsung FLASH
		2) Johan: Check PA3 implementation issue	
		3) Piero: Check for alternative	
4.11	Replace CAN transceiver	Check for quotes	Make compatible in layout
5.1	Remove/keep jitter cleaner	Check jitter cleaner needed for GBTx clock	Keep
	If jitter cleaner kept, change clock scheme for independent PA3 clock	TBD	Done

	Place R342 (select clock buff input from PA3)	TBD	Keep
5.2	Keep oscillator frequency 160.3…MHz	Order crystal oscillators	Ordered
5.3	Remove L26 and/or L24	Do	Done
6.1	Remove secondary JTAG scheme	Do	Done
6.2	Keep FX3/USB3 interface	Keep	Done
6.3	Replace FX3 dipswitch with single switch/slider	Do	FSLC removed from dipswitch
7.1	Replace R277/R278 with permanent connection to SCA I2C7 master	Do	Done
	Replace R279/R282/R285 with permanent connection dongle fuse power	Keep	Done
	Replace R280/R283/R286 with permanent connection dongle programpulse	Keep	Done
7.2	hardwire the GBTx mode resistors	TBI: Jo	Done
	hardwire the I2C ID resistors	Do	Done
7.3	Remove J42	Do	Done
7.4	Remove the VTRx/VTTx mod Abs resistors	Do	Made NP
7.5	Remove I2C3	TBI: Jo	Done
	Disable VTRX-Tx	Do	Done
New	Boot Xilinx from standard PROM	Under investigation by Piero	
new	Proposal to remove GBTx: TestClockOut Testoutput	TBD	
New	Keep R186?	TBD	