



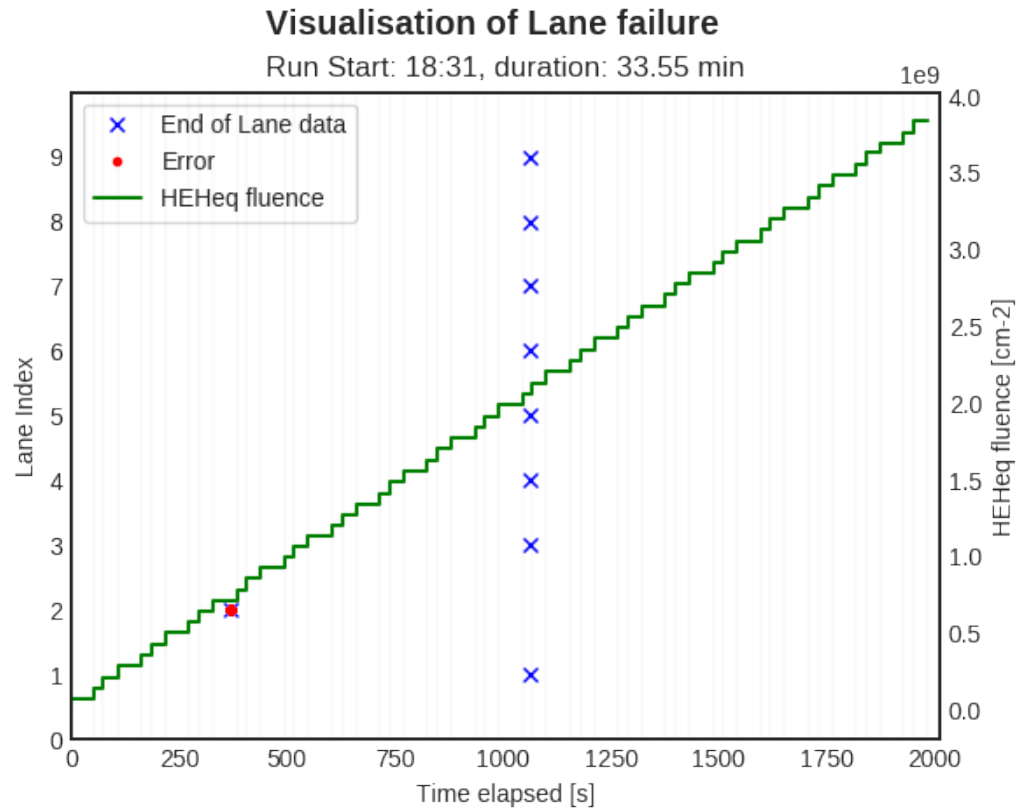
EVENT DATA ANALYSIS OF CHARM TESTBEAM

Summary

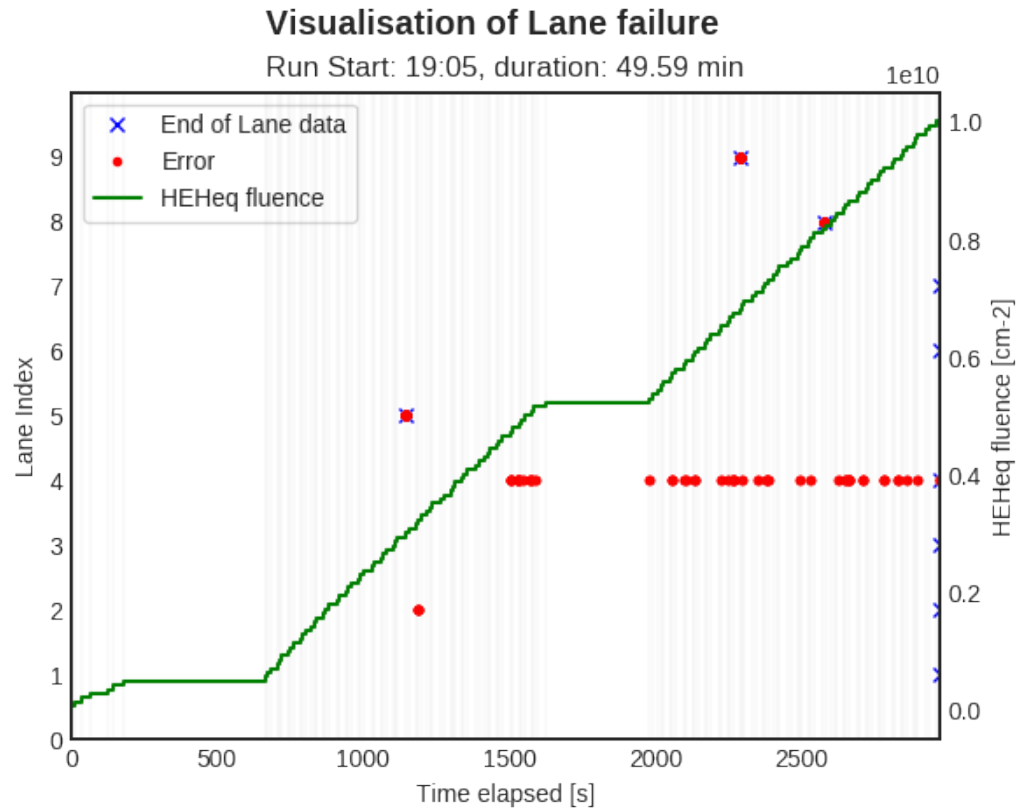
- Collected Results of 4 Runs
 - 2 short runs (< 5 min)
 - 2 long runs (> 30 min)
- Different events observed
 - Failure of all Lanes at ones
 - Failure of single lanes
 - Error bursts on single lanes
- First Estimation of Mean HEHeq Fluence To Failure for a lane structure
 - $3.04 * 10^9 \text{ cm}^{-2} (\pm 1.1 * 10^9 \text{ cm}^{-2})$

Run #1

- No Data from FPGA counters



Run #2



Run #2

Visualisation of Lane failure

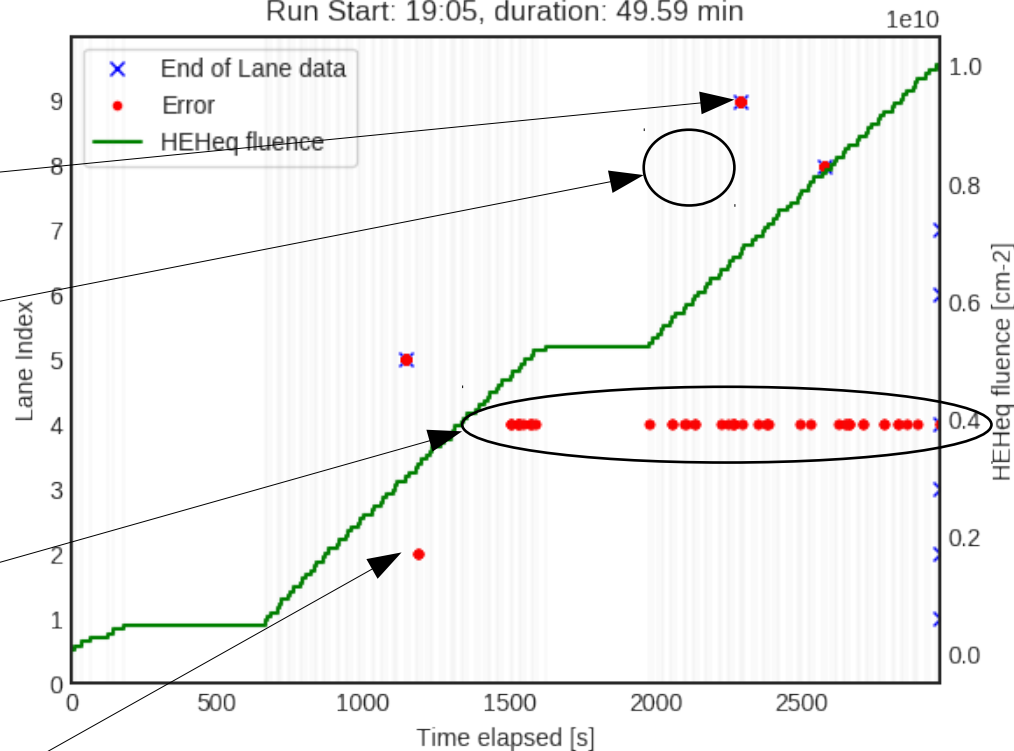
Run Start: 19:05, duration: 49.59 min

Decoding Errors
Detected

Decoding Errors
Detected
Wrong time info?

CDR Loss of Lock
Detected
Errors not detected
in FPGA

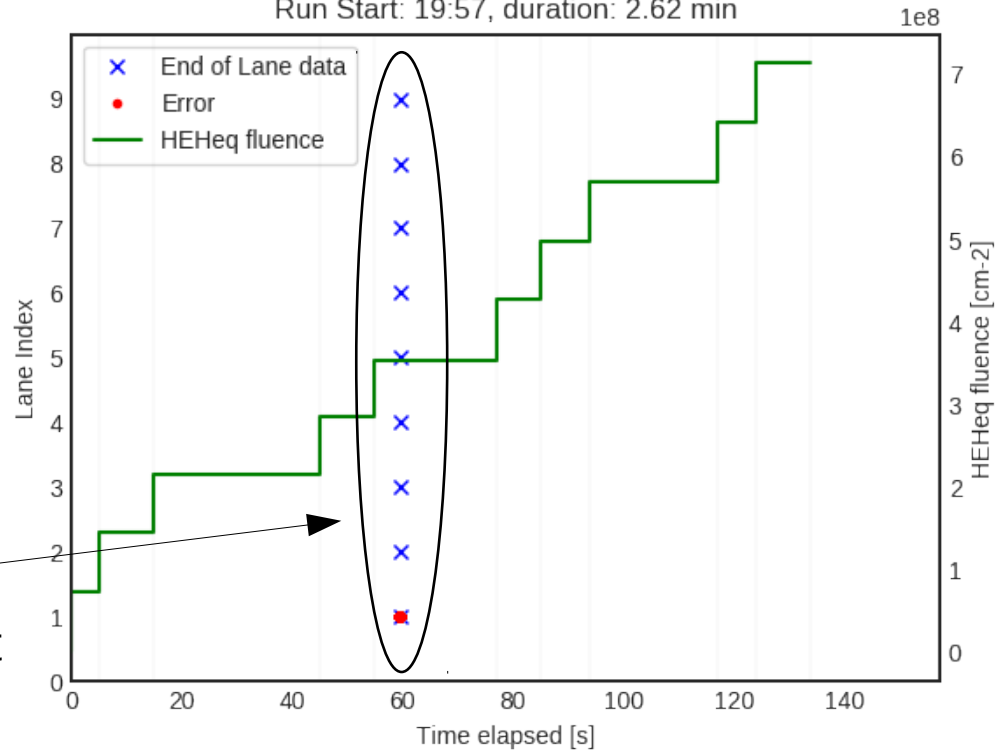
Realign to Comma
detected



Run #3

Visualisation of Lane failure

Run Start: 19:57, duration: 2.62 min

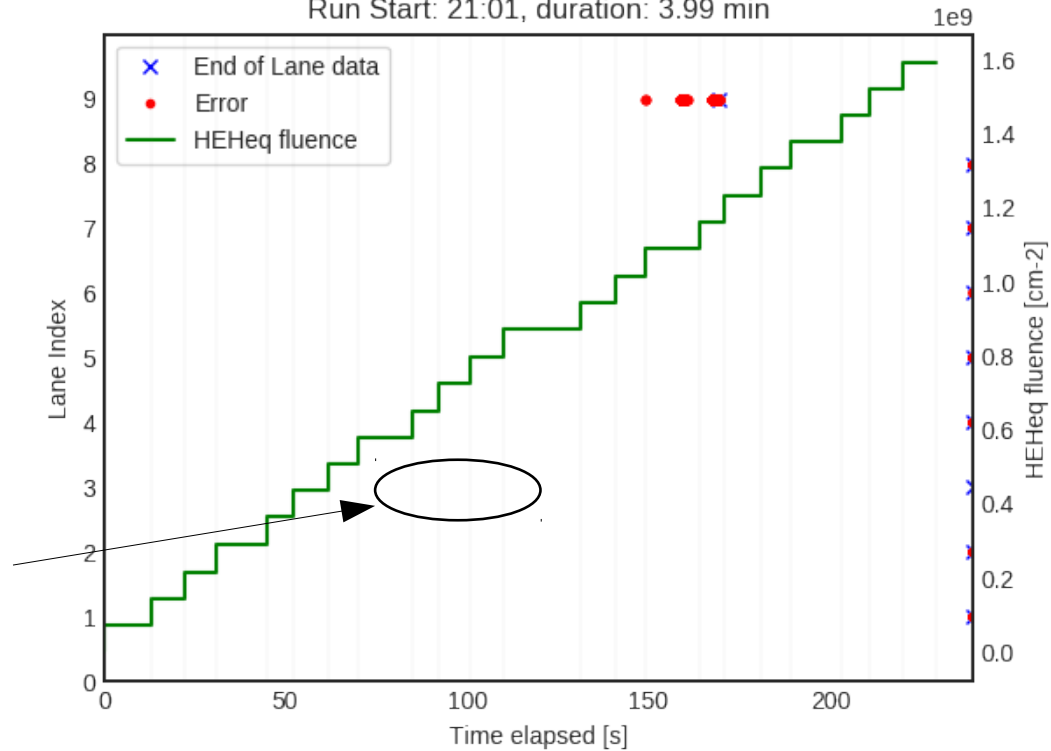


Fifo Full Count +
Fifo Overflow Count
Increase/Saturation

Run #4

Visualisation of Lane failure

Run Start: 21:01, duration: 3.99 min

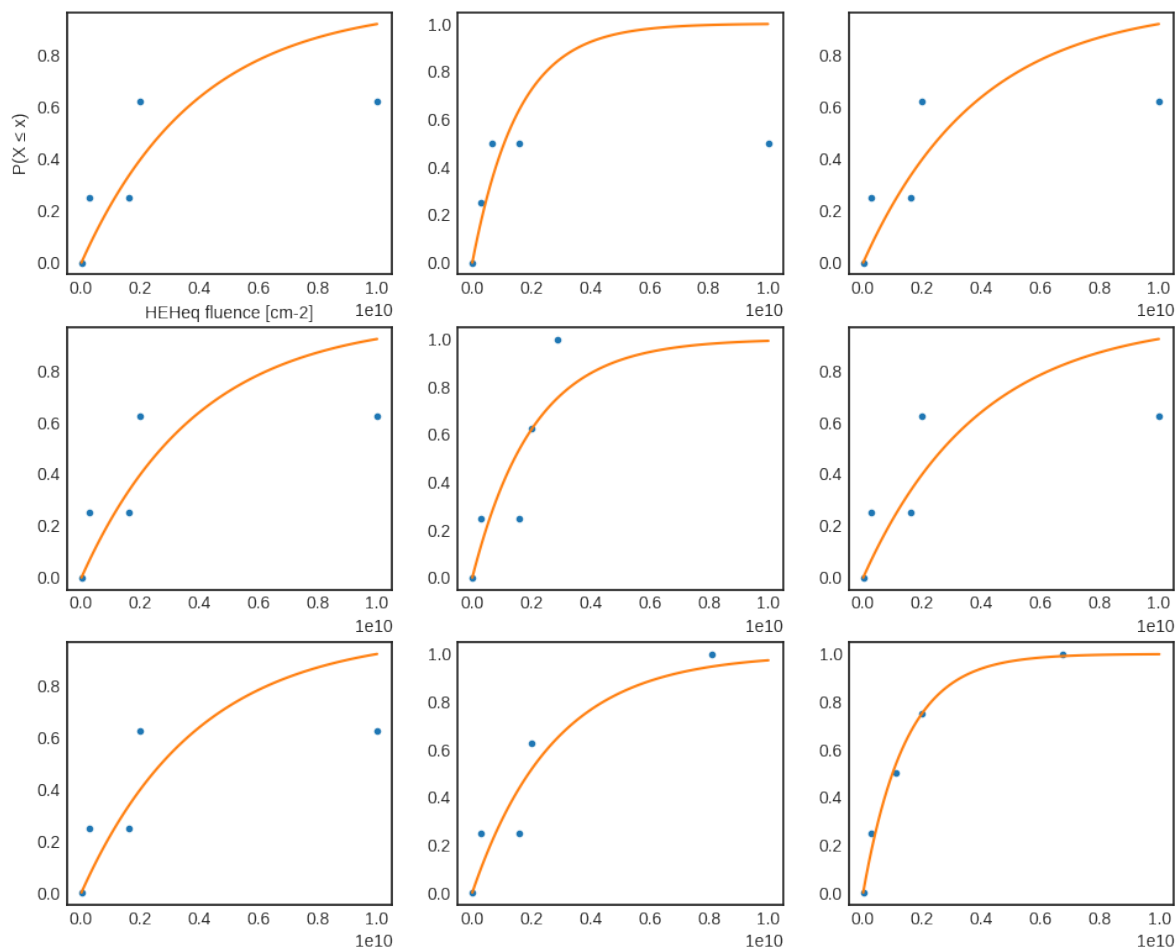


Fifo Full Count
Increase

Estimation of failure time of a single Lane (1)

Based on Event data

Probability of failure over HEHeq fluence
CDF per lane



Estimation of failure time of a single Lane (2)

Lane Average + bounds

