IB Commissioning

Magnus Mager

ITS Plenary 21/01/2019

Integration Plan

I. Half-layer test

- each layer is tested (in its own box)
- functional test
- stress-test

II. (rework of half-layer)

- possible problem need to be repaired (e.g. non-working PT100)

III. Service barrel integration

- half-layer by half-layer is installed into the service barrel
- this is done with final services

Milestones

Item	People	Status	ETC
Characterisation and tuning of HS link in final setup	Matteo, Miko, Piero	ongoing	Feb
Characterisation of supply, threshold + noise at up to 1 MHz rate	Matteo, Miko	pending	Feb
Readout of IB-HL-0, stress test	Arild	ongoing	Feb
Stave calibration (voltages, thresholds, bad pixels)	Miko	pending	Mar
Integration of DCS (ALF-FRED)	Paolo +Ivan	ongoing	Feb
Integration into QC (plots, event display)	Ivan	pending	Mar
Integration of Trigger (LTU)	Arild	ongoing	Mar
Integration of debugging and a calibration in DAQ, DCS	Ivan, all	pending	
Installation of RU+PB to final rack in 167	Gianluca, Arild	missing hardware	Mar
Connection of full HL-0	all		Feb
Connection of full HL-1	all		Mar
Full barrel asembly	all		?
Cosmic run	all		?

People (Proposal)

Name	(Current) main function	Percentage
Magnus Mager	Coordination, Software Architecture + Development	60%
Miljenko Šuljić	Single stave tests	80%
Matteo Lupi	Readout	80%
Arild Velure	Readout	80%
Ivan Cali	DCS/Calibration	80% (+ students)

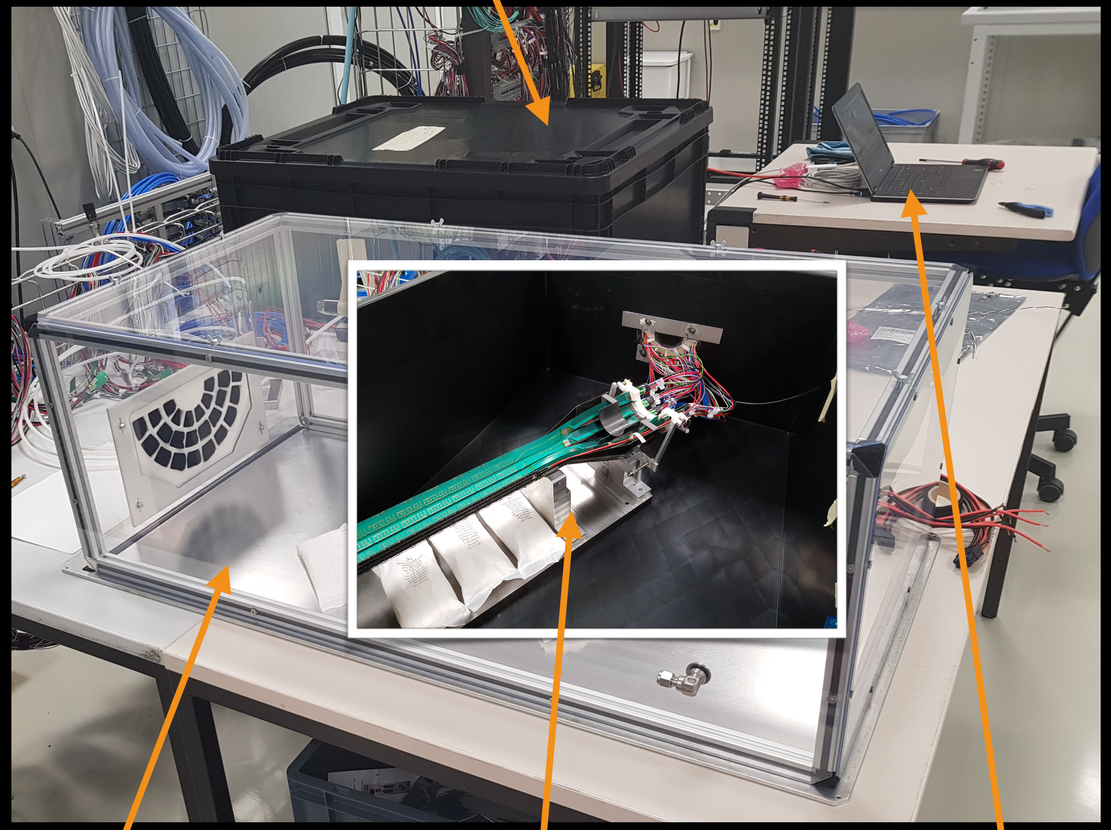
Support

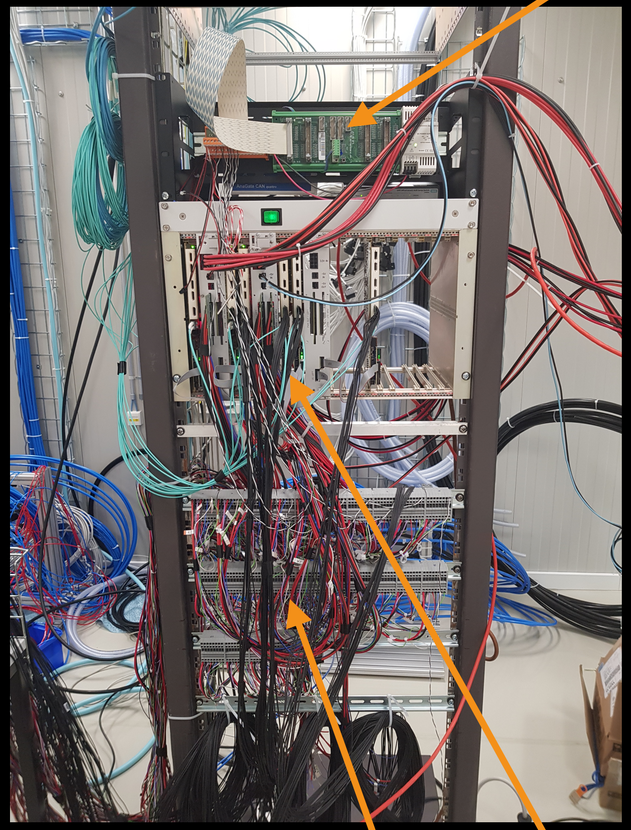
Name	Function
Paolo Martinengo	DCS
Hartmut Hillemanns	CAEN PS
Corrado Gargiulo	Cooling/Mechanics
Andres Galdames Perez	Mechanics
Filippo Costa, Sylvain Chapeland	DAQ
Joachim Schambach	RU FW
Gianluca Aglieri, Piero Giubillato	RU hardware, 167 infrastructure
Alberto Collu	PB
Markus Keil	DAQ-liason

Issues / Open items

Severity	Item	People	Status
high	RU documentation	Matteo, Arild, Jo	ongoing
high	Development of tools for data consistency checking	Matteo, Miko	ongoing, pending RU documentation
med	Power board startup	Matteo, Miko, Alberto	ongoing
med	Monitoring tools	?	pending
high	Cooling PS interlock	Paolo	pending
med	Connector fixation	Corrado	ongoing
med	Logbook	O2?	pending

Set-up Overview





1.2 Gbit/s link

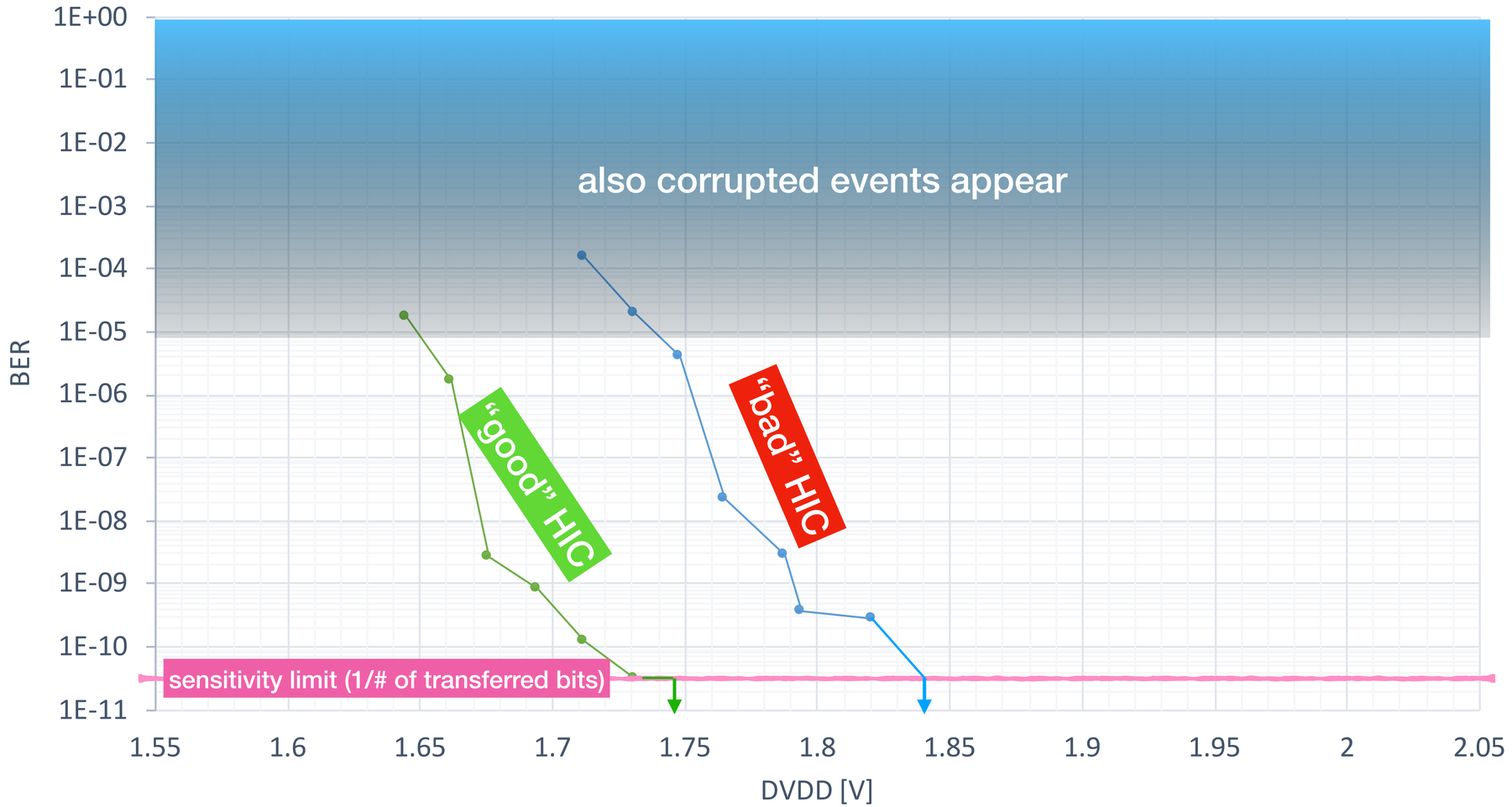
- A series of IB HICs was recently failing the qualification test in a similar manner: too many data errors on the high-speed link
- Comparison to earlier failing HICs: same pattern is present also there

➡ Started a in-depth debug and characterisation activity, including:

- oscilloscope measurements of supply nets (at different levels)
- oscilloscope measurements of HS-data + clock signals

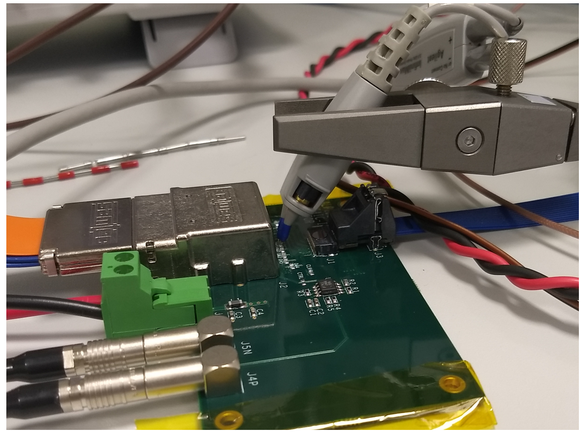
- Discussions with chip designers and MOSAIC, RU firmware designers to understand:
  1. Why some chips are different from others?
  2. What can be done on transmitting side?
  3. What can be done on receiving side?

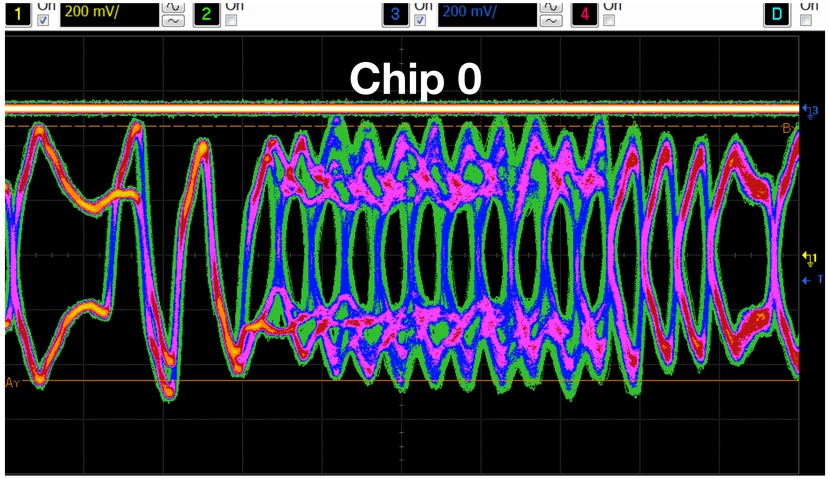
Observations (more details)



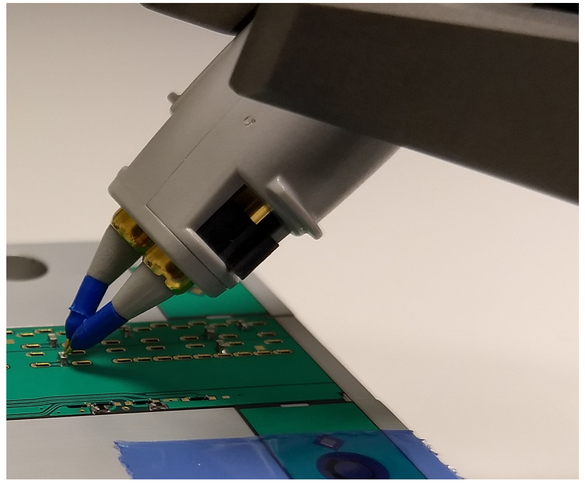
1. A series of IB HICs show systemically higher bit error rates in the HIC qualification test
2. This can be mitigated by increasing their digital supply
3. It turns out that also other "good" HICs are affected – just at with a different offset
4. We seem to be quite marginally

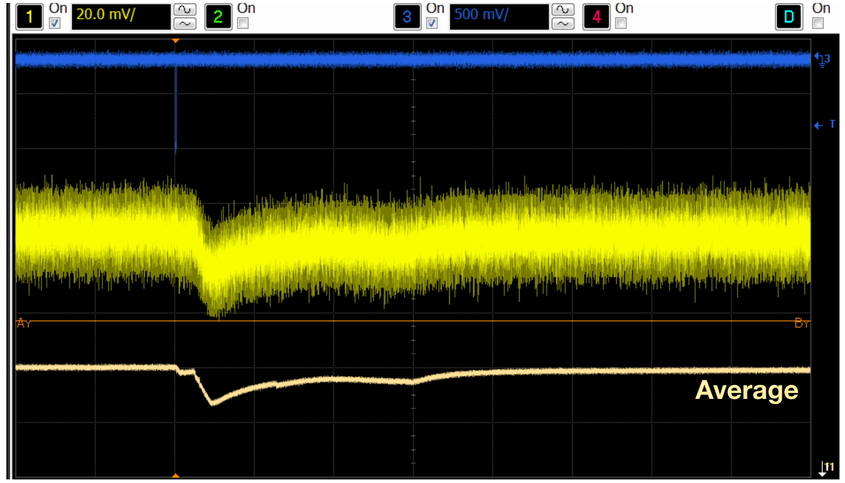
Oscilloscope measurements





high-speed link





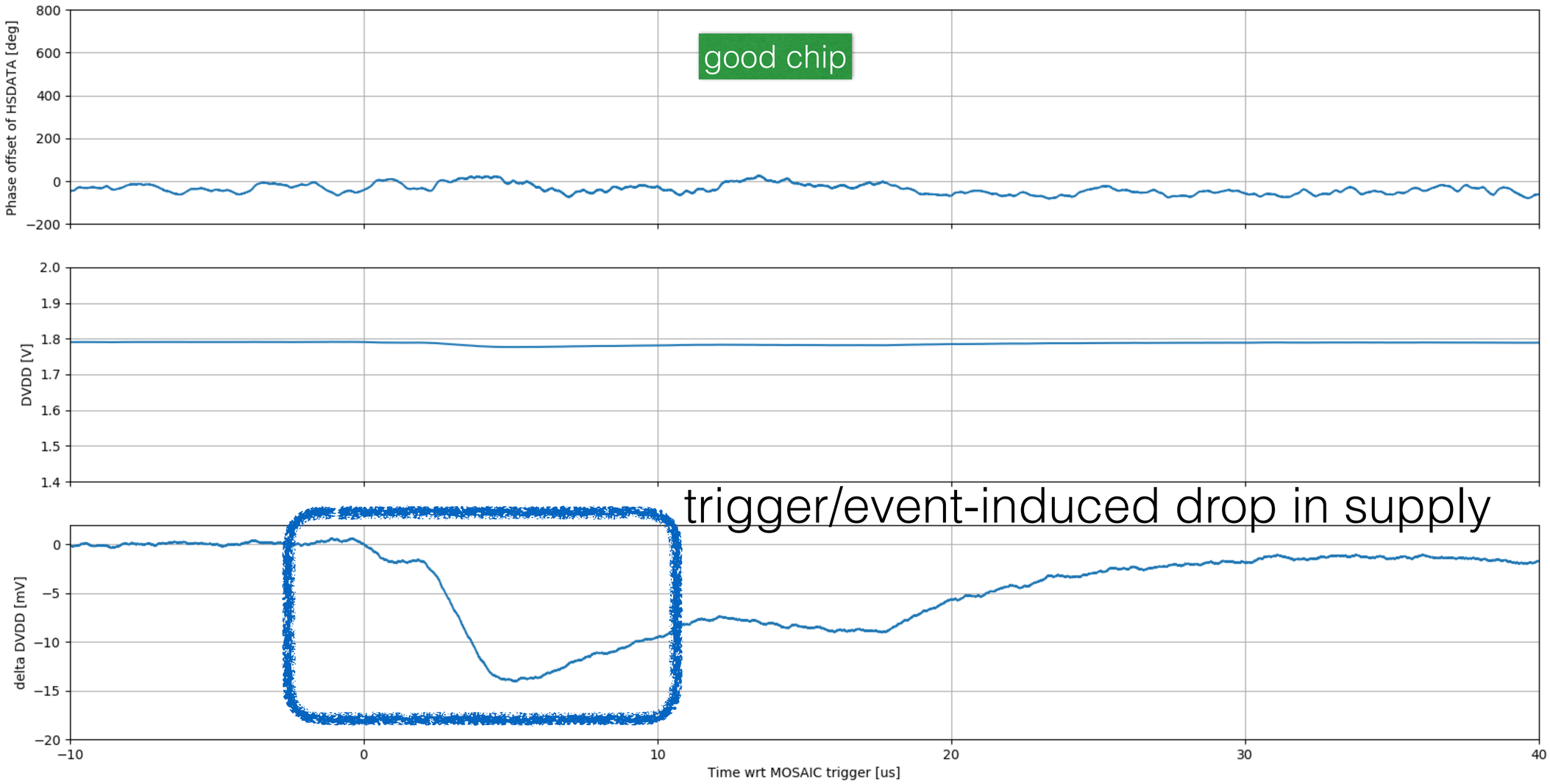
supply current (on chip decoupling)

1.2 Gbit/s link – decoding

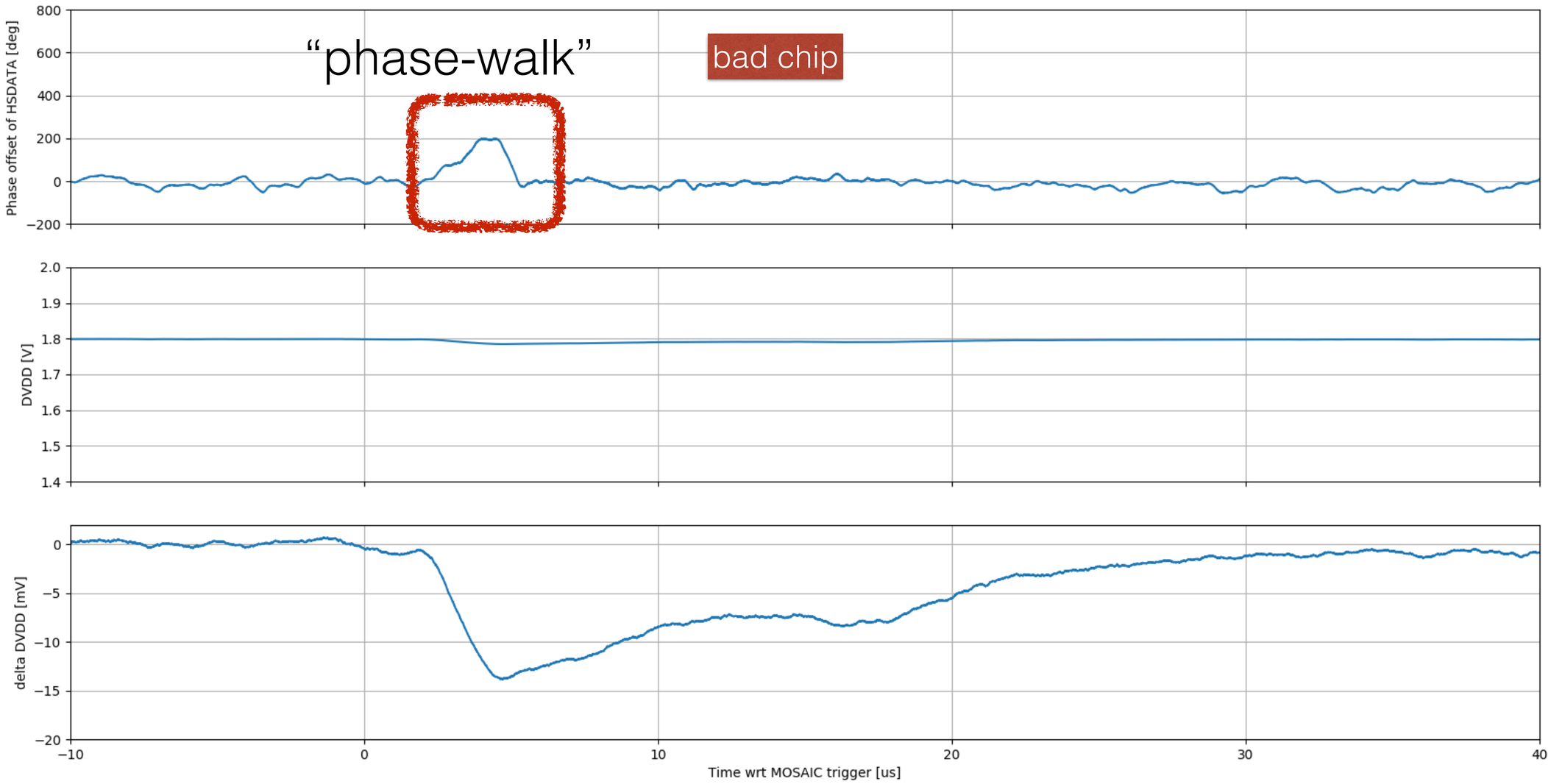
GOOD news: ALPIDE sends correct data
Decoding “by hand” always works

Decoding “by hand” always works

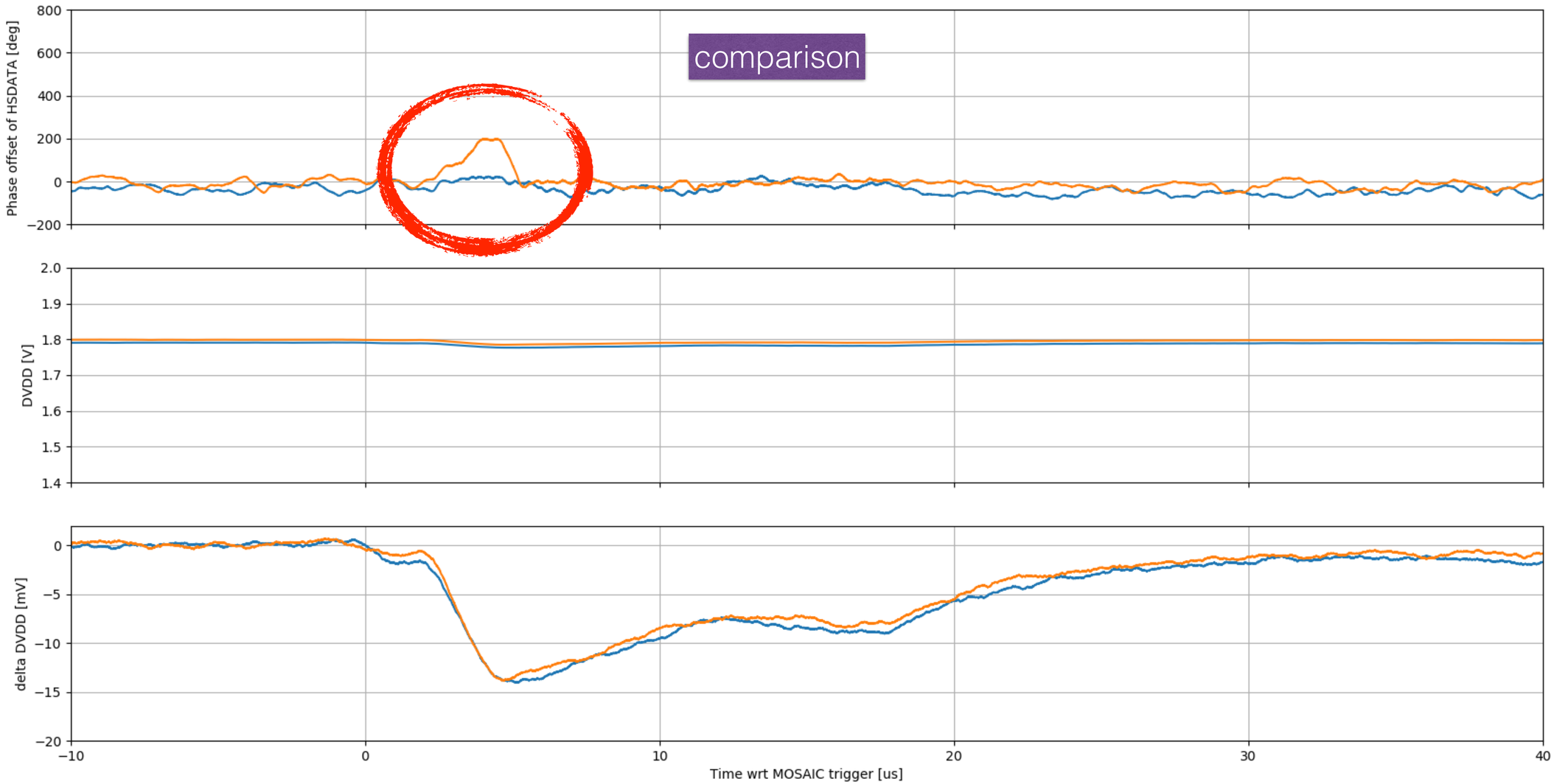
1.2 Gbit/s link



1.2 Gbit/s link

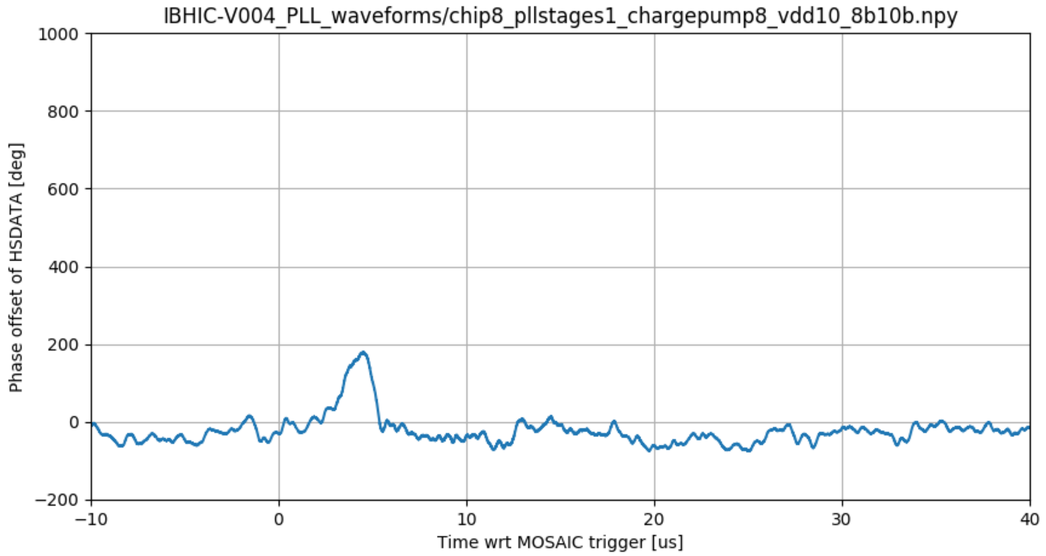


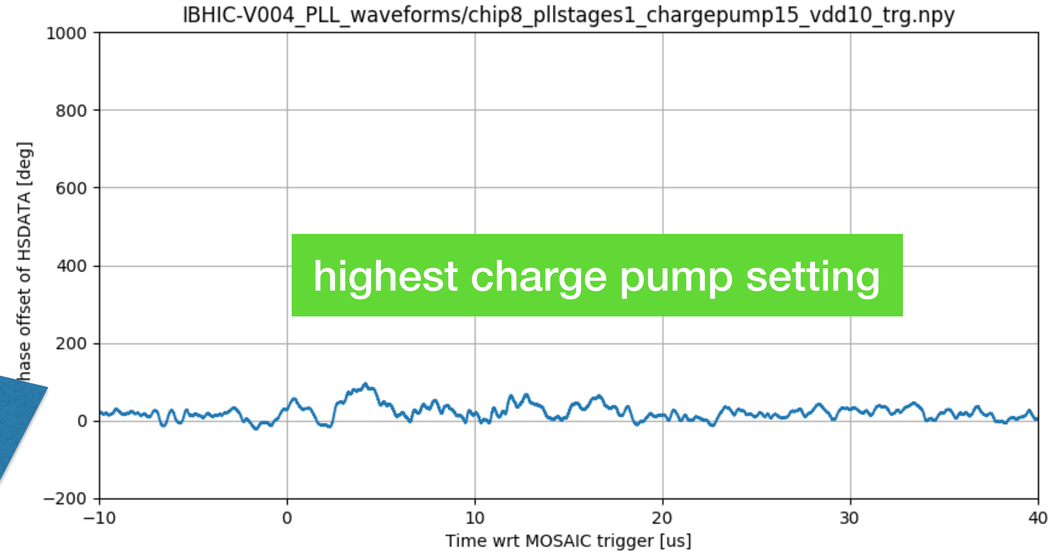
1.2 Gbit/s link

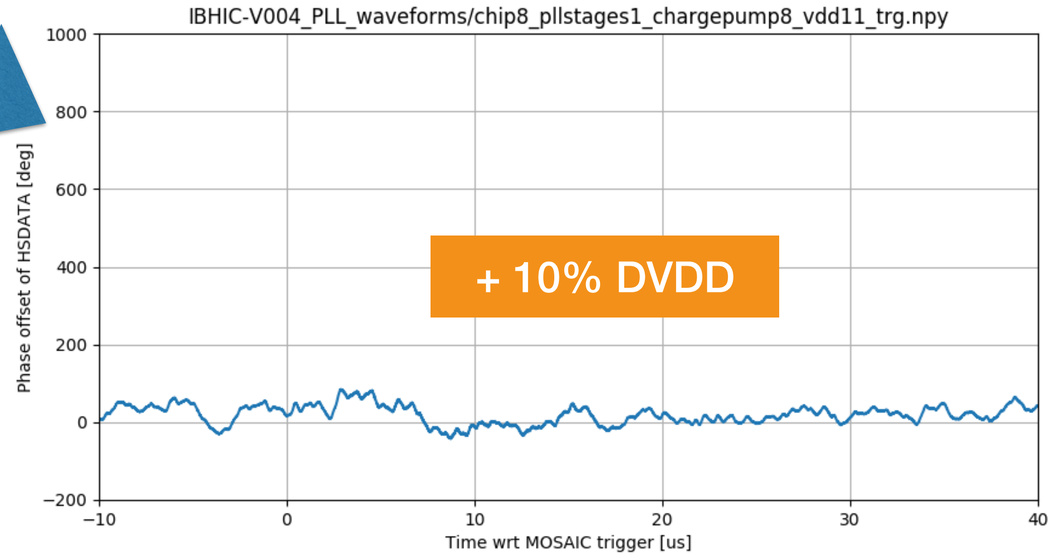


1.2 Gbit/s link

Possible mitigations
(under investigation)





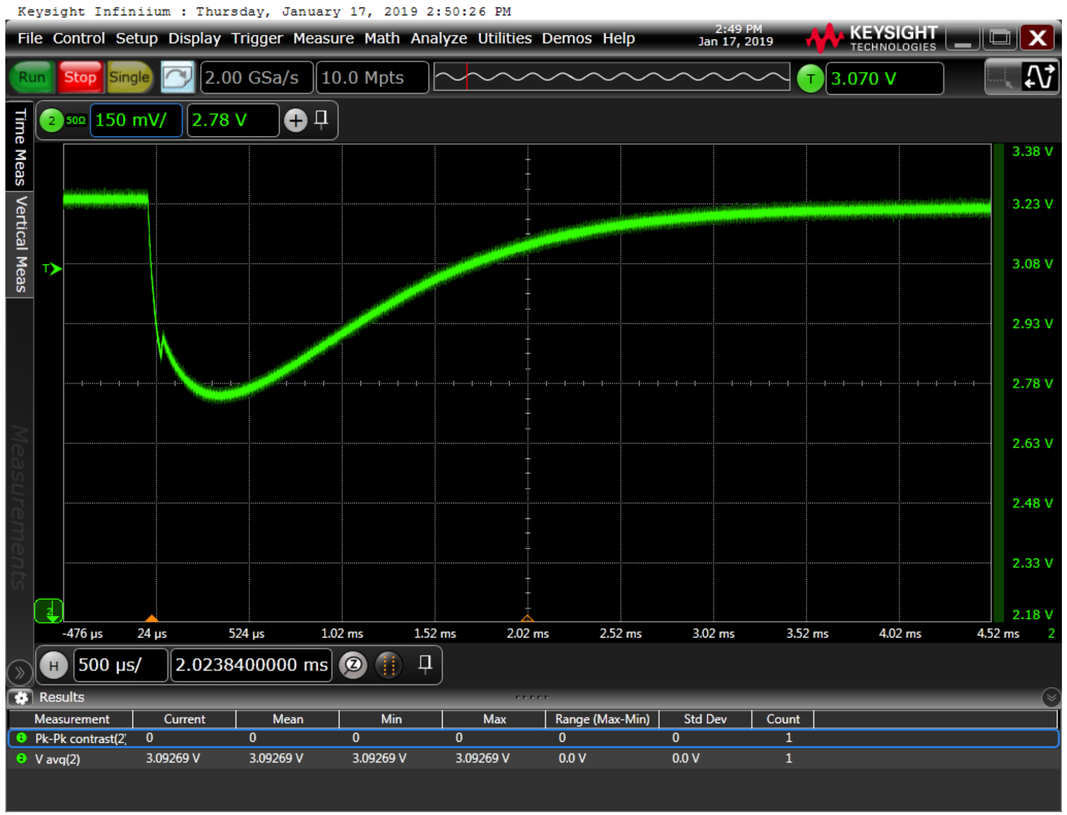


1.2 Gbit/s link

- This effect is at least chip dependent (likely wafer or lot dependent)
  - Need to *characterise* it on all chips
- This will also depend on receiver (so far tested with MOSAIC + Oscilloscope)
  - Need to *measure* and *tune* error rate with RU
- Integration of tests in 167 ongoing

Power board

- For some PU–stave-voltage combinations, the PU reports 0 voltage and currents
- This seems to be related to an voltage drip at the input of the PU upon powering a stave
- Under investigation



Power board

```
$ ./power_on.sh
2019-01-11 13:15:10,290 - Module Id 6: PowerUnit - INFO - Setup power for IB on module 0
2019-01-11 13:15:10,291 - Module Id 6: PowerUnit - INFO - All off
2019-01-11 13:15:10,491 - Module Id 6: PowerUnit - INFO - Power enable status: 0000, Bias enable status: 00
2019-01-11 13:15:10,492 - Module Id 6: PowerUnit - INFO - Bias powering ON
2019-01-11 13:15:10,492 - Module Id 6: PowerUnit - INFO - Analog + Digital powering on
2019-01-11 13:15:10,492 - Module Id 6: PowerUnit - INFO - Powering module 0
2019-01-11 13:15:10,693 - Module Id 6: PowerUnit - INFO - Power enable status: 0001, Bias enable status: 00
2019-                                    erUnit - INFO - Power enable status: 0003, Bias enable status: 00
2019-                                    erUnit - INFO - All on
2019-                                    erUnit - INFO - Power enable status: 0003, Bias enable status: 00
2019-                                    erUnit - INFO - Power enable status: 0003, Bias enable status: 00
2019-                                    erUnit - INFO - Power enable status: 0003, Bias enable status: 00
2019-                                    erUnit - INFO - Power enable status: 0003, Bias enable status: 00
2019-01-11 13:15:11,899 - Module Id 6: PowerUnit - INFO - Power enable status: 0003, Bias enable status: 00
2019-01-11 13:15:12,100 - Module Id 6: PowerUnit - INFO - Power enable status: 0003, Bias enable status: 00
2019-01-11 13:15:12,301 - Module Id 6: PowerUnit - INFO - Power enable status: 0003, Bias enable status: 00
2019-01-11 13:15:12,502 - Module Id 6: PowerUnit - INFO - Power enable status: 0003, Bias enable status: 00
2019-01-11 13:15:12,703 - Module Id 6: PowerUnit - INFO - Power enable status: 0003, Bias enable status: 00
2019-01-11 13:15:12,904 - Module Id 6: PowerUnit - INFO - Power enable status: 0003, Bias enable status: 00
2019-01-11 13:15:15,635 - Module Id 6: PowerUnit - INFO - Power enable status: 0x0003
2019-01-11 13:15:15,635 - Module Id 6: PowerUnit - INFO - Bias enable status: 0x00
2019-01-11 13:15:15,636 - Module Id 6: PowerUnit - INFO - Backbias: -0.000 V, 0.0 mA
2019-01-11 13:15:15,636 - Module Id 6: PowerUnit - INFO - Module 0, avdd: 0.000 V, 0.0 mA
2019-01-11 13:15:15,636 - Module Id 6: PowerUnit - INFO - Module 0, dvdd: 0.000 V, 0.0 mA
```

LDO status

Power is applied to Stave, but voltages + currents are reported as 0

ADC readback

Connector holder

- New design ready
- Replaces old locking mechanism
- Needs testing
- With new cables, connection to detector is also possible without these holders (though should not be touched afterwars)

Follow-up

- Documentation:
  - Need to write RU user manual
- Logbook:
  - Check availability of “official” ALICE logbook
- Meeting:
  - “reuse” former WP5 meeting: Wednesdays, 11 AM.