MVTX(INTT) Readout and Event Alignment

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sPHENIX HF TGM

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MVTX + INTT: 3 + 2 layers

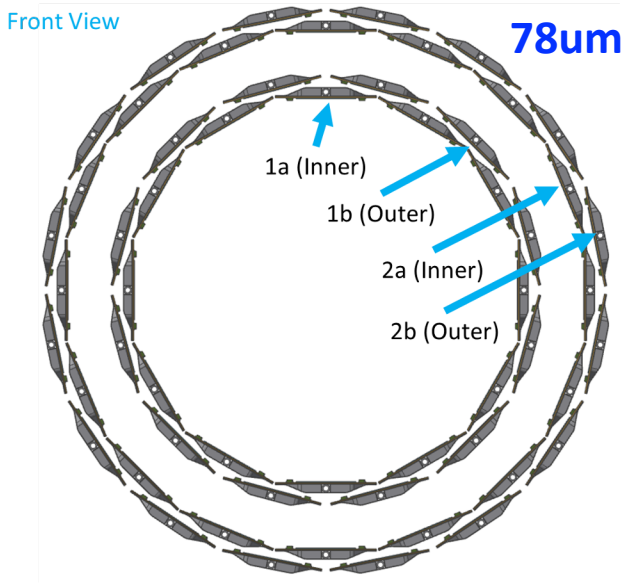
INTT

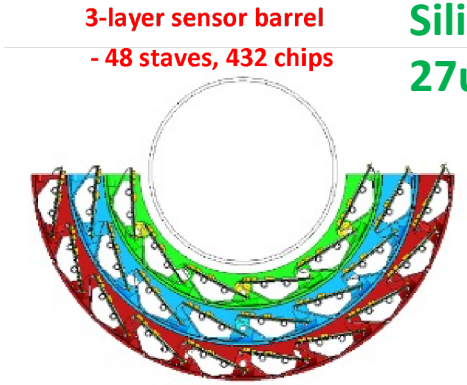
Barrel	Center of Sensor Tangent Radius (mm)
1	-
1a (Inner)	71.88
1b (Outer)	77.32
2	-
2a (Inner)	96.80
2b (Outer)	102.62

MVTX

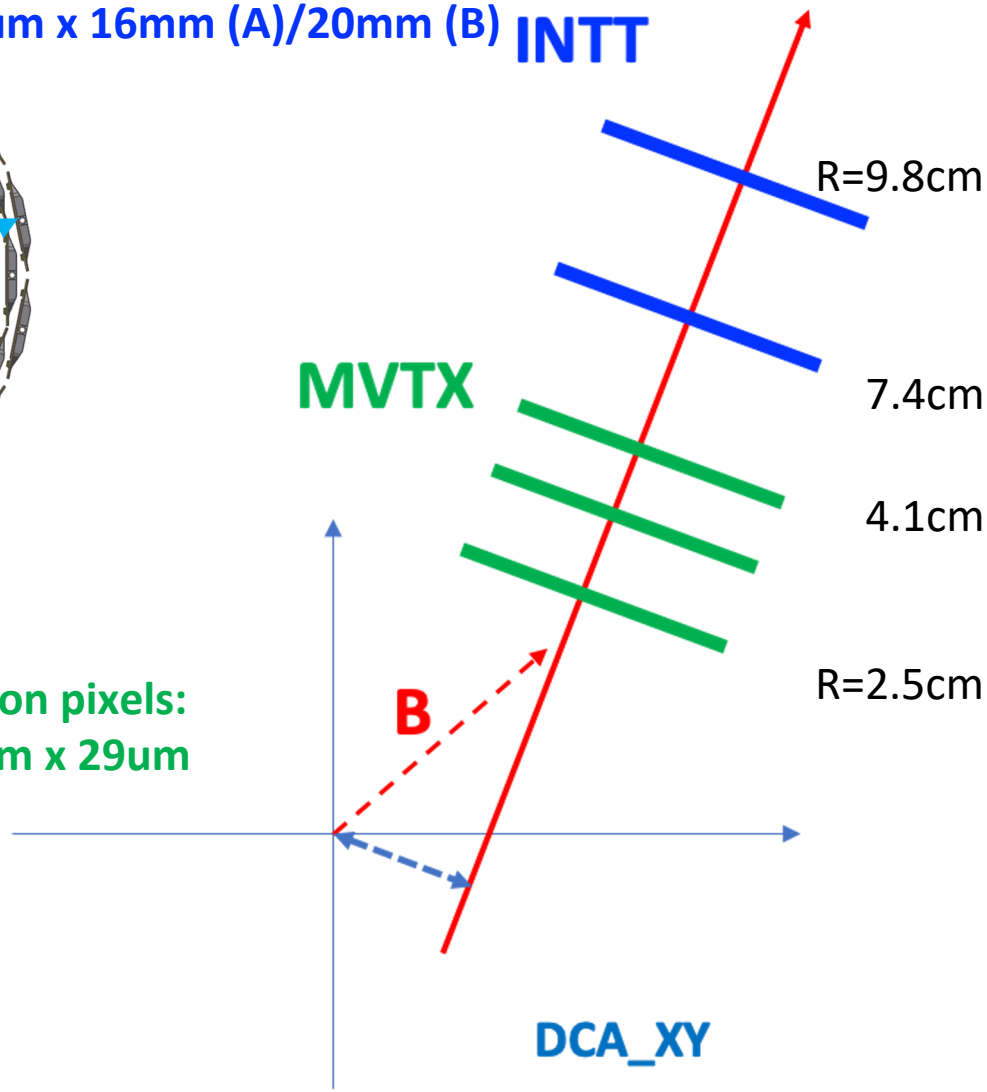
R (mm)	min	mid	max
Layer 0	24.61	25.23	27.93
Layer 1	31.98	33.35	36.25
Layer 2	39.93	41.48	44.26

Silicon Strips:
78um x 16mm (A)/20mm (B)





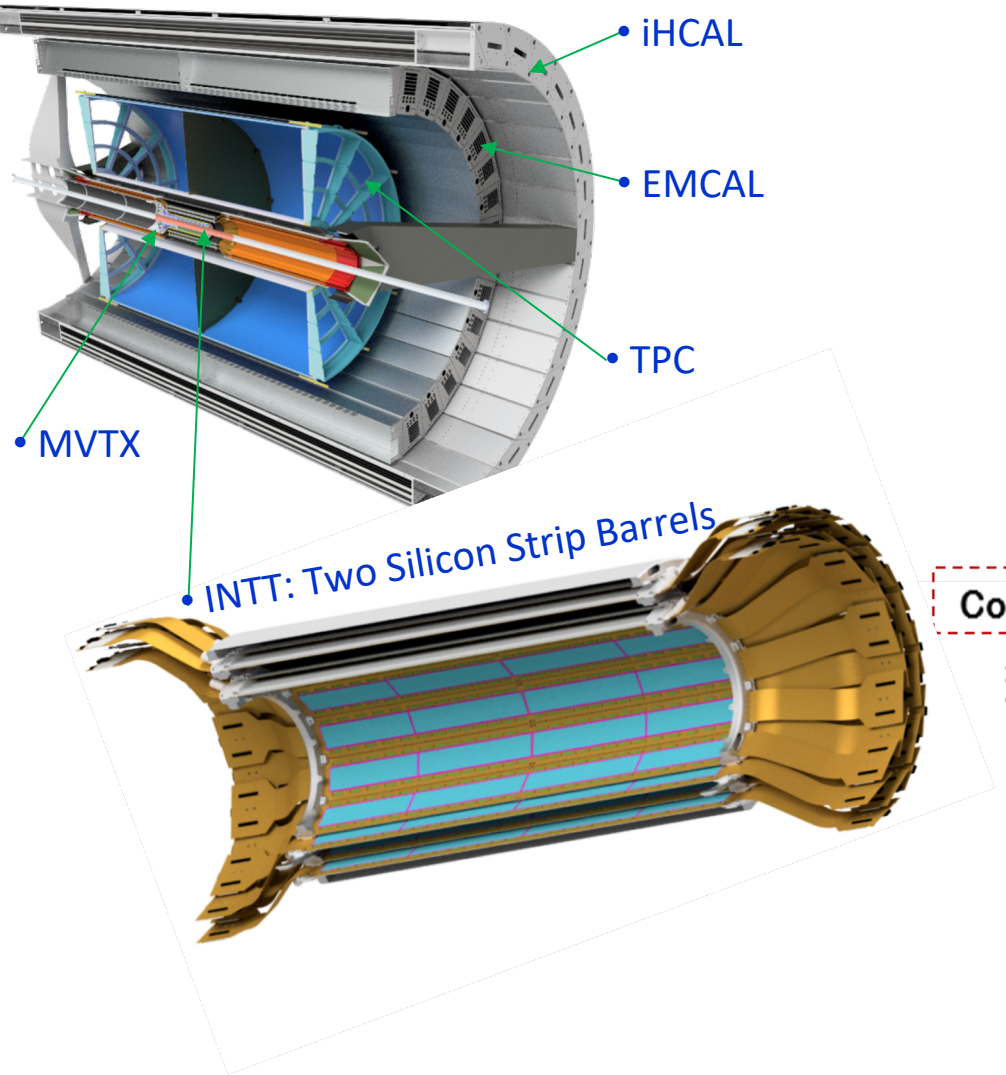
Silicon pixels:
27um x 29um

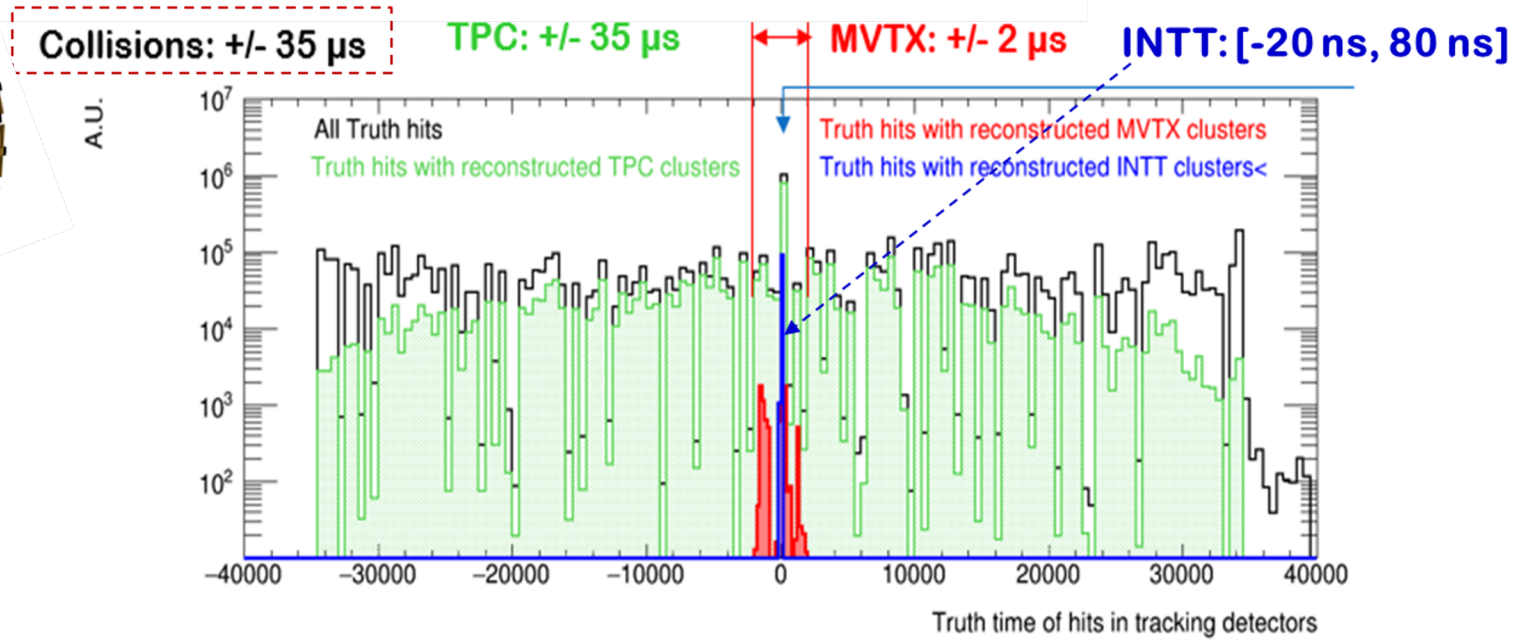


INTT: 1 RF timing resolution

- Strip sensor: AC-coupled silicon sensor
- FPHX: used successfully in FVTX/PHENIX tracker:

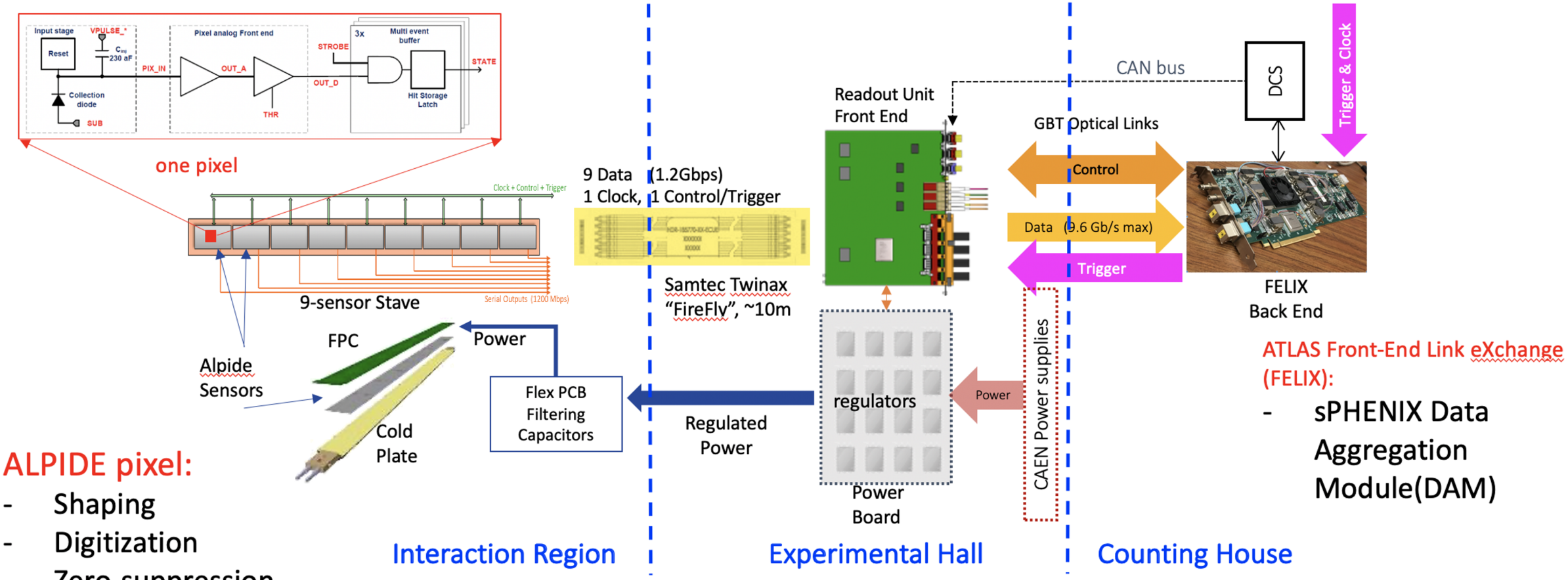
MVTX: ~5uS event timing resolution





MVTX Readout, Power and Controls

MVTX hits arrival @FELIX
- (rising+strobe) uS after collisions (dep. readout config.)



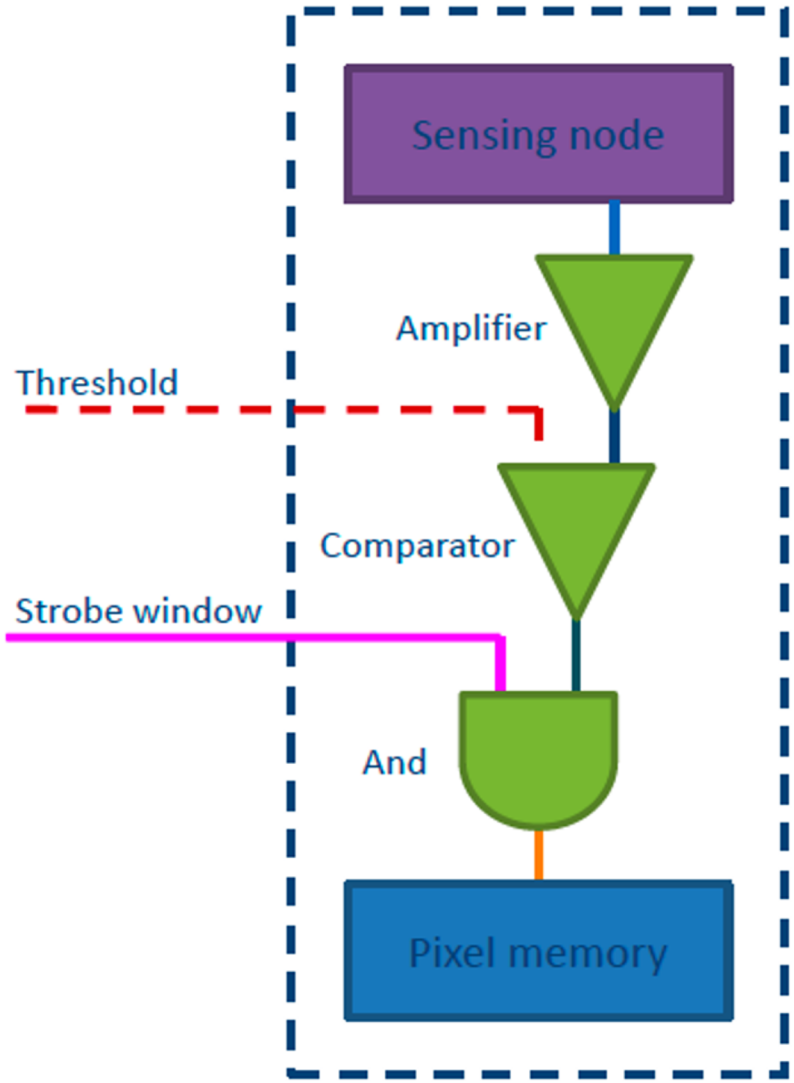
ATLAS Front-End Link eXchange (FELIX):
- sPHENIX Data Aggregation Module(DAM)

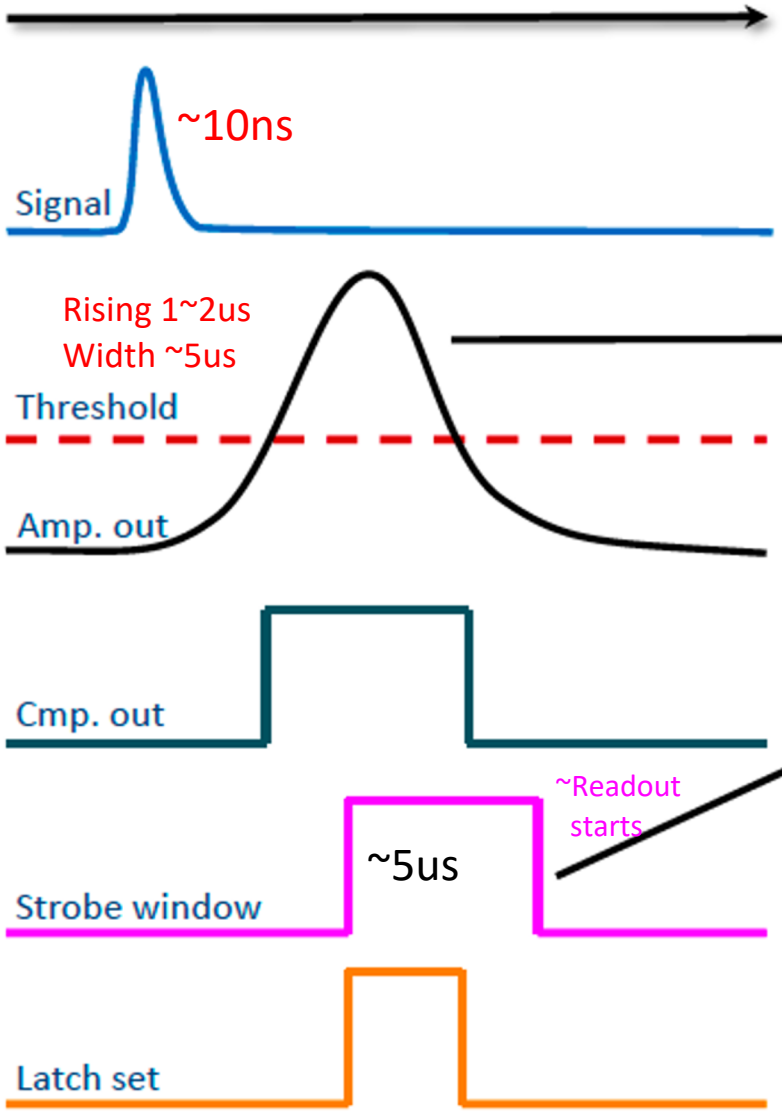
ALPIDE pixel:
- Shaping
- Digitization
- Zero-suppression
- 3x buffer

MVTX Detector Electronics consists of three parts

Sensor-Stave (9 ALPIDE chips) | **Front End**-Readout Unit | **Back End**-FELIX/DAM

ALPIDE Timing





Analog "slow" shaping time acts as a memory (µs order) to buffer the signal until the trigger arrives.
Called "pulse length"

Only pixel with signal higher than threshold DURING the strobe window will get latched in memory

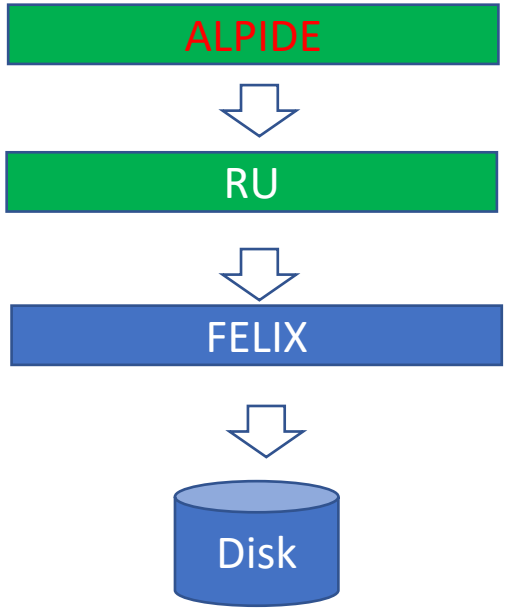
Confirmed at LANL: pulse length can be extended to meet sPHENIX trigger latency requirement

MVTX Readout – Continuous Readout

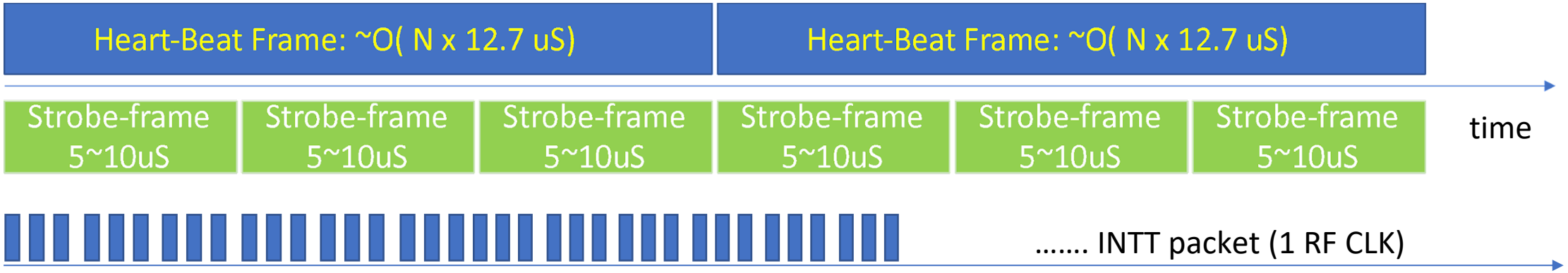
Time frames: all programmable

1) Fixed Heart Beat Frame (HBF): 10~100 uS,
   - Readout FELIX data to disk
   - Could be N x 12.7 uS (one RHIC cycle)

2) Fixed strobe frame (SF): ~5 uS
   - Readout ALPIDE data to RU
   - The smallest timestamp



MVTX data package:
~ strobe-frame, could be as short at ~2uS
shorter strobe-> duplicated hits/larger data volume

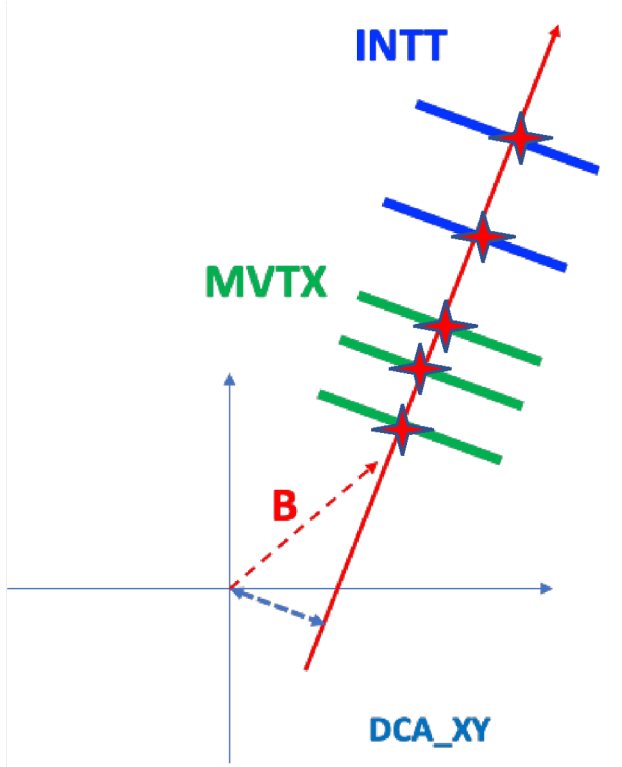


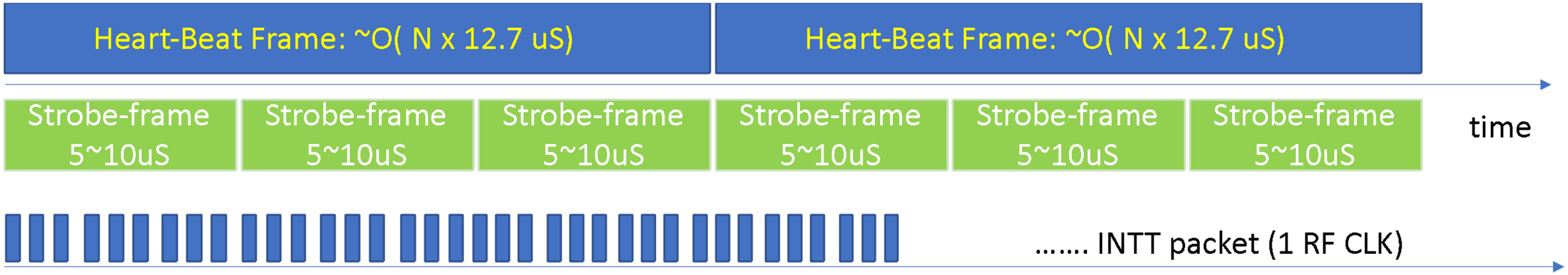
MVTX + INTT Event Alignment

INTT 1-RF packet ⇒ select MVTX hits (tracking fitting)
To form (MVTX_Hits + INTT_Hits) events

sPHENIX global RF timing (RF counters) used to sync MVTX and INTT packets
- MVTX: @beginning of strobe signal
- INTT: @ a given RF CLK

RHIC cycle: 120 RF budgets: 12.7 uS



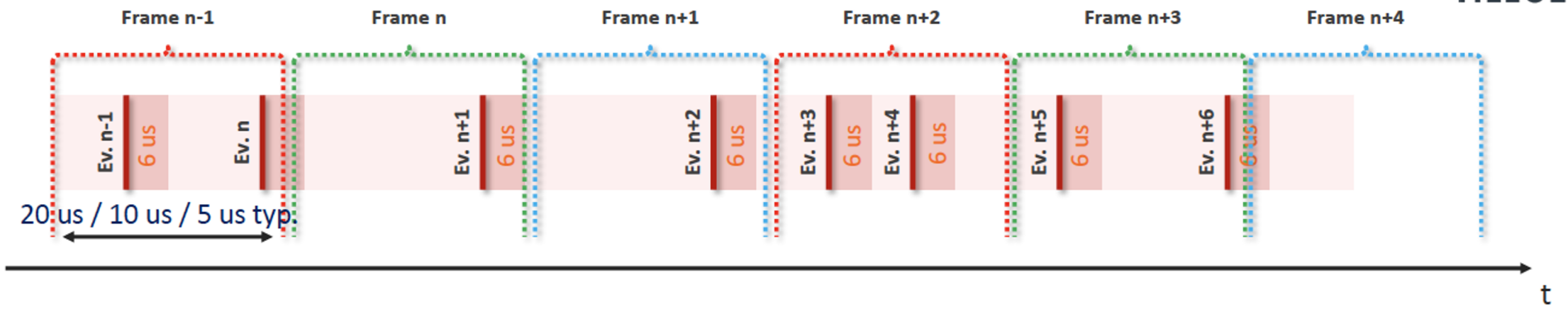


Backup

MVTX Hits vs Strobe Length (ITS Sim)

Strobe-Frame

Continuous Readout Mode (*free-running*)



Internal strobe has programmable duration

Periodic frames can be synchronized externally or generated internally (full camera mode)

For every frame *start*, ALPIDE produces a data packet with time stamp and (optional) payload with hits in coincidence with frame strobe

Hit data repetition can happen because of the duration of the discriminated pixel output

Event (n) and (n+6) in the sample diagram have hits repeated in two consecutive chip data packets (can be accounted for)

Decreasing frame duration *increases data throughput*

Increases hit data volume because of double sampling pixel hits

Increases overhead of chip data packet headers and trailers

Hit Rates and Data Rates

ALICE

ALPIDE *particle* rate max. capabilities

Assuming 2.5 average cluster size

Matrix to Periphery hit data transfer: ~ 50 MHz/cm^2

At slow frame rates. Reduces with faster frame rate

Chip output link max capacity: ~ 6 MHz/cm^2 (with on-chip data reduction), ~ 4 MHz/cm^2 (raw)

Table source: ALPIDE PRR

Operation in ALICE for Pb-Pb 100 kHz interaction rate

Combined Physics Simulation and SystemC model of ALPIDE

~1.5 MHz cm^{-2}
(Avg. Cluster size 3.7)

~1.9 MHz cm^{-2}
(This sustainable also with 5 us periodic frame)

Needs dedicated HS Link per chip

		Layer 0	1	2	3	4	5	6
Average fired pixels per event per sensor	**Total** (η = 0°)	**253.7** (326)	**152.7** (192.6)	**102.9** (127.2)	**4.8** (5.8)	**3.3** (4.1)	**1.9** (2.3)	**1.6** (1.8)
	Physics (η = 0°)	152.6 (224.1)	101.1 (141.0)	71.0 (95.3)	3.0 (4.0)	2.7 (3.5)	1.4 (1.8)	1.1 (1.3)
	QED	100.6	51.0	31.4	0.3	0.1	0.0	0.0
	Noise	0.53	0.52	0.5	0.5	0.5	0.5	0.5
Average data rate per master [Mbit/s]	Avg	**299.4**	**191.3**	**135.6**	**71.8**	**56.8**	**41.7**	**38.6**
	(η = 0°)	362.5	223.3	154.2	79.7	60.7	45.8	41.2

Triggered and Continuous Readout Modes

Triggered Mode

Randomly distributed STROBE pulses of short duration Θ(100 ns)

Scenario: external trigger commands derived from trigger system

Busy violation trigger commands still acknowledged with Chip Empty Frame response, e.g. once MEB is full

Continuous Mode

Periodic and repeating STROBE intervals, duration 1 – 5 us

Flush oldest event when MEB is becoming full and start new strobe interval. (Priority to latest framing interval)

Generation of STROBE

Duration programmable 50 ns -> 1.6 ms *(both modes)*

Start on external commands or internal sequencer *(both modes)*

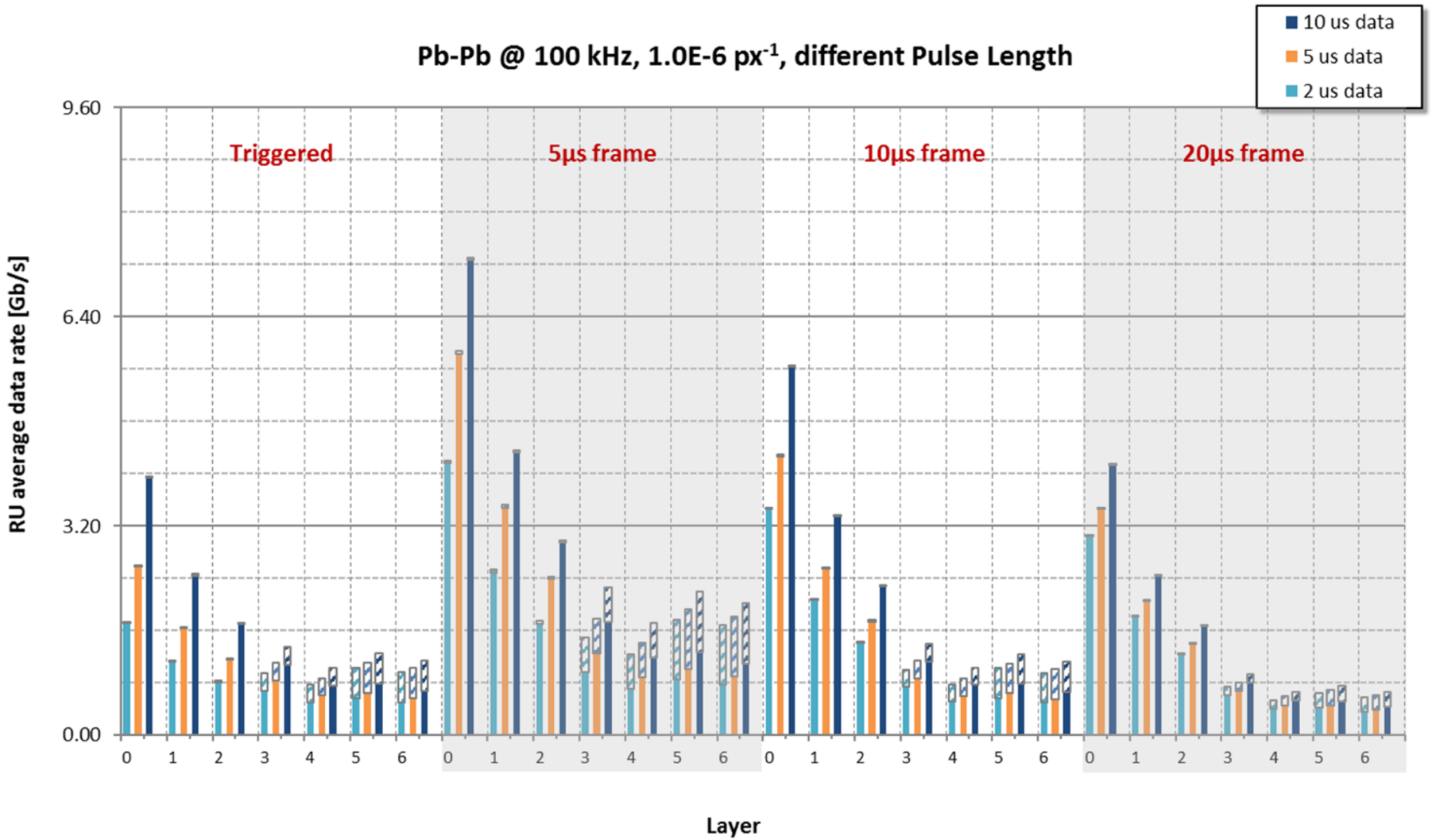
BUSY status

Triggered mode: *MEBs full* or *periphery FIFOs almost full*

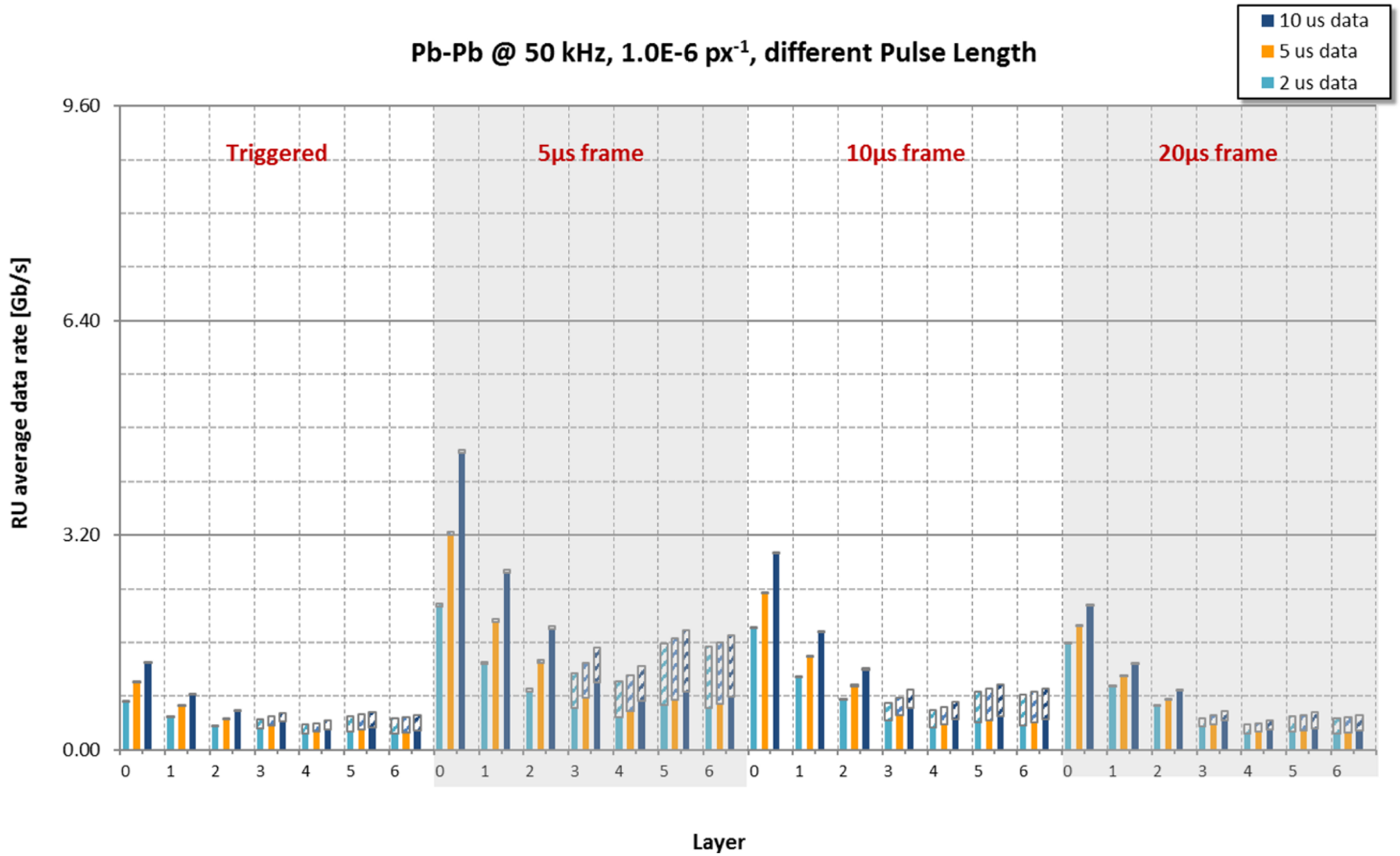
Continuous mode: *MEBs almost full* or *periphery FIFOs almost full*

Data rate – PbPb @ 100kHz per Readout Unit

ALICE ITS UPGRADE



Data rate – PbPb @ 50kHz per Readout Unit



FPHX Chip (Analog Section)

128 channel

46, 50, 60, 67, 85, 100, 150, or 200 mV/fC

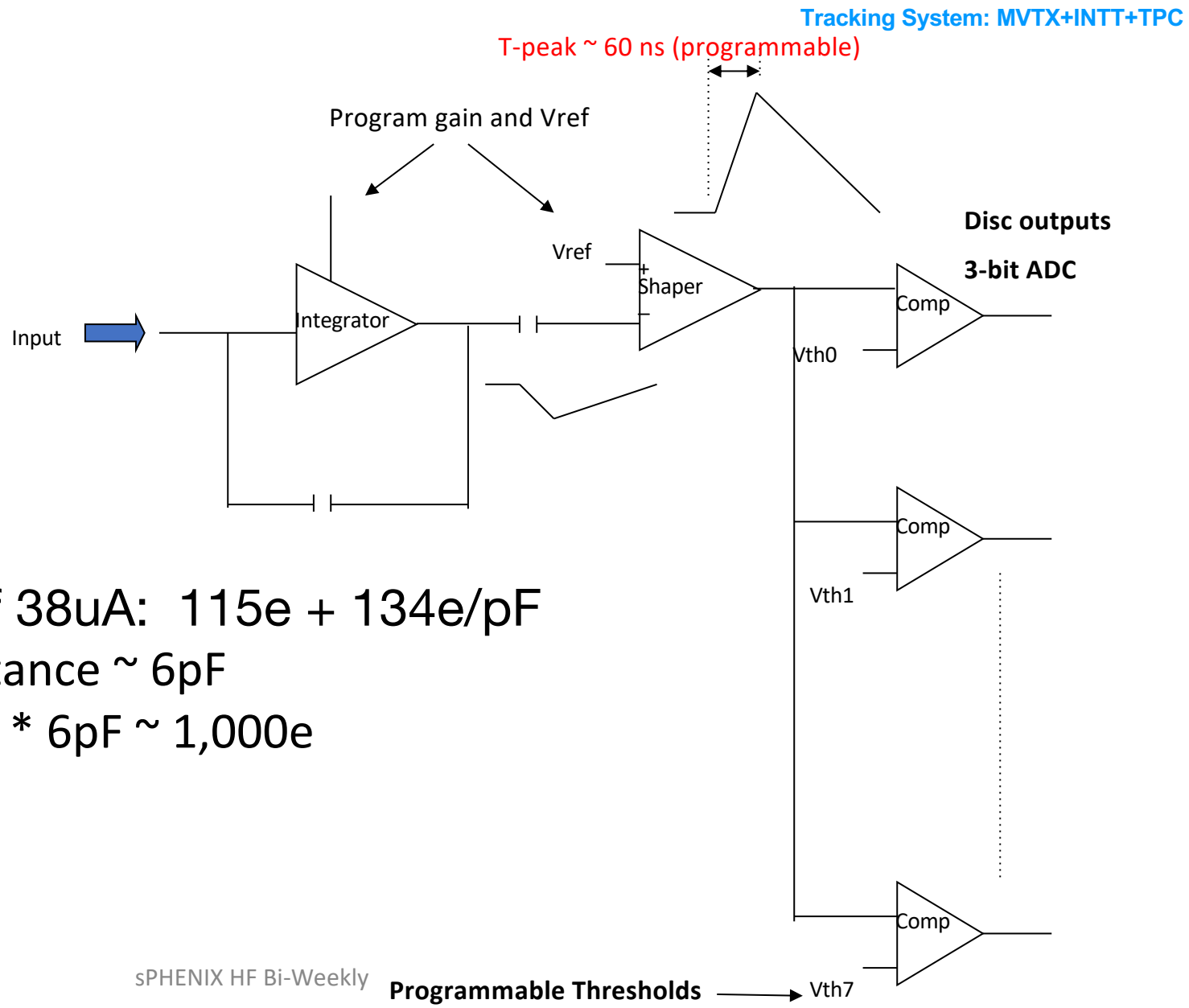
60 ns peak time (rt- pgmbl)

3—bit ADC (th-pgmbl)

Optimized to 1 to 2.5 pf input

115e + 134e/pf

~ 70 to 140 μW/ch (dep. gain)



At max. input transistor bias of 38uA: 115e + 134e/pF

Silicon strip + readout line capacitance ~ 6pF

Predicted noise ~ 115e + 134e/pF * 6pF ~ 1,000e

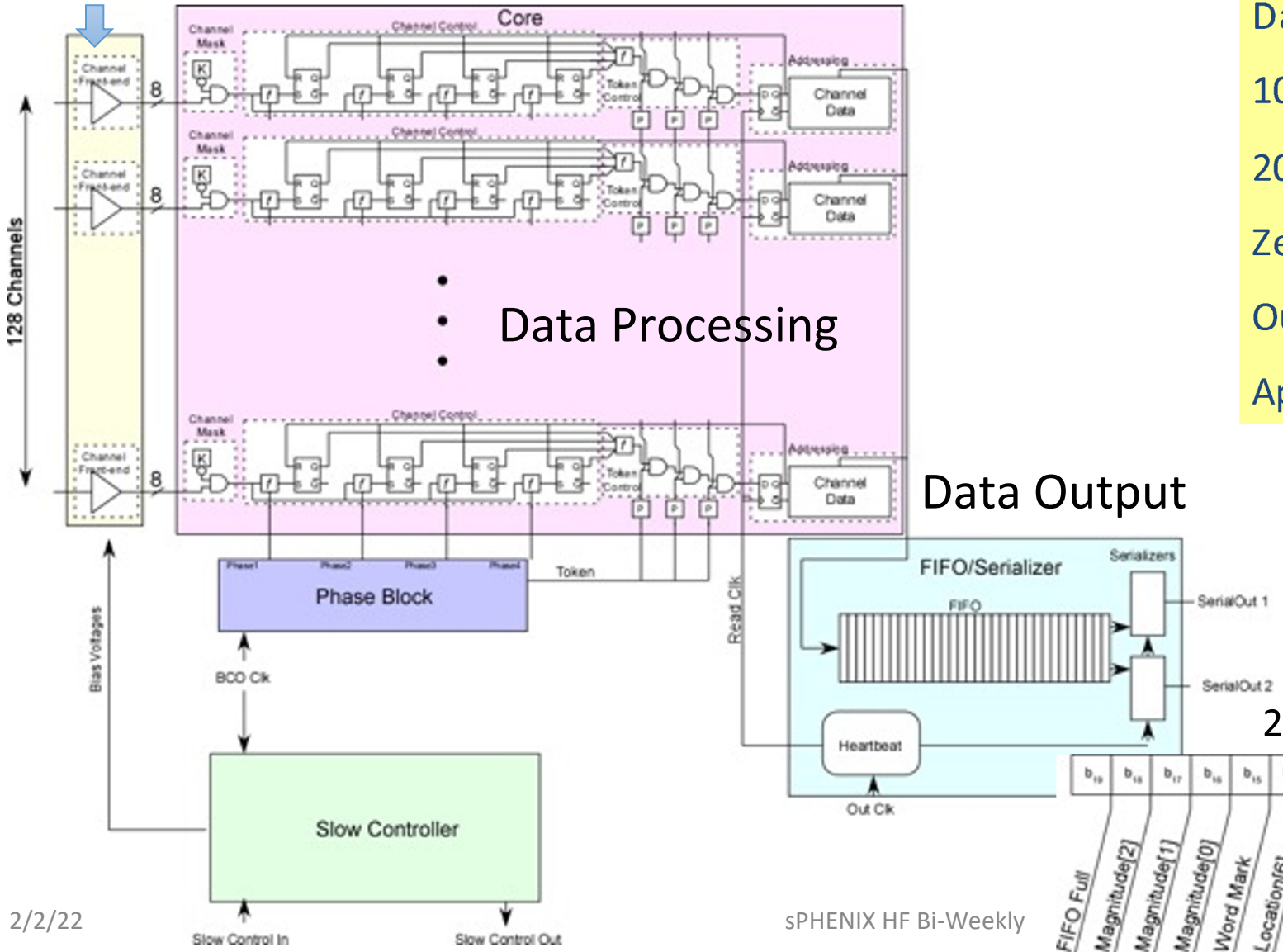
Signal ~ 20,000e

Expected S/N ~ 20/1

FPHX Chip (Digital Section)

Tracking System: MVTX+INTT+TPC

Analog



Data push architecture

10 MHz beam clock (BCO)

200 MHz data clock

Zero suppressed

Output 4 hits/chip in 4 BCO's

Approx. 300 uW/ch

Data Output

20 bit Serial data word structure