

# **MVTX Status & Plan**

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for the MVTX Group

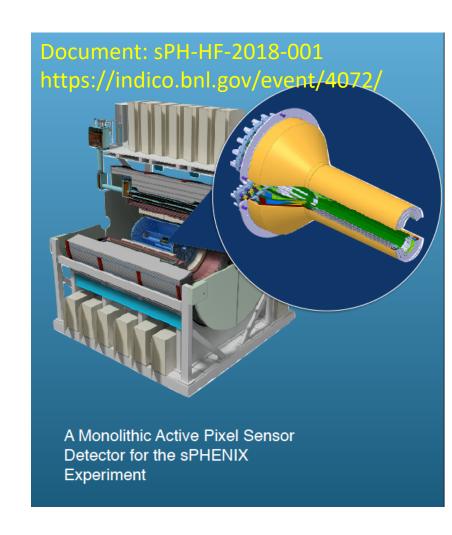
MVTX/HF Workfest @MIT



### Outline

- Project Status
- MVTX full proposal
  - Physics and Simulations
  - Readout and Controls
  - Mechanical Integration
  - Budget and Schedule
- R&D Highlights

Latest development





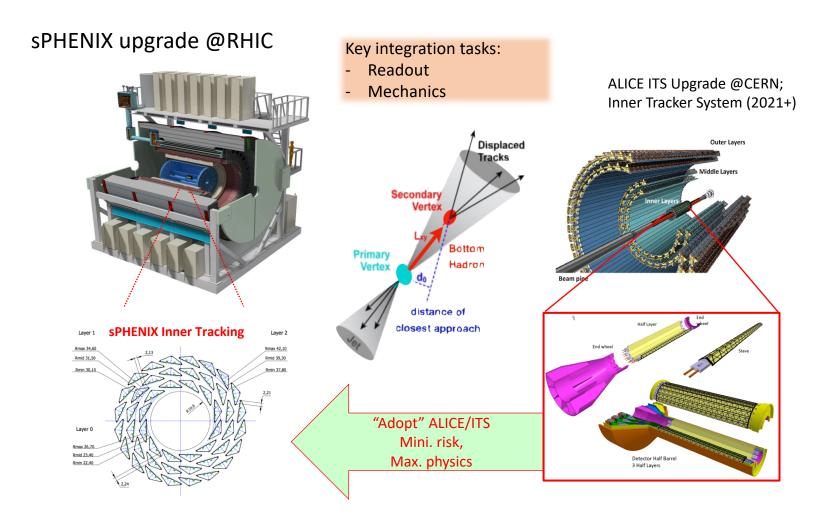
### MVTX Status: Where do we stand?

- Full proposal submitted to BNL Associate Laboratory Director Dr. Berndt Mueller in Feb. 2018
- March 27, a meeting of ALD, MVTX principals, co-SP and sPHENIX project office. Given improved DOE funding fiscal outlook, ALD recommended to bring MVTX into MIE baseline:
  - This would be post-OPC/CD-1 Review(5/23-25, 2018), MIE baseline will be defined in the CD-2 (~summer 2019); MS Project -> P6 in progress
  - Exploring advance-funding options to procure Readout Units (\$250K, now) and staves from ALICE at CERN (\$1.2M, fall 2018)
    - Cost saving and reduce technical and schedule risks
  - ALD seeks DOE agreement to proceed
- MVTX workfest at MIT 4/30-5/1, 2018
  - Refine MVTX roadmap cost & schedule etc
  - Prepare for sPHENIX integration mini review (~summer 18)
    - MVTX+INTT+TPC...
    - Both electrical and mechanical systems

https://indico.bnl.gov/event/4380/



### MVTX: Monolithic-Active-Pixel-Sensor-based VerTeX Detector



MVTX could also be a day-1 EIC detector

4



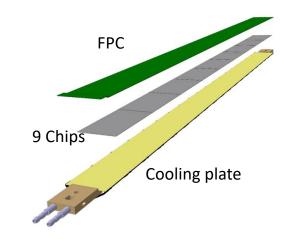
4/29/18

### Monolithic-Active-Pixel-Sensors (MAPS)

**ALPIDE:** The next Generation State of the Art Pixel Sensor

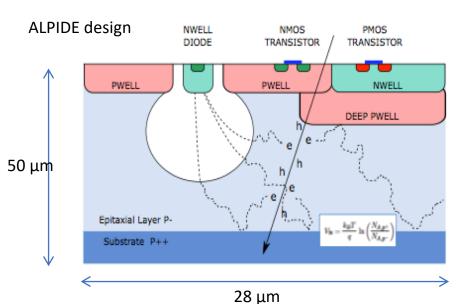
### Advantages of ALICE MAPS(ALPIDE):

- Very fine pitch (27x29 μm)
- High efficiency (>99%) and low noise (<10<sup>-6</sup>)
- Excellent time resolution, ~5 μs
- Ultra-thin/low mass,  $50\mu m$  ( $\sim 0.3\% X_0$ )
- On-pixel digitization, low power dissipation



A 9-chip MAPS stave,  $9 \times (1.5 \times 3 \text{ cm}^2)$ 

### An ideal detector for sPHENIX and EIC physics!



### Tower Jazz 0.18 µm CMOS

- feature size 180 nm
- metal layers 6
- gate oxide 3nm

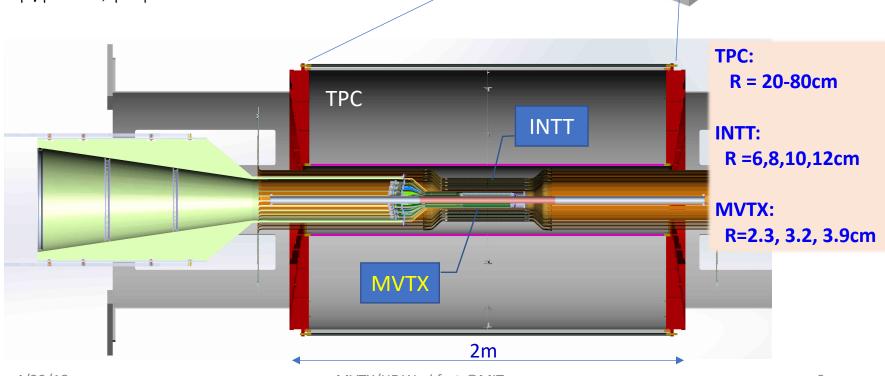
substrate:  $N_A \sim 10^{18}$ epitaxial layer:  $N_A \sim 10^{13}$ deep p-well:  $N_A \sim 10^{16}$ 



### sPHENIX Tracking System

- Excellent Tracking system:
  - TPC: Time Projection Chamber
  - INTT: Intermediate Silicon Strip Tracker
  - MVTX





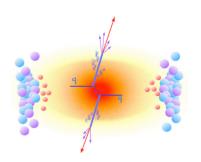


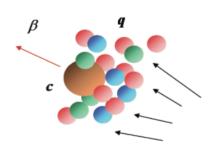
### MVTX Enables the 3<sup>rd</sup> Science Pillar

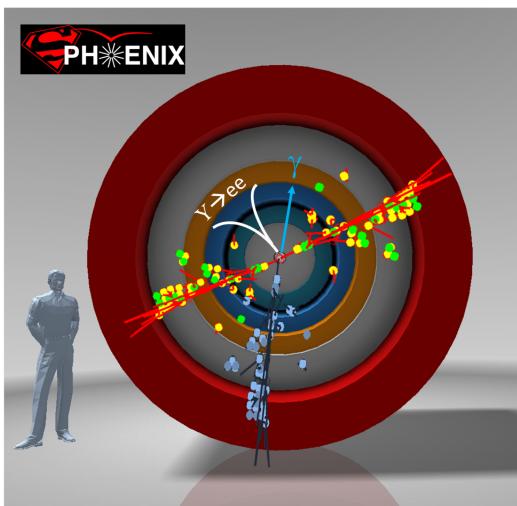
Xin's talk

- 1. Jets
- 2. Upsilons
- 3. Open Heavy Flavor

- Bottom quarks are heavy (4.2 GeV)
- Produced in initial collision, probe QGP evolution
- Well controlled in pQCD
- Provide access to fundamental transport properties





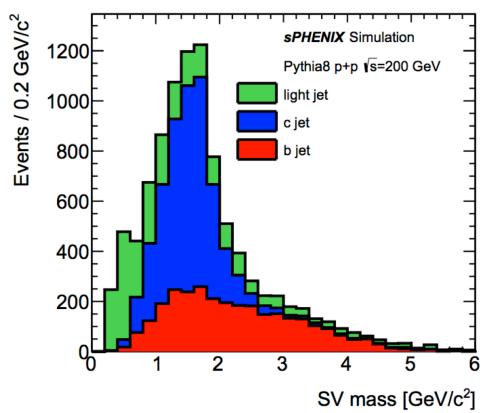


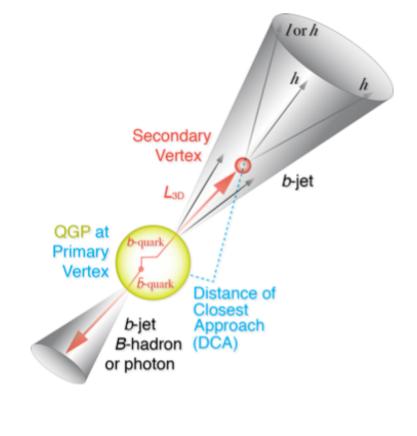


# **B-Hadron & b-Jet Tagging**

Haiwang/Jin's talks

- Detected using the long lifetime of bottom quark hadrons:
  - Displaced tracks
  - Large 2<sup>nd</sup> vertex invariant mass
- Need high precision tracking and vertex determination MVTX!
- Need excellent jet detection capabilities sPHENIX!







### Simulation for *b*-jet and *B*-meson tagging

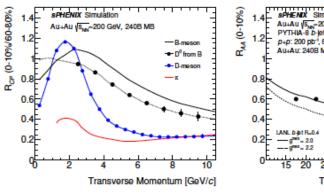
Haiwang's talk sPHENIX Geant4 display of  $p_T$ =30 GeV/c  $B^+$ -hadron Design to Simulation MVTX and INTT MVTX Ladders modeled in details **MVTX** sensors

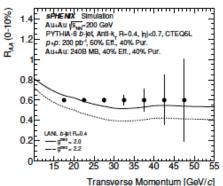
# **MVTX Physics Highlights**

Xin's talk

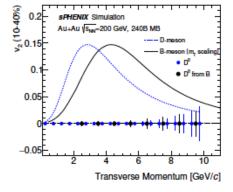
- Heavy quarks unique probe of QGP w/ new scales, m<sub>c</sub>, m<sub>b</sub>
  - Study mass dependence
    - Jet quenching & energy loss
    - Flow interaction with medium
  - Access QGP properties
    - Temperature, density, coupling, transport coefficients, viscosity etc.

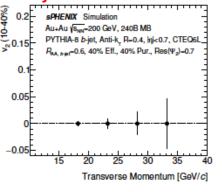
### "B meson and b-jet modification"

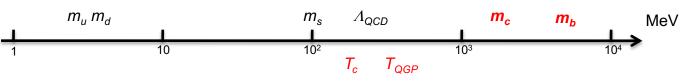




### "B meson and b-jet flow"









# **MVTX** Detector Integration

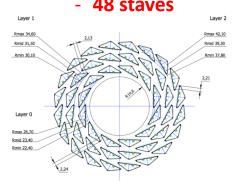
### Mickey/Walt's talks

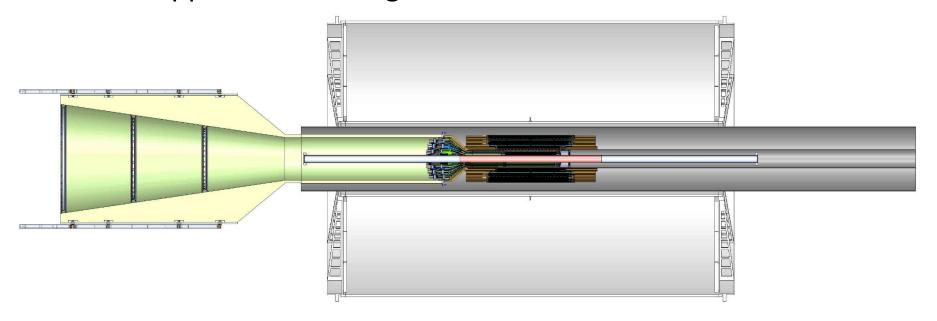
### **MVTX:**

- 3 layers
- 48 staves



- Readout, power, controls
- Mechanical system
  - Support and cooling

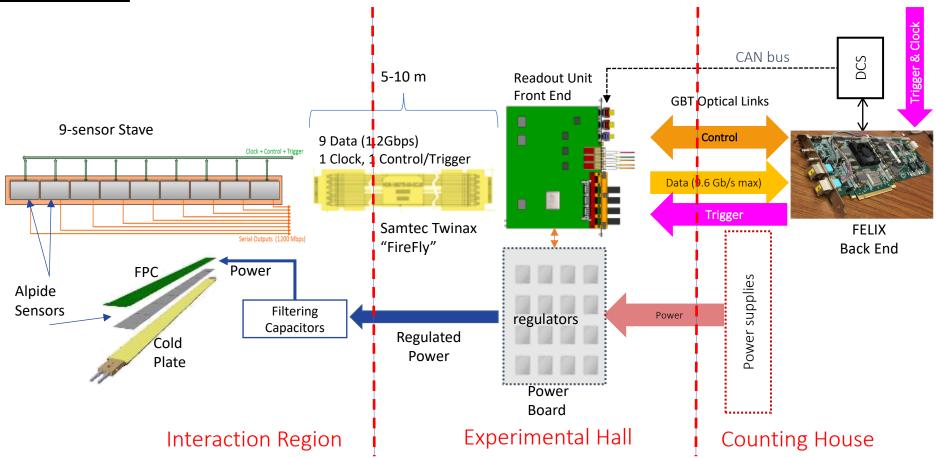




# Readout and Controls



### MVTX Electronics, Power and Controls

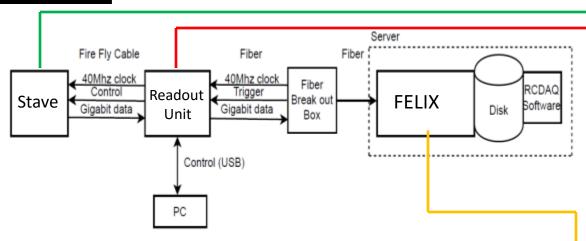


MVTX Detector Electronics consists of three parts

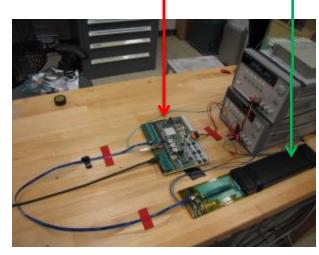
Sensor-Stave (9 ALPIDE chips) | Front End-Readout Unit | Back End-FELIX



### **MVTX Full Readout Chain Demonstrated**



- Readout Unit configures Stave using USB interface
- FELIX distributes clock to Readout Unit
- Readout Unit distributes clock to the Stave
- Stave is triggered, sends data at 1.2Gb/s
- Configured GBT link to recover clock from FELIX
- Readout Unit receives the data and sends the data to FELIX over fiber using GBT link
- FELIX packs data, stores it on disk using RCDAQ the sPHENIX data format and software



Readout Unit + Stave



Server + FELIX

Amazing work done by Sho & Alex + LANL LDRD team!
4/29/18
MVTX/HF Workfest @MIT

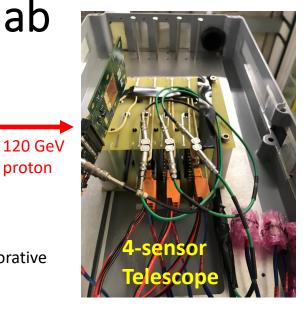


# MVTX Test Beam at Fermilab 02/20-03/10, 2018

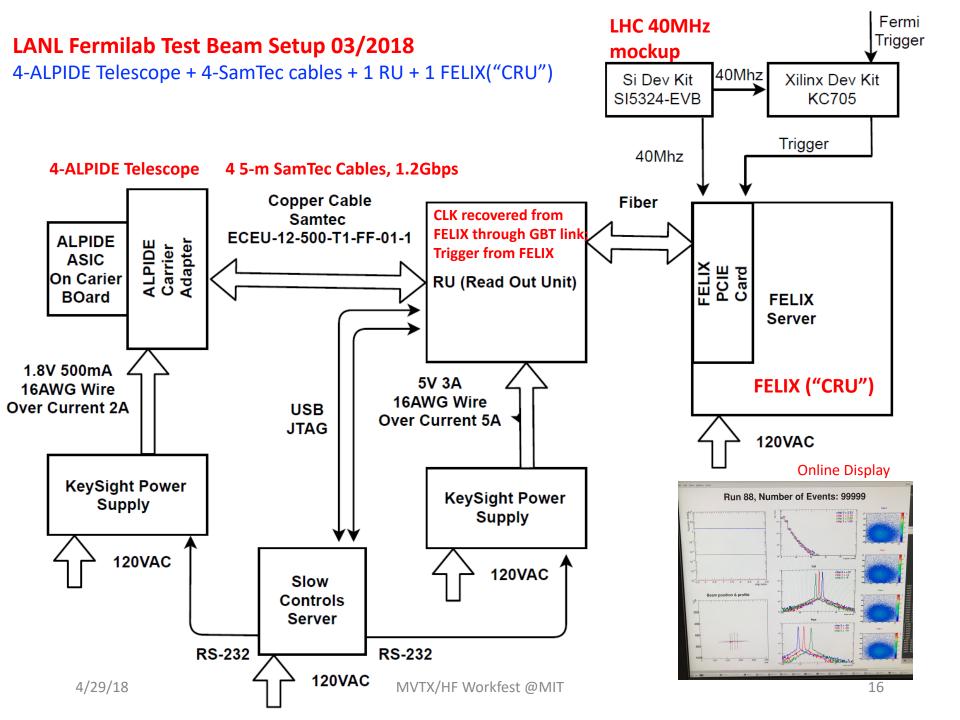
- Goals:
  - Test full readout chain
  - Evaluate ALPIDE sensor performance
- Experimental setup
  - A 4-sensor telescope
  - Full readout chain: MAPS+RU+FELIX+RCDAQ

proton

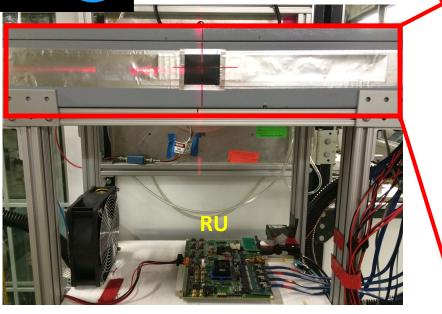
- Parasitic with INTT run
- Very productive & collaborative







### 4-ALPIDE Telescope Setup at Fermilab Test Beam





FELIX("CRU") in Server

### **Summary:**

SPHENIX

- Successfully operated the full readout chain
- Confirmed all communications links and data path
- Confirmed telescope performance
  - Primarily 120GeV proton beam; also with low energy pion beams
  - Beam trigger rate ~7kHz
  - Tested High ALPIDE occupancy runs, with
     10cm lead bricks in front of the sensors

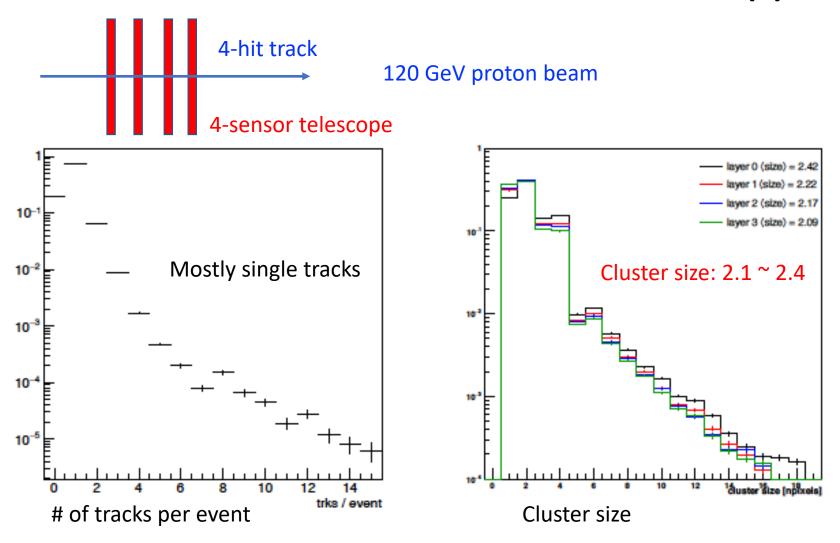
runs, with e sensors

- others
MVTX/HF Workfest @MH

Nice work by Sho, Alex, Hubert, Chris + others



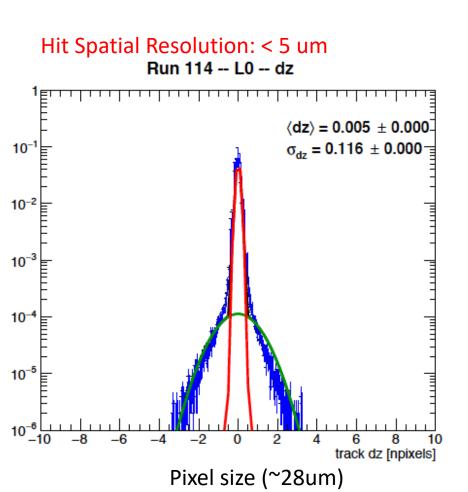
# | Fermilab Test Beam Results (I)

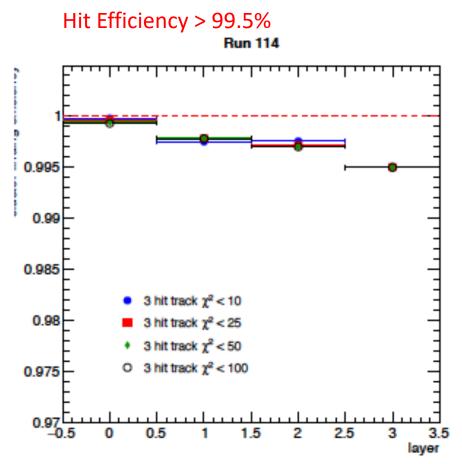


Beautiful analysis done by Sanghoon and Darren + others



# Fermilab Test Beam Results (II)

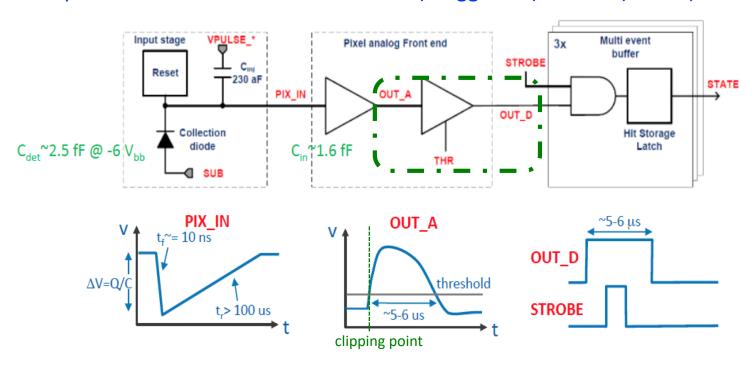






### **ALPIDE Readout Optimization and Trigger Latency Study**

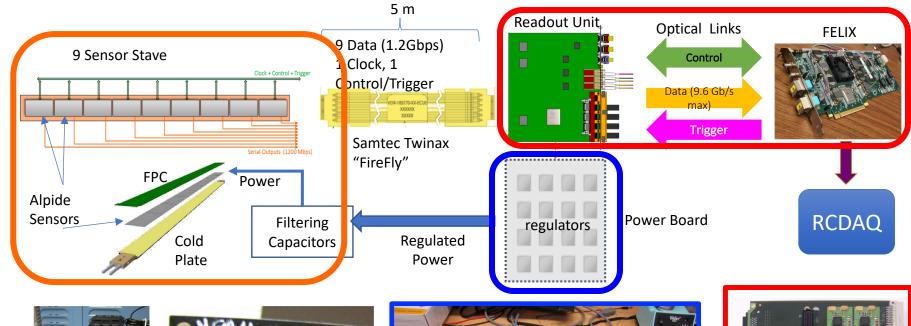
- Expected sPHENIX trigger latency 4~5 uS
- Two possible readout modes for MVTX: 1) Triggered (less data) and 2)Continuous



- OUT\_A clipping: VCLIP. Decreasing VCLIP decreases clipping point.
- OUT\_A returns to baseline time: ITHR, VCLIP. Increasing ITHR decreases discharge time, and decreasing VCLIP decreases discharge time after clipping.
- OUT\_D return to baseline time: IDB. Increasing IDB increasing charging time hence decreasing pulse duration.



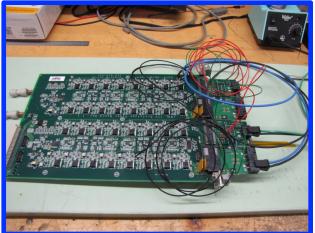
### A Test Bench at LANL







One HIC and 5+ individual ALPIDE chips.



**Power Board** 



**MOSAIC** miniDAQ



### Trigger Latency and Signal Shaping Time Study

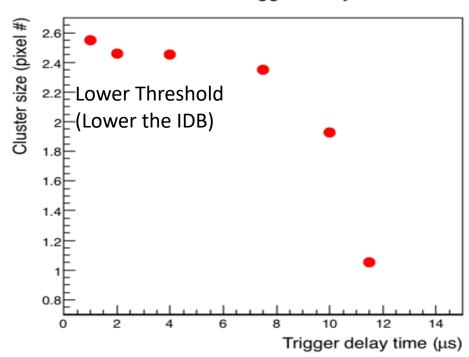
 Lower the OUT\_D threshold (IDB) increases the trigger duration time, but also increases the cluster size which might include more background hits.

In the continuous readout mode, "trigger/strobe" can start as early as ~1uS

### Cluser Size VS trigger delay time

# Default set | SPHENIX | 1.8 | 1.6 | 1.4 | 1.2 | 1.2 | 1.2 | 1.4 | 1.2 | 1.2 | 1.5 | 1.6 | 1.4 | 1.2 | 1.2 | 1.5 | 1.6 | 1.4 | 1.2 | 1.5 | 1.6 | 1.4 | 1.2 | 1.5 | 1.6 | 1.4 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5

### Cluser Size VS trigger delay time



Nice work done by Xuan, Sho and Alex + others



### To Do List

- Update firmware, sync with latest ALICE firmware
  - Scrubbing etc.
  - Burn-in test, stability
- Detector Control System (DCS) integration
  - Power distribution and monitoring
  - LV, "HV" and temperature
- Sensor operation optimization
  - Scan parameters for optimal operation
  - Laser test bench setup at LANL
- Multi-stave readout
  - Up to 3 staves per RU
  - Default: 1 stave per RU

# sPHENIX System Integration

# INTT-MVTX Space Conflict

INTT Acceptance

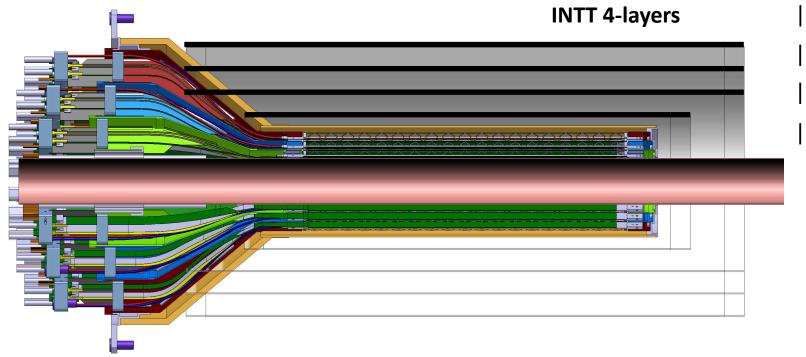
@ |z|=10

|η|<0.95

|η|<1.09

|η|<1.28

|η|<1.12

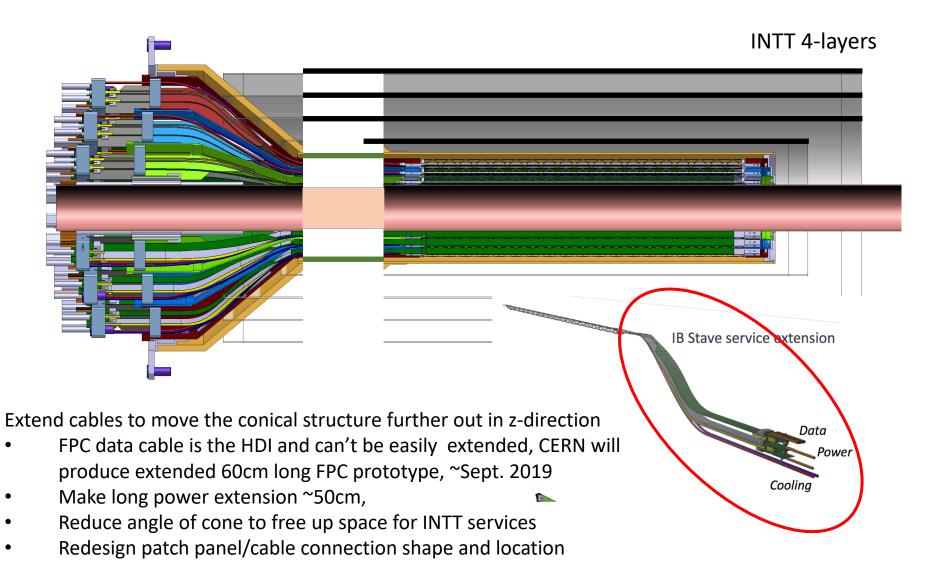


- Currently a clear conflict between the INTT and MVTX
  - INTT only includes ladder, no connectors, cooling barbs, etc

### R&D items:

- 1) Extend cables to move the conical structure further out in z-direction;
- 2) Design/optimize INTT layers to fit current MVTX geometry;
  - FPC data cable can't be easily extended (max additional ~10cm, machine limit)
  - Reduce angle of cone redesign C-structures and connectors

# INTT-MVTX Conflict





4/29/18

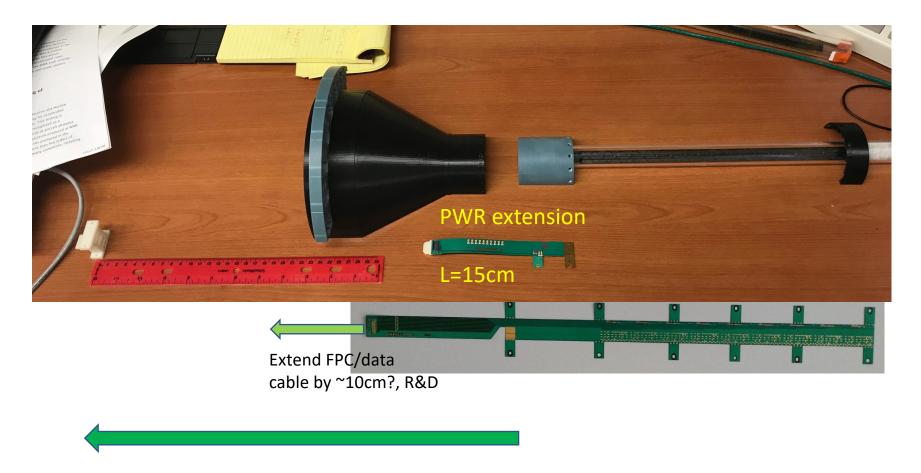
# MVTX Flexible Printed Circuit (FPC)

Extend MVTX Service Cables?

Maximum ~60cm for HS signal, TBD through R&D

506.2 mm CHIP 9 CHIP 2 Extend FPC/signal path by ~10cm The 9 silicon chips are read out in parallel: each chip sends its data stream to the end of Stave by a dedicated differential pair, 100  $\mu m$  wide. Two additional differential pairs distribute the clock and configuration signals.

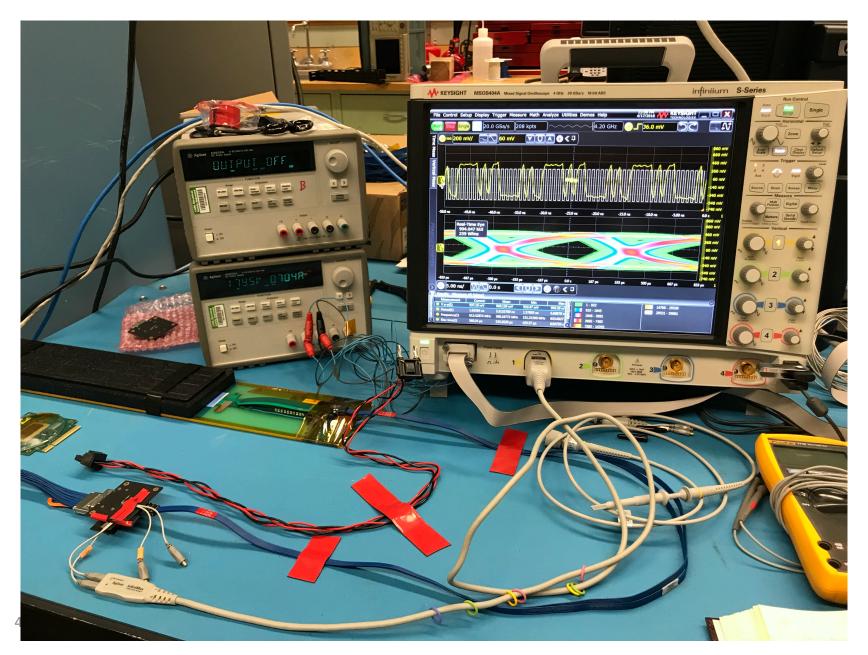
# MVTX Mockup & FPC Extension R&D



Extended power cables AVDD/DVDD:

 $L = ^50$ cm, and possibly with  $2^3$  different lengths, like 30cm and 40cm Separate PWR and signal connections at different Z-locations.

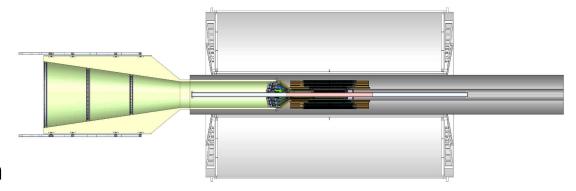
# SamTec Cable and FPC Extension R&D





### To Do List

- FPC extension
  - Signal path, +10cm
  - Power extension, ~50cm



- SamTec cable length vs signal quality
  - 5~7m
  - RU location, MVTX electrical system integration

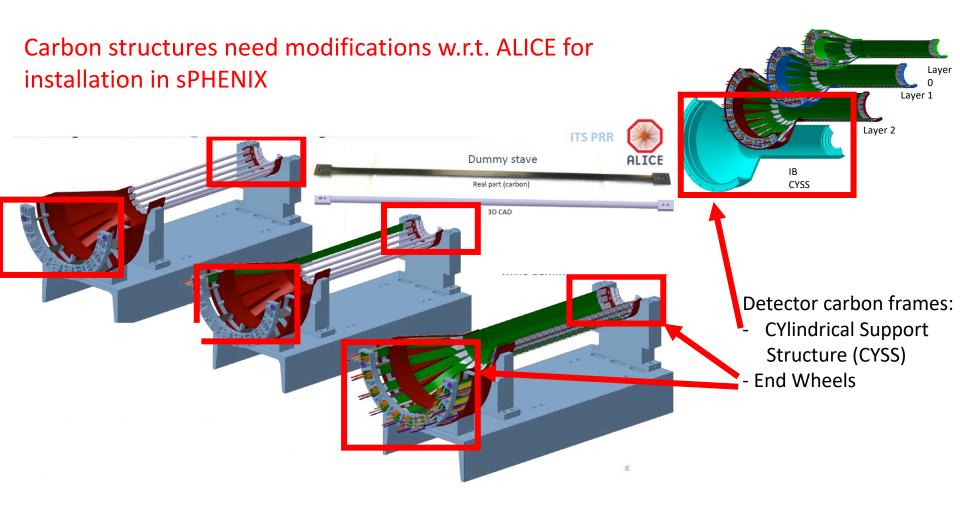
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- Carbon structure and connector design
  - FPC HS signal connectors
  - FPC power extension connectors
  - MVT Service barrel and mechanical system integration
  - Installation procedure

# Carbon Structures



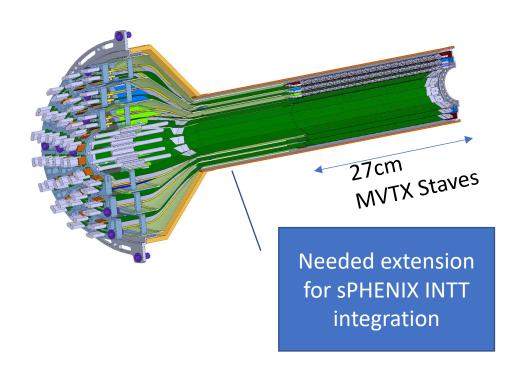
# **MVTX Carbon Structures**

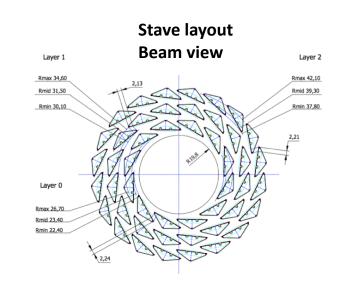


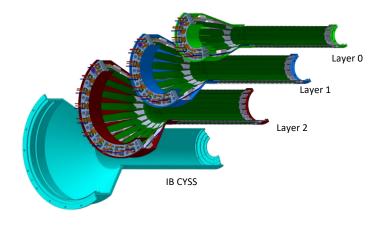


# MVTX Mechanical Conceptual Design

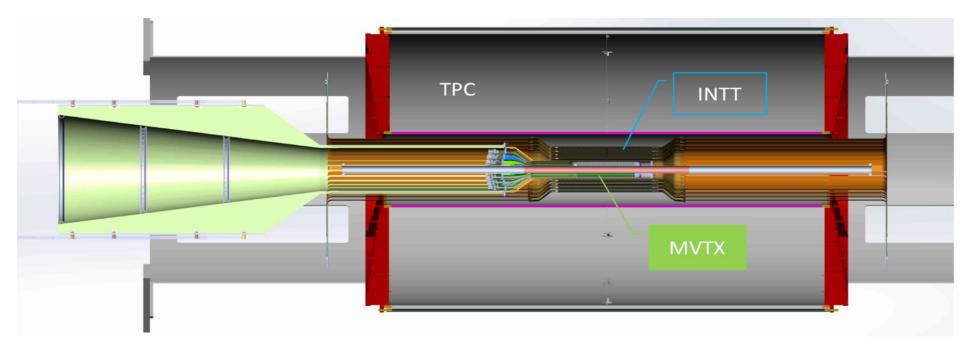
 View of MVTX half detector assembly with extended central barrel



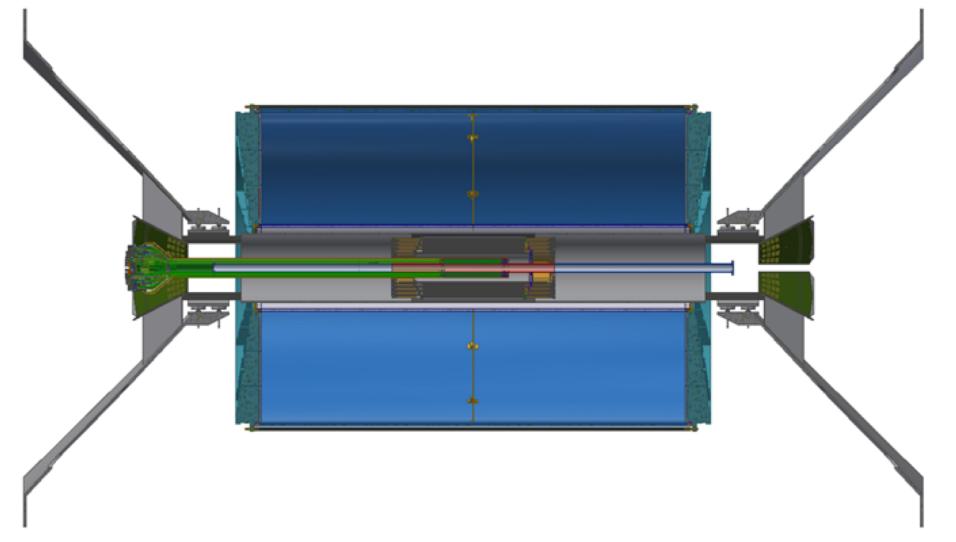




# sPHENIX Integration: MVTX + INTT + TPC



# Another one: MVTX + INTT + TPC from Dan Cacace, 4/27/2018



# Cost & Schedule

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## Updated Major Cost Items

Potential saving: ~\$500K

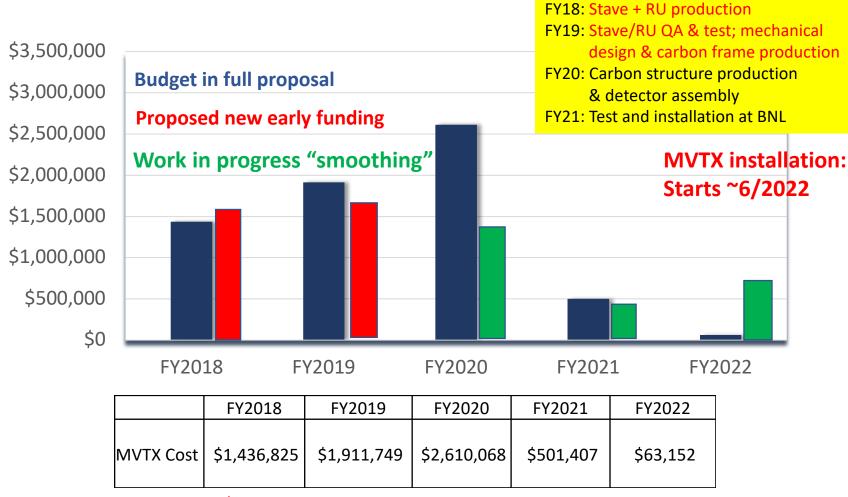
WBS	Task Name	Cost (K)	Cost with Contingency+ Passthru (K)
1.5.3.1.1	Produce 84 staves	\$966	\$1.2M <b>\$1337</b>
1.5.2.2	Readout Units(RDO)	\$480	\$250K <b>\$664</b>
1.5.5.3.2.3.2	CYSS Cylindical Structure	\$319	\$424
1.5.5.3.2.3.3	COSS Conical Half Shell	\$329	\$438
1.5.4.3	Safety Systems	\$139	\$191
1.5.4.4	Stave Support+ Global Interface	\$308	\$465

Table 6: Major Cost Items

1 CHF = 1.01 US \$, 4/29/2018



#### **sPHENIX MVTX Cost & Schedule Profile**



New numbers: \$1.52M \$1.6M

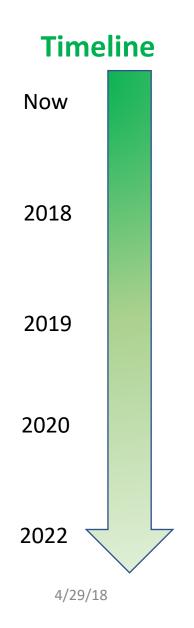
**RU units moved from FY19 to FY18** 

\* 50% cost reduction due to joint production with ALICE

FY20-22: funding profile smoothing



### Possible Contributions from China?



- Offline detector and physics simulation
  - sPHENIX
  - EIC

(MVTX & Heavy Flavor Topical Groups)

- FPC extension R&D at CERN, LANL
  - MVTX+INTT+TPC integration
- Electronics production test and QA
  - Readout Units/CERN, FELIX/BNL
  - Power boards and control system
- Stave assembly, test and QA
  - CERN, China, US
- Slow control firmware/software development
  - Online monitoring
  - Safety controls
- Carbon structure design and/or fabrication?
- Detector assembly and test
  - LBNL, half-barrel assembly, test, QA
  - Final assembly & installation at BNL



### **RU Production Plan**

#### Plan-A

- To be part of ALICE ITS production
- Timeline:
  - Production starts ~May 2018, available by ~end of 2018, fully tested
- Need to make commitment "NOW"
  - BNL management actively working on funding RU through RHIC \$

#### Plan-B

- Produce RU later, ~2019 as funding allows?
  - Procure GBT chips from CERN
  - Production & test in US, UT-Austin, LANL et al.
- Higher cost, 2x
- Higher technical and schedule risks



## Stave Production Plan

#### Plan-A

- Produce staves following the completion of ALICE IB at CERN, using ALICE facility
- Timeline:
  - Starting as early as Aug/Sep 2018 +, last about 6 months for production and test
- All 84 staves produced and tested at CERN
- BNL management actively working with DOE to build staves at CERN

#### Plan -B

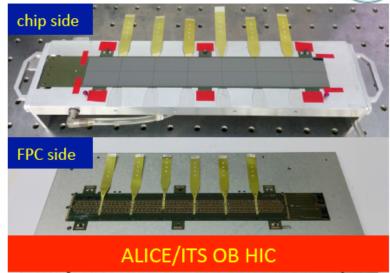
- Produce full staves at CCNU later as funding allows, ~2019?
- Earliest starting date May 2019 + , ~12 months (could be shorter)
- Higher technical and schedule risks
- Impact on cost, TBD

#### Following Slides from Yaping Wang/CCNU, 1st sPHENIX workshop in China

#### Effort & Plan on MVTX – Feasibility



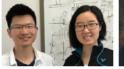
- Efforts on ALPIDE chip design since 2012
- Machine workshop (~150 m²)
- Clean room was constructed and run in good status since November, 2016
  - ✓ Ground floor (vibration velocity RMS ~ 3 µm/s)
  - √ Temperature/humidity controllable
  - √ ISO6 clean level ~ 70 m² (2.6 m head room) +
    ISO7 clean level ~ 20 m² (2.9 m head room)
  - ✓ Grounding terminals provided (ESD protection)
  - √ Gas supply system
- Pixel chip assembly & inspection machine (IBS ALICIA-6), wire-bonding machine (F&K Delvotec G5 64000), pull tester (DAGE 4000) and HIC testing system are in working status
- 20% ALICE/ITS OB HIC module assembly & test (~7500 ALPIDE chips) for one year
- Pre-series production started in Dec. 2017
- Series production started in April, 2018
- Long-term plan: (1) ALICE ITS calibration and alignment; (2) open-bottom production at LHC.





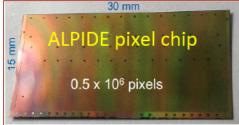
#### **Expertise @CCNU**

#### Effort & Plan on MVTX – Feasibility





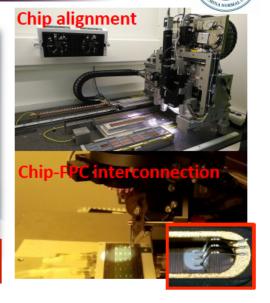




ALICE/ITS Chip Design/ Testing (CCNU): Chaosong, Ping, Mangmang, Shuguang



ALICE/ITS OB HIC Assembly Team (CCNU): Biao Jun Daming Kai Peipei Wenjing





April 22, 2018

Effort & Plan on MVTX -- Yaping (CCNU)

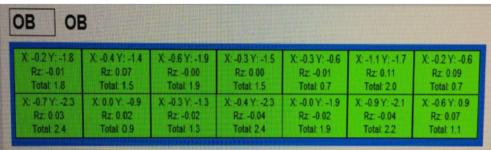
#### **HIC Production @CCNU**

#### Effort & Plan on MVTX - Feasibility

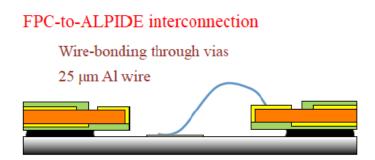


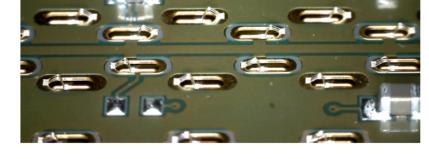
 ALPIDE chips (dimension of 3cmx1.5cmx100μm) can be automatically aligned with positioning accuracy of better than 5 μm@3σ by the ALICIA machine.





 The chip-FPC interconnections are realized with wire-bonding method, which is done fully automatically by the F&K G5 64000 machine with positioning accuracy ~ 5 μm@3σ (large working area).





R&D on chip-FPC interconnections technology, such as laser bonding.

#### **Stave Production @CCNU**

#### Effort & Plan on MVTX - Interests



- Physics interests on the sPHENIX/MVTX at RHIC
  - B-jets & B-hadrons
  - > HF-jet correlations
  - **>** ...
- MVTX stave assembly and test
  - > sPHENIX MVTX effort can be started after the ALICE ITS upgrade project (around May, 2019)
  - > Facilities and technical resources of CCNU and other institutes are available for HIC production (replace assembly jigs + short-time training)
  - Infrastructures and tooling need to be constructed for stave assembly & test + technical training
  - > Estimated production period: 1 year for 84 staves (~4 months for HIC assembly/test + ~8 months for stave assembly/test incl. training)
- MVTX detector and physics simulations

#### Effort & Plan on MVTX – Organization & Time Schedule



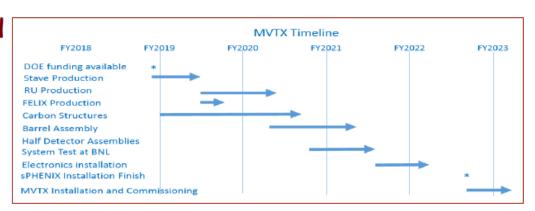
#### Participants from China side:

- 1) Central China Normal University (CCNU): stave assembly & test
- Institute of Modern Physics (IMP/CAS): stave assembly & test (collaborated with CCNU)
- University of Science and Technology of China (USTC): chip & stave test, simulations
- 4) Sun Yat-Sen University (SYSU): MVTX detector and physics simulations

#### Manpower: New: Also IHEP silicon group possibility

- > 2 FTE + few students from CCNU (additional postdoc in due time)
- > 2 FTE + few students from IMP/CAS
- Other institutes?

## Production can be started since May 2019 after ALICE ITS upgrade:





## Carbon Structure Design and Fabrication

- Mechanical system design
  - MIT + LANL + LBNL + BNL
- Production
  - LBNL
- Alternative path for fabrication being explored
  - Europe (France & Italy, used for ITS Upgrade)
  - Asia (Korea, China)

## Quote on "CYSS" from Korea

#### from Prof. Kwon/Yonsei Univ.

NO: YS18042701



인천 남동구 논현동 429-11 남동테크노 파크 B 동 401호

: 032-463-7948 / Fax : 032-463-7949

Cust Cust Name Provider C.C Date

연세대학교 권 영 일 교수님 27-Apr-18 15 days

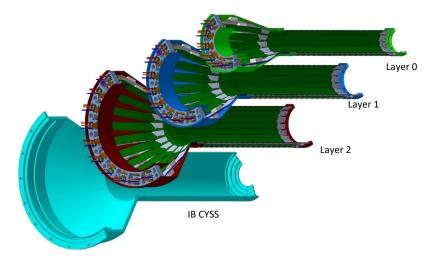
Payment Delivery Place Cancellation

T/T Advance 100% Korea 90% for less than 1 weeks after Purchase Order received

#### QUOTATION

O Price List for Fabrication for ITS detector Upgrade parts

NO	DESCRIPTION	Q'TY	U/PRICE	AMOUNT	
	* ITS Detector Upgrade	1 Set		\$	3,00
1	IB-CYSS Flange	1			
	- Matrial - AL (Treatment : Hard Anodizing (Black)				
	Need to reconfirm matrial (AW-7075)				
	Normally we are using AL 6061				
2	IB-CYSS Cone	1			
	- Matrial - Carbon Fiber				
3	IB-CYSS Cylinder	1			
	- Matrial - Carbon Fiber				
4	IB-CYSS Flange C Side	1			
	- Matrial - AL (Treatment : Hard Anodizing (Black)				
	Need to reconfirm matrial (AW-6082)				
	Normally we are using AL 6061				
	Total Amount			\$	3,00



Based on **ALICE CYSS** design AutoCAD:

~\$3K, 5 weeks delivery

- One of two IB CYSS shell only
- Will follow up on this development, also for the end-wheels/conical shells

**MVTX Project:** 

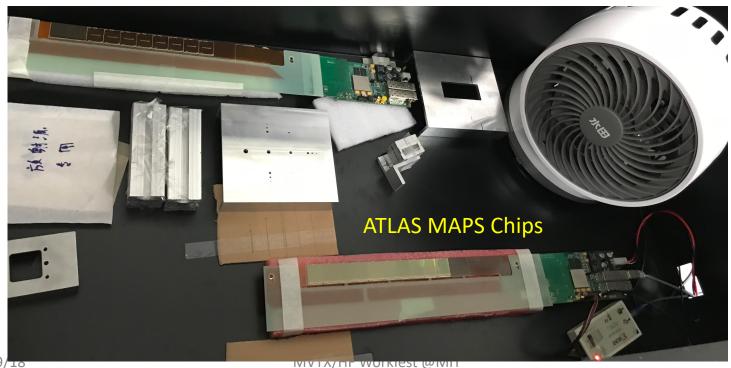
CYSS: \$424K (included review/design: \$40K)

(\$103K Material + 216K Labor + 37%)



## Institute of High Energy Physics in China (IHEP) - Silicon Group

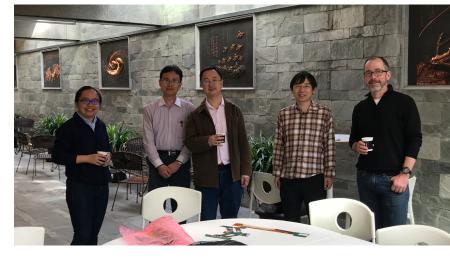
- IHEP is working on ATLAS MAPS detector R&D
  - Carbon structure
  - Sensor and readout
  - Very interested in sPHENIX MVTX project



# Encouraged IHEP Silicon Group to join sPHENIX!

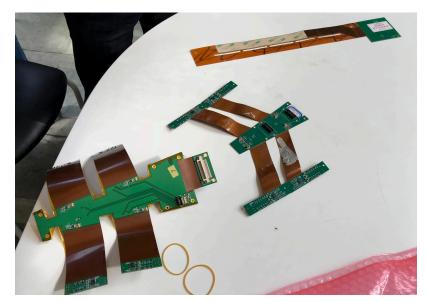
- Carbon structure R&D
  - A local institution, material science, in Hangzhou





#### • FPC R&D

 A local company, can make up to ~100cm long "Copper FPC", "Al" not clear





## Summary and Outlook

MVTX full proposal completed

Document: sPH-HF-2018-001

Expanded science

https://indico.bnl.gov/event/4072/

- sPHENIX baseline
- Cost and schedule update in progress
  - Major item cost and production plan
  - Funding profile smoothing
- Excellent progress in R&D
  - Readout and controls proof-of-principle demonstrated
  - Conceptual mechanical system design being developed
  - Possible new collaboration on carbon and FPC work
- MVTX+INTT+TPC integration in progress
  - Electrical and mechanical system
  - sPHENIX wide coordination through Office of Integration
    - Mini sPHENIX integration review in ~June 2018?
- To be ready for sPHENIX Day-1 Physics in 2023
  - sPHENIX and later EIC possibility



## Backup slides

4/29/18 MVTX/HF Workfest @MIT 52

## Physics

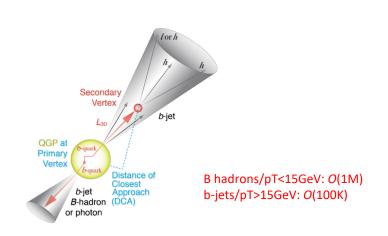


#### RHIC Multi-Year Plan: sPHENIX 2023-2027+

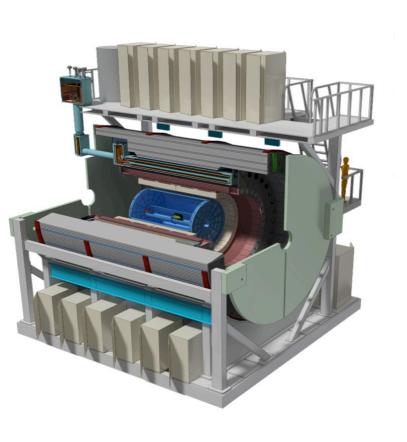


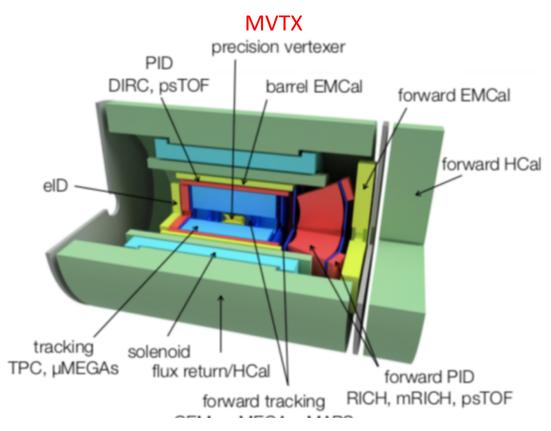
Year	Species	Energy [GeV]	Phys. Wks	Rec. Lum.	Samp. Lum.	Samp. Lum. All-Z
Year-1	Au+Au	200	16.0	$7~{ m nb^{-1}}$	$8.7 \; { m nb^{-1}}$	$34~\mathrm{nb^{-1}}$
Year-2	p+p	200	11.5	_	$48~{ m pb}^{-1}$	$267 \ { m pb^{-1}}$
Year-2	p+Au	200	11.5	_	$0.33 \; \mathrm{pb^{-1}}$	$1.46~{ m pb^{-1}}$
Year-3	Au+Au	200	23.5	$14~\mathrm{nb^{-1}}$	$26~{ m nb}^{-1}$	$88 \; { m nb^{-1}}$
Year-4	p+p	200	23.5	_	$149~{ m pb}^{-1}$	$783 \; { m pb}^{-1}$
Year-5	Au+Au	200	23.5	$14~\mathrm{nb^{-1}}$	$48 \; { m nb}^{-1}$	$92 \; { m nb^{-1}}$

- Precision B-tagging w/ MVTX:
  - Tracking resolution better than 50um @pT=1GeV
  - High multiplicity HI collisions
  - Low multiplicity but high rate p+p collisions
  - High efficiency and high purity



## Physics & Simulations: from sPHENIX to EIC



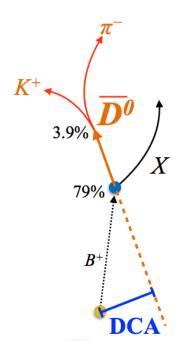


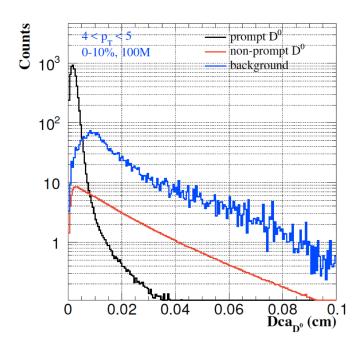


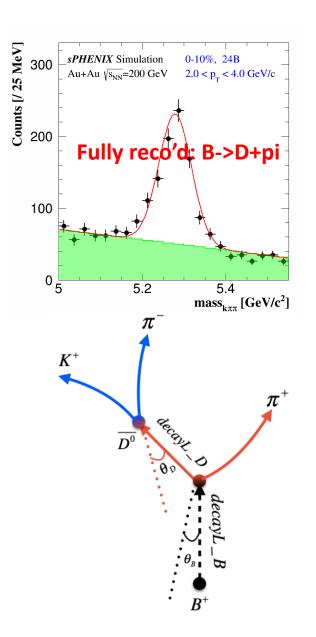
## **B-hadron Tagging**

- Impact parameter (DCA) method to tag non-prompt D<sup>0</sup> from B-meson decays
- Inclusive and exclusive channels possible

#### Partial reconstruction: B->D+x



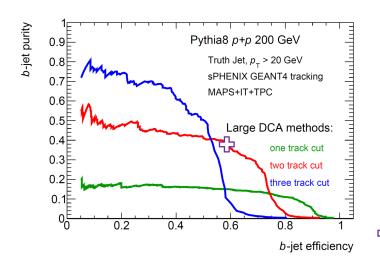


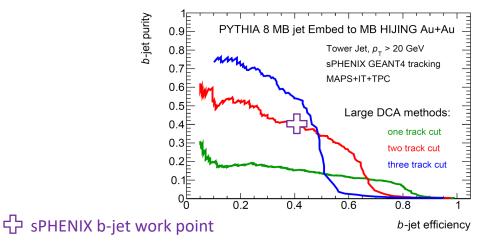




## b-jet Tagging in p+p and Au+Au

- Fully implemented MVTX models used in performance projection
- b-jet tagging projection evaluated with full tracking + calorimetry simulation
  - Tagging work point has been stable (60% Purity 40% eff for pp)
  - Central Au+Au Tagging work point has been stable (40% Purity 40% eff)
- Performance has been stable using truth jet finding or calorimetry reconstructed jet finding

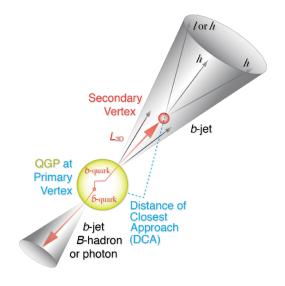


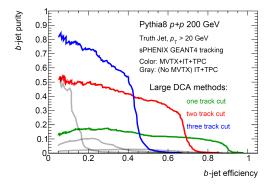


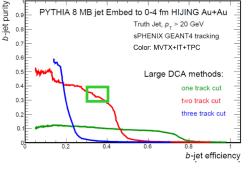


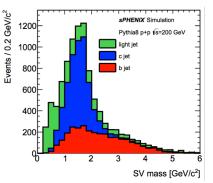
## B-jet tagging

- Multi-tracks w/ large DCA
- 2<sup>nd</sup> vertex mass reco'd







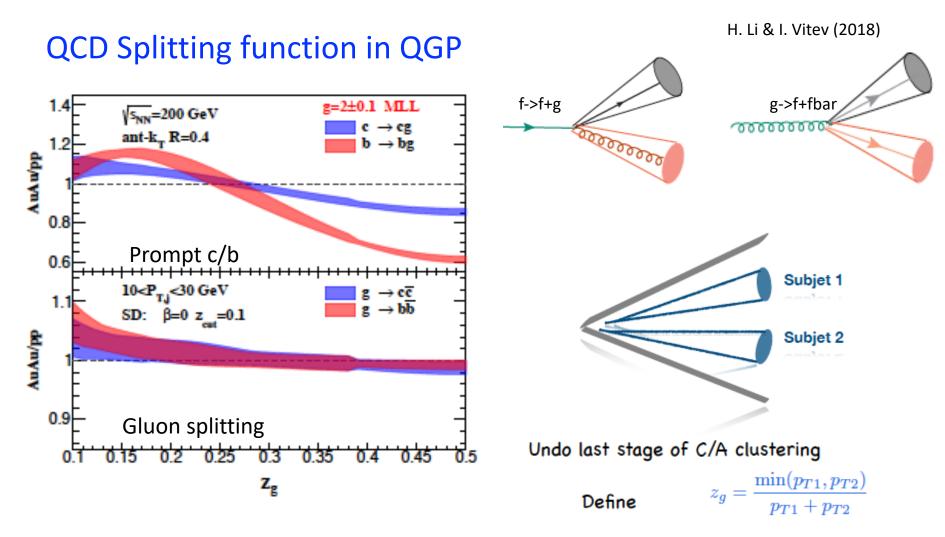


58

CMS work-point, Phys. Rev. Lett. 113, 132301 (2014)



## New Insight into QGP: HF-Jet Substructure





## New Insight into QGP: B v2

#### Very active theoretical investigation:

°2 (10-40%) 0.15 (0.40%)

0.1

0.05

-0.05

sPHENIX Simulation

- LANL model
- **CUJET**
- Duke model
- **TAMU**
- **UrQMD**
- **AMPT**
- **PHSD**
- Ads/CFT
- **BAMPS**
- **HQ+EPOS2**
- **JetScape**

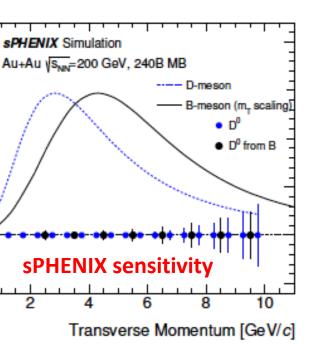
#### Various new model calculations, PHSD, AMPT etc, for B-hadron v2:

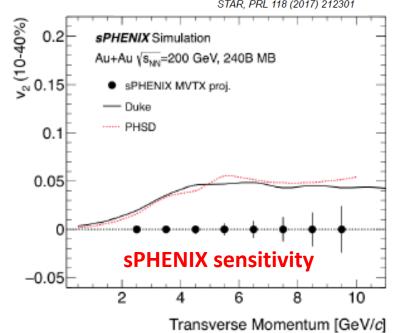
- Significant non-zero v2 suggested, but may NOT follow the scaling due to large b-mass!

#### STAR Au+Au @ 200 GeV 10-40% 1.5 2.5

 $(m_{_{\rm T}} - m_{_{\rm 0}}) / n_{_{\rm d}} (GeV/c^2)$ 

D-meson: v<sub>2</sub> scaling observed at RHIC

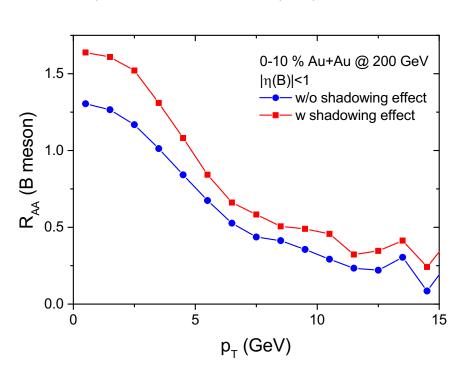


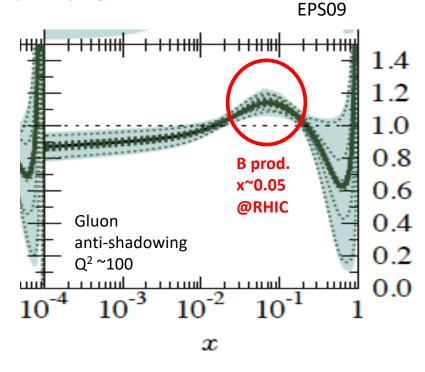


## e Theoretical Inputs (II): B-meson R AA

#### New calculations from PHSD for B-hadrons:

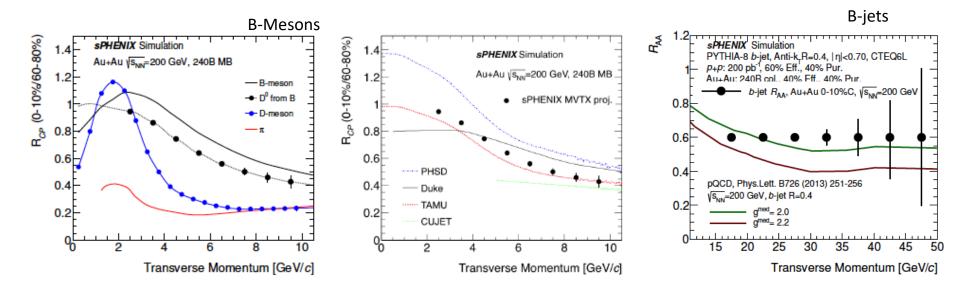
- Potential significant anti-shadowing effects
- Open b-bar in AuAu, very important baseline for Upsilon program!





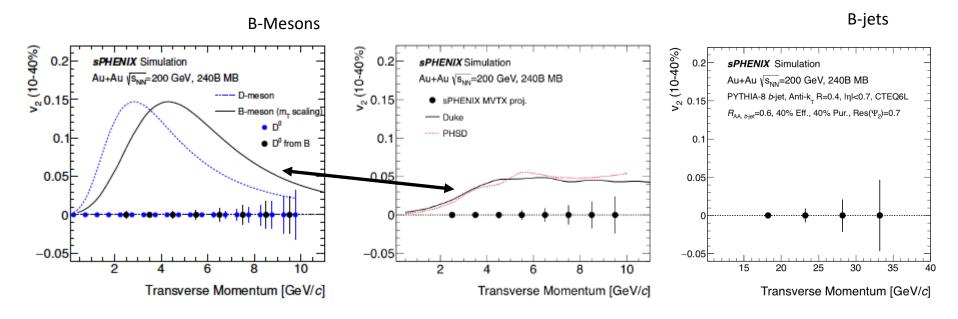
## sPHENIX Projected R<sub>AA</sub> Sensitivity

Open questions to be answered: energy loss mechanisms and QGP medium properties



## sPHENIX Project Elliptical Flow v<sub>2</sub>

Open questions to be answered: nature of quasi-particles, medium interactions and transportation





## More information



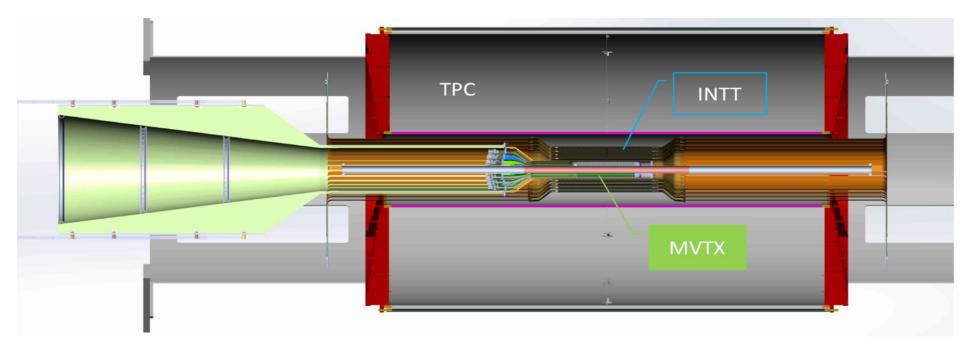
## Summary: Major Remaining R&D

- Mechanical/Electrical integration with INTT+TPC
  - Carbon structure design
  - FPC extension

- Full electrical system control
  - Power
  - Safety
  - Online monitoring & controls
  - Integrate readout system firmware/software with slow controls

## Mechanical Integration

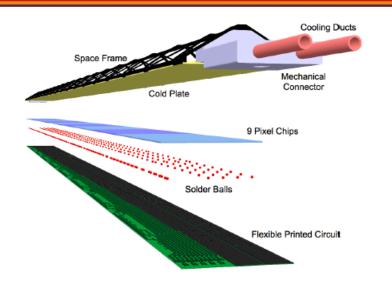
## sPHENIX Integration: MVTX + INTT + TPC

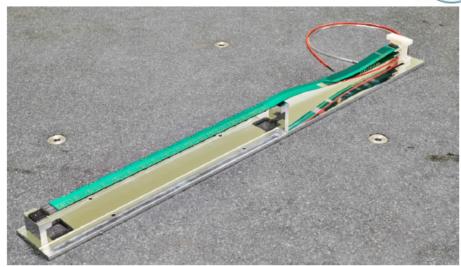


#### **Stave Production @CCNU**

#### Effort & Plan on MVTX – Stave Assembly and Test







Radius (mm) 23, 31, 39 Nr. Staves: 12, 16, 20

Nr. Chips/layer: 108, 144, 180

Length in z (mm): 271.2 mm

Nr. chips/ Stave: 9

Material thickness: ~0.3% X<sub>0</sub>

Coolant Single-phase H<sub>2</sub>O leak-less Pixel operational temperature < 30°C Pixel max temperature non-uniformity < 5°C Chip Power dissipation < 50mW/cm<sup>2</sup>

- Facility and technical resources are ready at CCNU for HIC assembly, and only replace assembly jigs
- Infrastructures need to be prepared for stave assembly (deploy a Coordinate Measurement Machine with identical tooling), and technical training is necessary
- HICs & Staves test setups

## INTT-MVTX Conflict

**INTT Acceptance** 

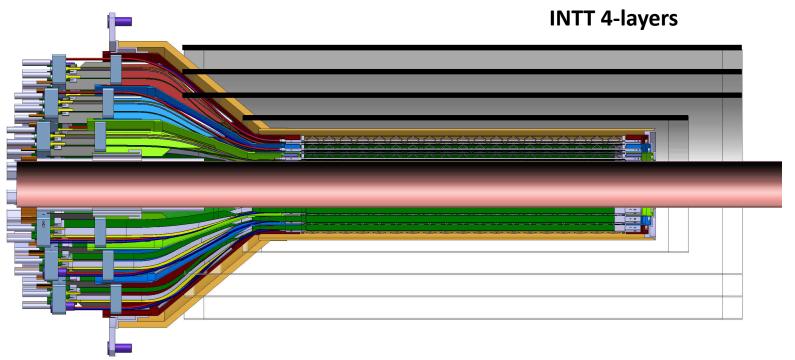
@ |z|=10

|η|<0.95

|η|<1.09

|η|<1.28

|η|<1.12

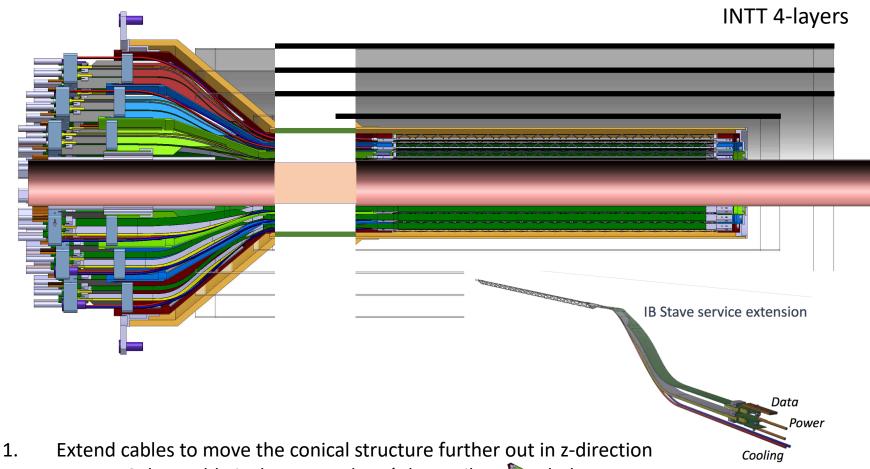


- Currently a clear conflict between the INTT and MVTX
  - INTT only includes ladder, no connectors, cooling barbs, etc

R&D items: 1) Extend cables to move the conical structure further out in z-direction; 2) Design/optimize INTT layers to fit current MVTX geometry;

- FPC data cable is the HDI and can't be easily extended, short "firefly" cables possible?
- Reduce angle of cone redesign C-structures and connectors

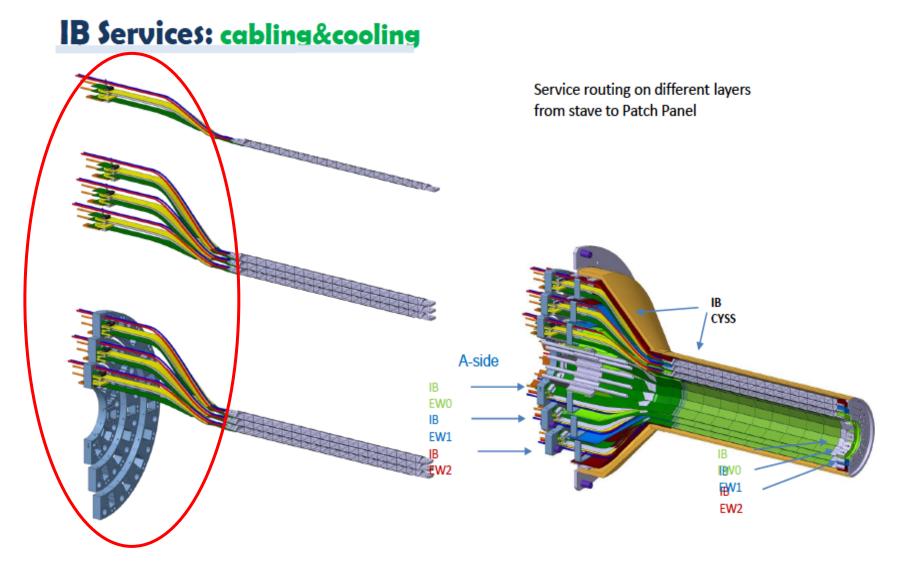
## INTT-MVTX Conflict



- FPC data cable is the HDI and can't be easily extended
- Possibly add short "firefly" cables to hook up to patch panel, R&D needed
- 2. Reduce angle of cone – redesign



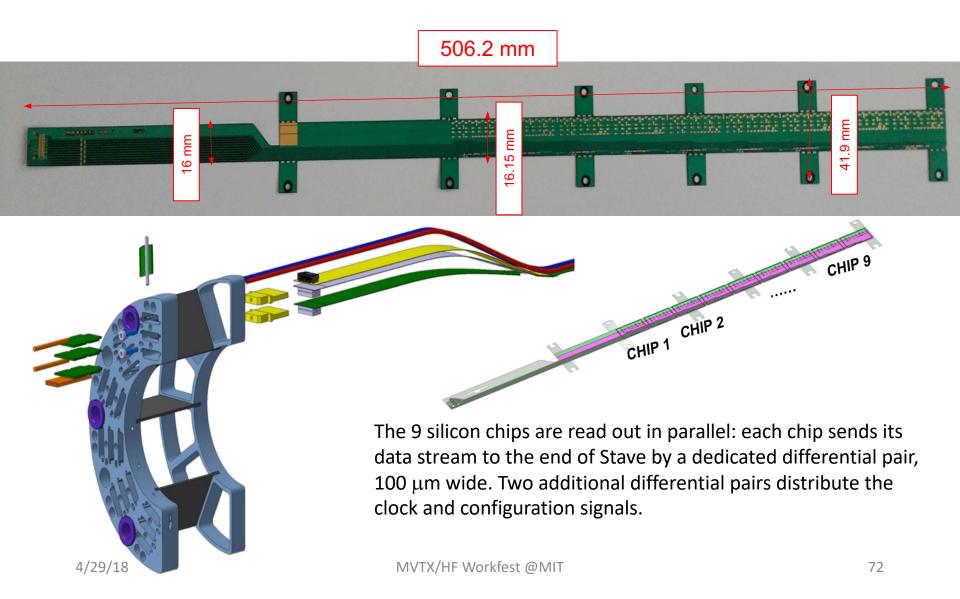
## Signal and Power Extension for FPC



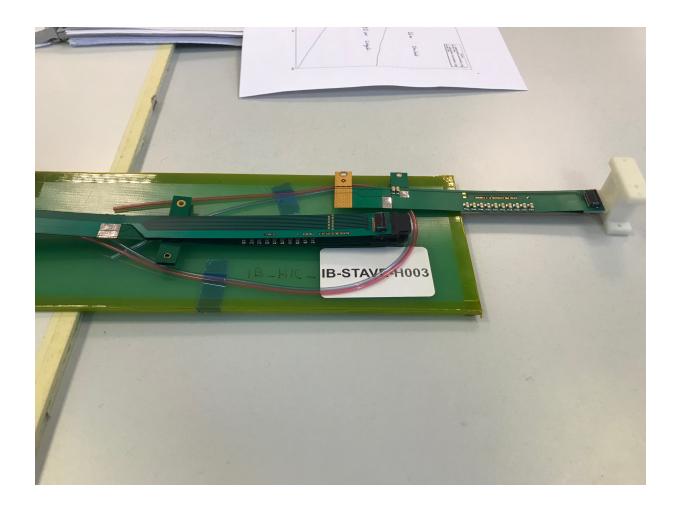


## MVTX/INTT Integration

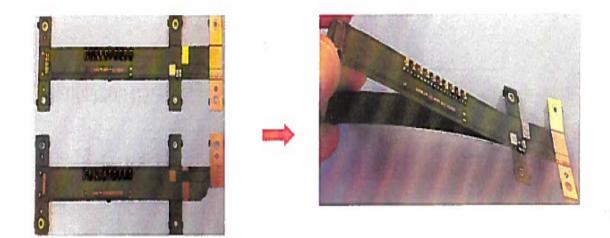
#### Extend MVTX Service Cables?

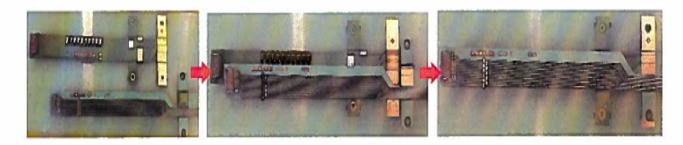


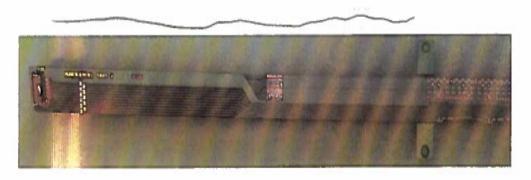
# MVTX FPC R&D @CERN and LANL

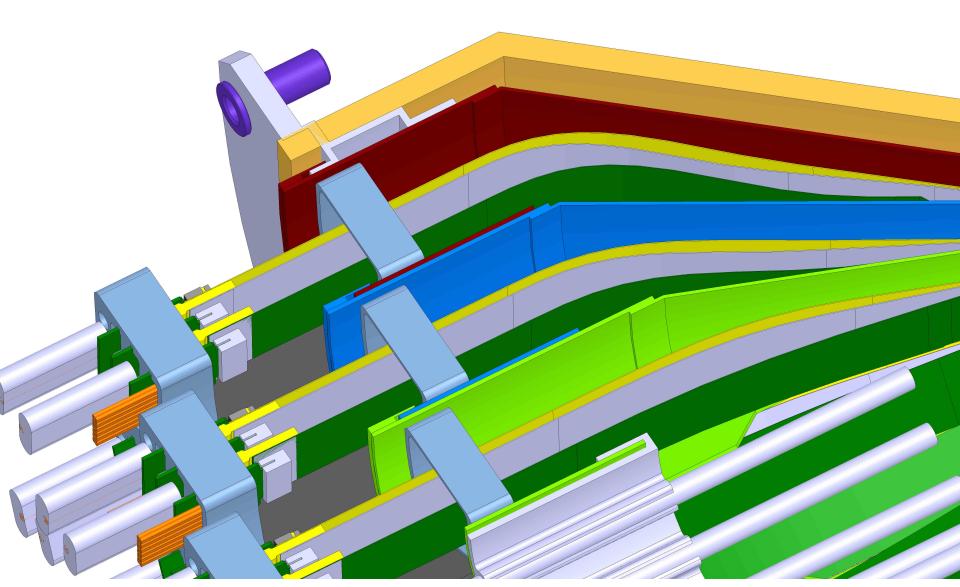




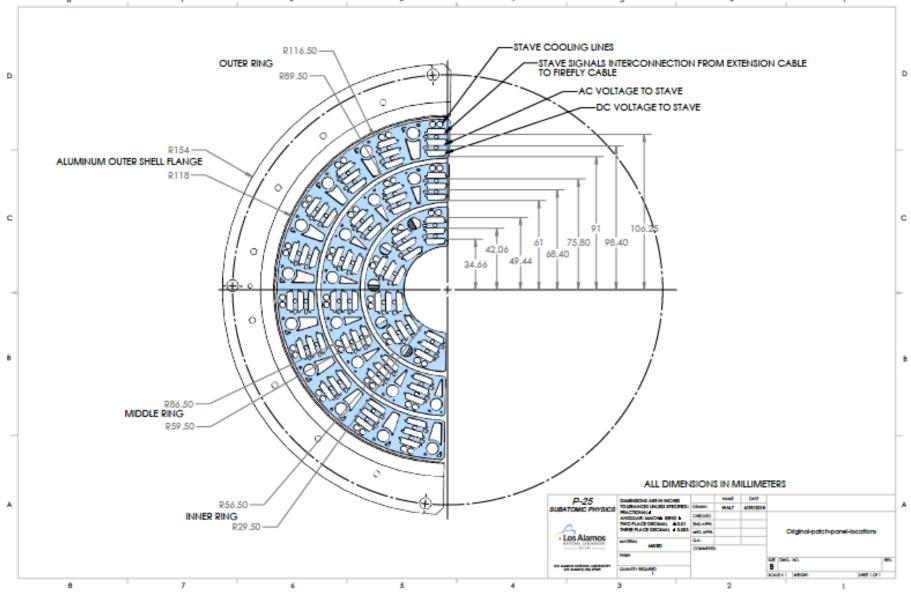


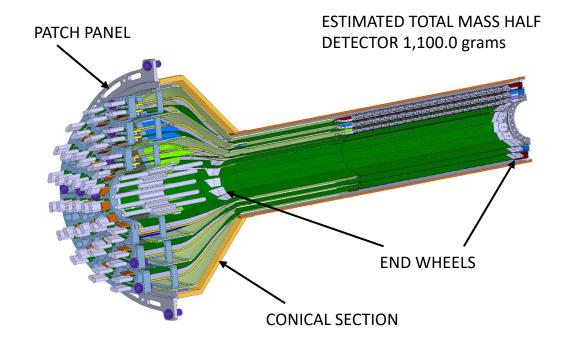






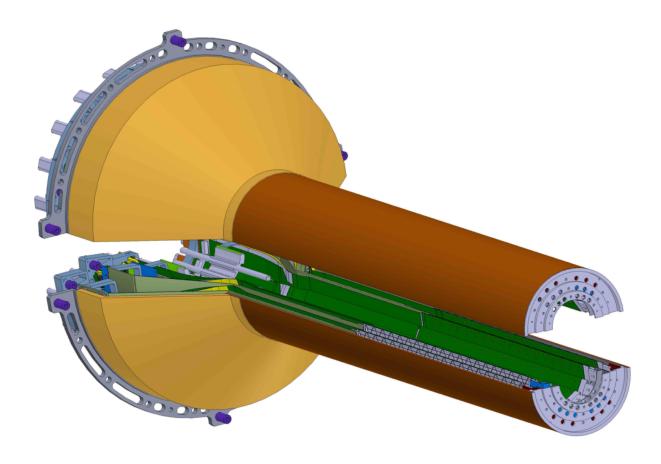
# End View of ALICE Patch Panel





#### MVTX half detector assembly

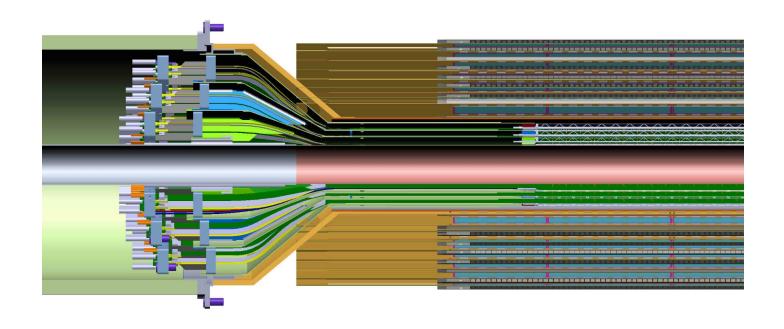
#### **MVTX** Detectors





# MVTX and INTT Integration

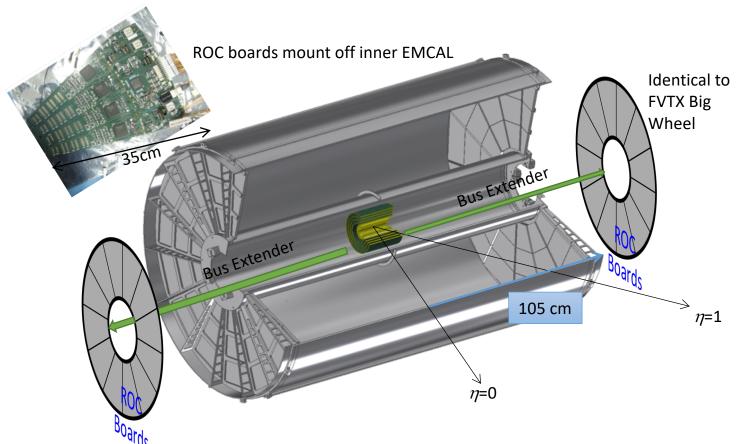
#### Work in Progress



It is clear from this detail view the conical region of the MVTX detector barrel with the INTT that the MVTX will need to translate in Z...



#### INTT Readouts from both North and South

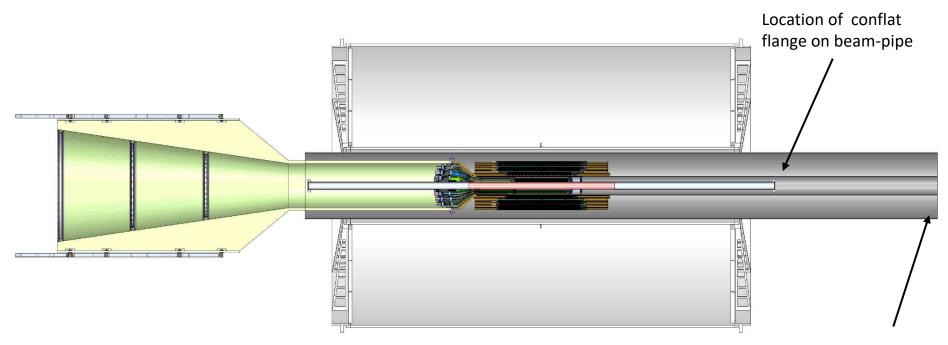


The bus extender needs to run to ROC boards (reuse FVTX ROC) outside TPC. Minimum length is 105cm – ladder length + distance to ROC board.



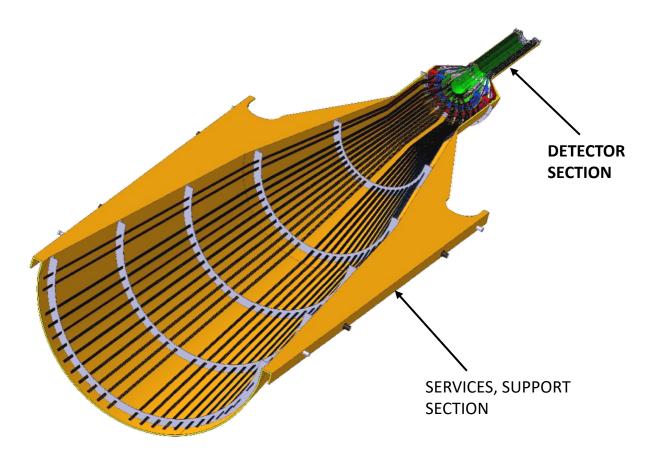
#### Mechanical Integration

Model of MVTX with INTT inside TPC with the addition of two concentric composite cylinders;



Location in Z where the inner-hcal ends (see control drawing) Z=2175.0 mm

#### Service Barrel: Design and Fabrication

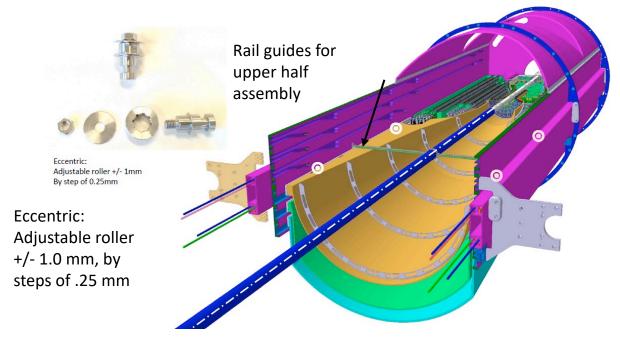


ALICE HALF-BARREL ASSY

# ALICE Inner Tracker Rail

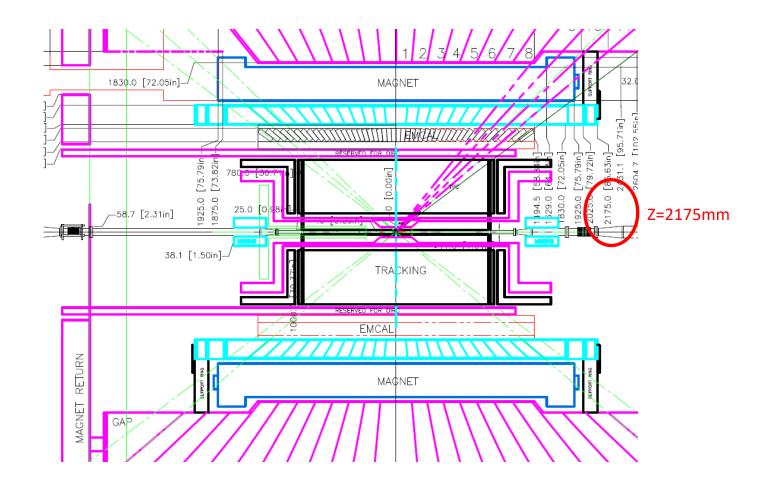
Support
The MVTX plus INTT half barrel assemblies loca

The MVTX plus INTT half barrel assemblies location position is provided by the engagement of 4 rollers on the half-barrel, which would be previously measured and aligned, into four precise inserts housed in the "cage-rail" assembly.

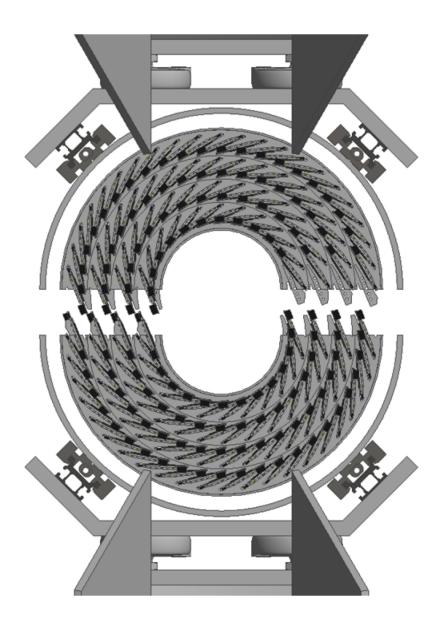


In sPHENIX we will not use a "service cone, rail system" anywhere near the size of that planned for the ALICE detector, but we will use their concept.

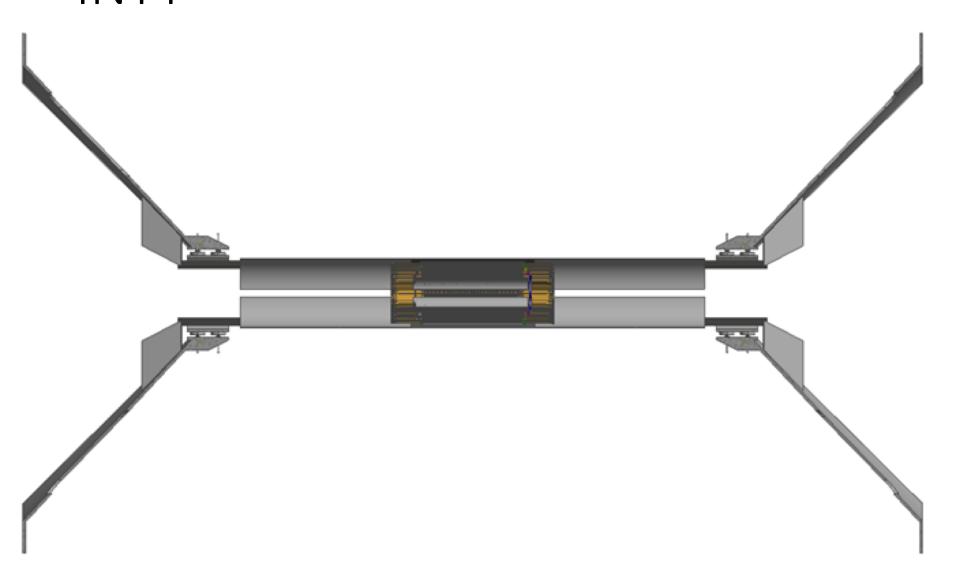
# BNL control envelope drawing; Z location of the inner hcal is at 2175,0mm



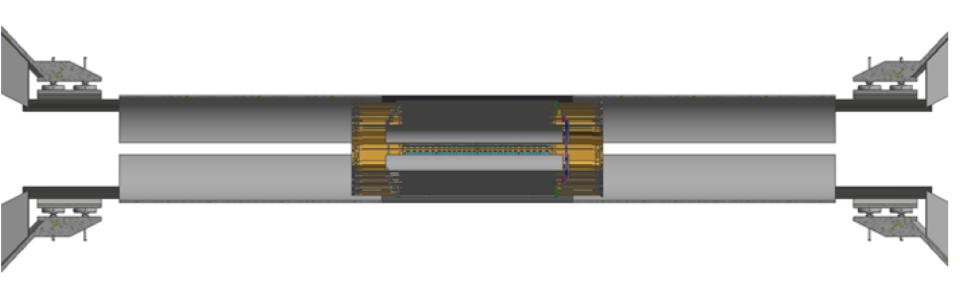
# INTT



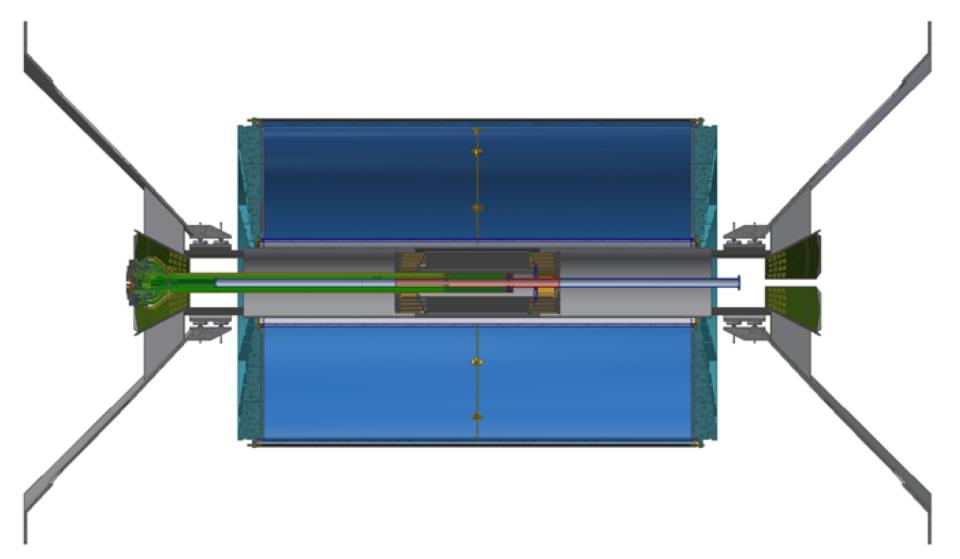
# INTT



# INTT

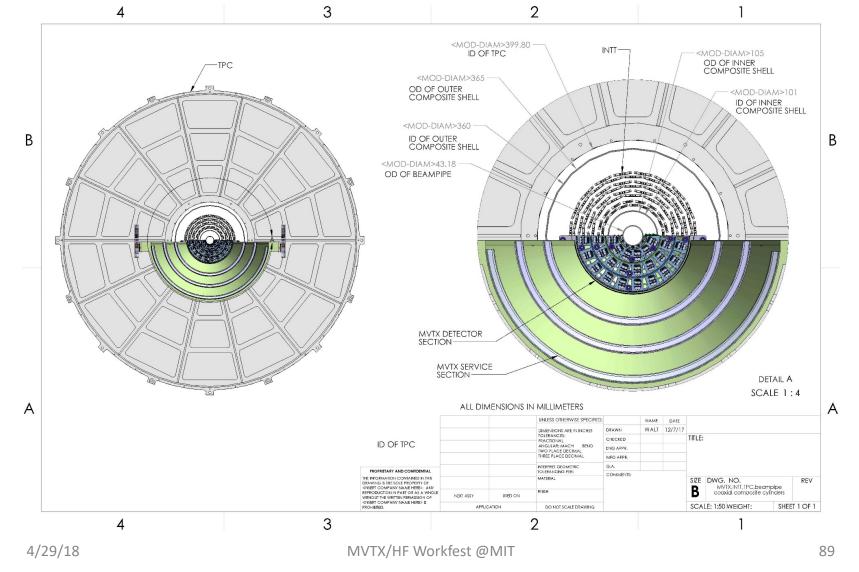


# MVTX + INTT + TPC

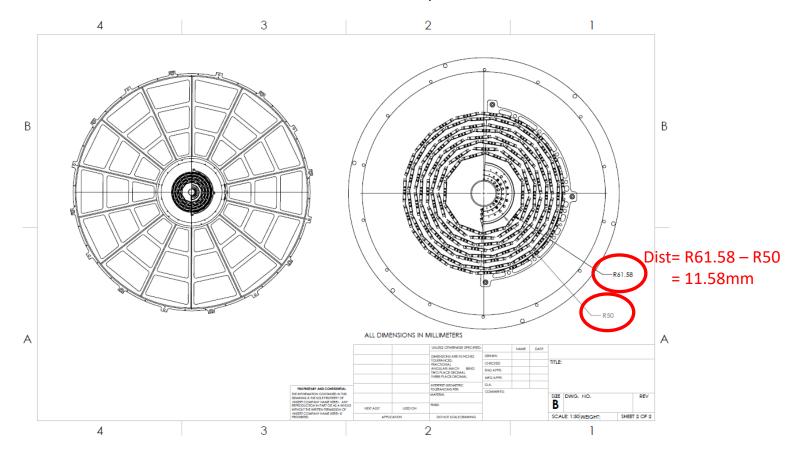


Cross-section view from CAD model of MVTX, INTT, TPC, beam-pipe, plus two composite conical shells:

MVTX radius are increased by 1.5mm to have a minimum 2mm gap between beam pipe and then inner MVTX structures

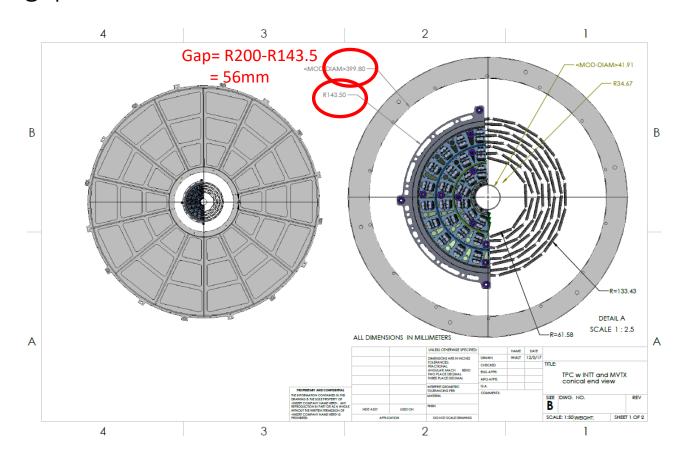


#### Gap between conical shell of MVTX and inner layer of INTT is 11.58 mm



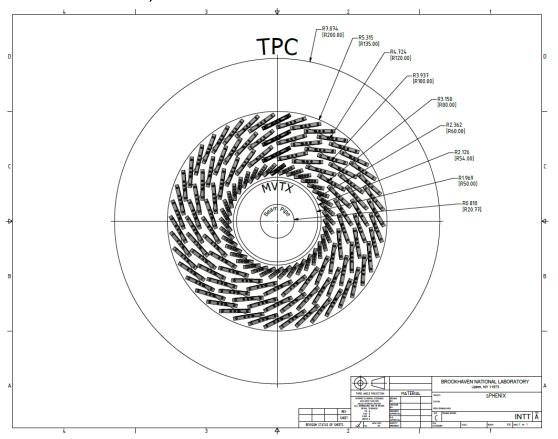


#### 56.0 mm gap between INTT and inner radius of TPC



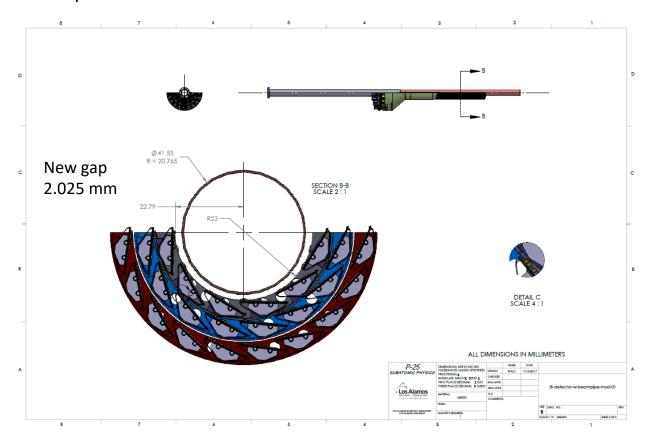


# Earlier model for the INTT, chevron configuration, inner layer half ladders in width;

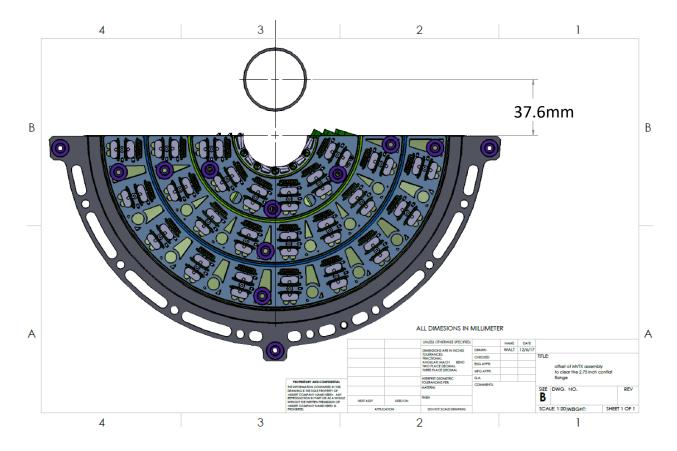


Number of ladders:
Layer 0 – 38 half ladders,
Layer 1 – 26
Layer 2 – 34
Layer 3 - 42

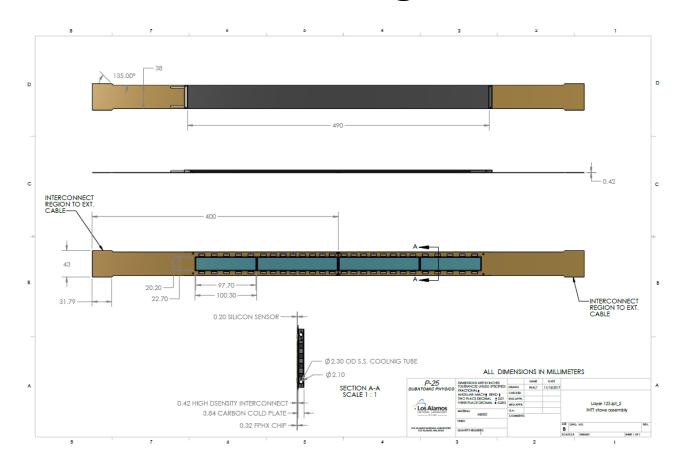
# Offset from OD of beampipe and innermost component of the MVTX



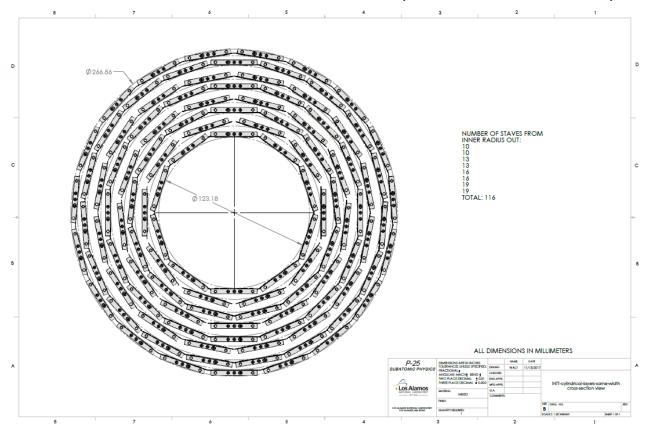
Offset needed to install split MVTX into run location around beampipe, passing over 2.75 in conflat flange



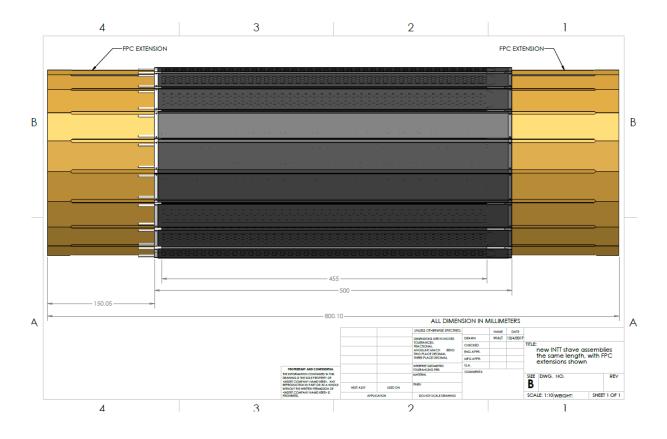
### INTT stave design with HDI



Latest configuration of ladders in the INTT, 4 layers where each is made from two layers for hermeticity



#### New INTT model with HDI extensions;



#### Cost & Schedule



#### Cost and Schedule in the Full Proposal

- Total budget: 6.5M
  - Production
  - Assembly
  - Integration
- About 9 months schedule float

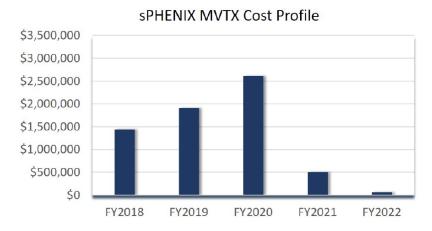


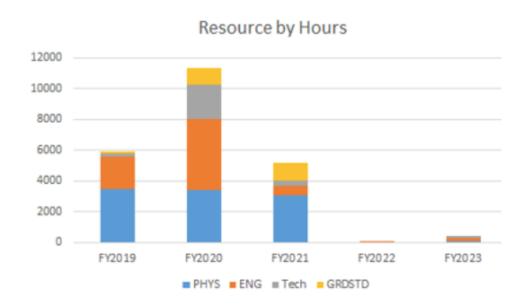
Figure 42: MVTX Funding Profile.

Major Items	Cost (\$M)	Schedule
Staves (WBS 1.5.3.1)	1.3	8/2018-5/2019
Readout & Controls (WBS 1.5.2)	1.3	1/2019-6/2019
Mechanics & Detector Assembly (WBS 1.5.3)	1.8	2019-2022, TBO
Integration (WBS 1.5.4)	1.0	2021-2022, TBO
Project Management	1.0	8/2018-1/2023



#### MVTX labor profile in the full proposal

	Escalation + Overhead + Contingency	
Labor	\$2.5M	
M&S	\$4M (\$3.75M if RU produced in FY18)	



Only engineers and Technical staff costed to the project



# Early funding motivation for MVTX FY18,FY19

- Buy 84 good staves from CERN following ALICE production, end FY18
  - Includes: sensors, space frame, FPC, assembly and tests
  - Very low technical risk
  - CERN will deliver 100% working staves
- Buy 58 Readout Units with the ALICE production in FY18 (was FY19)
  - FPGA chips and GBT chips as part of the ALICE production
    - GBT not commercially available product
  - ~50% cost saving w.r.t. to estimated budget (exact number confirmed 04/18)
- MVTX telescope Fermilab test beam confirmed the readout chain and sensor performance in early March 2018
  - Sensors(ALPIDE) + RU(frontend) + FELIX(backend) + sPHENIX RCDAQ
- To attract external funding & support for MVTX
  - Foreign consortium, individual institution



#### M&S cost options & risks

Green: low risk / MVTX baseline budget

Red: High technical risk, low cost saving or increased cost

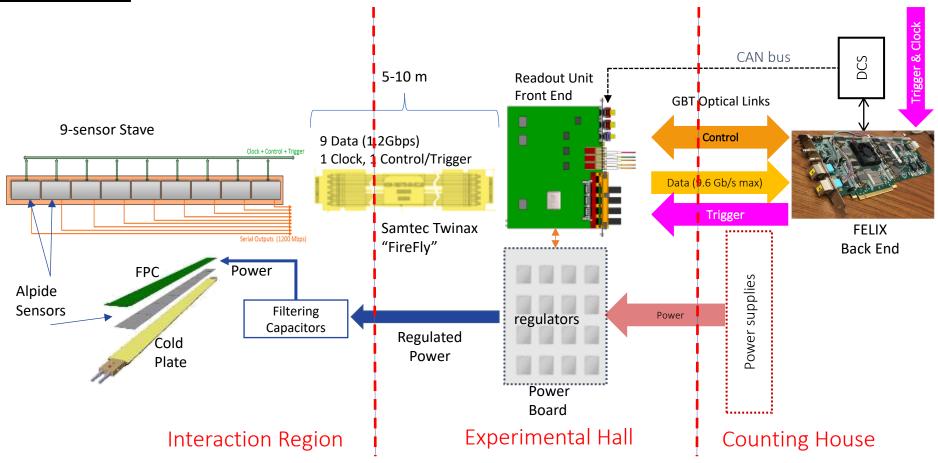
#### Staves:

- Oprion1: MVTX production following ALICE production at CERN, ~Aug 2018
  - · All material included and 100% working staves delivered
- Option2: Stave assembly at CCNU (China)
  - MVTX project would still need to buy sensors, Flexible Printed Circuit (FPC) and space frames
  - Wuhan could assembly sensor and FPC; assembly with space frame may be done elsewhere
  - No experience assembly inner barrel → training required and hardware modified
  - Potential saving on some labor assembly work
  - Yield unknown -> schedule and cost uncertainty
- Readout Units (radiation hard electronics):
  - Option1: Produce with ALICE batch (FPGA & GBT chips) in FY18
    - 50% cost reduction w.r.t. budgeted cost
  - Option2: MVTX produces its own batches → cost increase/double and schedule impact
- Carbon structures:
  - Exploring cost-saving options, build carbon structures elsewhere (France, Italy, Korea, China?) instead of LBNL etc.
- Reuse hardware from LDRD
  - Electronics, Power System etc.

#### **Electronics and Controls**



#### **MVTX** Electronics Overview

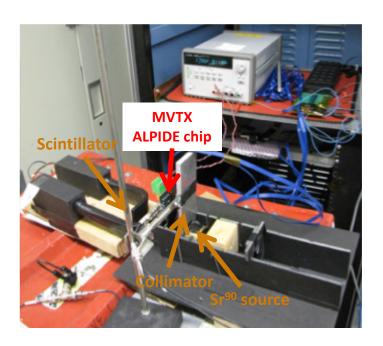


MVTX Detector Electronics consists of three parts

Sensor-Stave (9 ALPIDE chips) | Front End-Readout Unit | Back End-FELIX

#### Sensor and Electronics R&D @LANL

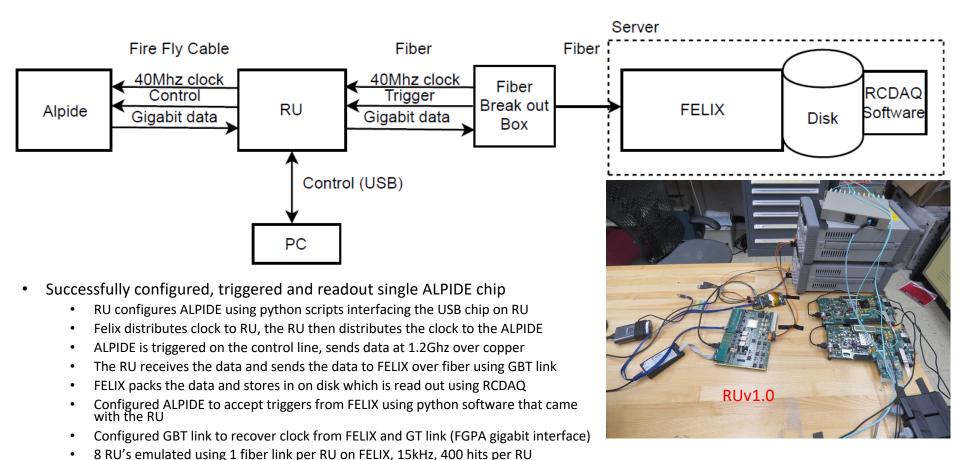
- ALPIDE evaluation and optimization
  - MOSAIC + Single Chip/Stave
  - Cosmic and source
  - Laser system
- Power unit tested
  - PU + MOSAIC
  - PU + RU
- Full readout chain demonstrated
  - ALPIDE + RUv1.0 + FELIX v1.5 + RCDAQ
  - Full stave + RUv1.x + FELIX v2.0 + RCDAQ
- Mechanical system integration
  - Conceptual design developed
  - MVTX+INTT integration



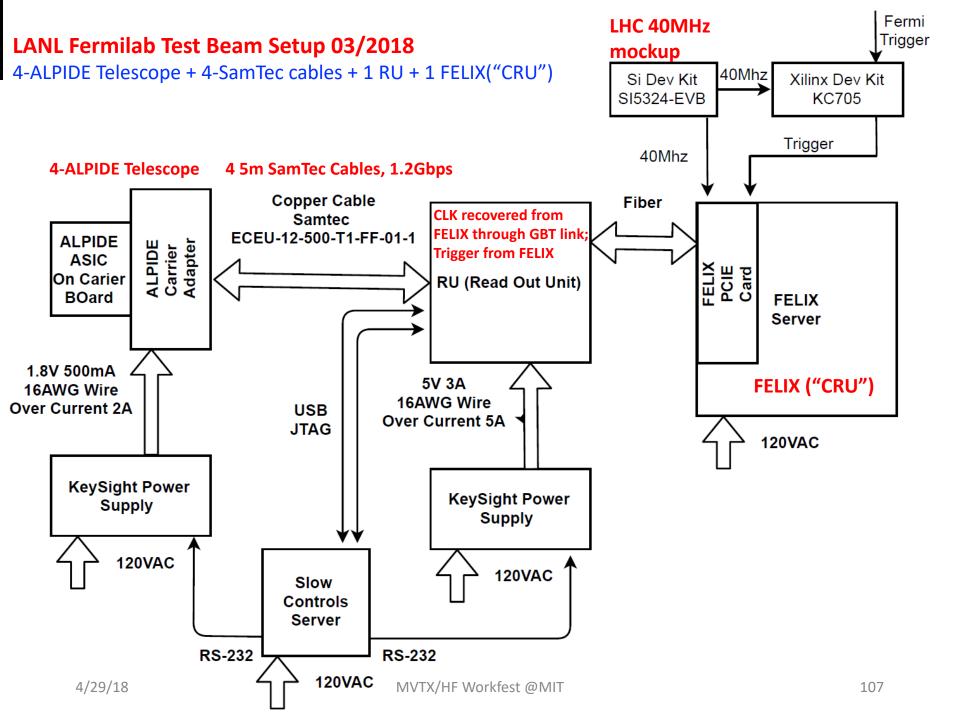


#### First Full Chain Readout: Success!

LANL + Martin, JohnH et al



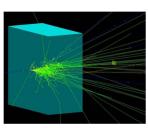
Currently working the implementation of the above using a Stave





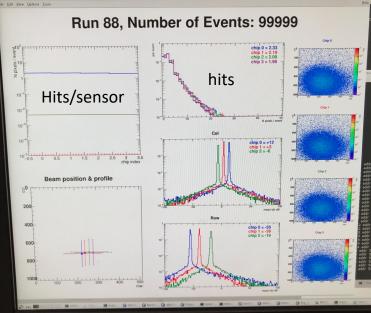
### Achieved all goals and more!

- Tested a new readout scheme
  - 4 sensors (~3 "staves"+1 Chip) per RU
    - ALICE: 1 stave per RU for IB
- Sensor performance evaluation
  - Cluster size
  - Threshold, signal shaping, trigger delay
- System stress test
  - High multiplicity events created via lead bricks "shower"
  - With 5, 10, 20cm lead bricks
- Analysis software developed
  - Online monitor
    - hit distribution, relative alignment etc.
  - Offline reconstruction, alignment etc.
    - Preliminary alignment, ~O(100um)





4 sensors Connected to one RU



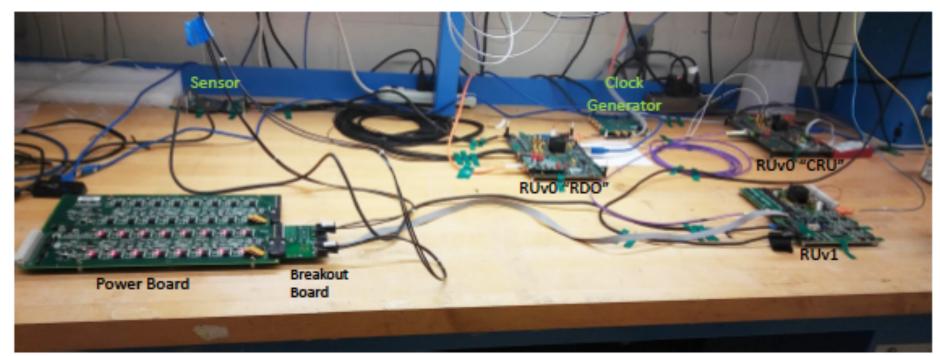
# Parallel Effort at UT-Austin – Shared R&D

#### Test Setup at UT Austin



- RUv1 with transition bd + power mezz
- RUv0 as CRU emulator
- Single sensor on chip carrier board with interface board (only usable for IB tests, wrong pins for OB)

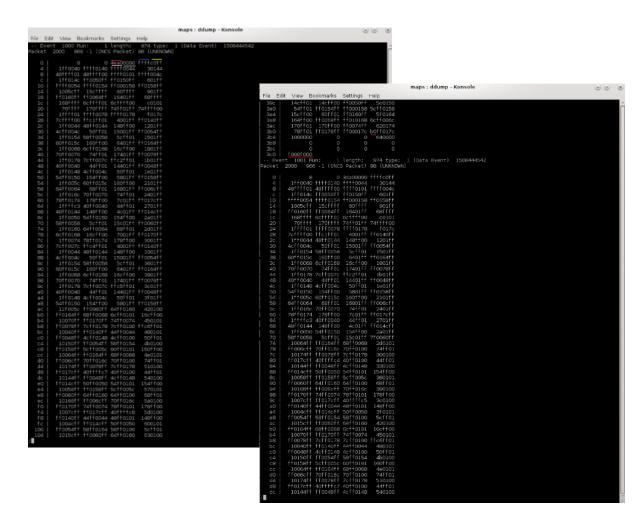
- Long (5m) FireFly cables
- Power board with single breakout board
- Now also tested with 9-sensor Inner Barrel module





#### RC DAQ event Data Screen Shot

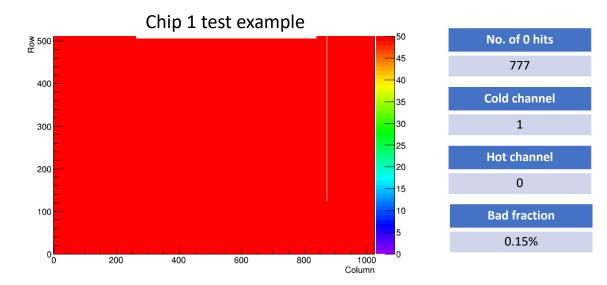
- Rcdaq receiving events from FELIX using ddump utility
- ffff0044ffffc0ff4ea0
- a0 Chip Header
- 4e bunch counter
- ff IDLE
- c0 Region Header
- 40 00 first Hit
- Second screen shot showing end of one event (b0..., f000f000) and the beginning of another





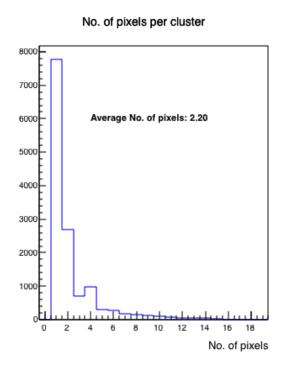
#### LANL R&D: Single ALPIDE Chip Scan – Active Channel Fraction

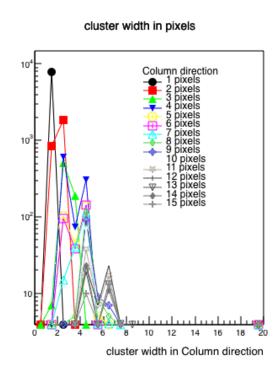
- Scanned the available chips and stave at the LANL lab through digital scan to verify the dead channel fraction: the bad channel fraction is <1%.</li>
- Similar results with different readout speeds.

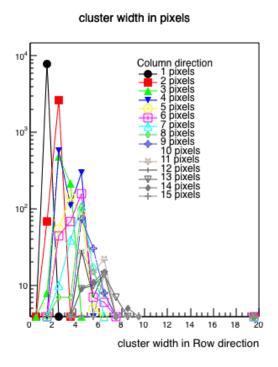




#### Hit Pixel Cluster Distribution from Source Test (Sr<sup>90</sup>)









#### Data Rate Calculations

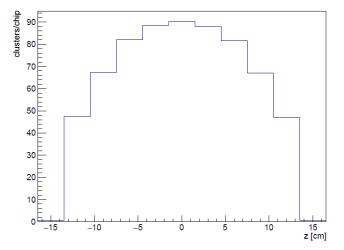
	Collision Rate
Au Au	200kHz
PP	10Mhz

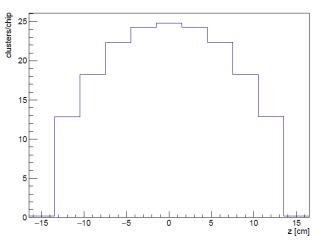
Assume 10us window and cluster size 3

	Au Au	PP
# of collisions	<b>2</b> = 10us * 200kHz	<b>100</b> = 10us * 10Mhz
# of hits, hottest chip	<b>270</b> = 3 * 90	<b>75</b> = 3 * 25
# of hits in a stave	<b>1983</b> = 3 * 661	<b>543</b> = 3 * 181









# Expected Data Rate (from the proposal)

1, 1349 hit pixels/ er 2 1003 hit nivelskte

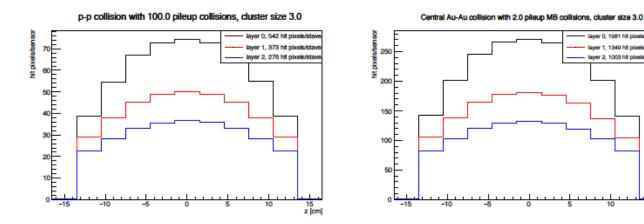


Figure 9: Average hit occupancy per event. Conservative assumptions are made regarding integration time (10  $\mu$ s) and cluster size (3 pixels/cluster). In addition, the pileup collisions are assumed to occur inside the MVTX acceptance ( $|Z_{Venex}| < 10$  cm) when in fact they will be widely distributed along the beam axis.

The highest occupancies are expected in layer 0, at  $\eta = 0$ , with central Au+Au collisions. Figure 9 shows that MVTX sensors average 271 hit pixels/event, for an occupancy of 0.052%. Lab tests (further described in Section A) have demonstrated successful MVTX readout at larger hit occupancies.

Noise < 10^-5		10 <sup>-4</sup> noise	Hit occupancy only		Hit + noise occupancy	
@Fermilab test bean		occupancy	p+p [MB/s]	Au+Au [MB/s]	p+p [MB/s]	Au+Au [MB/s]
	L0 FEM	26	29	107	55	133
~30 Gb/s max.	DAM	219	173	630	392	848
	MVTX	1305	1041	3781	2346	5089

Table 2: Raw (uncompressed) data rates based on a worst-case noise occupancy of 10<sup>-4</sup>, the hit occupancies of Fig. 9 at 15 kHz trigger rates, and the sum of the hit and noise.

# Project Organization

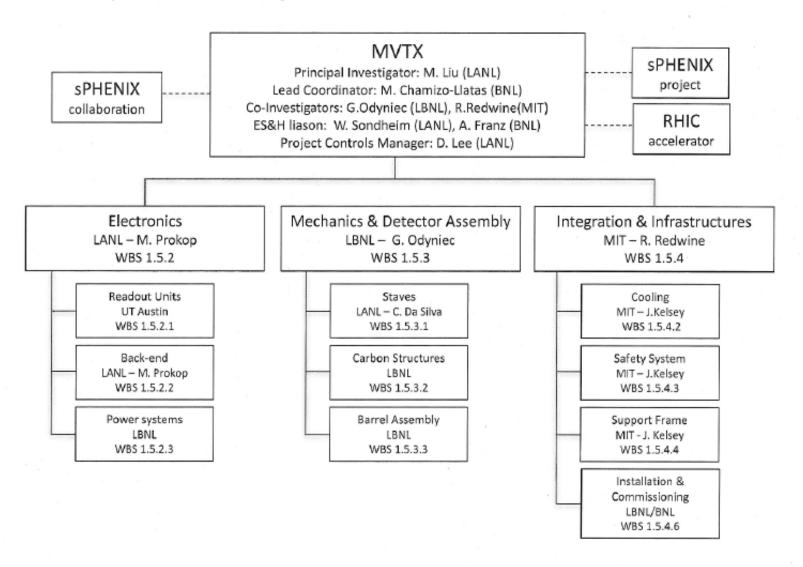


Figure 40: Organization chart of the MVTX project.