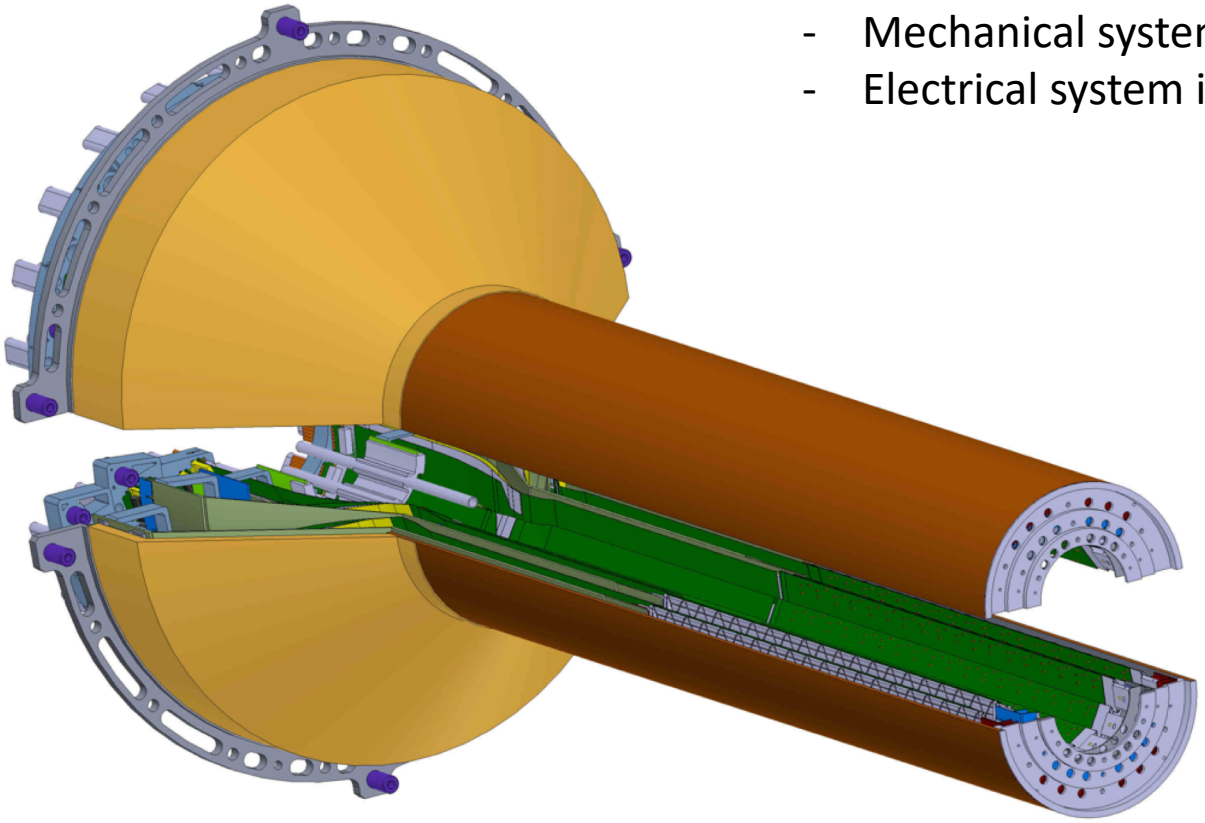
MVTX R&D

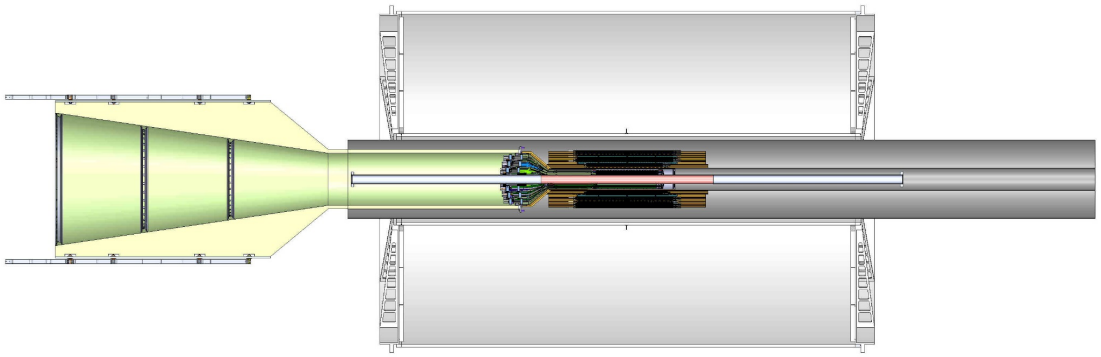
Ming Liu
Los Alamos
Many inputs from Walt, Alex, Sho, Hubert,
Cesar, Xuan, Rachid, Itaru and the MVTX group

MVTX Detectors



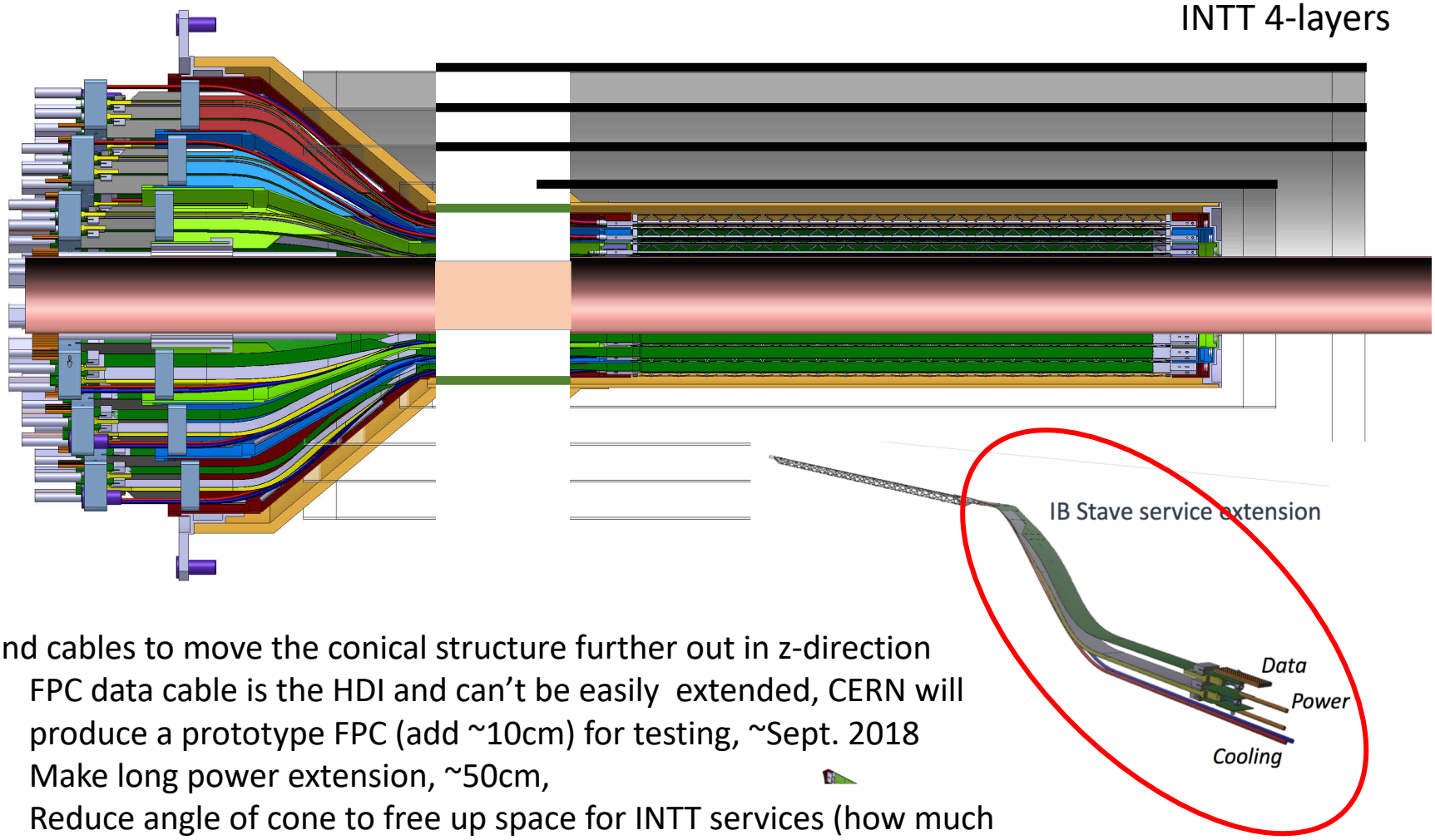
- Mechanical system integration
- Electrical system integration

To Do List – Mechanical Integration



- FPC extension
  - Signal path, +10cm
  - Power extension, ~50cm
- SamTec cable length vs signal quality
  - 5~7m
  - RU location, MVTX electrical system integration
  -
- Carbon structure and connector design
  - FPC HS signal connectors
  - FPC power extension connectors
  - MVT Service barrel and mechanical system integration
  - Installation procedure

INTT-MVTX Conflict



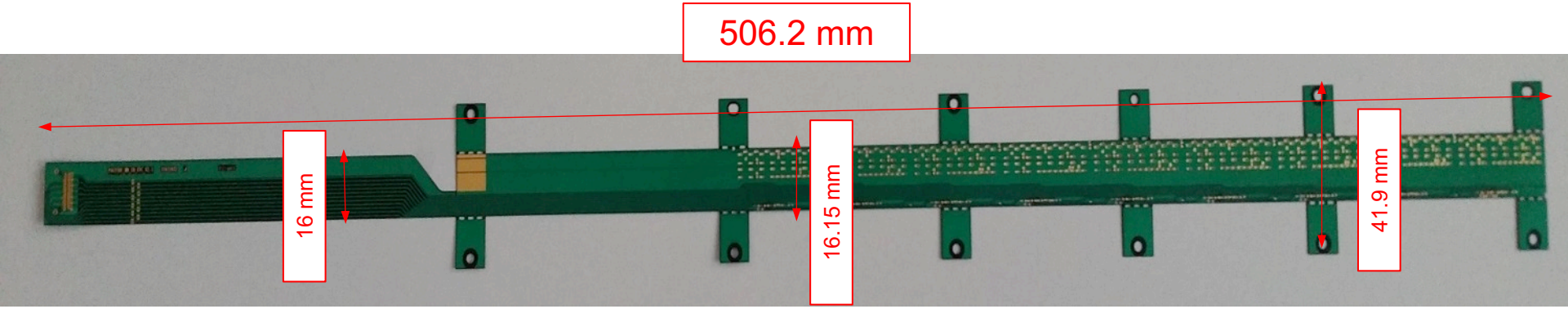
Extend cables to move the conical structure further out in z-direction

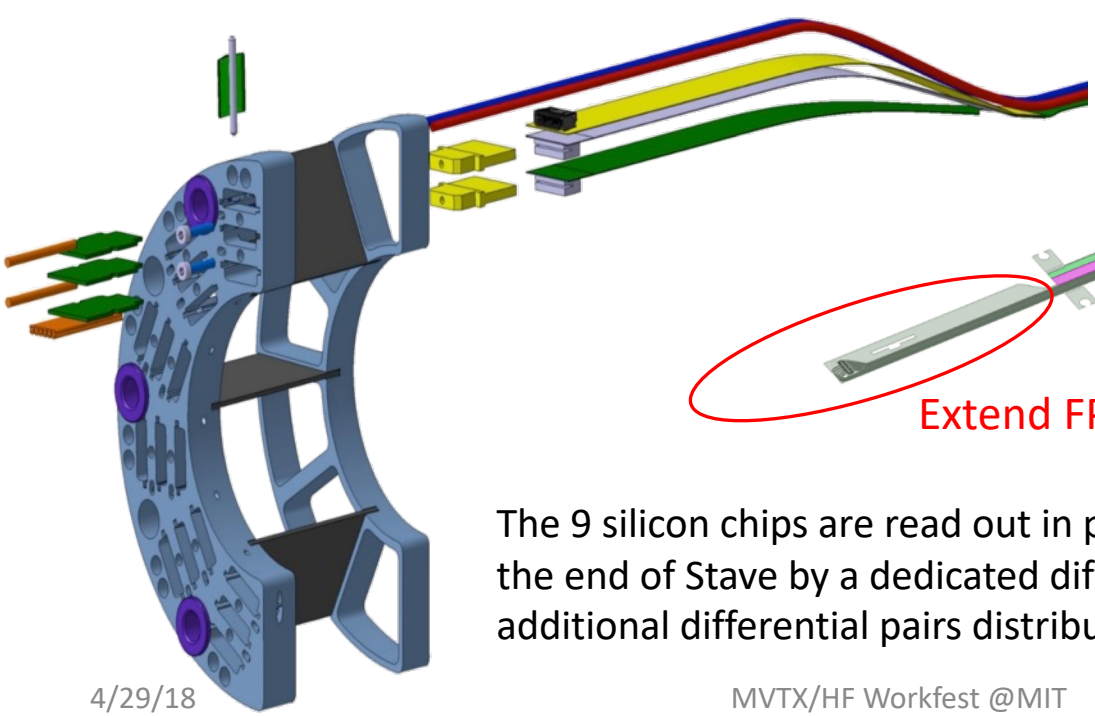
- FPC data cable is the HDI and can't be easily extended, CERN will produce a prototype FPC (add ~10cm) for testing, ~Sept. 2018
- Make long power extension, ~50cm,
- Reduce angle of cone to free up space for INTT services (how much is needed?)
- Redesign patch panel/cable connection shape and location

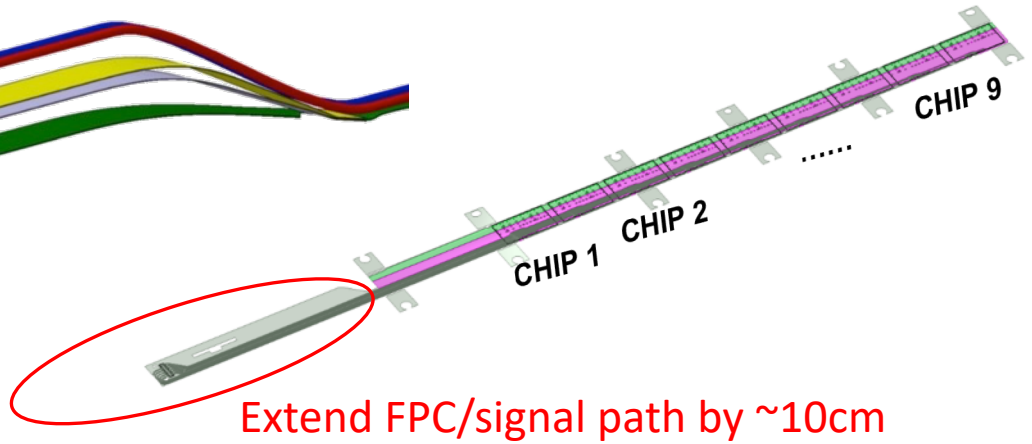
MVTX Flexible Printed Circuit (FPC)

Extend MVTX Service Cables?

Maximum +10cm for HS signal, TBD through R&D



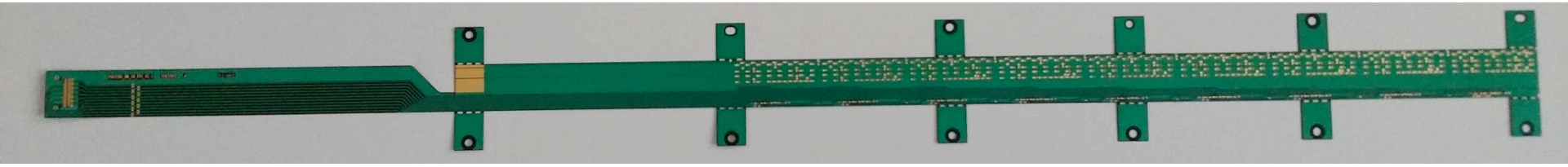


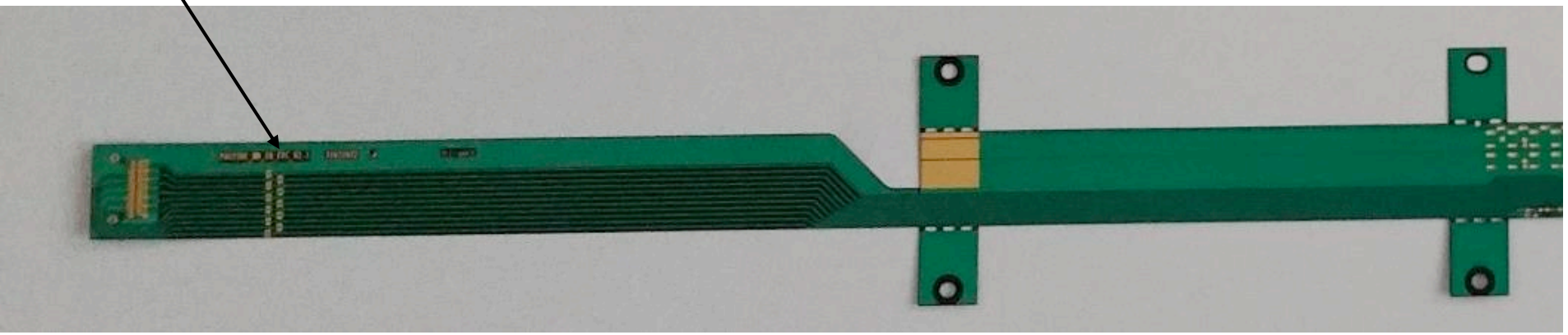


Extend FPC/signal path by ~10cm

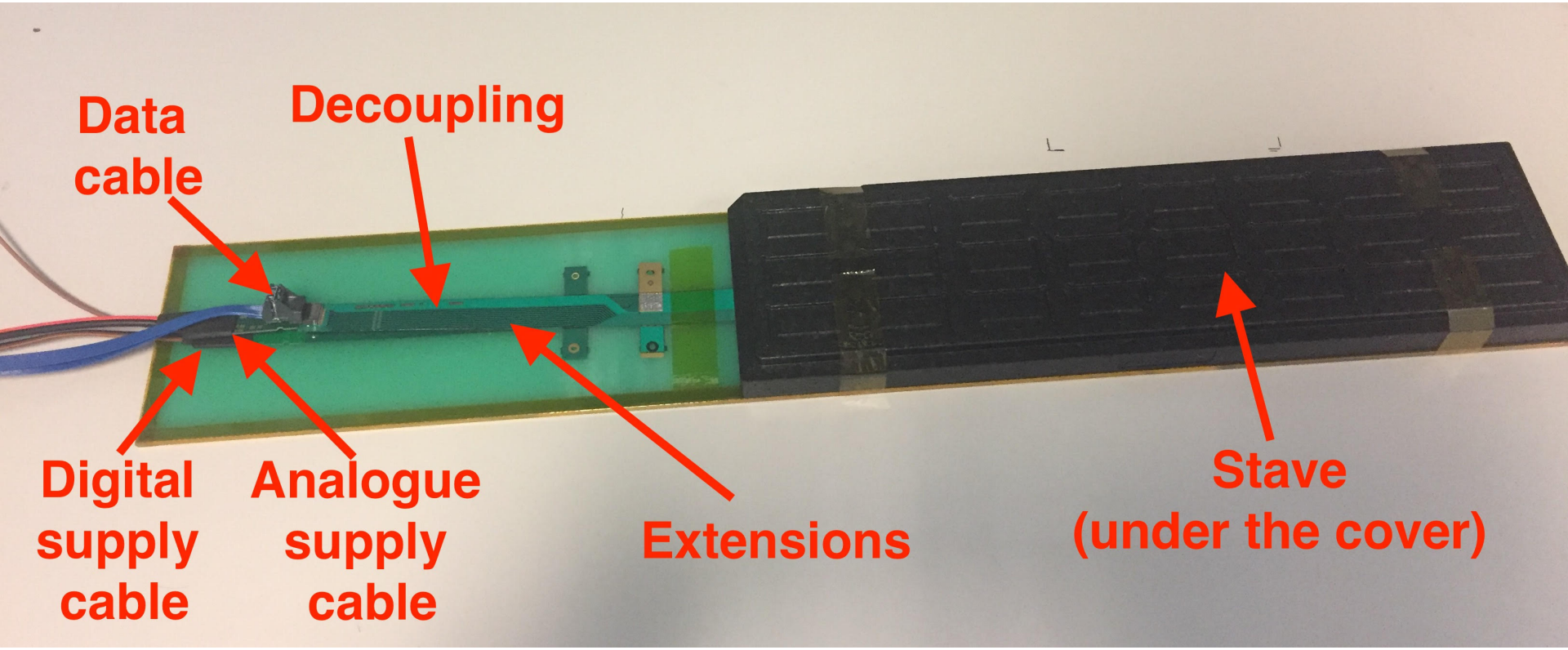
The 9 silicon chips are read out in parallel: each chip sends its data stream to the end of Stave by a dedicated differential pair, 100 μm wide. Two additional differential pairs distribute the clock and configuration signals.

ITS/IB FPC, 50cm long;
CERN can make FPC up to 60cm long, but needs to be confirmed

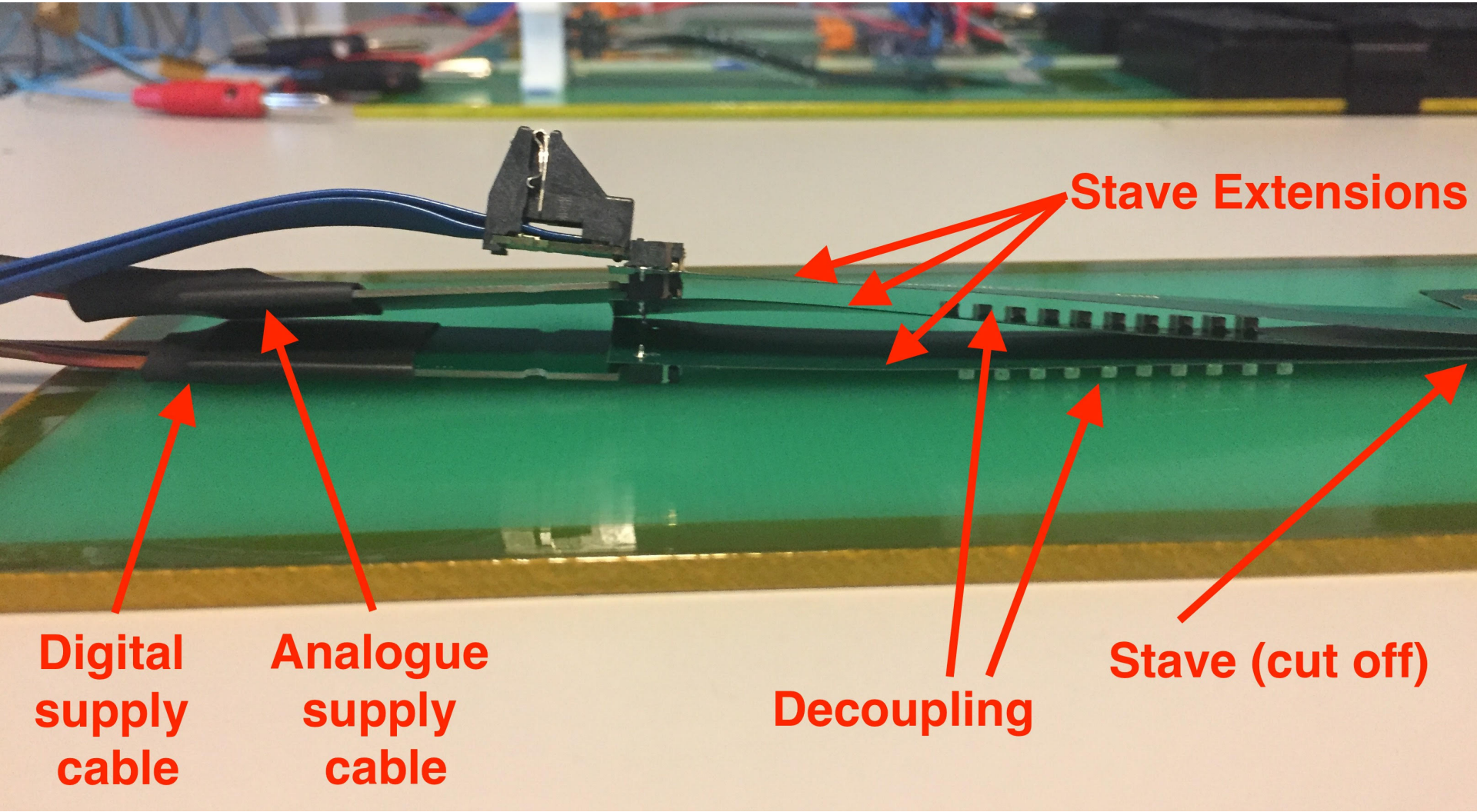




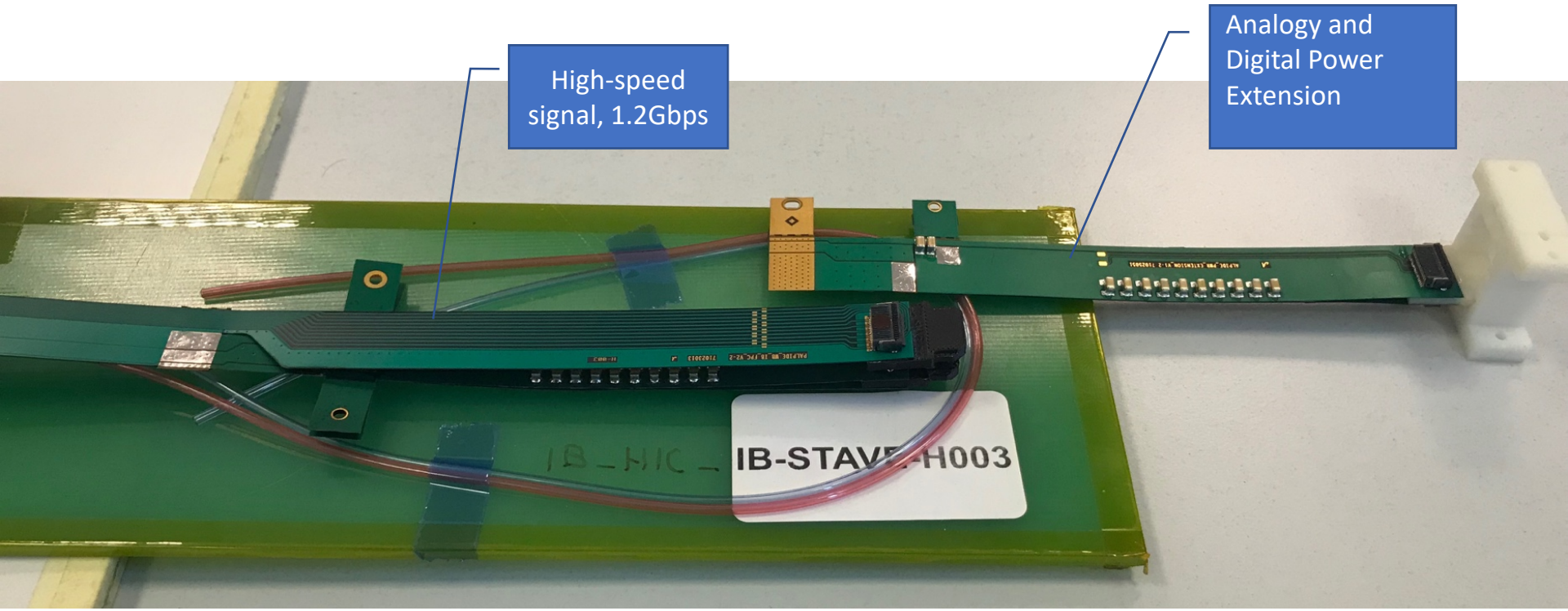
ALICE ITS/IB HIC: Signal, AVDD and DVDD



ALICE ITS/IB HIC: Signal, AVDD and DVDD



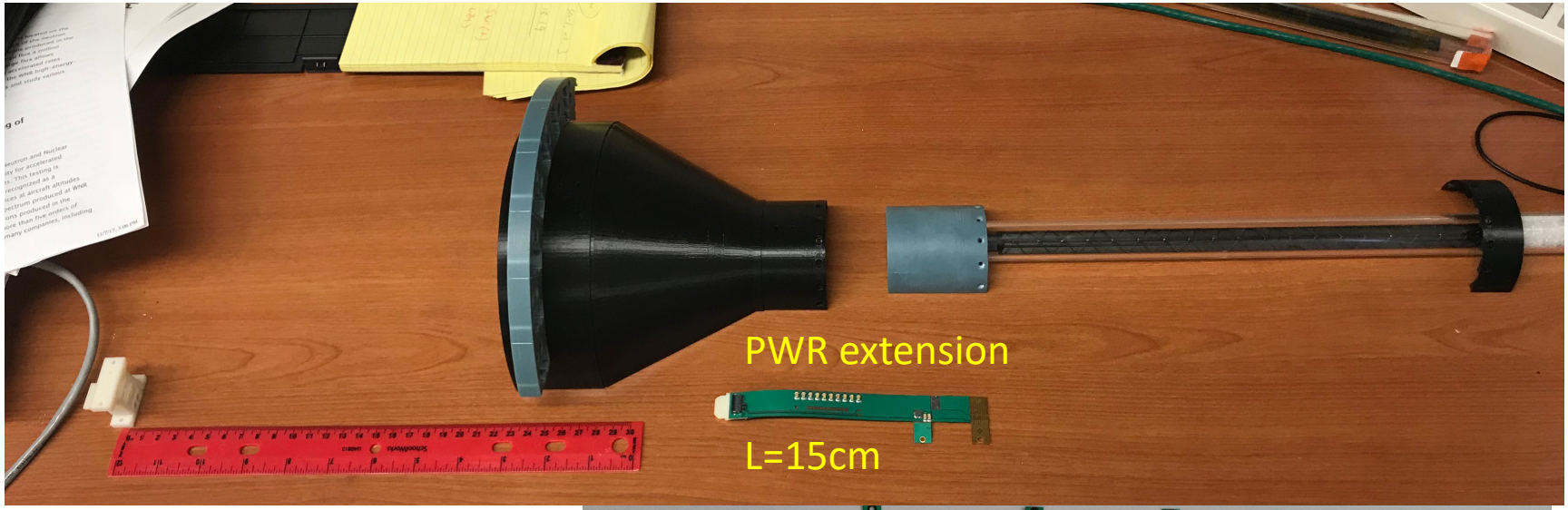
FPC R&D @CERN and LANL

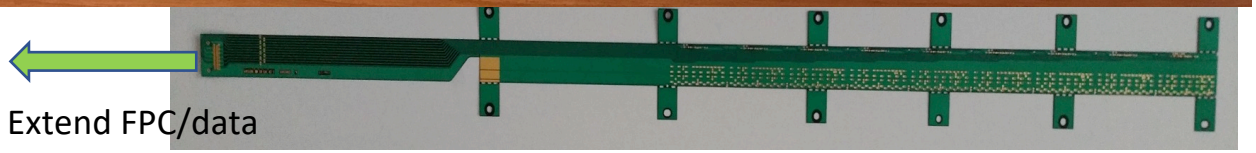


1) Try to extend high-speed portion of FPC by 10cm @CERN, ~September 18

2) Try to extend AV and DV by ~50cm at LANL, ~summer 18

MVTX Mockup & FPC Extension R&D

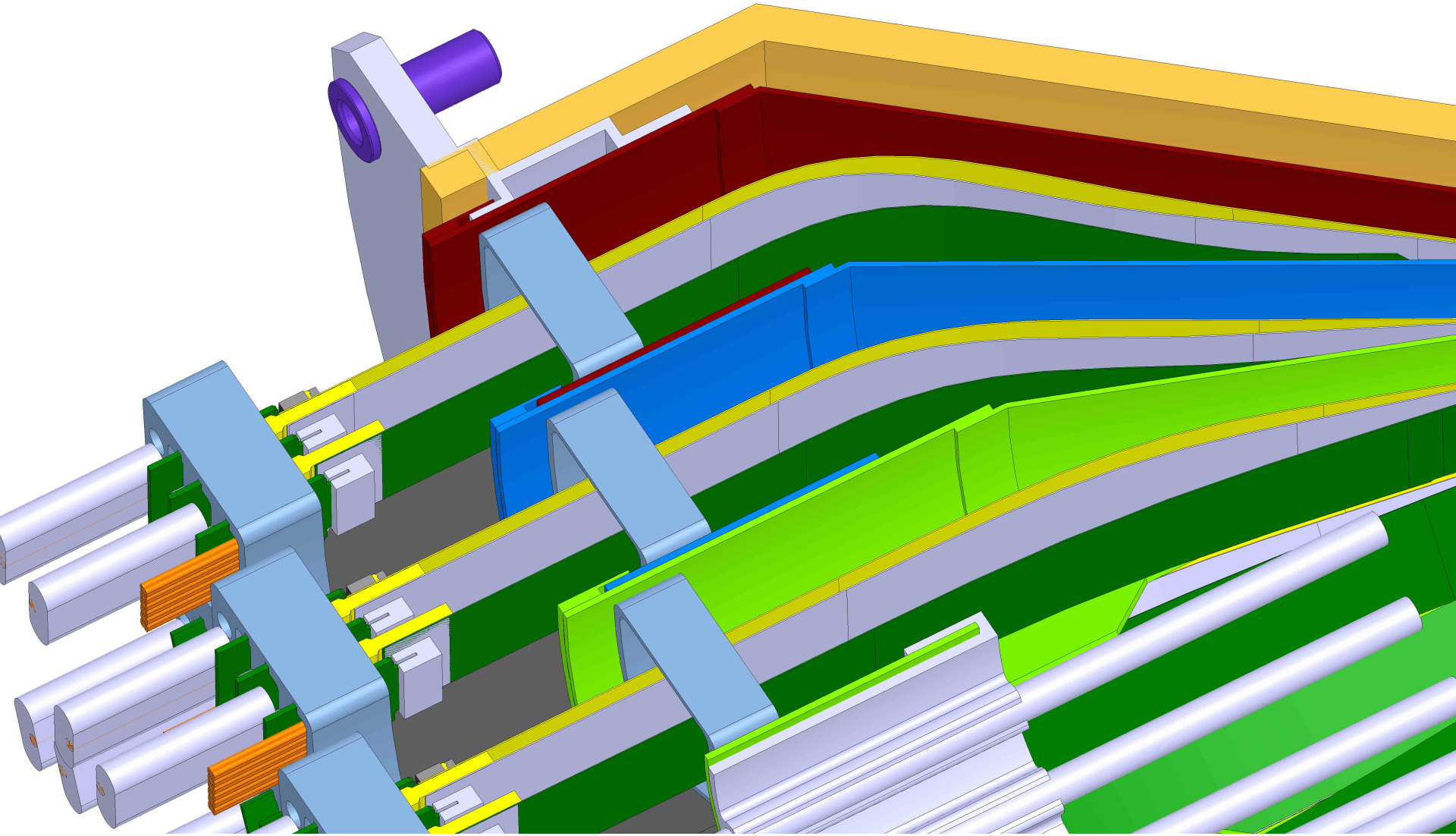




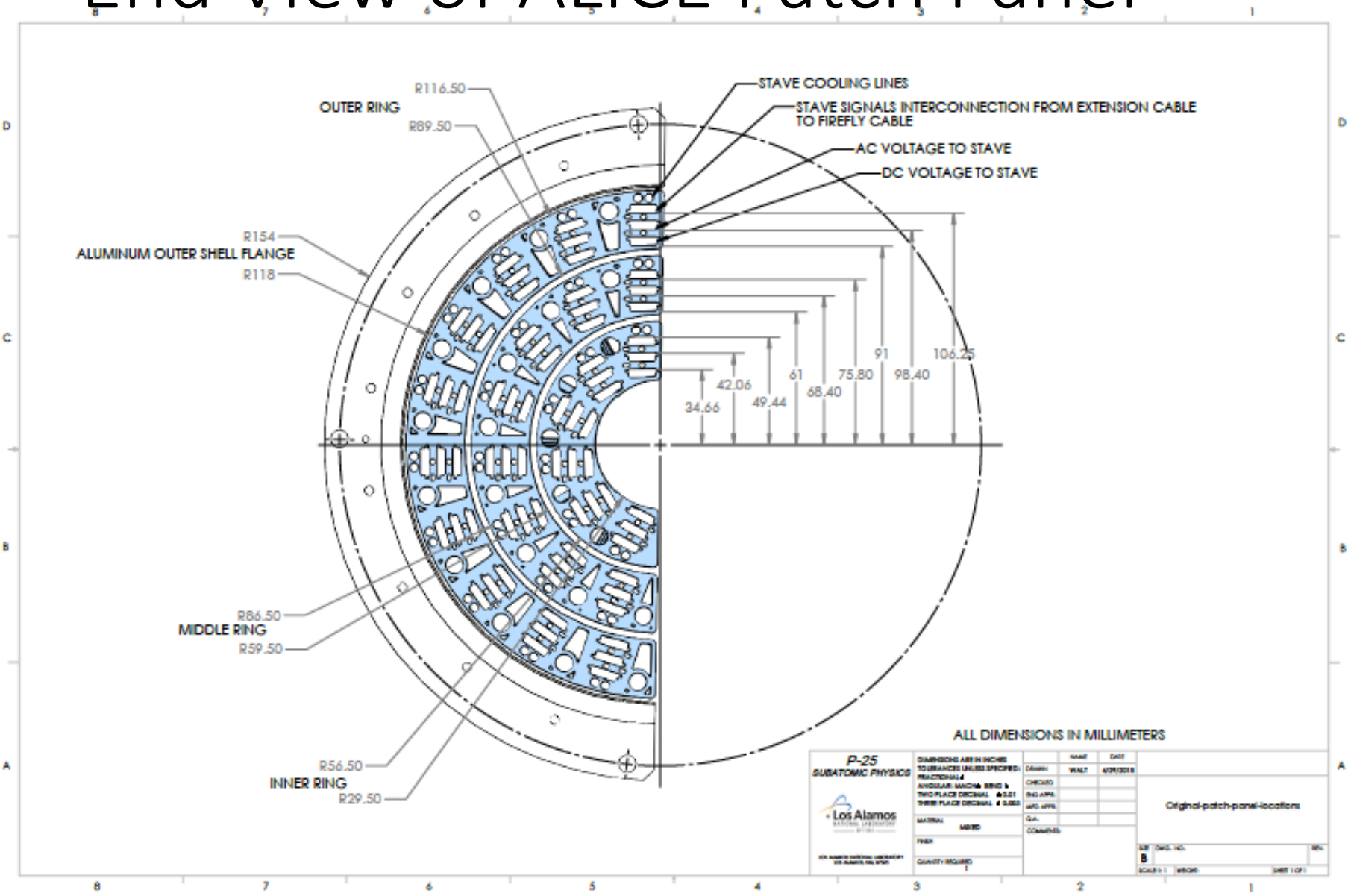
Extend FPC/data
cable by ~10cm?, R&D

Extended power cables AVDD/DVDD:
L = ~50cm, and possibly with 2~3 different lengths, like 30cm and 40cm
Separate PWR and signal connections at different Z-locations.

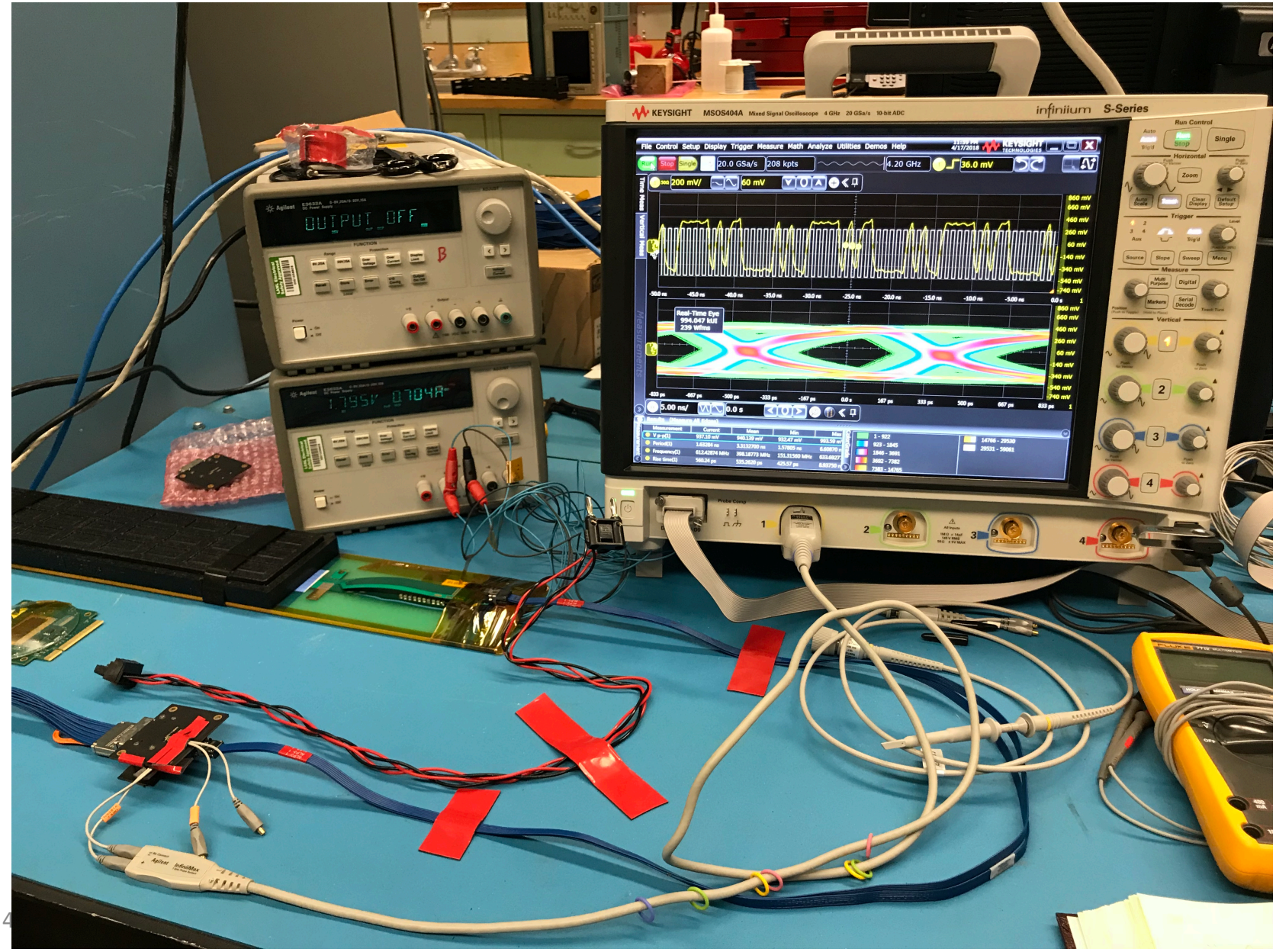
Requires New Design



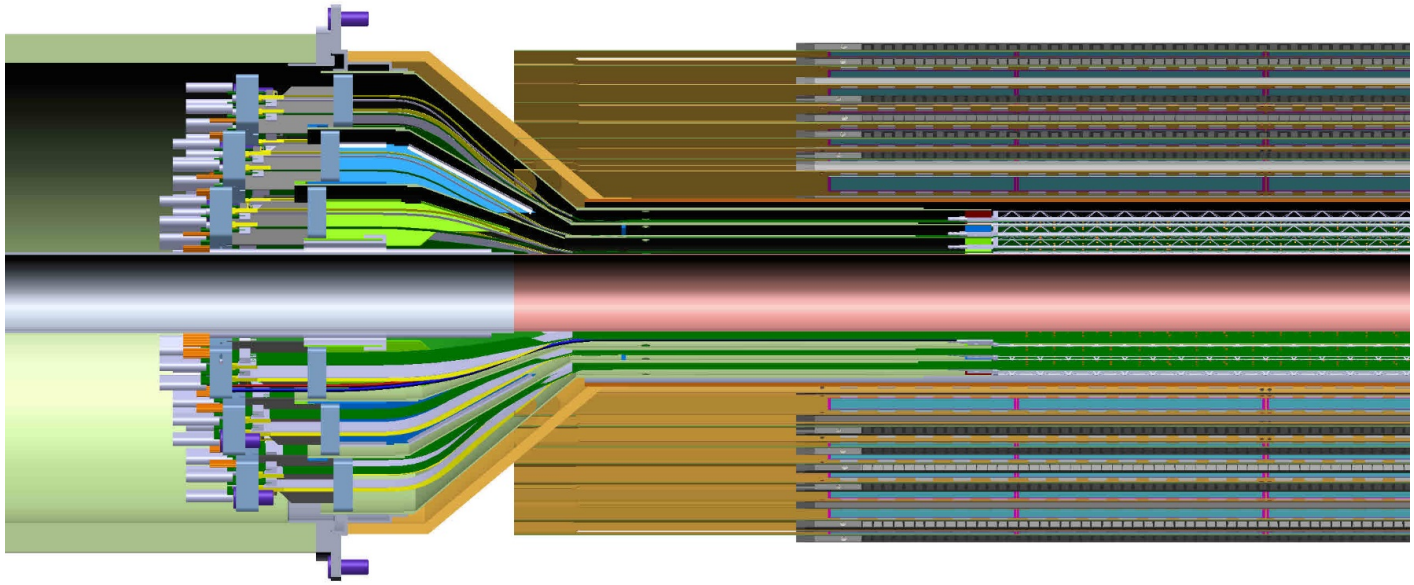
End View of ALICE Patch Panel



SamTec Cable and FPC Extension R&D



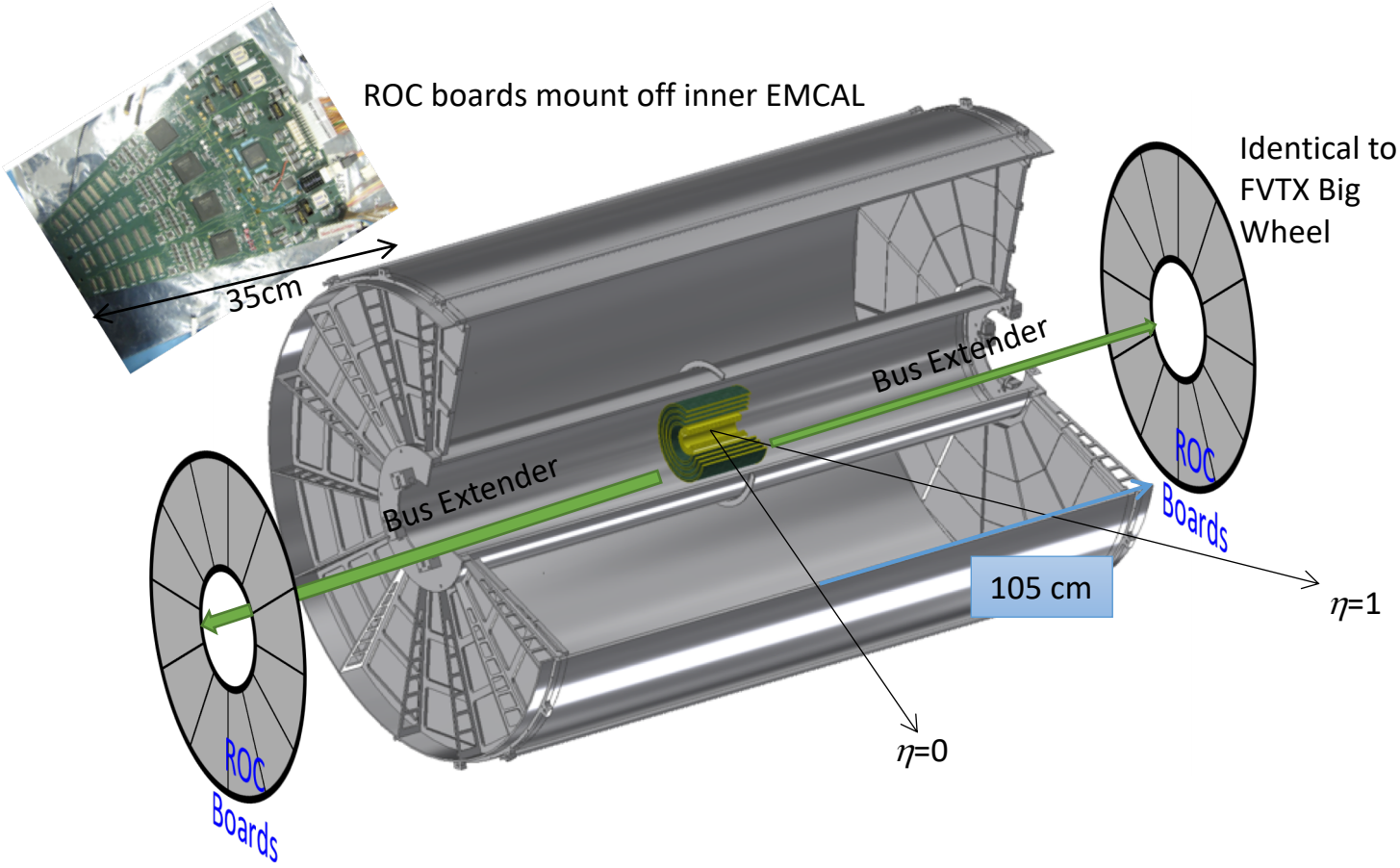
MVTX and INTT Integration



- It is clear from this detail view the conical region of the MVTX detector barrel with the INTT that the MVTX will need to translate in Z…, but there is a limitation;

- Optimize INTT design to fit within the limitation

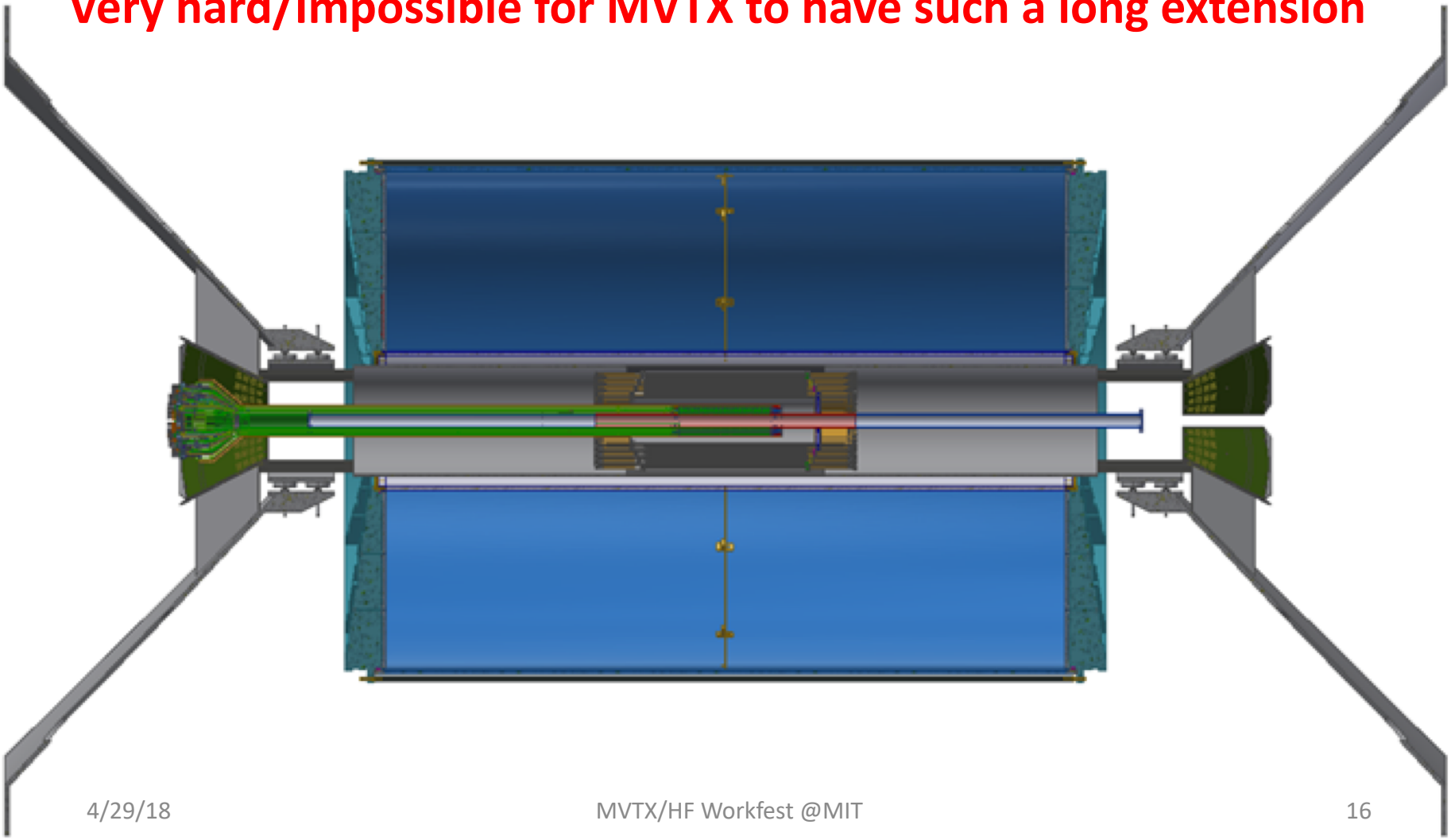
INTT Readouts from both North and South



The bus extender needs to run to ROC boards (reuse FVTX ROC) outside TPC.
Minimum length is 105cm – ladder length + distance to ROC board.

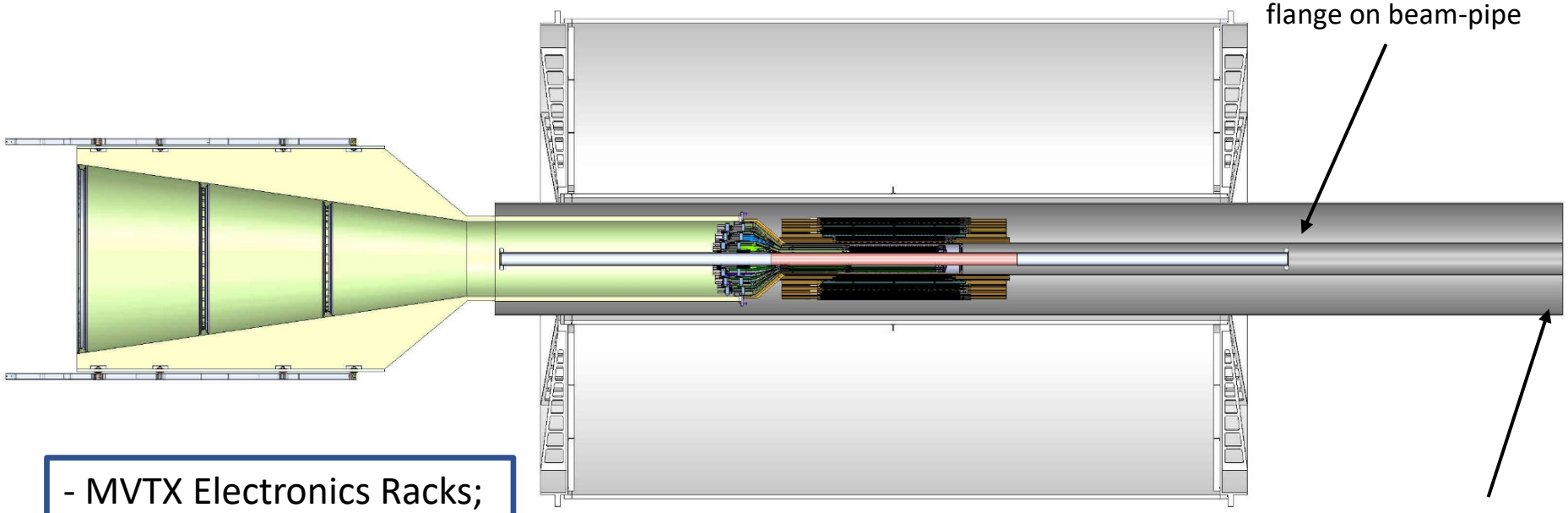
INTT supported off Inner HCal
from Dan Cacace/BNL

Very hard/Impossible for MVTX to have such a long extension



Mechanical Integration

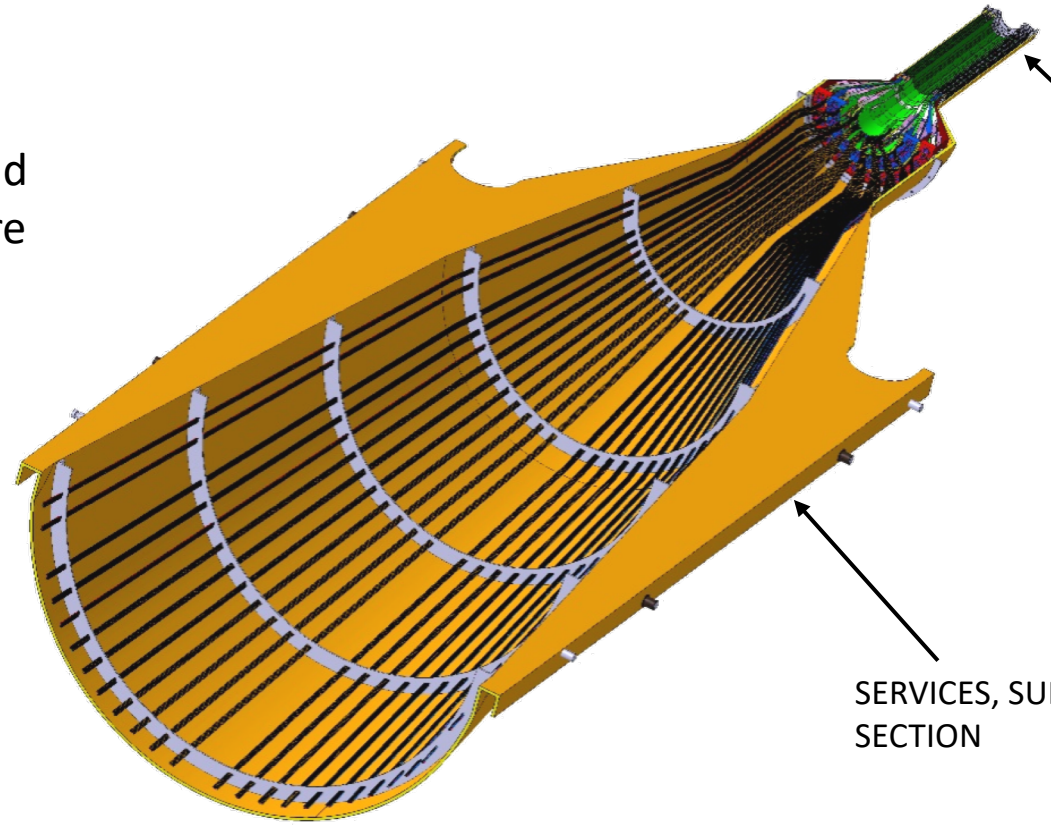
- Model of MVTX with INTT inside TPC with the addition of two concentric composite cylinders;
- INTT would like to use the outer shell of the MVTX as the inner shell of the INTT half detectors as a part of their cooling gas containment volume.



- MVTX Electronics Racks;
- PS racks

Service Barrel: Design and Fabrication, modify ALICE design
MVTX will have a similar but much smaller service barrel

Need:
Support structure and installation procedure

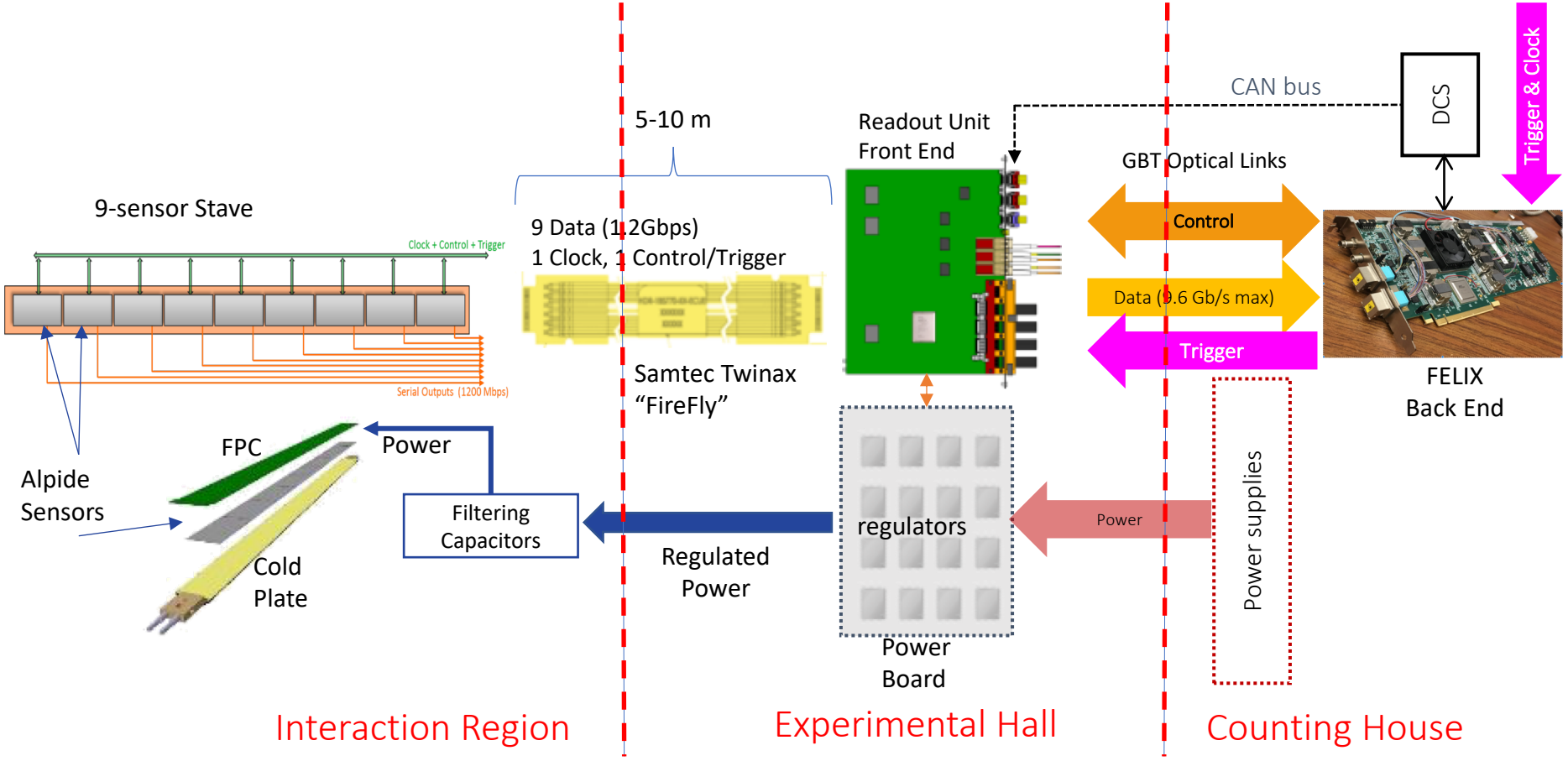


ALICE HALF-BARREL ASSY

To Do List – Readout and Controls

- Update firmware, sync with latest ALICE firmware
  - Scrubbing etc.
  - Burn-in test, stability
- Detector Control System (DCS) integration
  - Power distribution and monitoring
  - LV, “HV” and temperature
- Sensor operation optimization
  - Scan parameters for optimal operation
  - Laser test bench setup at LANL
- Multi-stave readout
  - Up to 3 staves per RU
  - Default: 1 stave per RU

MVTX Electronics, Power and Controls

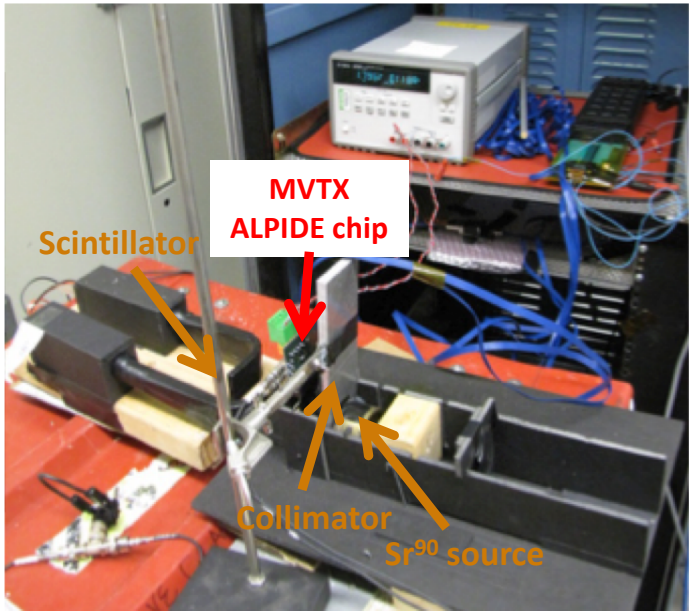


MVTX Detector Electronics consists of three parts

Sensor-Stave (9 ALPIDE chips) | **Front End**-Readout Unit | **Back End**-FELIX

Sensor and Electronics R&D @LANL

- ALPIDE evaluation and optimization
  - MOSAIC + Single Chip/Stave
  - Cosmic and source
  - Laser system
- Power unit tested
  - PU + MOSAIC
  - PU + RU
- Full readout chain demonstrated
  - ALPIDE + RUv1.0 + FELIX v1.5 + RCDAQ
  - Full stave + RUv1.x + FELIX v2.0 + RCDAQ
- Mechanical system integration
  - Conceptual design developed
  - MVTX+INTT integration
  - FPX & SamTec cables
  - RU location etc

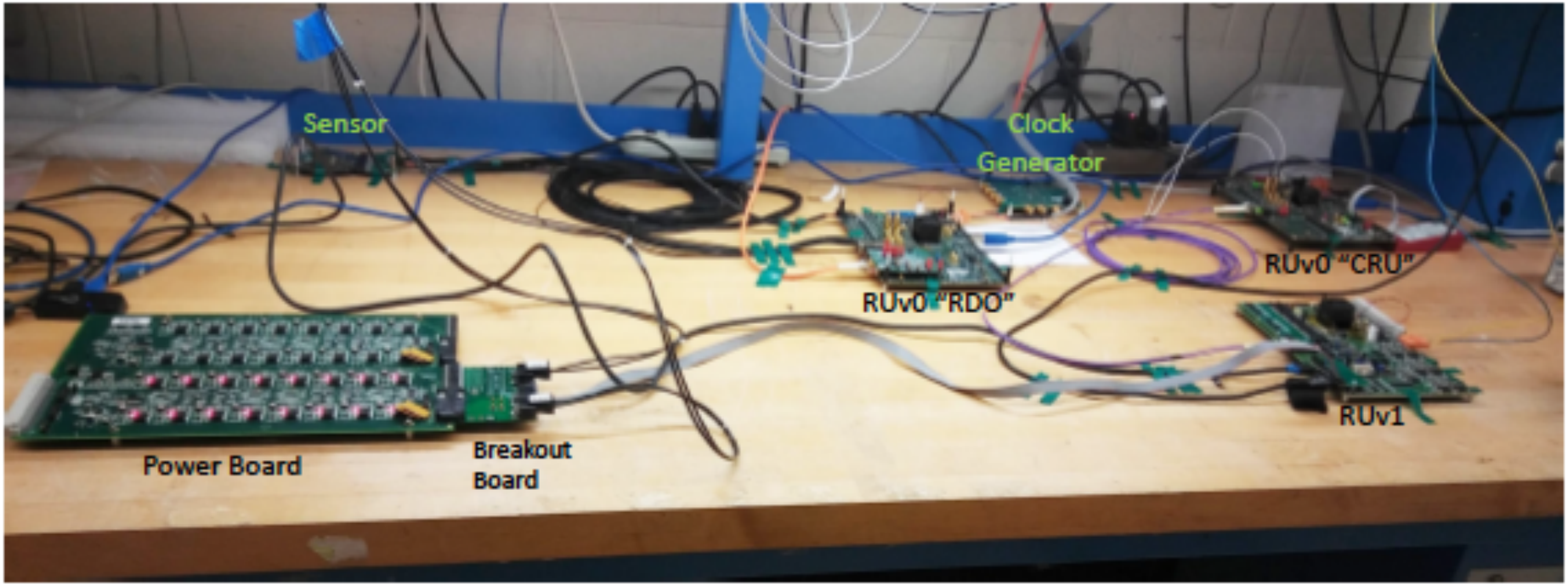


Parallel Effort at UT-Austin – Shared R&D

Test Setup at UT Austin

ALICE ITS UPGRADE

- RUv1 with transition bd + power mezz
- RUv0 as CRU emulator
- Single sensor on chip carrier board with interface board (only usable for IB tests, wrong pins for OB)
- Long (5m) FireFly cables
- Power board with single breakout board
- Now also tested with 9-sensor Inner Barrel module



Summary: Major Remaining R&D

- Mechanical/Electrical integration with INTT+TPC
  - Carbon structure design
  - FPC extension
  - Support structure and installation procedure
- Full electrical system control
  - Power
  - Safety and interlock
  - Online monitoring & controls
- Integrate readout system firmware/software with slow controls
  - Multi-stave readout with single RU
- Detector & Physics simulations

backups

More slides

What if we have to reuse PHENIX VTX Pixel Detectors for the sPHENIX?

Could the new RU be used for reading out old PHENIX VTX pixel detector?

Some Issues with VTX Pixel detector during Run16/15/14 …

- PHENIX experienced some serious problems with VTX pixel readout during the runs, and this affected the data quality… some of them being corrected offline, work in progress

A good technical summary note:

https://www.phenix.bnl.gov/phenix/WWW/publish/rnouicer/VTX/2016_VTX/Technical_Note_Silicon_Pixels_Tracker.pdf

- The causes of these problems are not very clear, at least to me …
  - Sensor quality issues?
  - Readout electronics related issues?
  - Noise and/or grounding issues?
  - ….
- Observations:
  - Event misalignment
  - Unstable and jump pixels/chips …
  - Significant dead areas …

VTX groups has 6 fully 100% working spare ladders for replacement, and enough good readout boards

Can somehow the new RU be used to improve the PHENIX pixel detector readout if we have to use the old pixel detector?

Run16 Au+Au

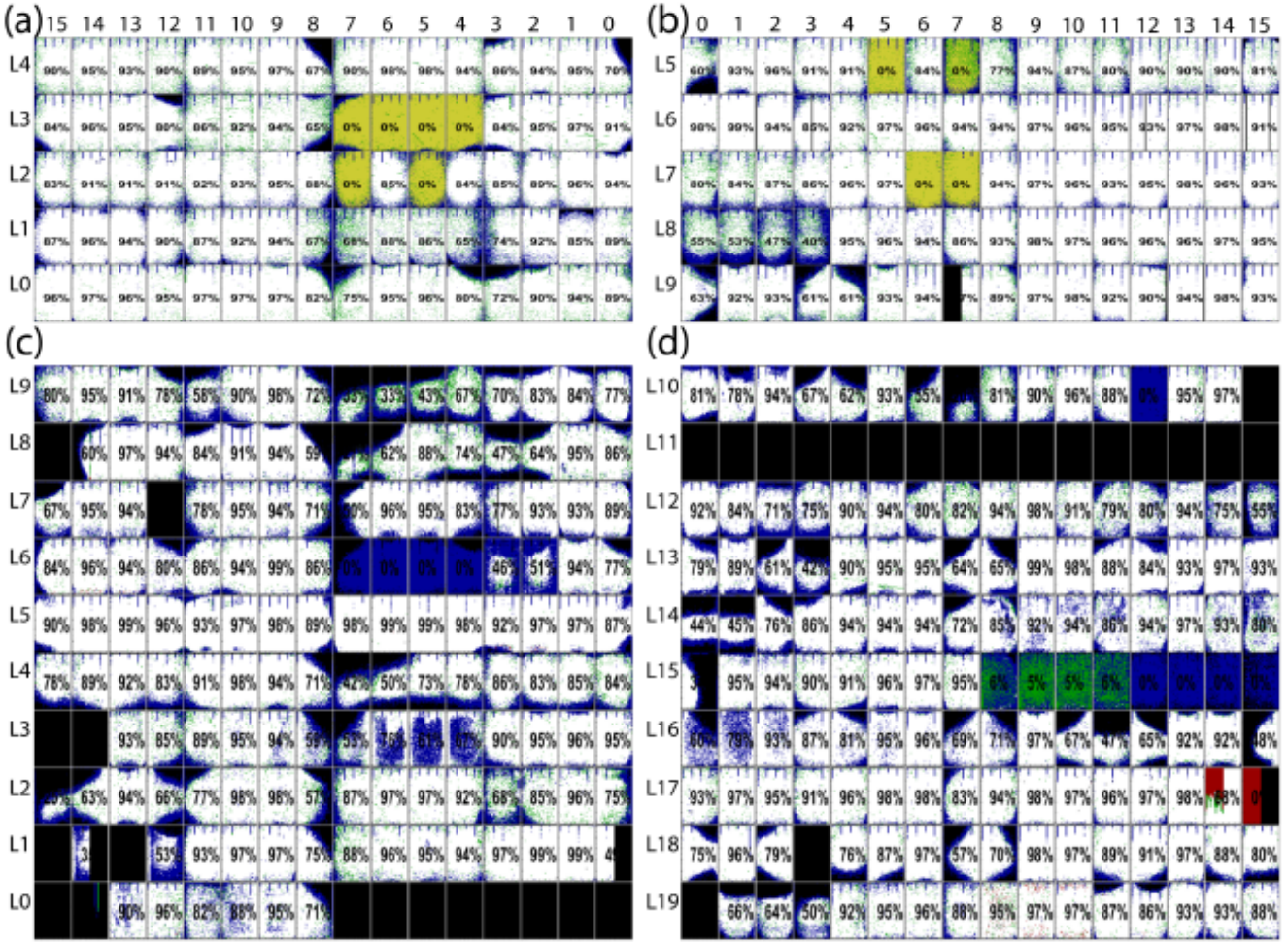


Figure 8: Data quality assurance from Run 446864 in Au+Au at 200 GeV (Run-16). Black point indicates a dead pixel. Red and blue points indicate hot and cold pixels, respectively. Green and yellow points indicate unstable and jump pixels, respectively. See text for more details.

From the PHENIX VTX pixel technical note

	West	East
B0	82 % (88 %)	84 % (88 %)
B1	72 %	69 %

Run15 p+p

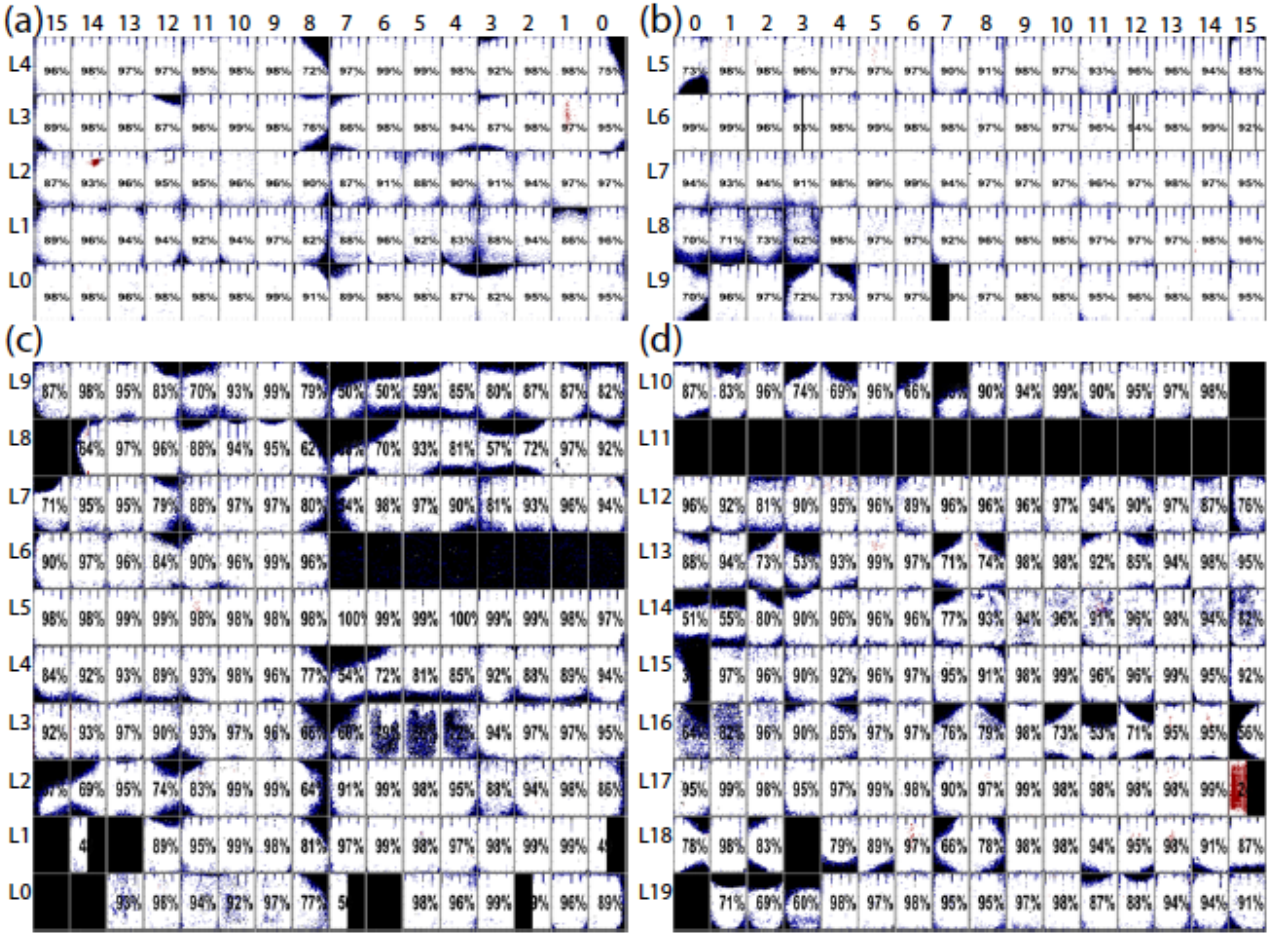


Figure 10: Data quality assurance from Run 421716 obtained in p+p collisions at 200 GeV (Run-15). Black point indicates a dead pixel. Red and blue points indicate hot and cold pixels, respectively. Green and yellow points indicate unstable and jump pixels, respectively. See text for more details.

From the PHENIX VTX pixel technical note

	West	East
B0	93 %	93 %
B1	80 %	78 %

Run14 Au+Au

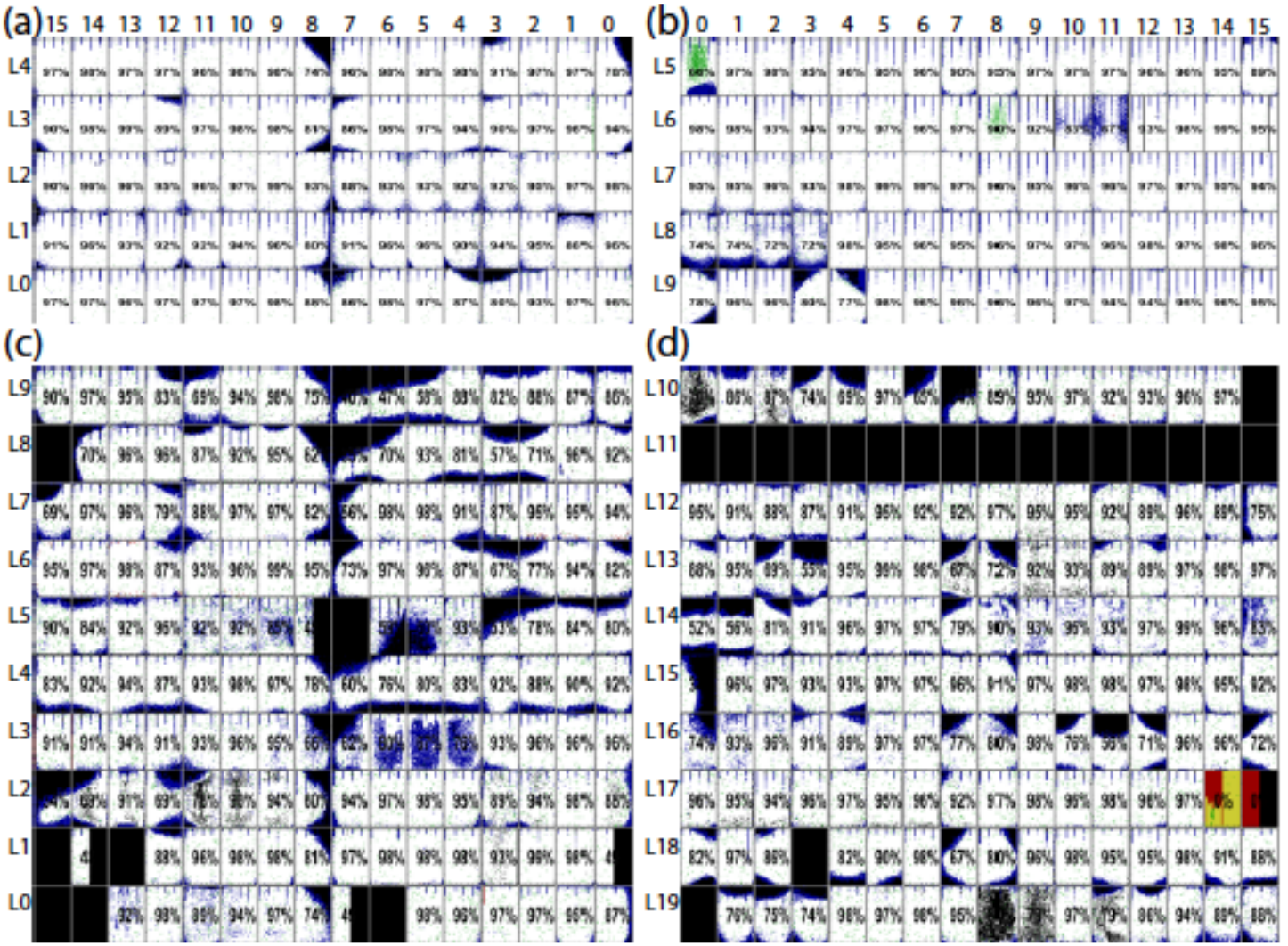


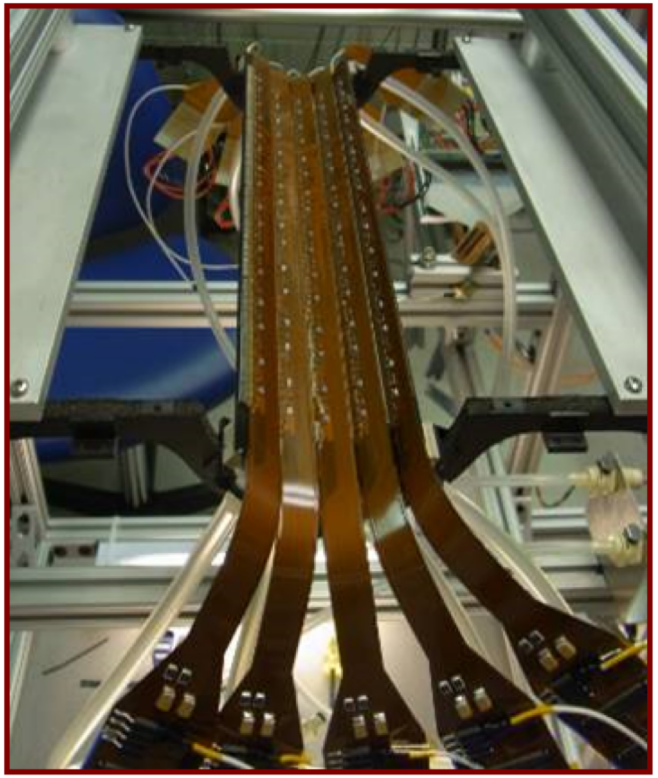
Figure 11: Data quality assurance in Run14 (Run 405860: Au+Au at 200 GeV).

From the PHENIX VTX pixel technical note

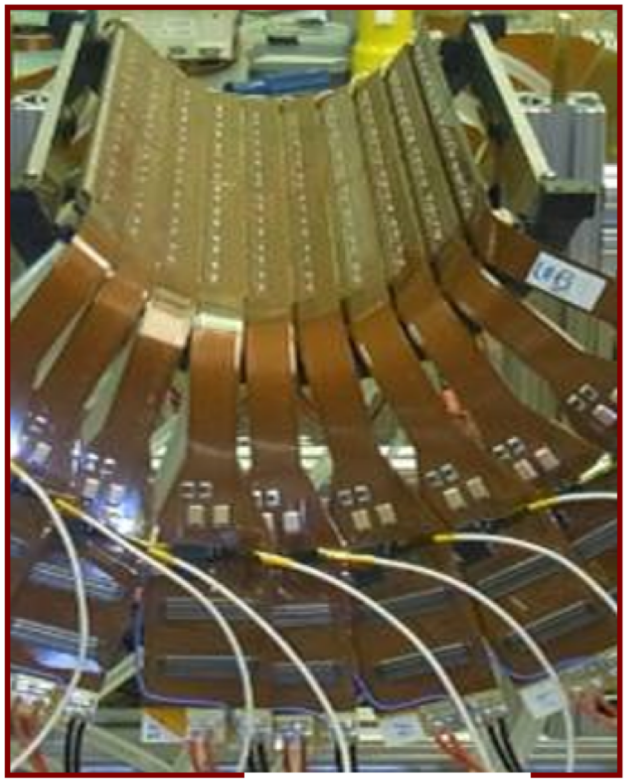
	West	East
B0	94 %	93 %
B1	81 %	77 %

PHENIX Pixel Detector

Layer 1: 5 x 2 Pixel Ladders

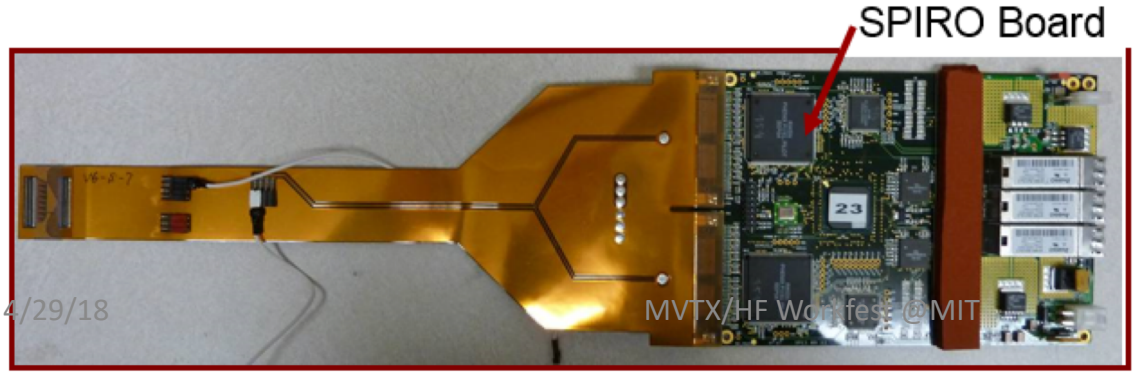


Layer 2: 10 x 2 Pixel Ladders

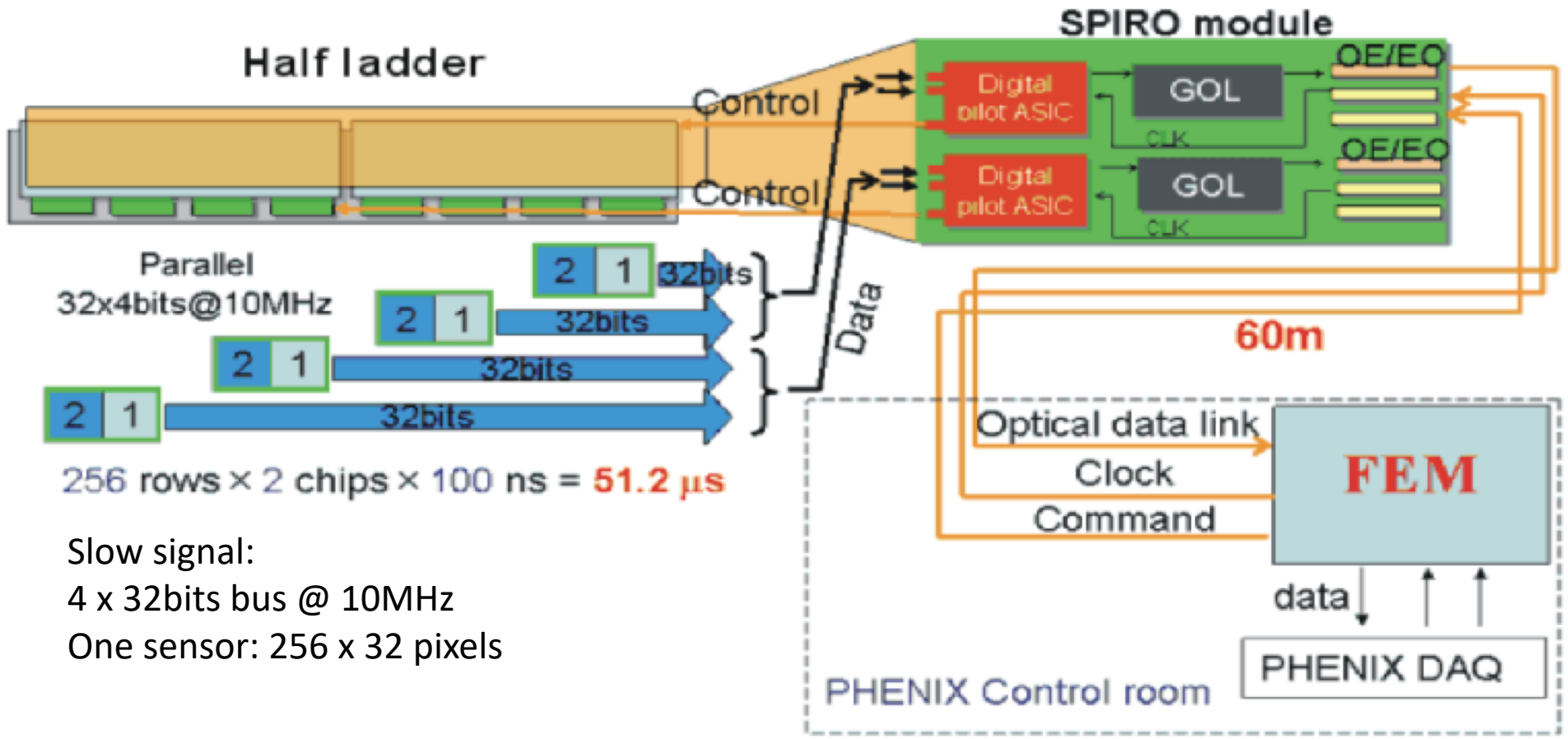


R0= 2.5cm
R1 = 5.0cm
Lz = 20cm

Pixel:
425 um x 50 um,



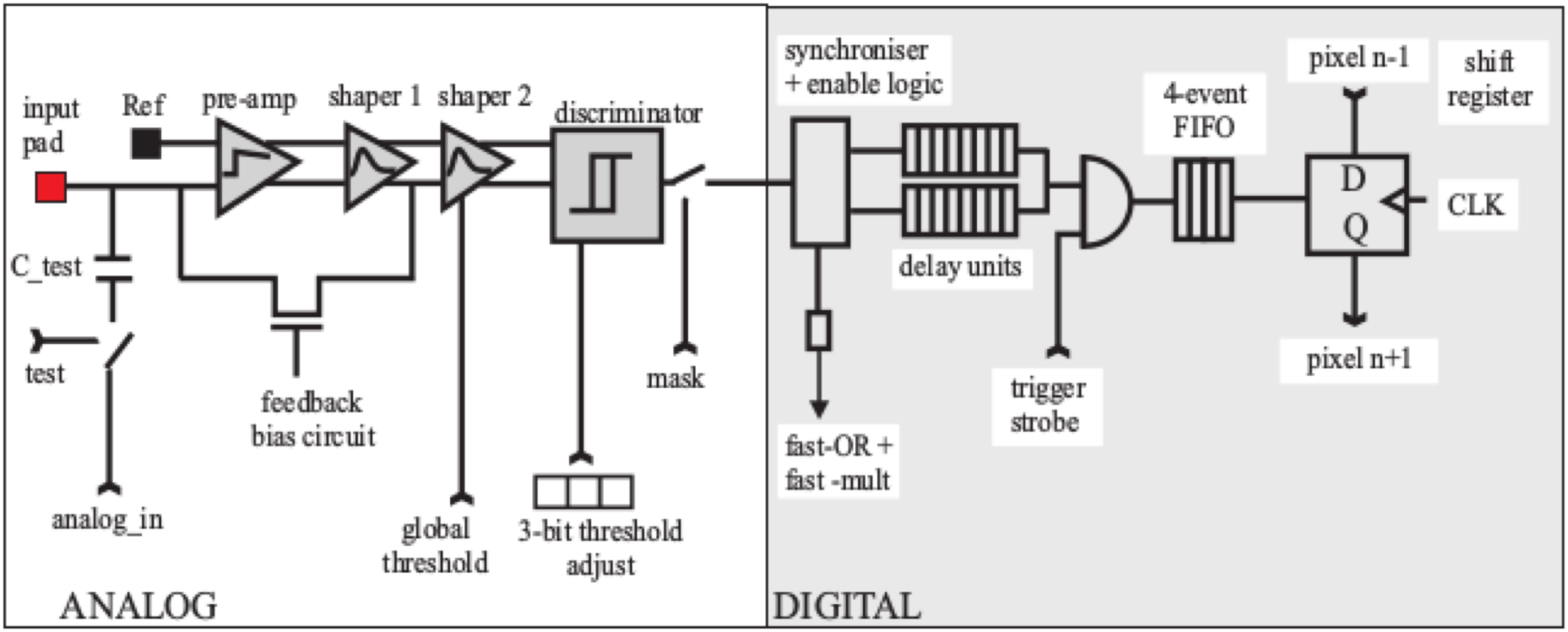
Readout the old PHENIX Pixel Sensors with new RU for sPHENIX?



Slow signal:
4 x 32bits bus @ 10MHz
One sensor: 256 x 32 pixels

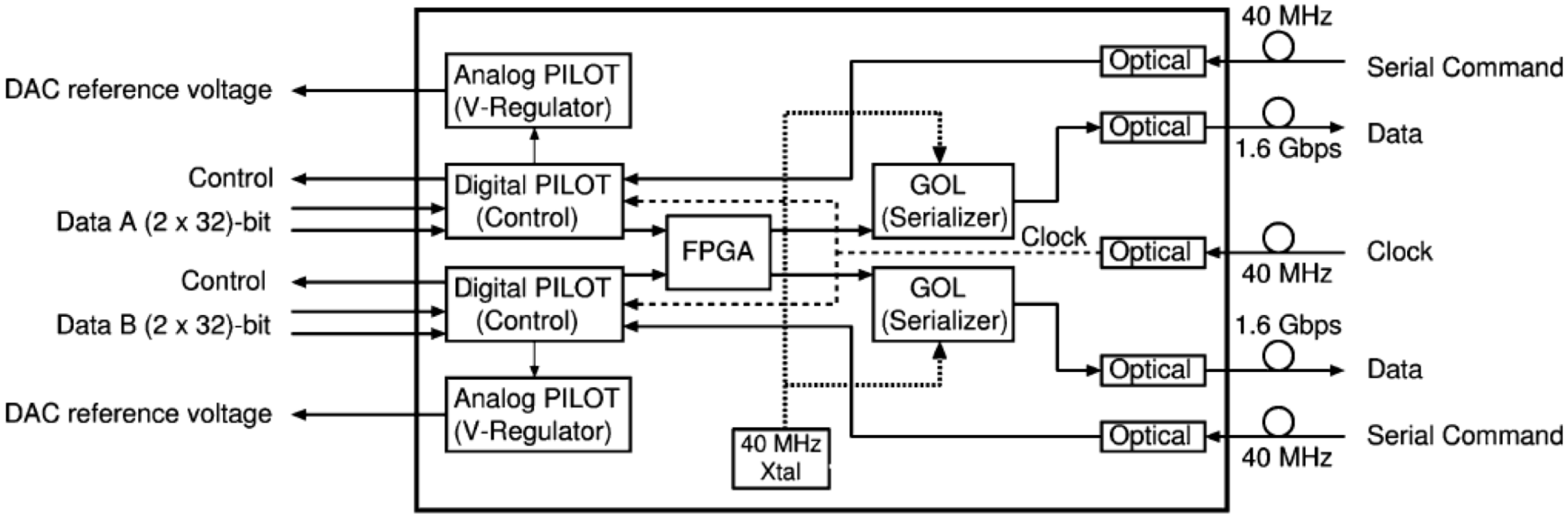
It takes 25.6 sec to read-out one ALICE1LHCb chip at 10 MHz with a 32-bit data width. Thus in order to achieve the detector readout time of 50 sec, two of the four ALICE1LHCb readout chips in a sensor hybrid should be read out in parallel simultaneously. There are two sensor hybrids on a half-ladder that is read-out by a single bus. This means that the bus should read out four ALICE1LHCb readout chips simultaneously.

Pixel Readout



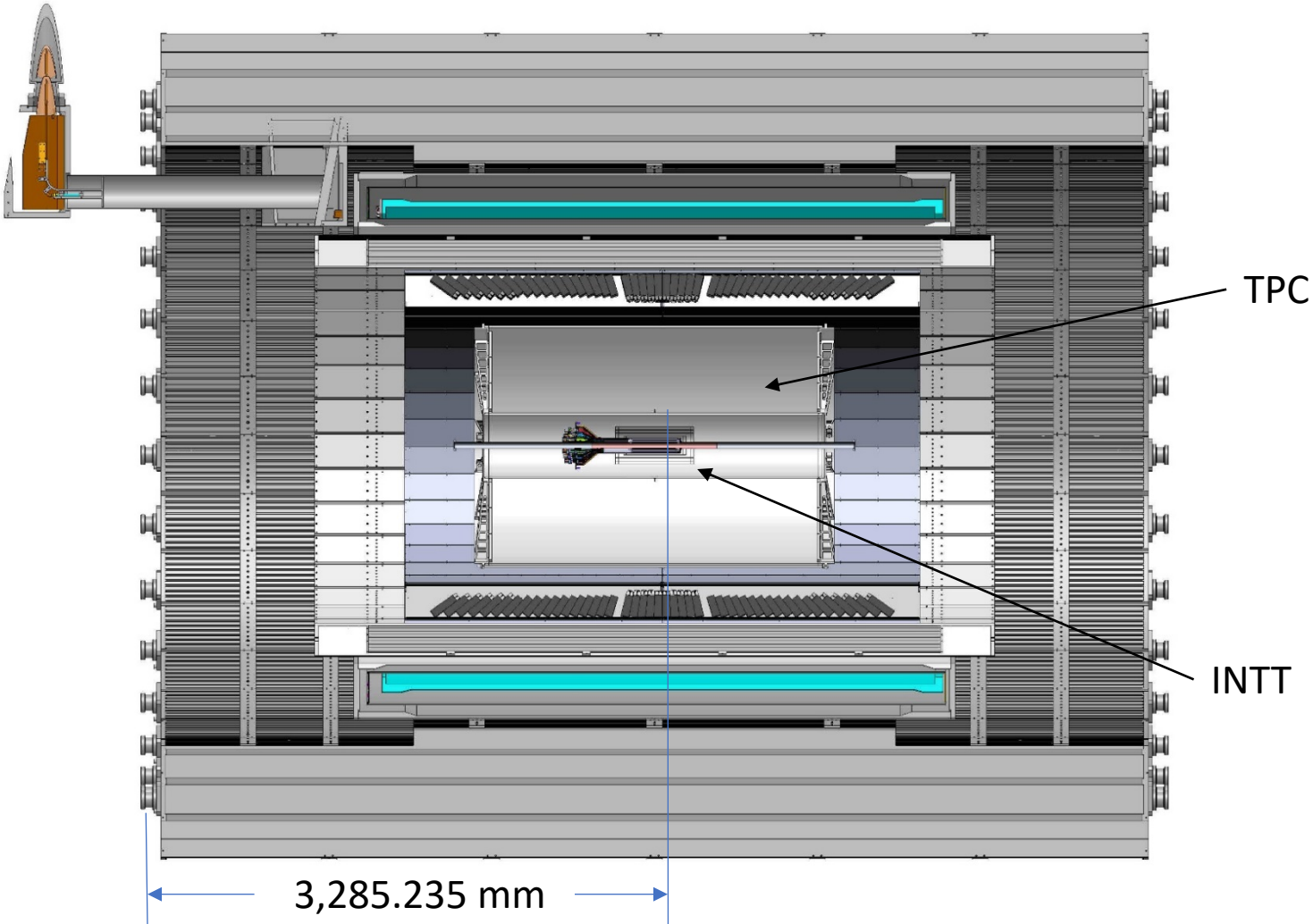
256 in Raw x 32 in Colum:
- 32bit Bus x 256 readout

SPIRO (Phenix Pixel ReadOut)



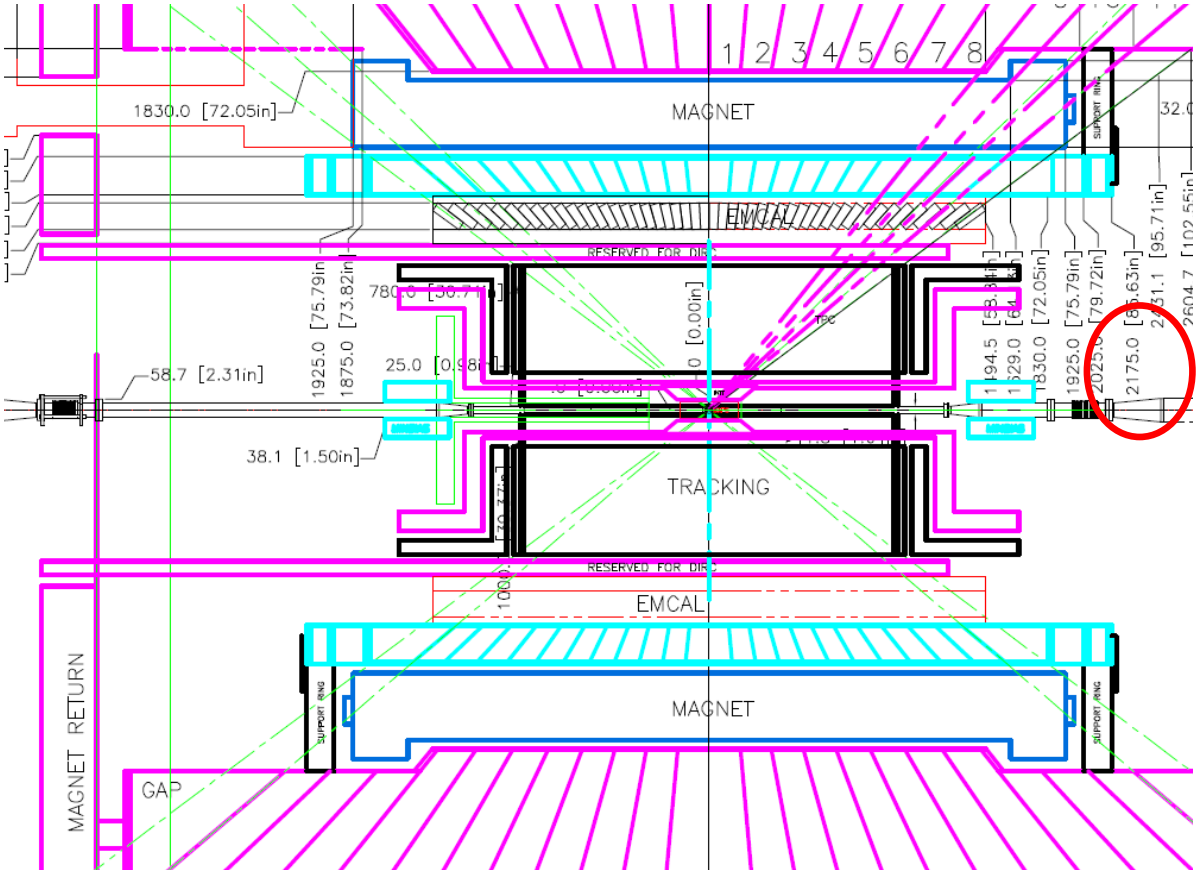
- Very similar functionalities in the new RU,
  with more powerful FPGA and GBT
- A daughter board could be used to match the slow 10MHz parallel 2x32bits bus outputs from the old pixel sensors to the RU inputs,
- can be directly connected to the RU inputs (# I/O?)?

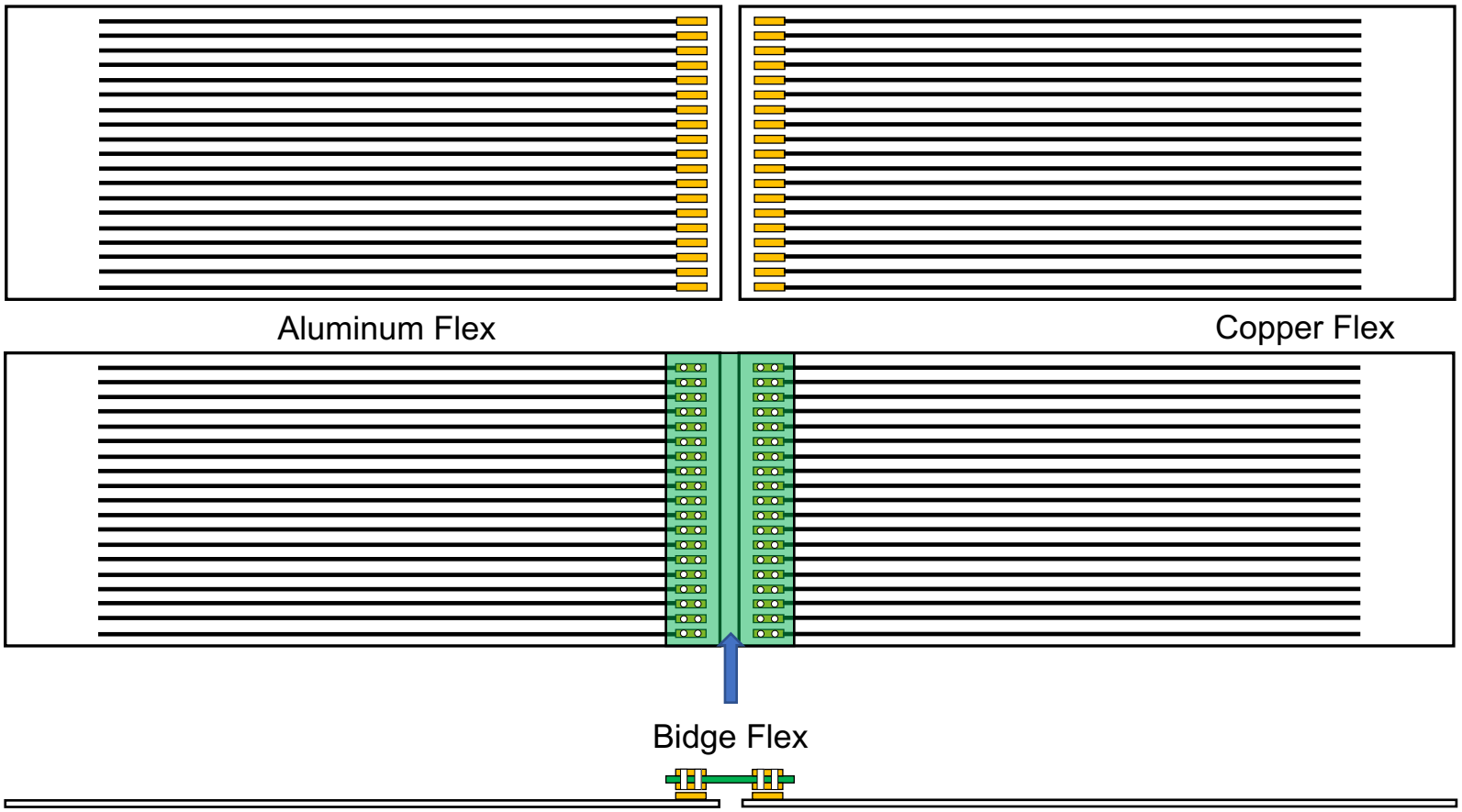
sPHENIX CAD model sectioned - view showing overall scale of sPHENIX detector; including all three tracking elements; MVTX, INTT and TPC

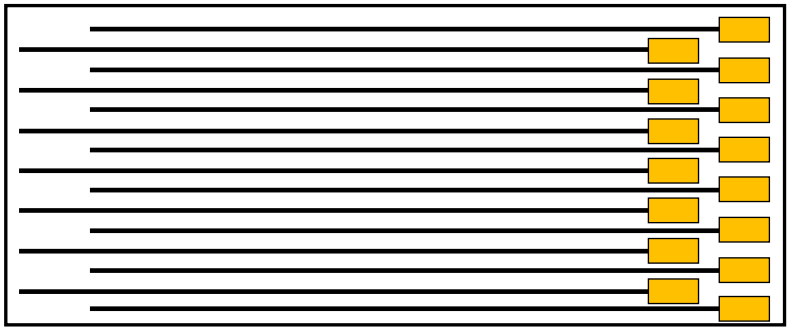


NOTE; MVTX service cone and supports are not shown, MVTX offset in Z by 18cm

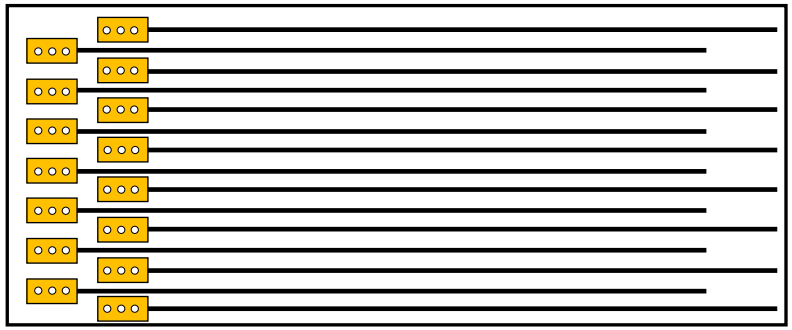
BNL control envelope drawing - needs update for TPC, INTT, MVTX, MB
Z location of the inner Hcal is at 2175,0mm



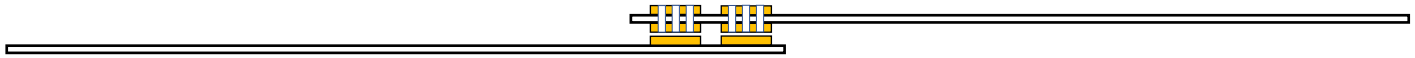

Aluminum Flex
Copper Flex
Bidge Flex

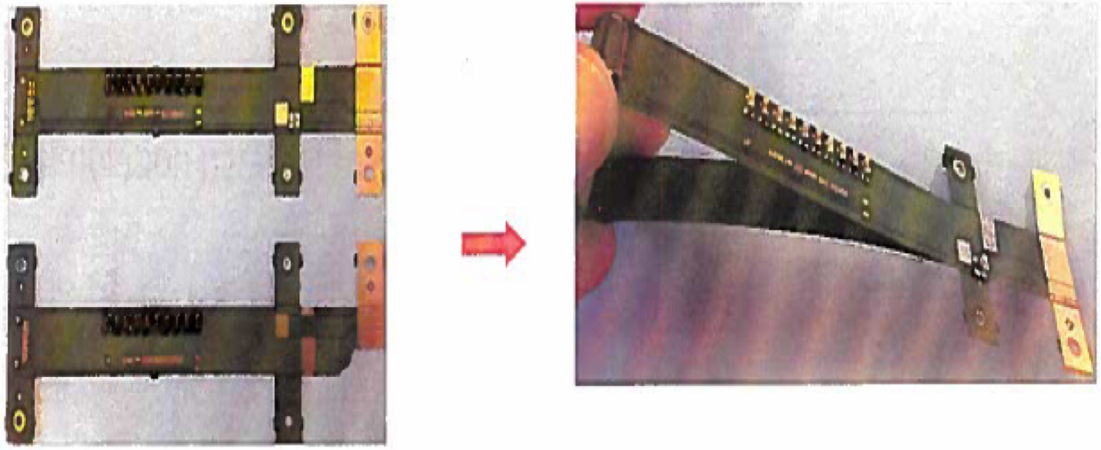


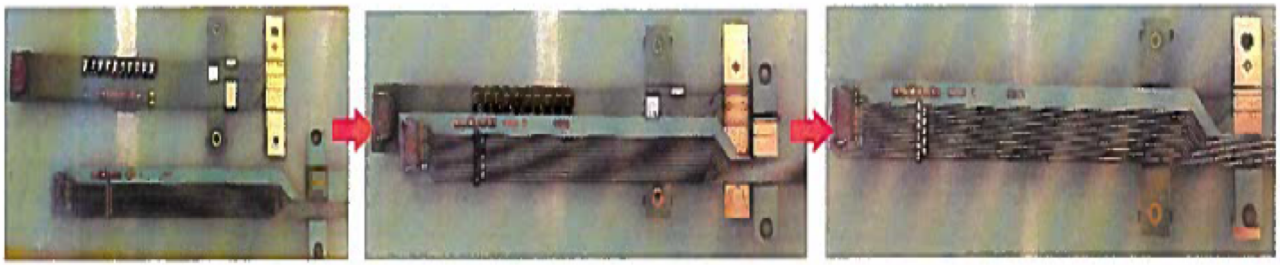
Aluminum Flex

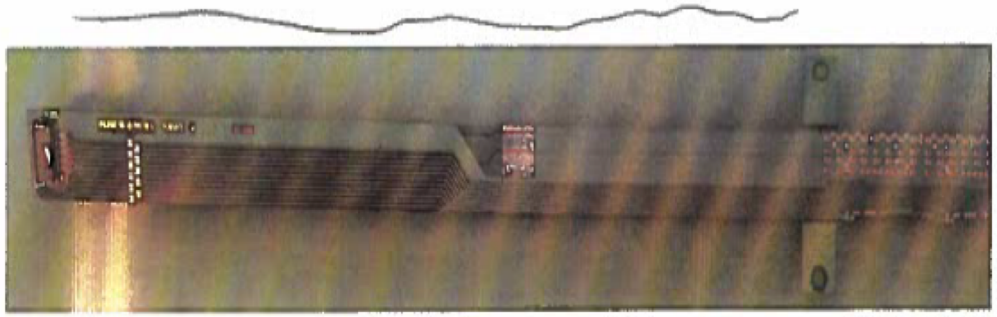


Copper Flex









IB FPC

11

INTT-MVTX Space Conflict

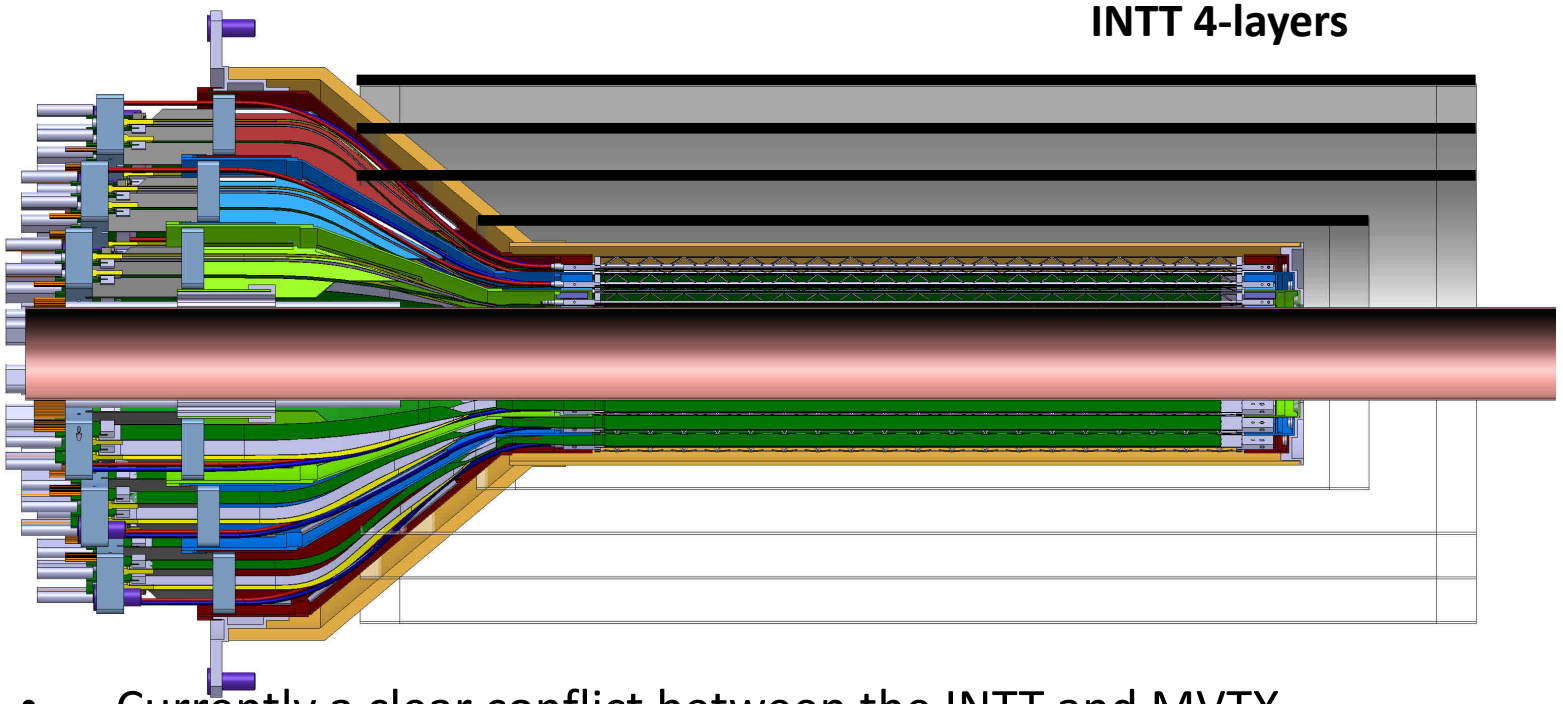
INTT Acceptance @ |z|=10

|η|<0.95

|η|<1.09

|η|<1.28

|η|<1.12

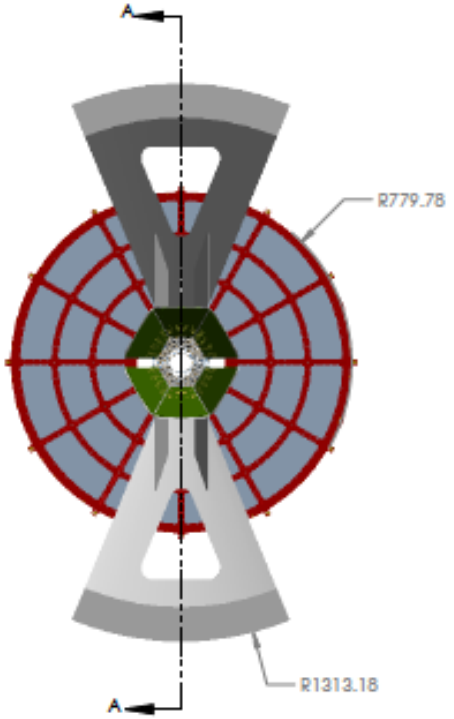


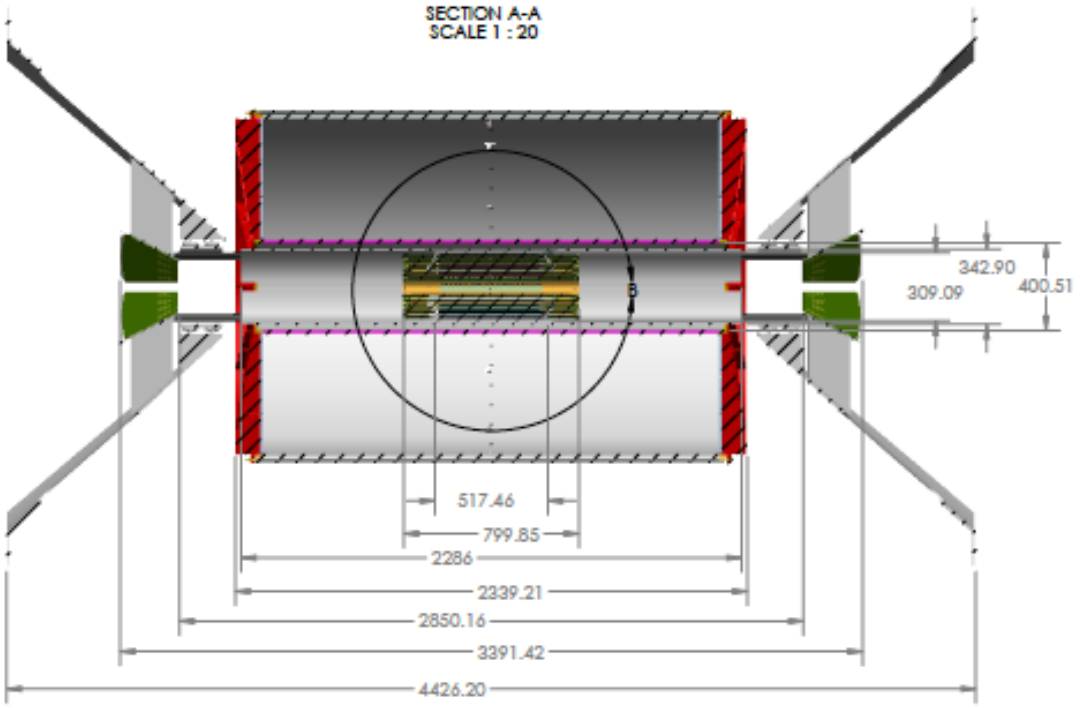
- Currently a clear conflict between the INTT and MVTX
  - INTT only includes ladder, no connectors, cooling barbs, etc

R&D items:

1) Extend cables to move the conical structure further out in z-direction;
2) Design/optimize INTT layers to fit current MVTX geometry;
   - FPC data cable can't be easily extended (max additional ~10cm, machine limit)
   - Reduce angle of cone – redesign C-structures and connectors

INTT + TPC





ALL DIMENSIONS IN MILLIMETERS

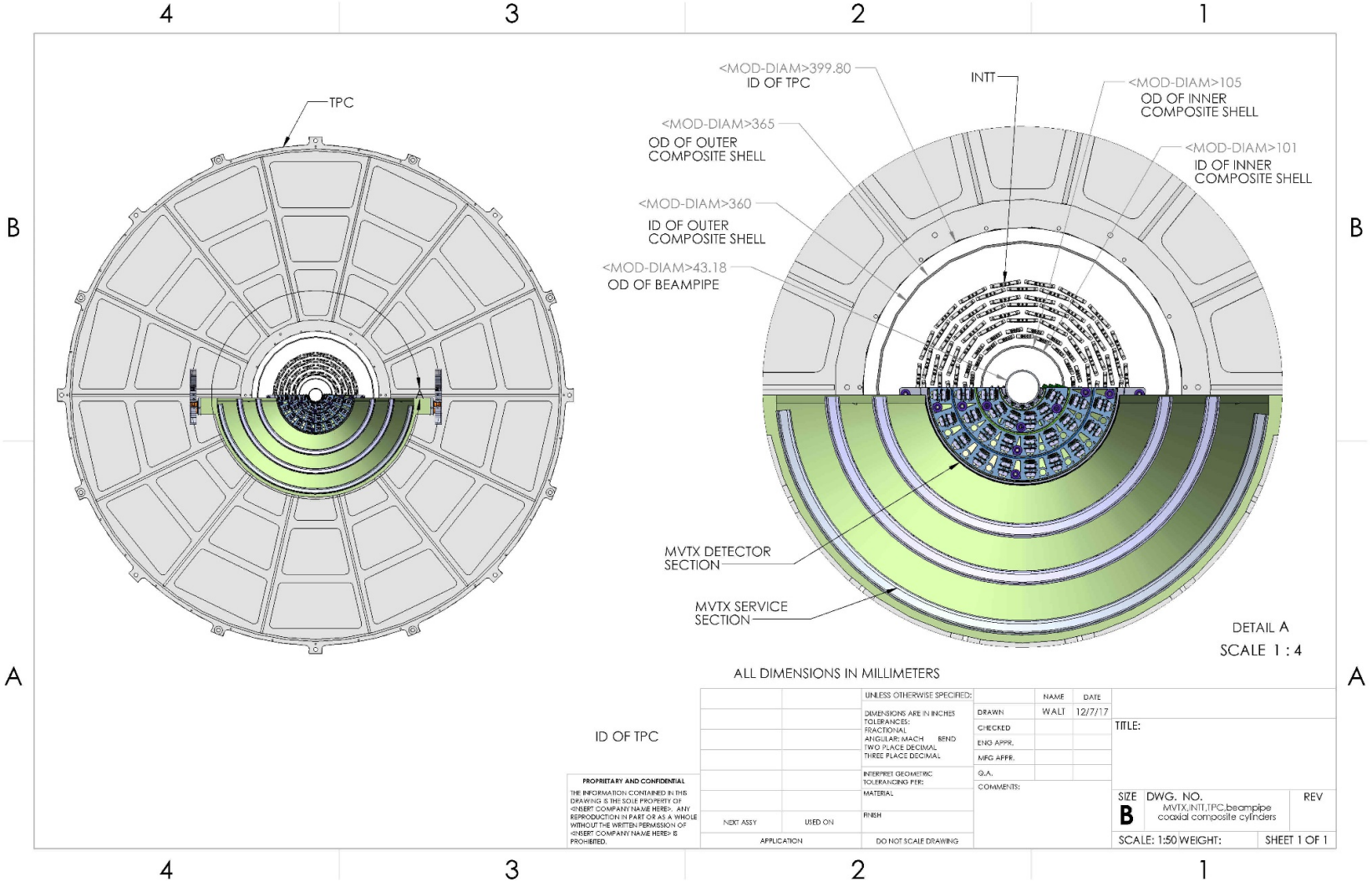
P-25 SUBATOMIC PHYSICS

Los Alamos

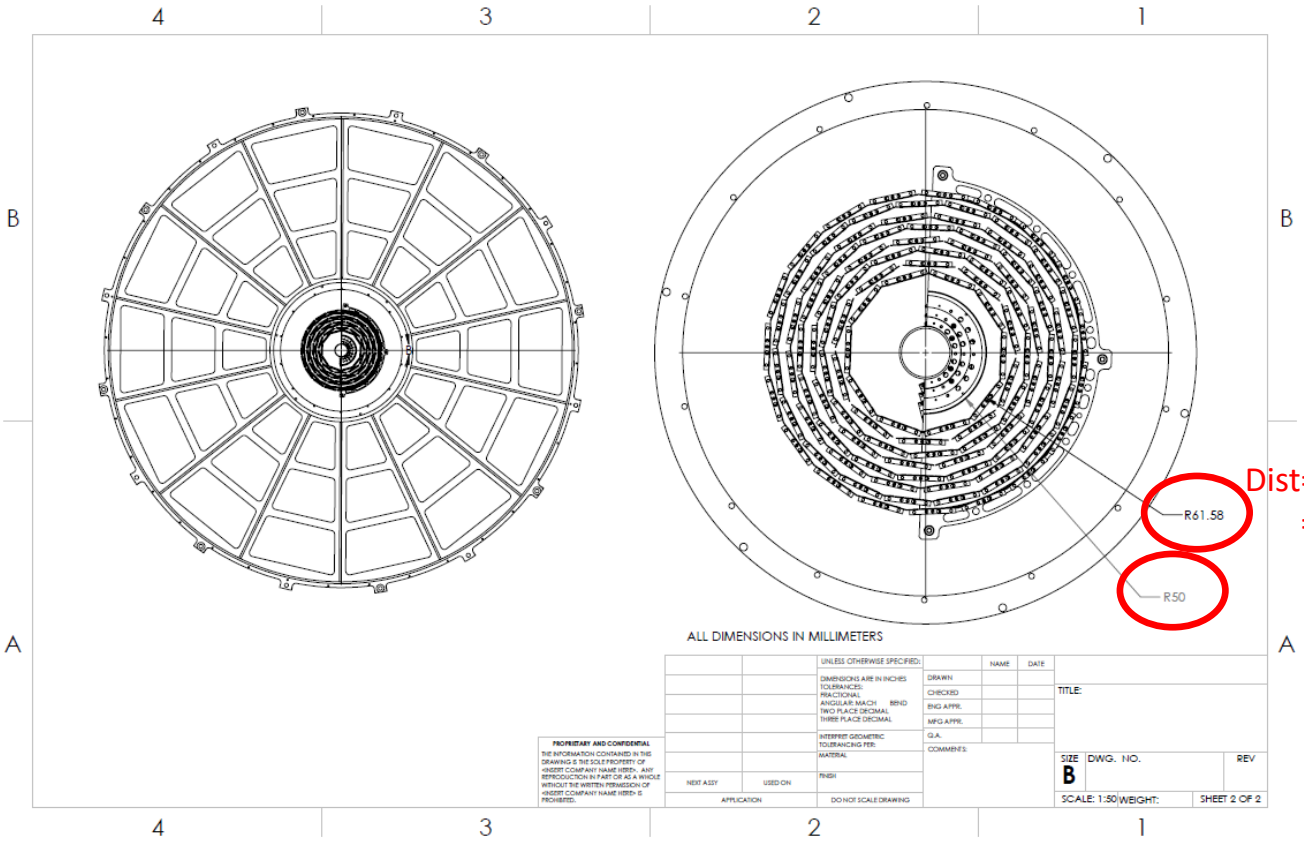
MVTX INTT TPC
DAN CACACE MODEL INTT with TPC

Cross-section view from CAD model of MVTX, INTT, TPC, beam-pipe, plus two composite conical shells:

MVTX radius are increased by 1.5mm to have a minimum 2mm gap between beam pipe and then inner MVTX structures

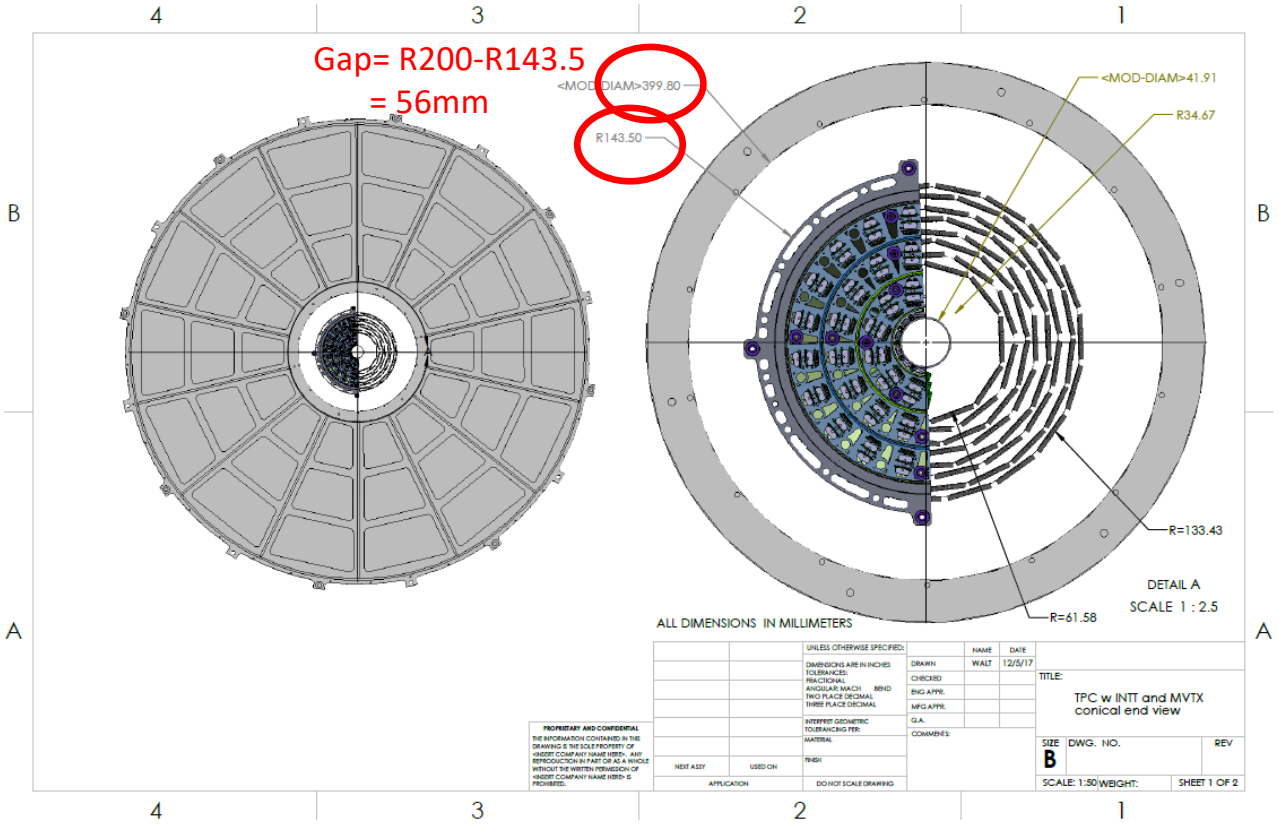


Gap between conical shell (CYSS) of MVTX and inner layer of INTT is 11.58 mm

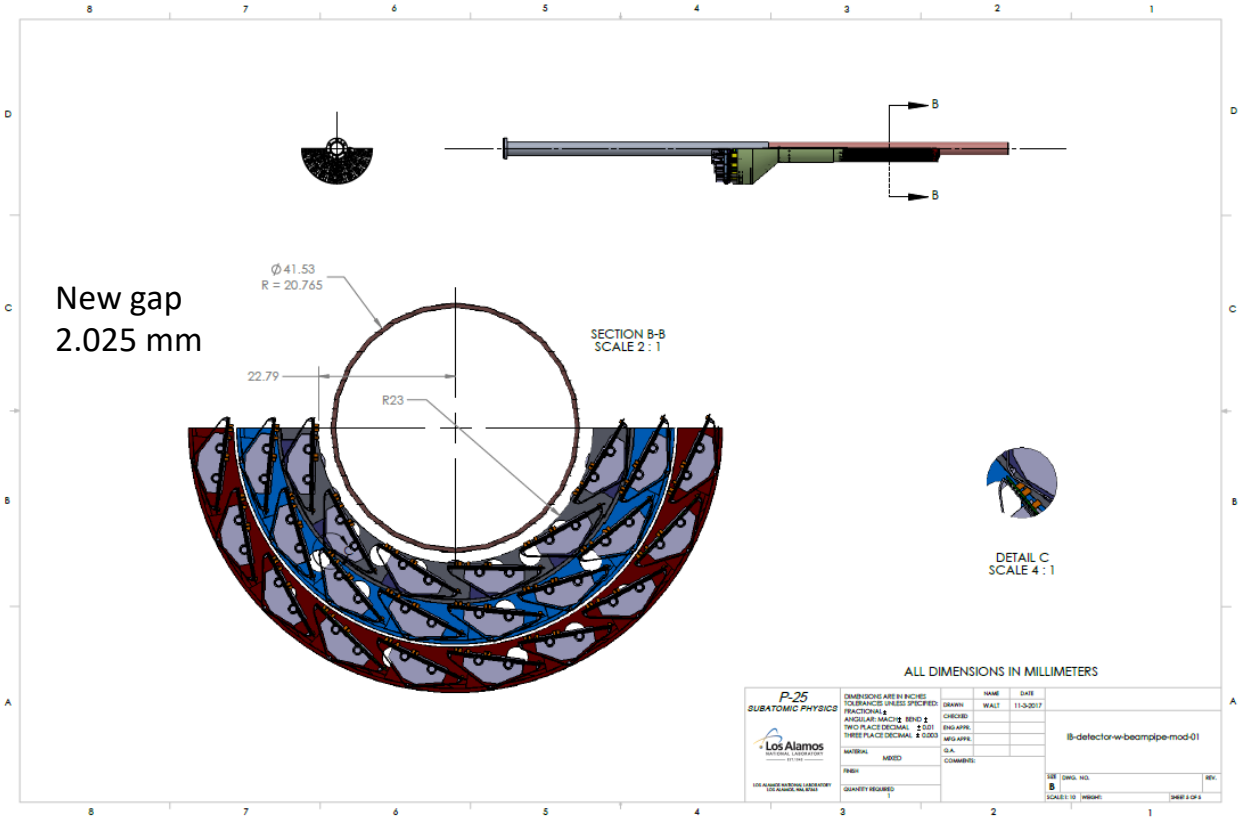


Dist= R61.58 – R50
= 11.58mm

56.0 mm gap between INTT and inner radius of TPC



Offset from OD of beampipe and innermost component of the MVTX



Offset needed to install split MVTX into run location around beampipe, passing over 2.75 in conflat flange