Characterisation of IB HIC and Stave Prototypes

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ALICE ITS Upgrade

Stave Production Readiness Review

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Executive Summary

An extensive characterisation program has been executed with inner barrel HICs and staves.

The electrical characterisation shows characteristics well in agreement with simulations of the FPC whereas the functional characterisation demonstrates a performance comparable to single ALPIDE chips. On the level of individual chips the results of the HIC tests clearly reflect the results of prior probe station tests.

No significant difference in performance was found between bare HICs and HICs mounted on staves.

Ageing studies showed no evidence of damage, neither due to thermal cycles nor due to wire bond vibrations in a magnetic field.

Outline

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① Introduction

② Electrical Characterisation

③ Data Transmission

④ Threshold and Noise

⑤ Ageing

⑥ Stave Tests

Test Setup

In order to guarantee conditions as close as possible to the final detector, the test setup used for the measurements shown in this presentation has been modified with respect to the production test setup:

- Powering: powering is done with a prototype power board, which is connected to the HIC through 5 m long cables
- Data readout: Data readout is done through a 5 m long FireFly cable
- Data transmission: for tests of the data transmission a prototype of the ITS readout unit is used instead of the MOSAIC test board

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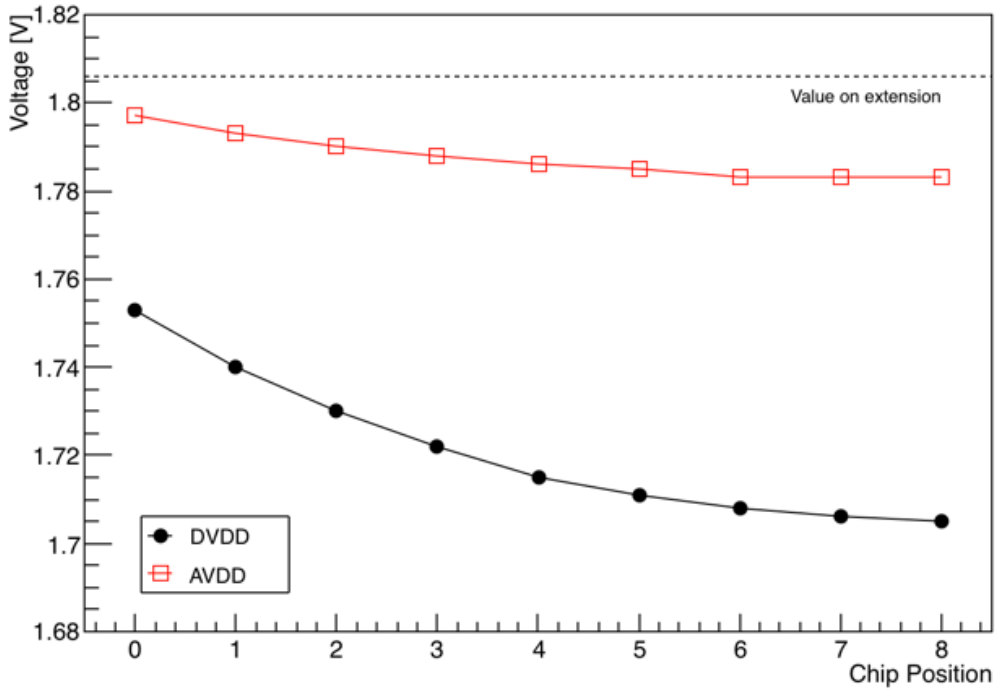
Static Voltage Drop

Measurement of the supply voltages at the decoupling capacitors along the HIC

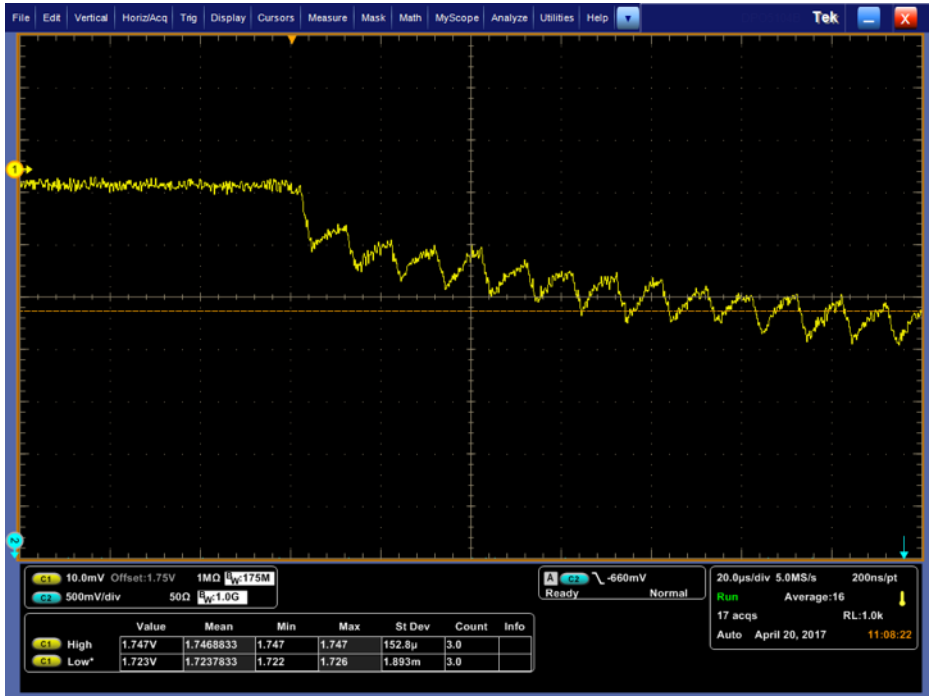
- Drop between first and last chip in DVDD 48 mV, in AVDD 14 mV
- Both comparable to values from the simulation (52 mV / 15 mV)
- Drop in extension comparable to drop along HIC
- Currents during measurement: digital 885 mA, analogue 110 mA



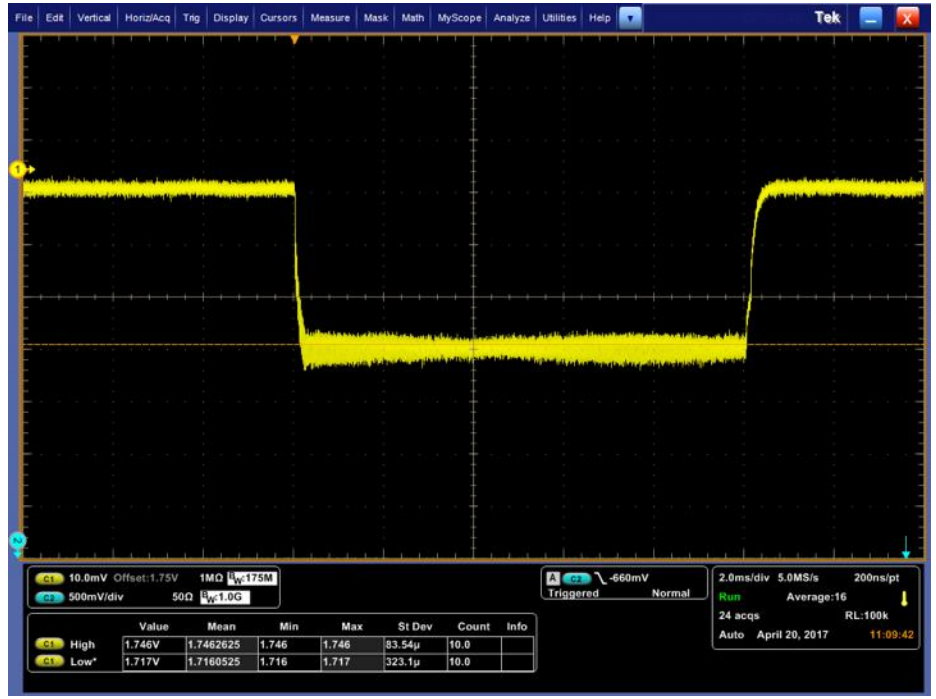
Dynamic Voltage Drop

Digital Voltage at last chip on HIC during digital injections with 100 kHz into 512 pixels
Powering scheme: power board with full length (5 m) power cables

Train of 1000 triggers, voltage saturates at ΔV = - 30 mV



Time scale: 20 us / div

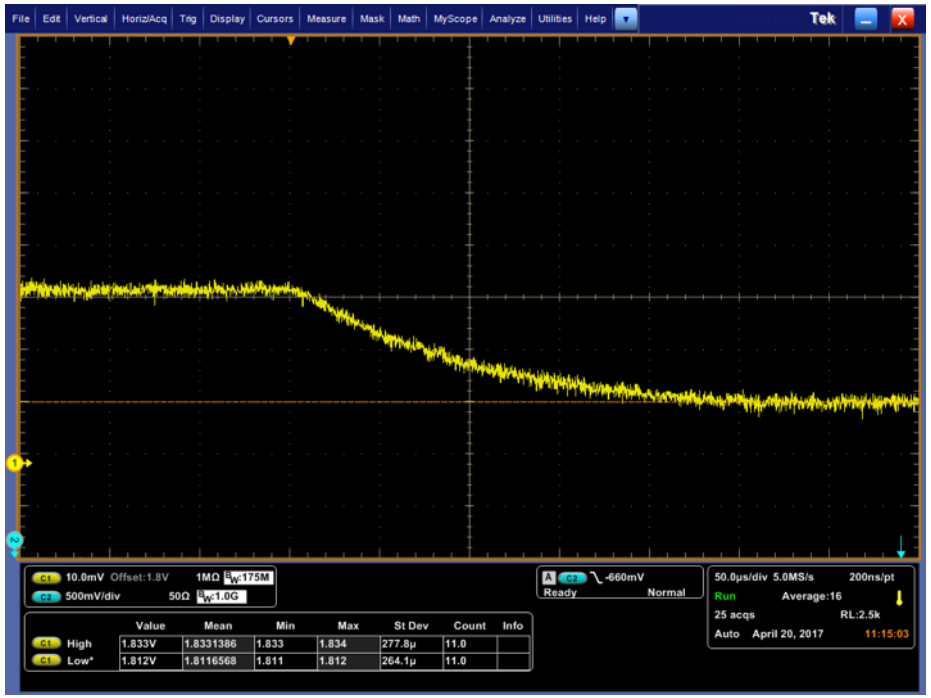


Time scale: 2 ms / div

Dynamic Voltage Drop

Same conditions but measured on the power extension

High-frequency component completely filtered by capacitors, voltage drop -22 mV



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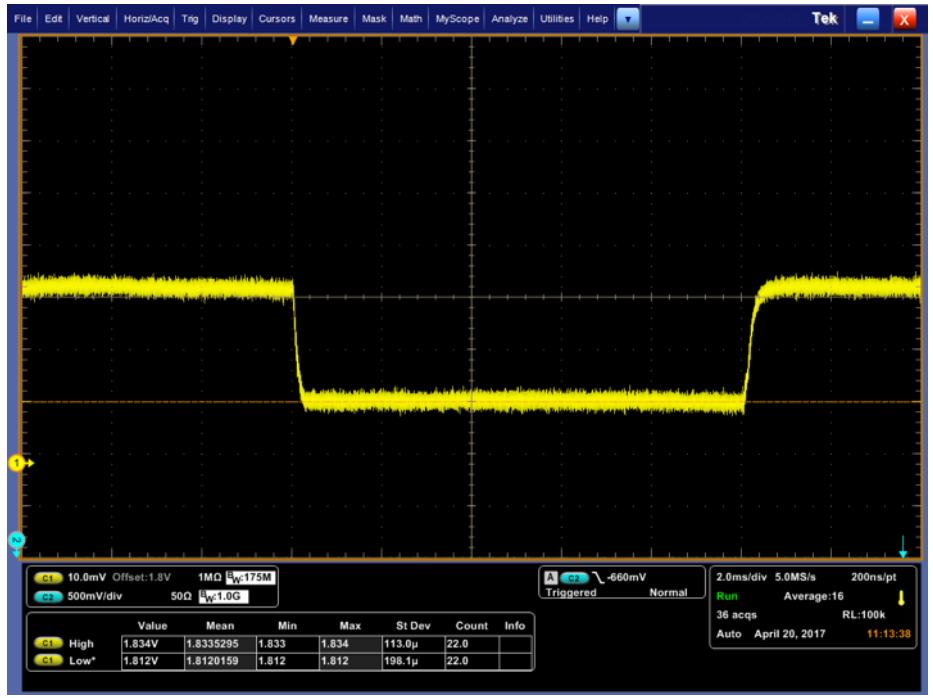
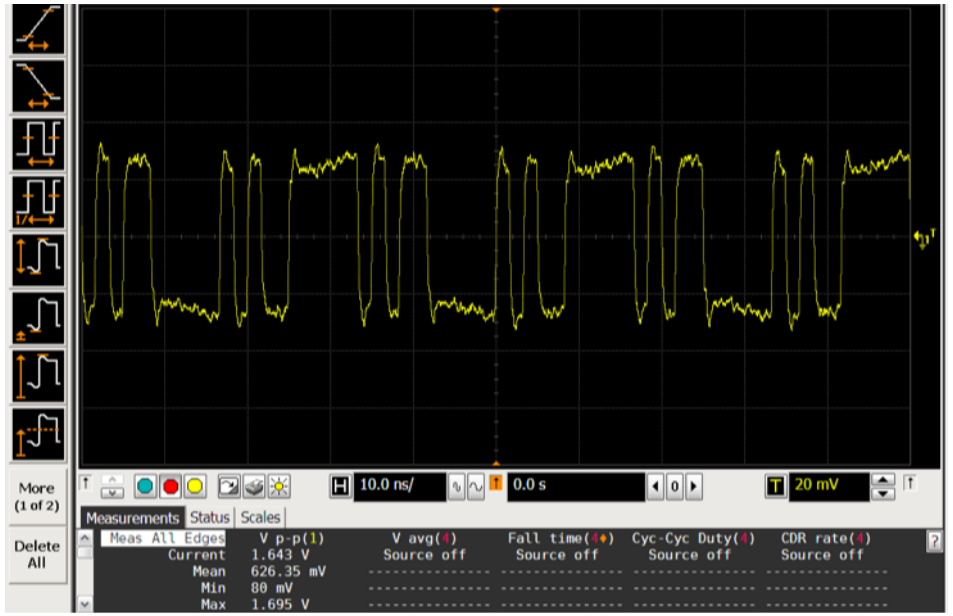
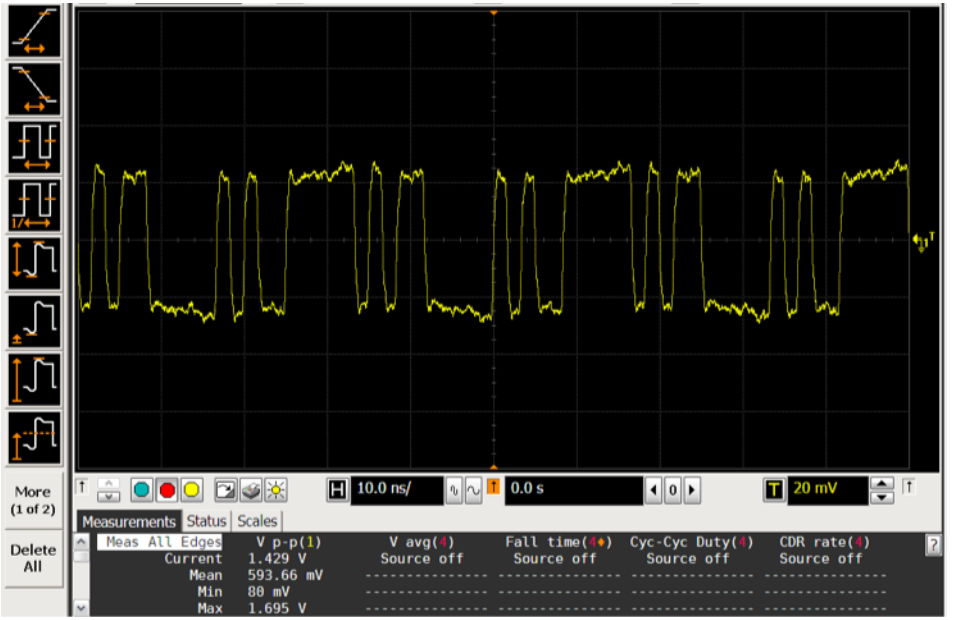


Time scale: 2 ms / div

Signal Attenuation

Comparison of HS data lines of first and last chip, measured on the FPC (connector end)
Measured attenuation ~13% , corresponding to -1.2 dB
(note: distance between first and last chip is only half of total FPC length)





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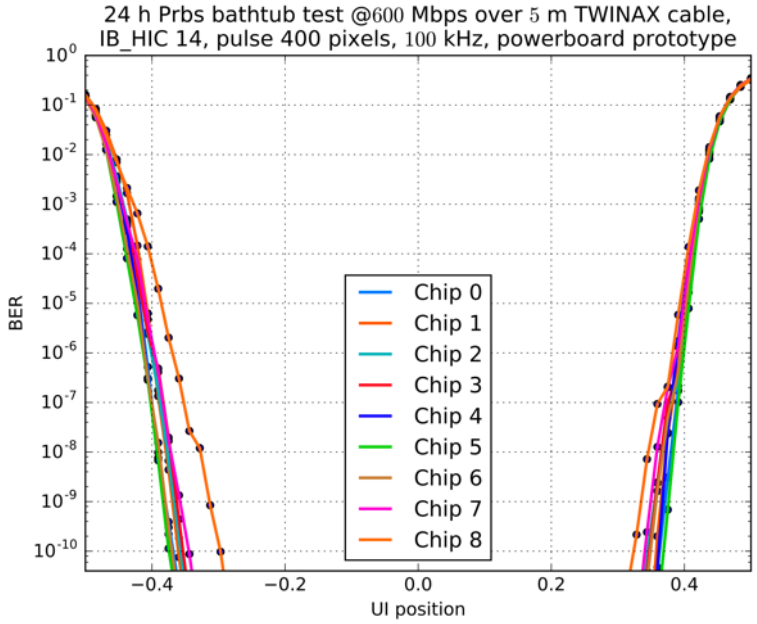
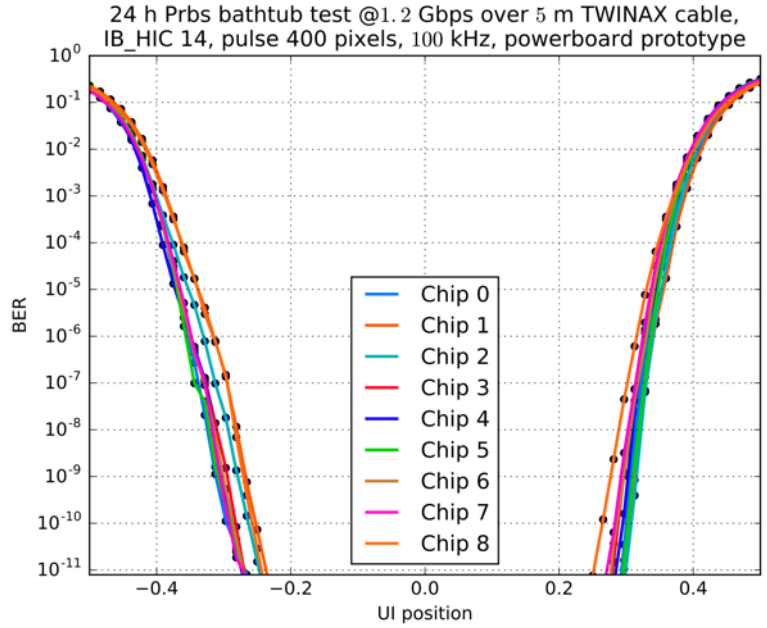
Data Quality

24 h PRBS bathtub tests with full detector slice
Measurement conditions: 100 kHz injections (max. L0 occupancy) and trigger, readout with 600 Mbps (left) and 1.2 Gbps (right)



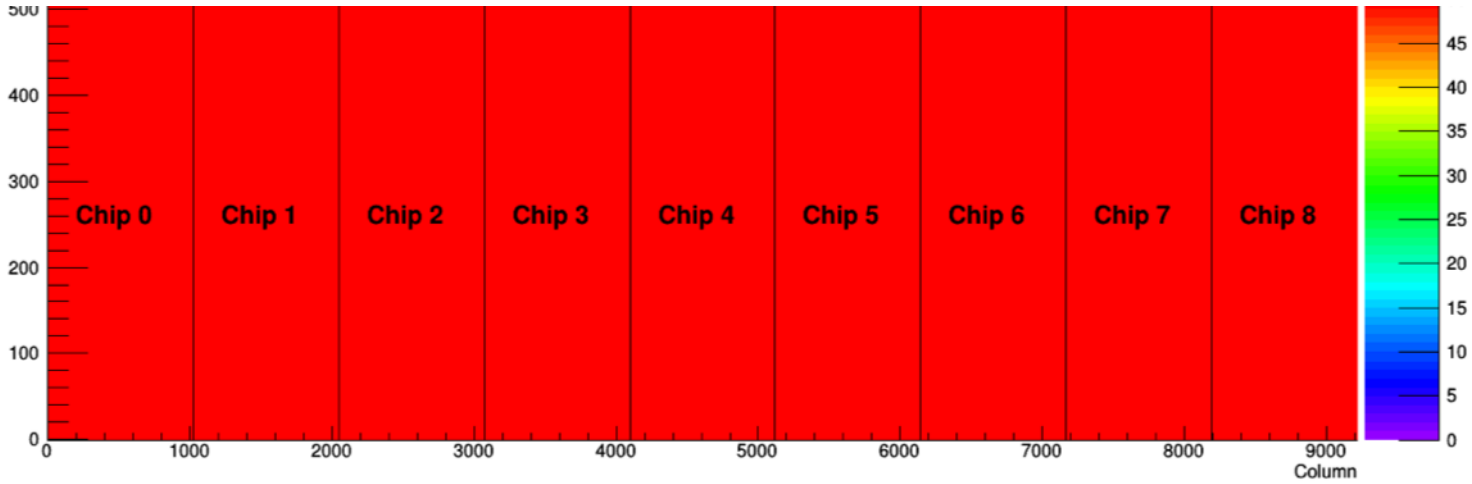


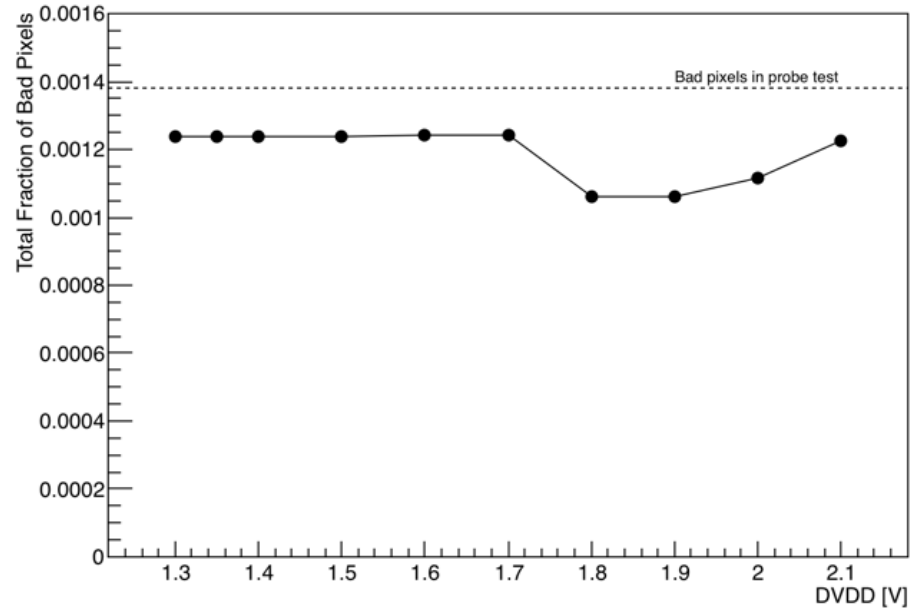
BER (with 99% CL): < 9.87 x 10^{-15} for 600 Mbps and < 4.94 x 10^{-15} for 1.2 Gbps (limited by measurement time)

Readout Stability / Operating Range

Control Communication working for DVDD >= 1.1 V
Data readout working for DVDD >= 1.3 V

Left figure: digital scan @ 1.5 V (lowest set voltage of power board, voltage on HIC: 1.39 V)
Right figure: scan of voltage over broader range with lab power supply
no data corruption over full range, slight change in number of bad pixels (sub-per-mill)





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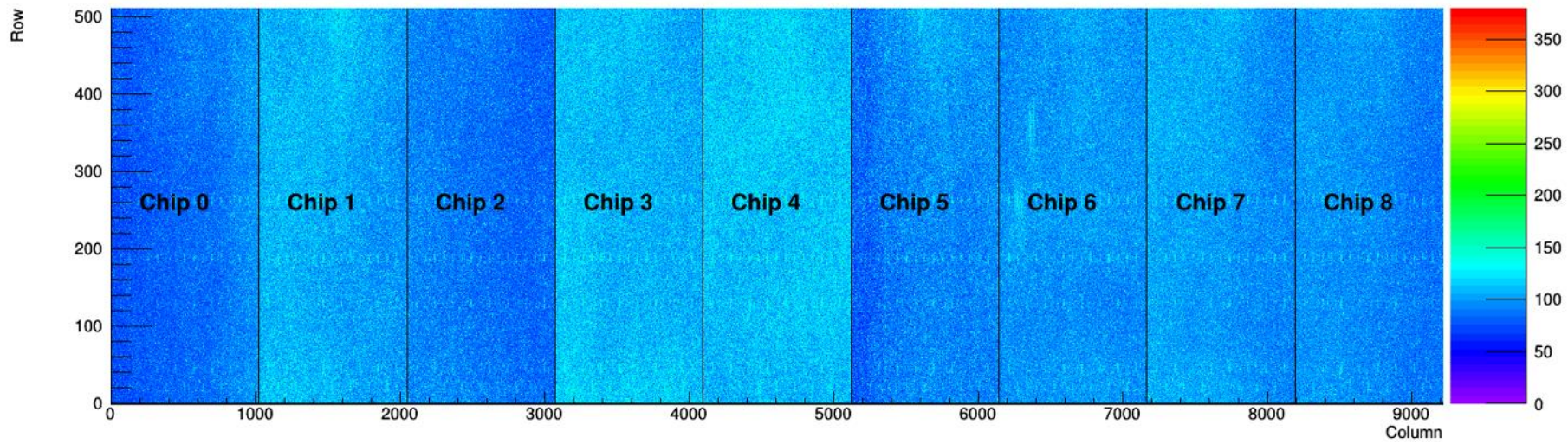
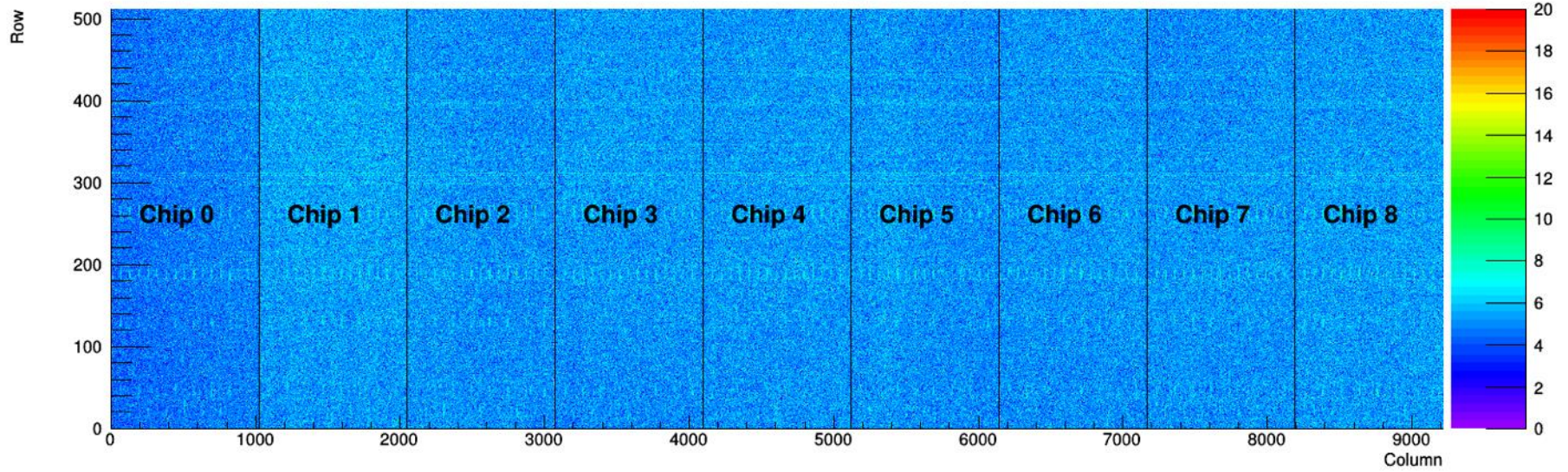
Threshold Scan

Threshold (top) and noise (bottom) measured on HIC 14 (after thermal cycling)

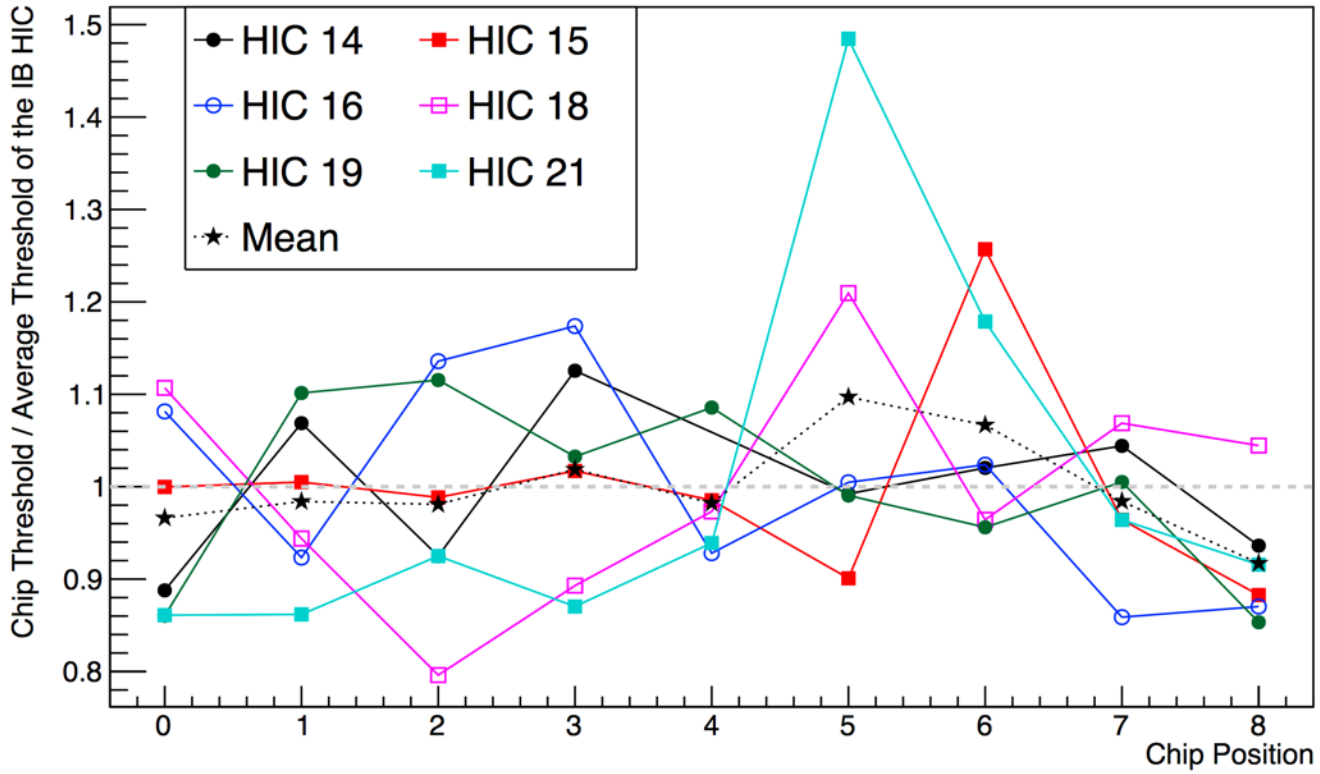




Threshold Variation

Threshold vs. chip position for 5 different HICs (normalised to average of resp. HIC)

- No systematic trend visible, threshold variation dominated by random chip-to-chip variation
- (In either case variation can be adjusted for)

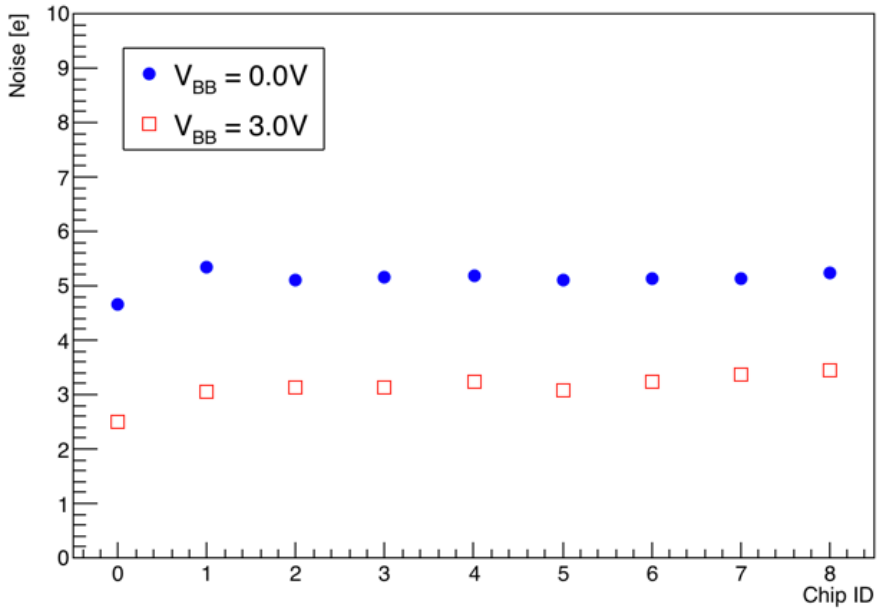


Noise Performance

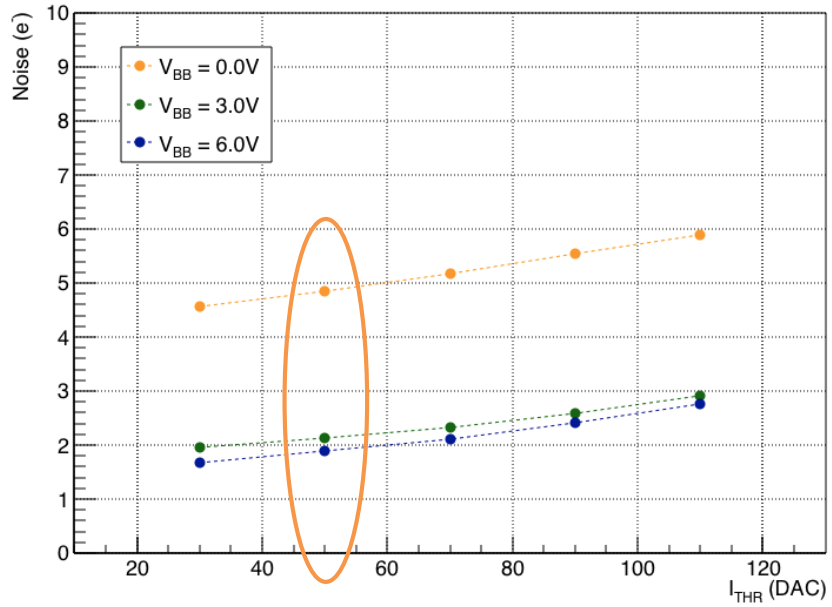
Noise extracted from threshold scan (s-curve fit):

- Measured noise values ~5e without back bias, ~3e with 3 V back bias
- Noise independent on position of chip on HIC
- Noise values in good agreement with values measured on single chip

Avg. noise of chips on HIC as a function of chip position

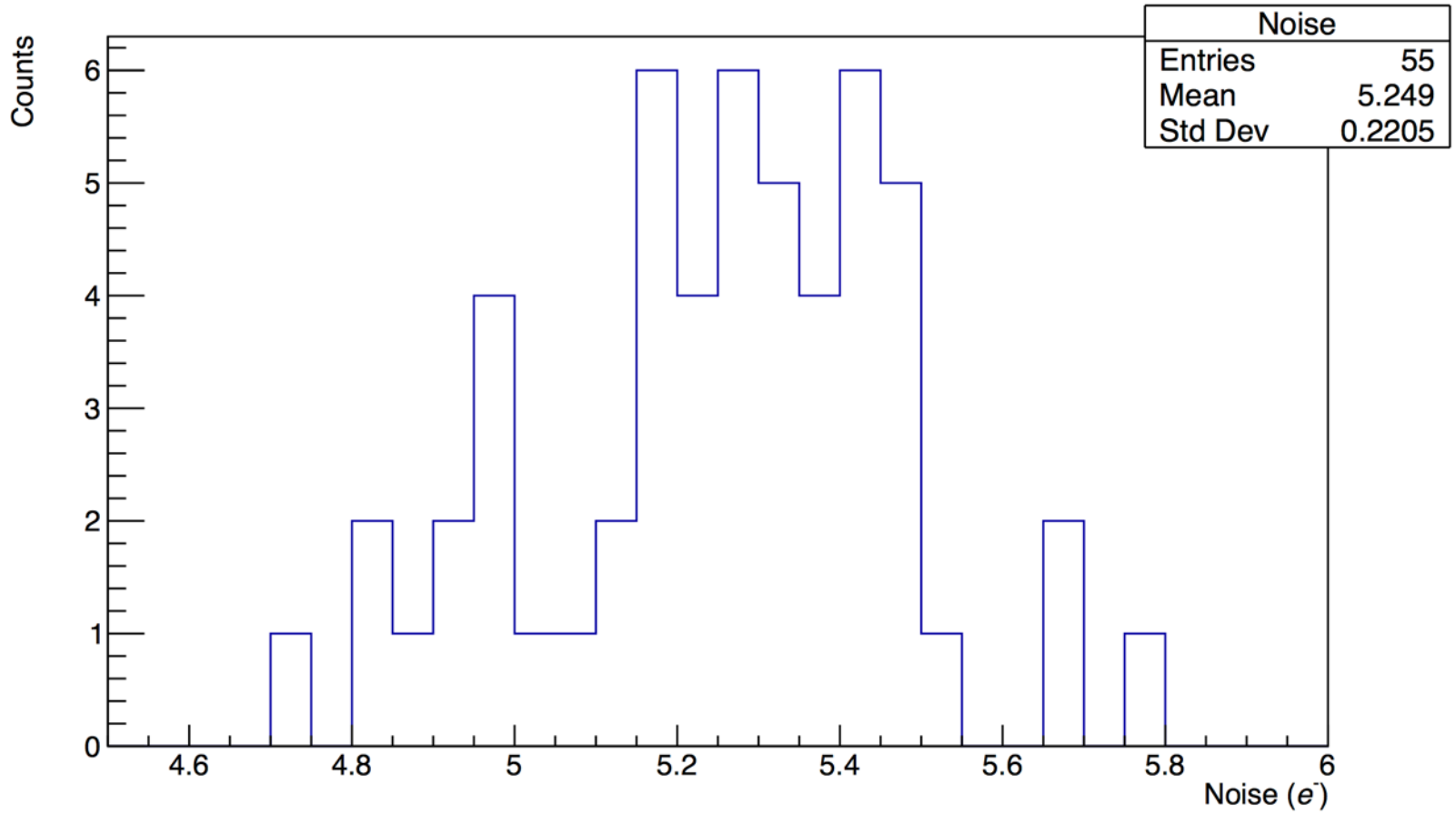


From ALPIDE PRR (for comparison):
Noise of single ALPIDE chips as a function of ITHR



Noise

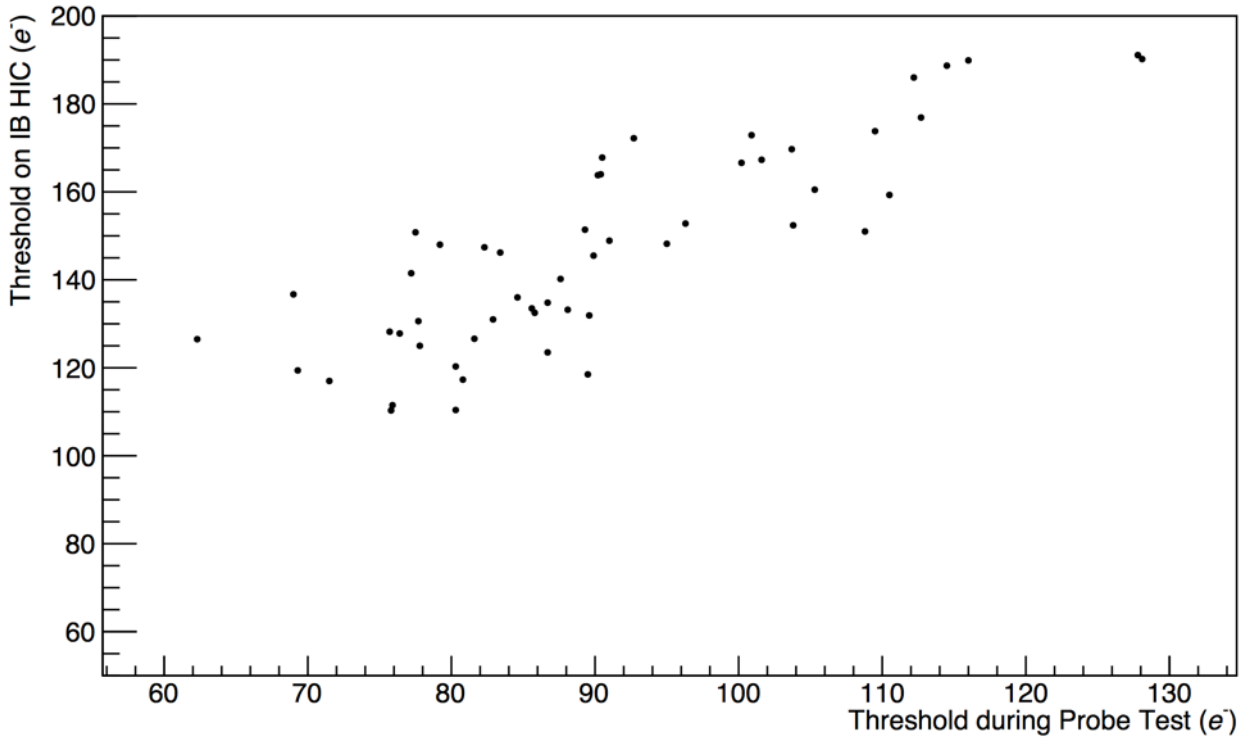
Noise homogeneous over all tested HICs (here: average noise values for the chips of 6 HICs)



Comparison with Chip Tests

Comparison of thresholds (chip average) between probe test and measurement on HIC

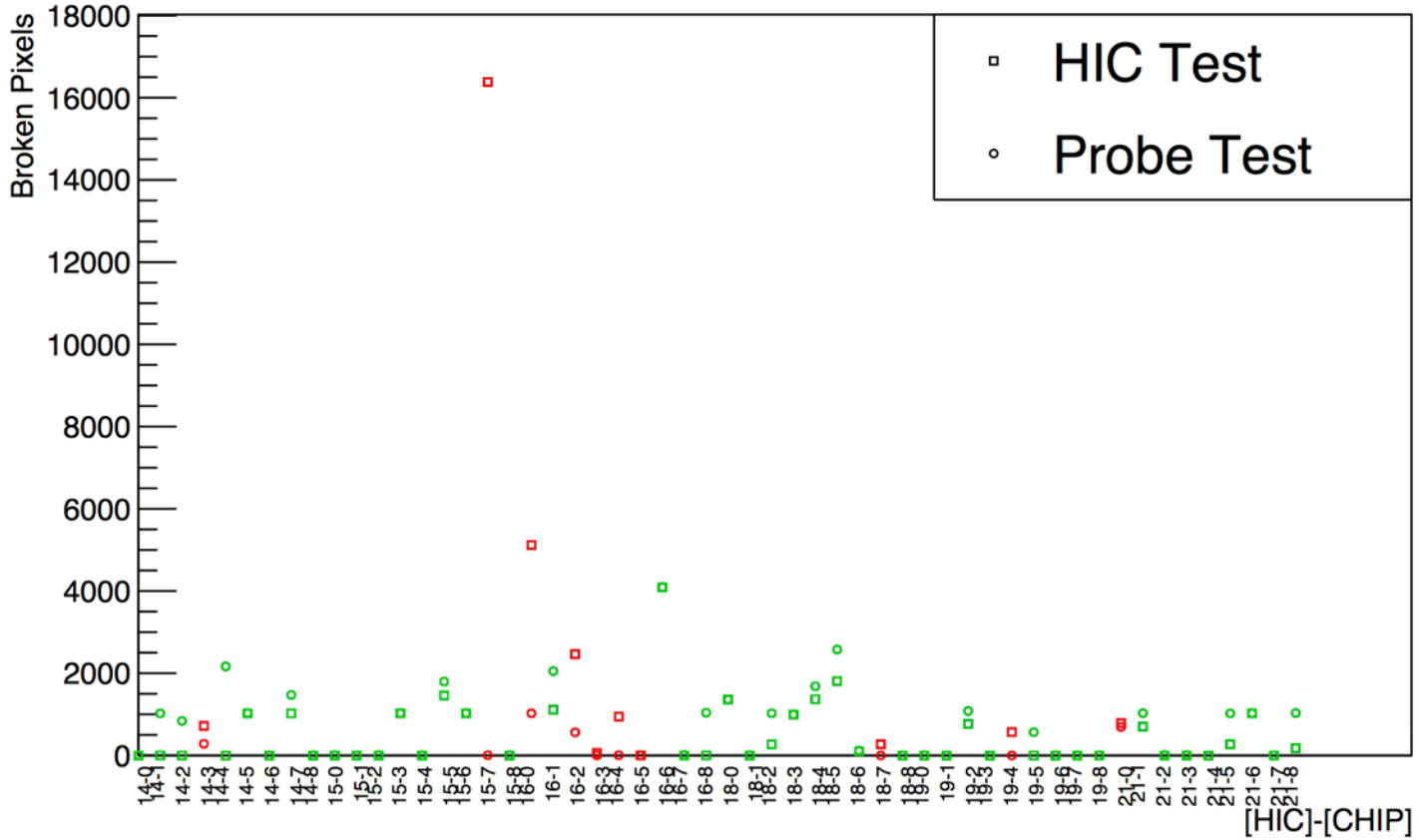
- Absolute value depends on measurement condition, but values clearly correlated



Comparison with Chip Tests

Comparison of number of broken pixels between HIC and Probe tests for all chips of 6 HICs:

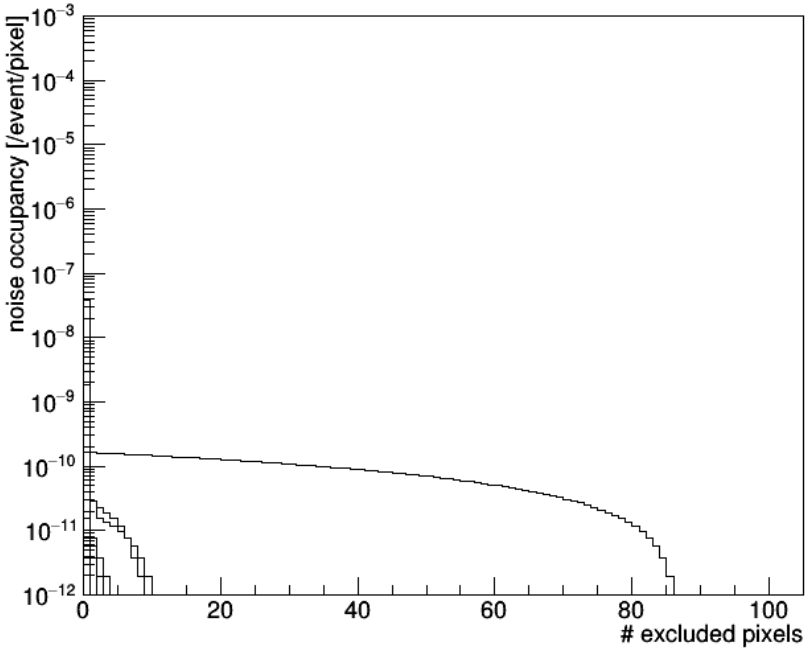
- Green: number of broken pixels for same chip lower on HIC, Red: lower in probe test
- In large majority of cases number is lower on HIC
- In particular, very few instances where number of broken pixels was 0 in probe test, > 0 on HIC

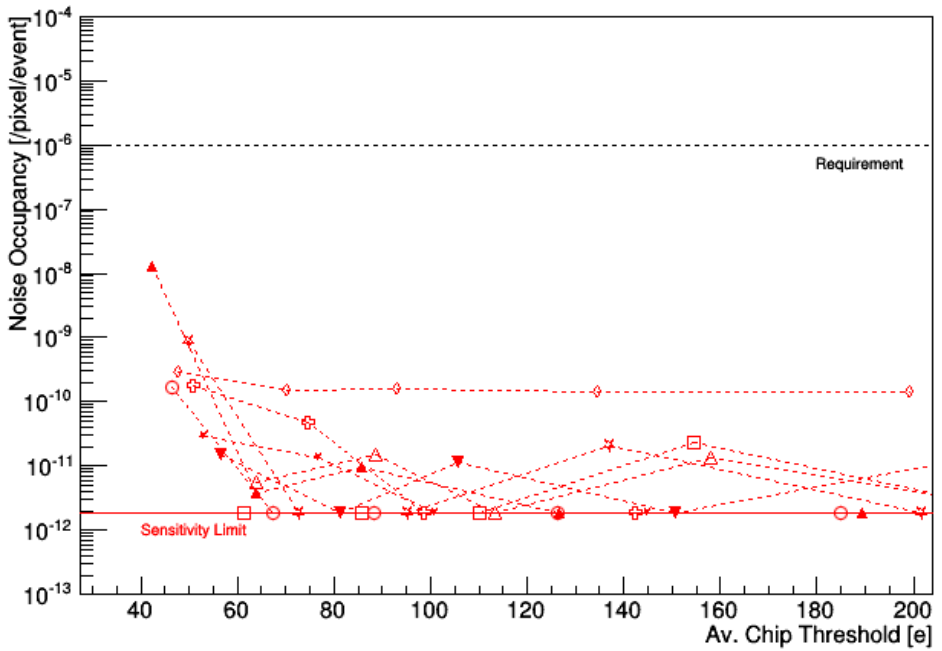


Noise Occupancy

Noise occupancy measured from data taking with random triggers:

- Left plot: noise occupancy as function of masked pixels
  -> in most cases noise concentrated in < 10 noisy pixels
- Right plot: noise occupancy with 5 pixels (i.e. 1/100000) masked as a function of threshold





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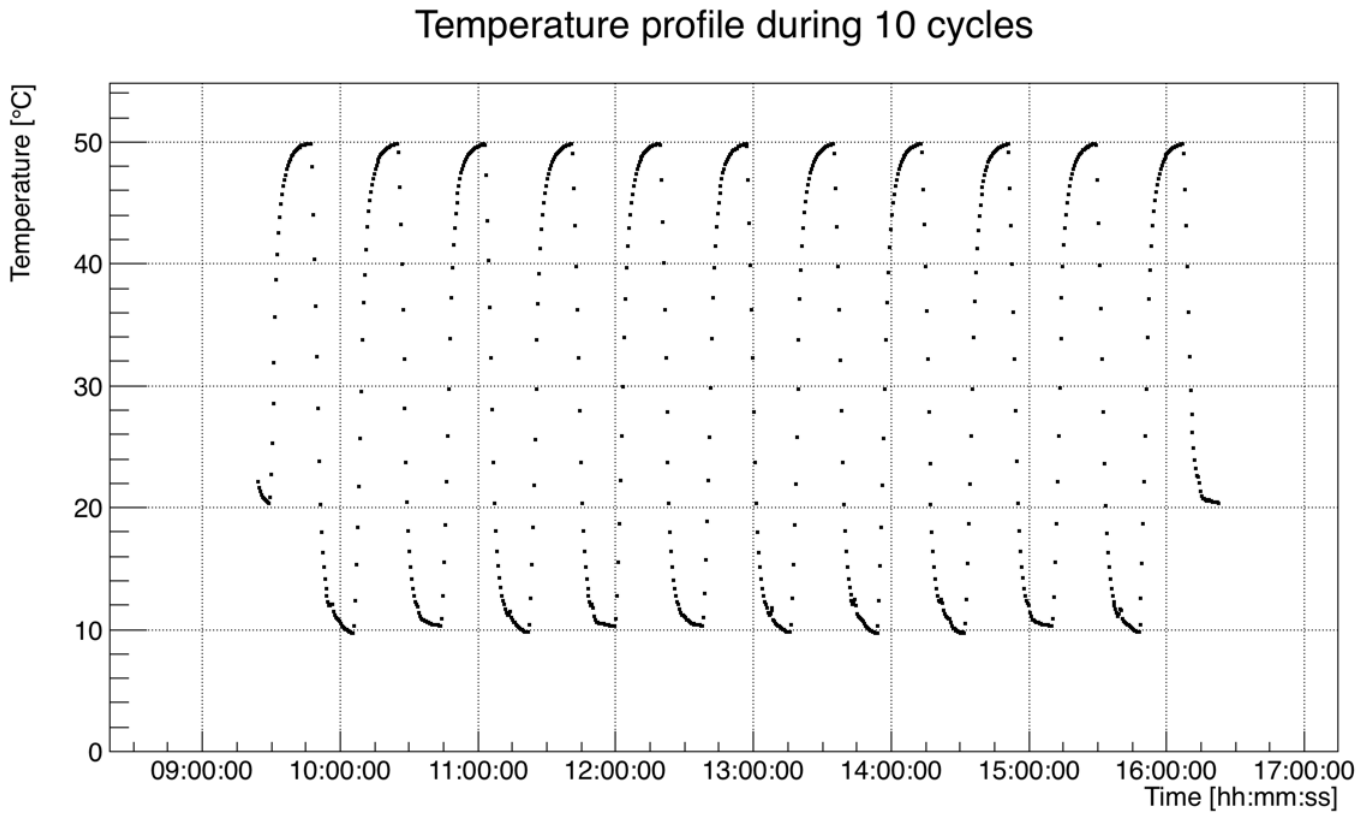
Thermal Cycling

Performed thermal cycling on several devices:

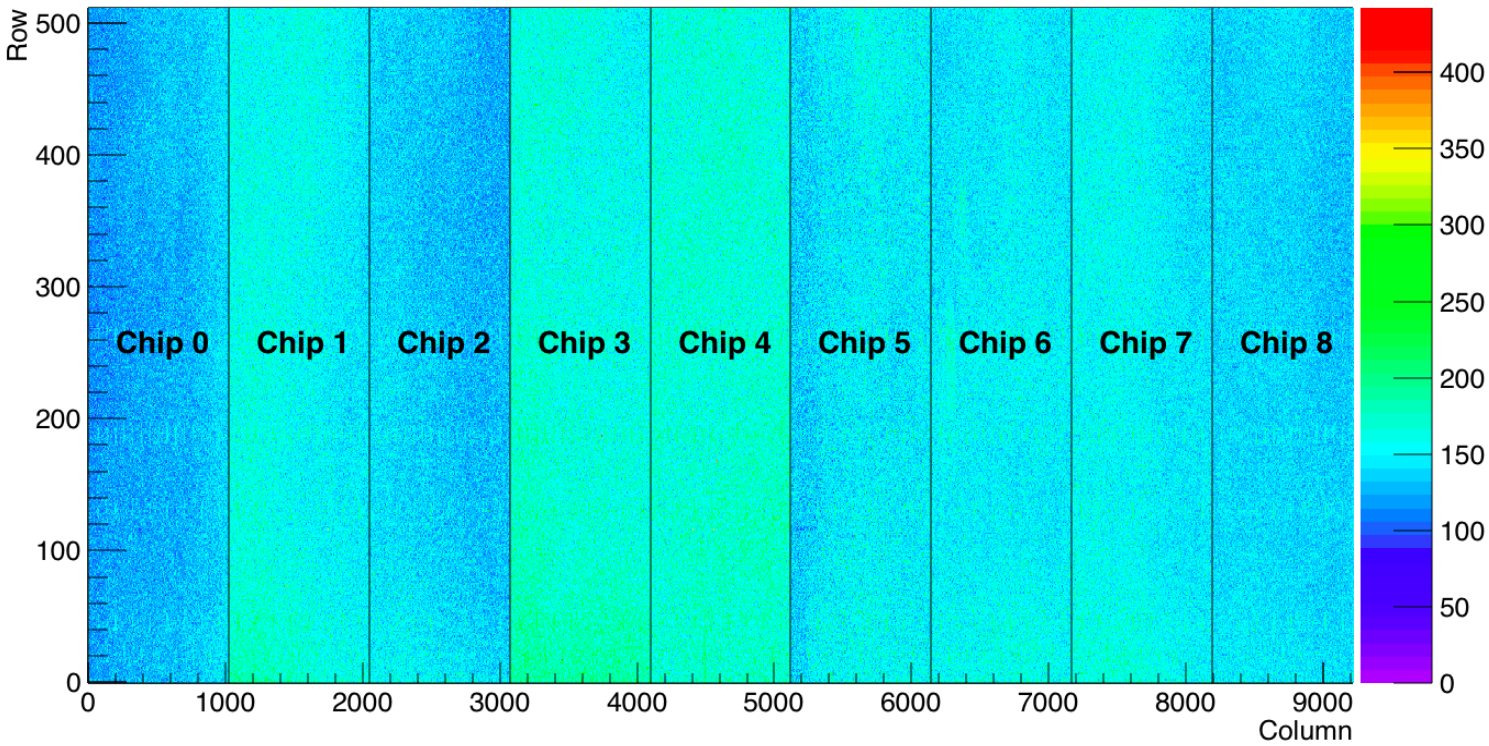
- 300 cycles 10 – 50 deg C (corresponding to 10 years of operation) plus “non-operative” cycles (10-60 deg C)
- Tested devices: 7 HICs (5 complete) and 1 stave (expected to finish Mon, April 24)



Thermal Cycling Results

All devices still working after full number of cycles:

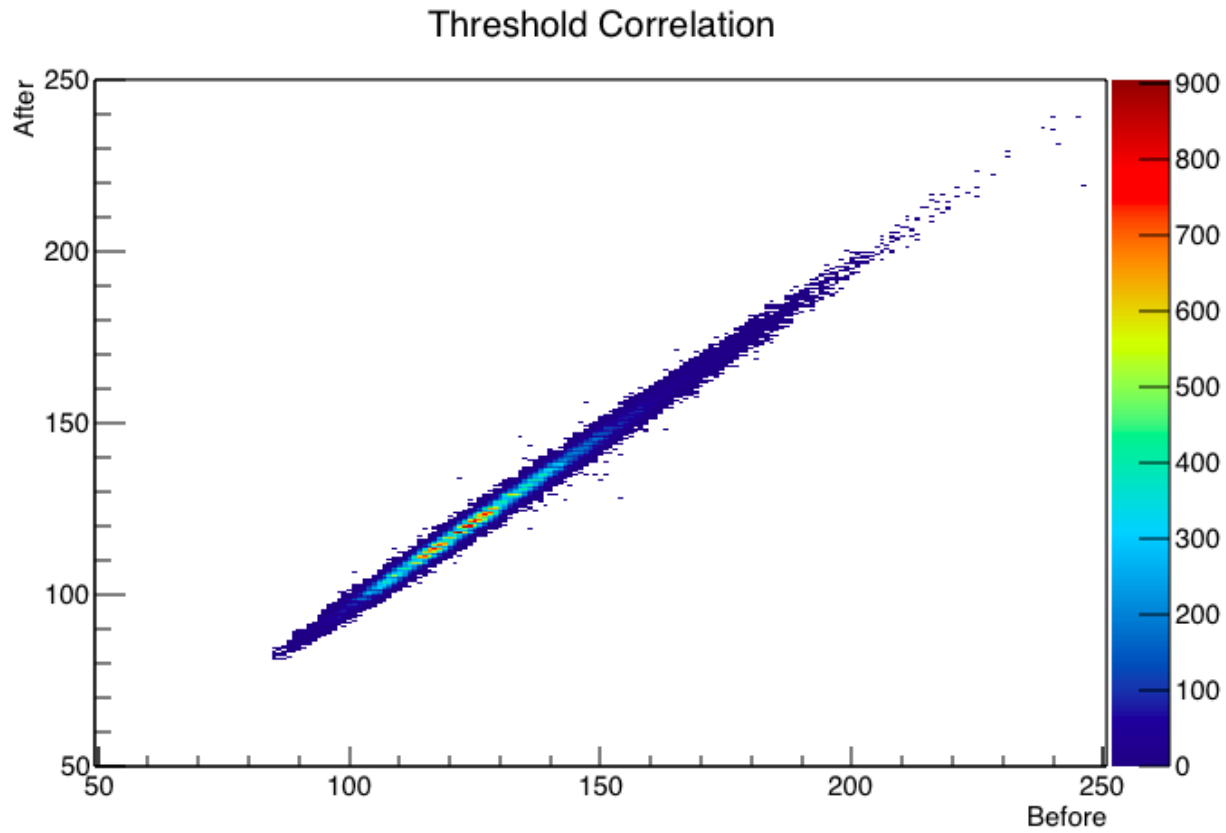
- Visual inspection shows no broken wire bonds
- Functional tests show no or only very minor differences (below: threshold map of HIC after cycling)



Thermal Cycling: Comparison Before – After

Comparison of performance before an after thermal cycling (HIC 14)

Chip	Dead Pixels	
	Before	After
0	0	0
1	1	1
2	0	0
3	678	678
4	1701	1701
5	1022	1022
6	0	0
7	1022	1022
8	0	0



Tests in Magnetic Field

Setup and Procedure:

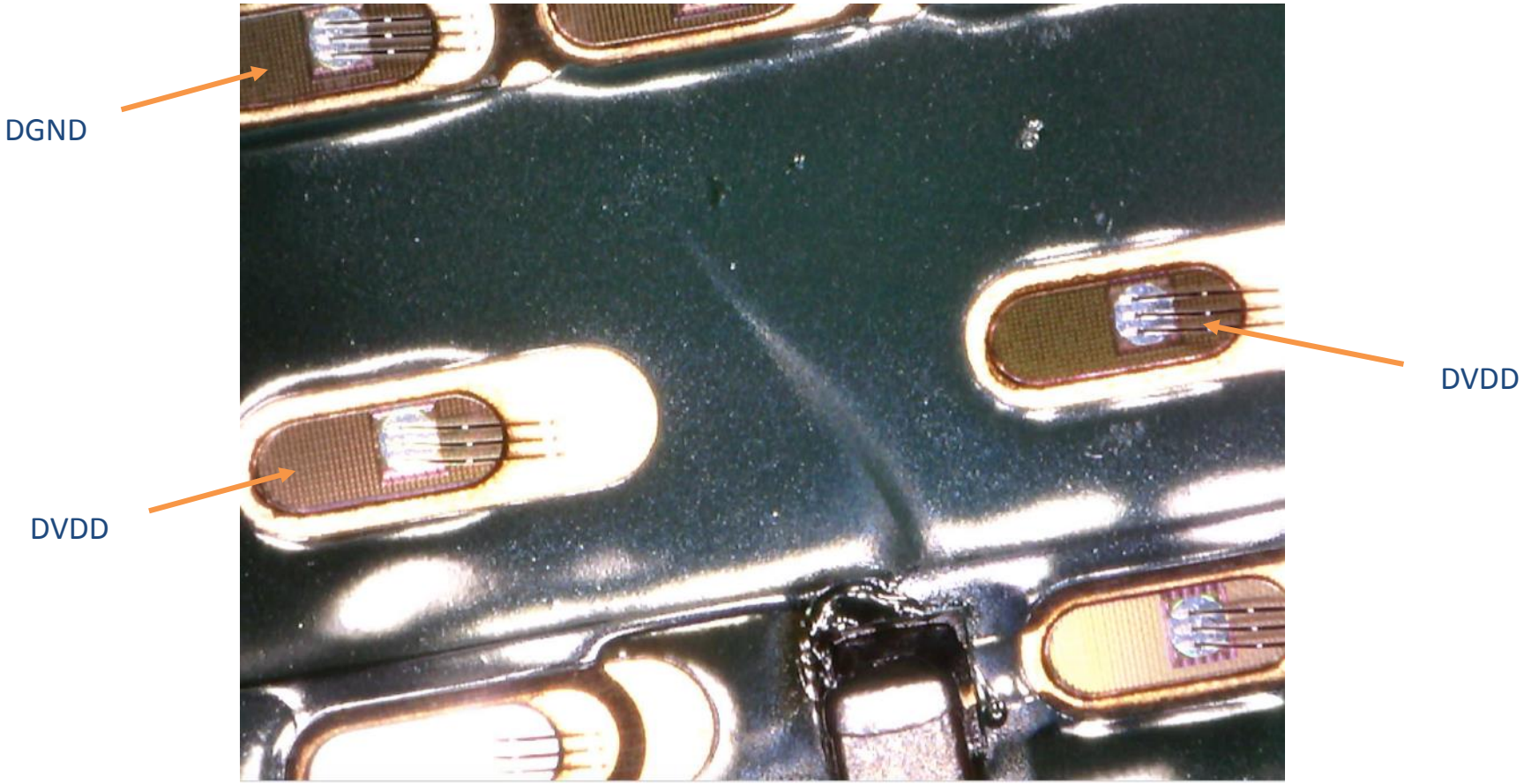
- Chip placed in 0.5 T magnetic field with bond wires parallel to B-field
- Digital injections into 1024 pixels (3 – 4 times max. occupancy expected in L0)
- Scan of trigger frequency between 40 kHz and 400 kHz

Observations:

- Chip kept working throughout (and after) test
- Monitoring of bond wires with USB microscope did not reveal any movement of the bond wires (next slide)

Tests in Magnetic Field

Microscope picture of bond wires (digital supply) during magnetic field test



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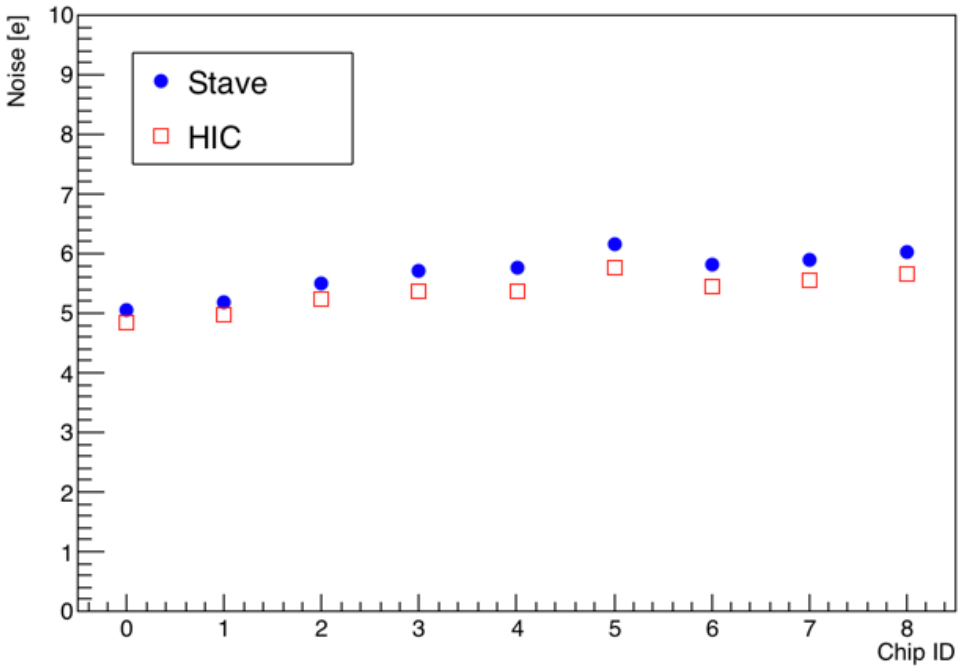
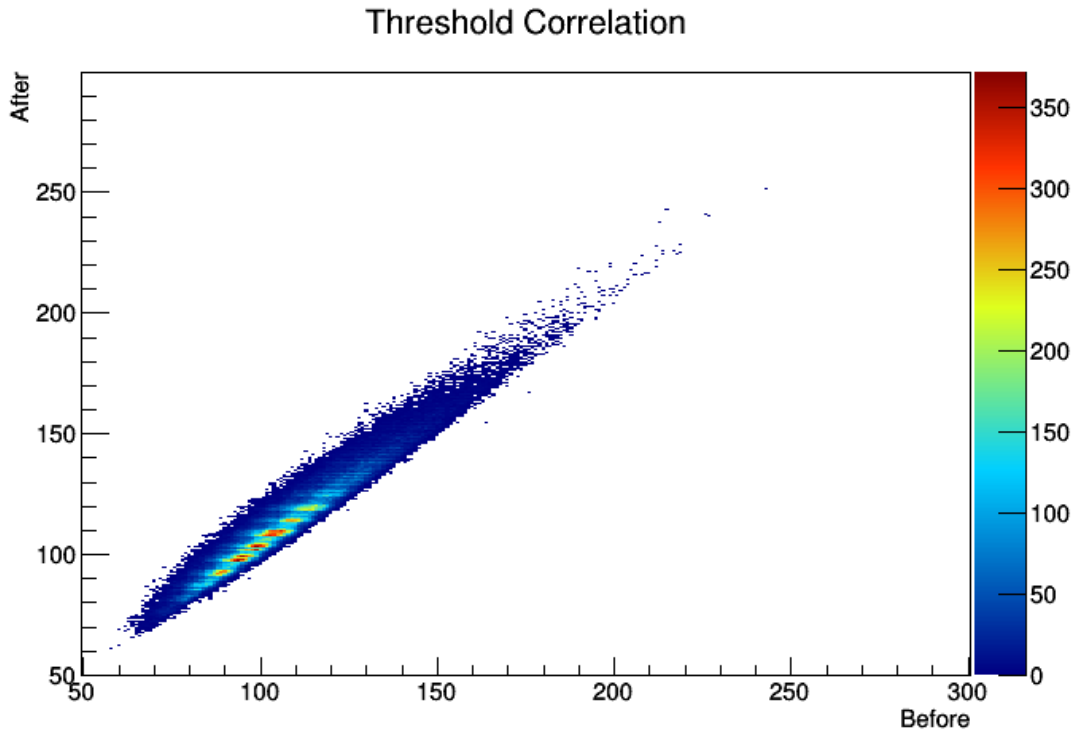
Stave Tests

The same functional characterisation has been performed for HICs and staves; no difference in performance has been observed. Below: comparison for a HIC before and after mounting on a stave

- Left: Comparison of noise per chip
- Right: Correlation of thresholds



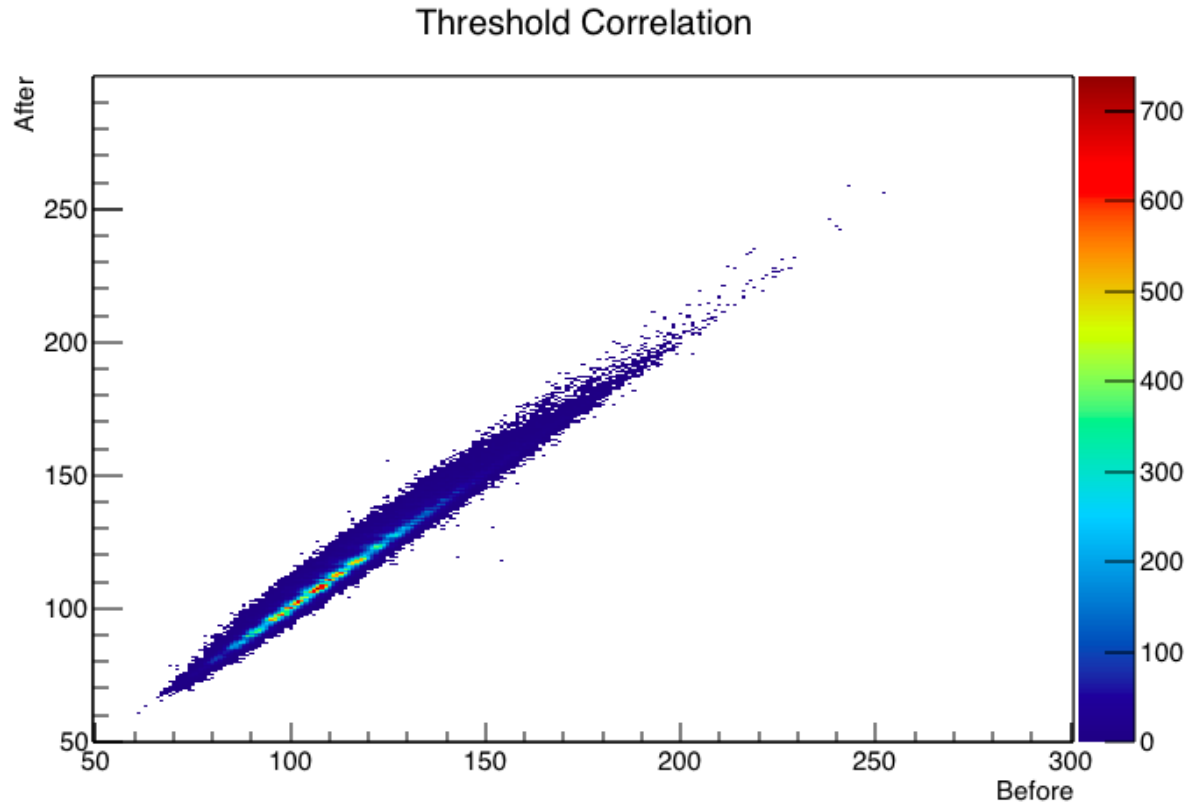


Thermal Cycling: Comparison Before – After

Comparison of performance of an IB stave before an after thermal cycling (Stave 02)

New Slide
(added after completion of thermal cycles)

Chip	Dead Pixels	
	Before	After
0	553	552
1	700	700
2	0	0
3	0	0
4	0	0
5	263	264
6	1024	1024
7	1	1
8	176	176



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