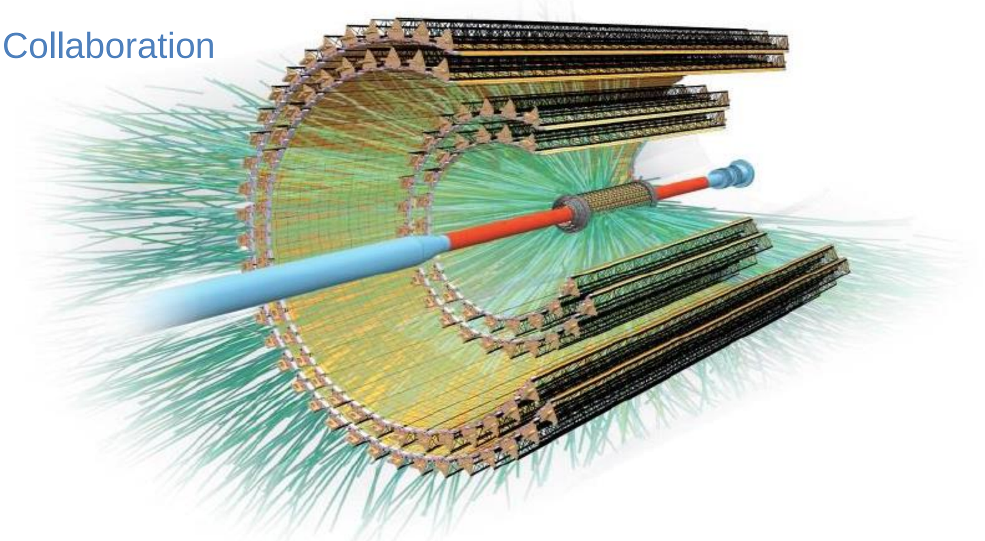
A Large Ion Collider Experiment

The new Inner Tracking System of the ALICE experiment

Paolo Martinengo – CERN

on behalf of the ALICE Collaboration

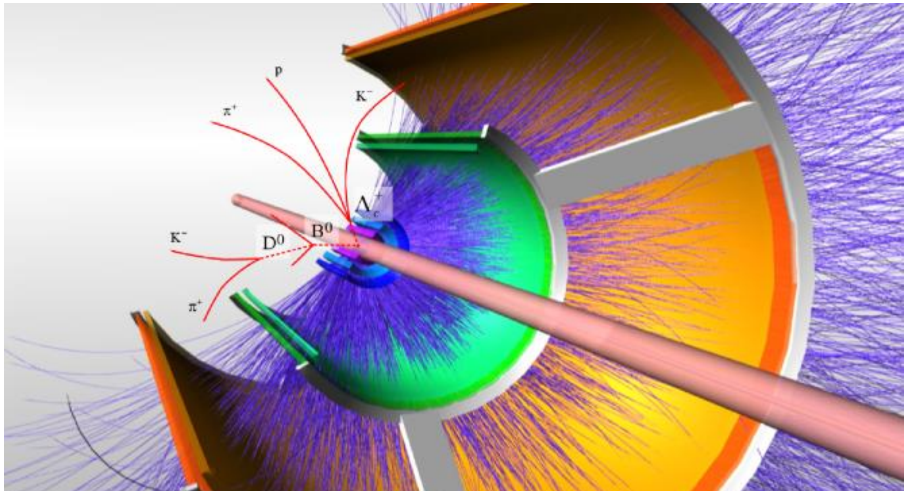


Chicago, 7-11 February 2017

The new ALICE Inner Tracking System

OUTLINE

- Motivations and Experimental Strategy
- Design Objectives and Layout
- Selected topics from the R&D
- Construction and Integration Schedule
- Conclusions



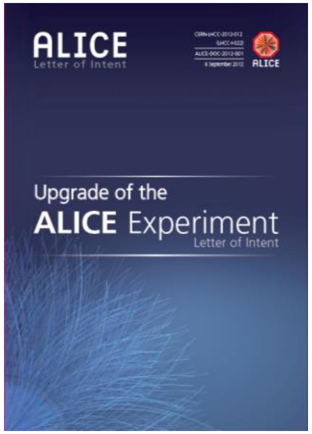
Sketch of the ITS upgrade with half a Pb-Pb event superimposed

ALICE Upgrade – From observation to precision measurement

In March 2013 a new physics programme for ALICE was approved

Physics Goal ➔ high-precision measurements of QGP properties

- Open HF (charm & beauty, mesons & baryons), Quarkonia down to zero p_T
  - thermalisation, hadronization, recombination, temperature evolution of the QGP
- Vector mesons and low-mass di-leptons
  - chiral symmetry restoration, virtual thermal photons
- High-precision measurement of light (anti-)nuclei and hyper-nuclei
  - nucleosynthesis, exotics
- and more



ALICE Upgrade LoI
March 2013

ALICE Upgrade – From observation to precision measurement

Main requirements for the new Inner Tracking System:

- High tracking efficiency and resolution at low p_T (60% @ 100 MeV/c)

  Increase granularity, reduce material thickness

- Excellent secondary vertex resolution (Λ_c $c\tau \sim 60\ \mu$m)

  Move closer to Interaction Point (IP), new beam pipe, smaller diameter

- High-statistics, un-triggered data sample (>10 nb^{-1} Pb-Pb)

  Increase readout rate, reduce data size (online data reduction)

ITS Upgrade TDR March 2014

New ITS Design Objectives

1. Improve impact parameter resolution by a factor of 3 (5) in rφ (z) @ p_T = 500 MeV/c

- Get closer to IP (position of first layer): 39 mm ➡ 23 mm
- Reduce x/X_0 /layer: ~1.14% ➡ ~ 0.3% (for the 3 innermost layers)
- Spatial resolution: currently 12 μm x 100 μm (SPD) ➡ 5 μm x 5 μm

2. Improve tracking efficiency and p_T resolution at low p_T

- Increase granularity:
  - 6 layers ➡ 7 layers
  - silicon pixel, drift and strip ➡ all-pixels

3. Exploit LHC luminosity increase ➡ fast readout

- readout Pb-Pb interactions up to 100 kHz, i.e. 2 x expected peak luminosity after LS2 (currently limited at 1kHz)

4. Withstand radiation load (10 years operation):

- TID: ~ 270 krad, NIEL: ~1.7×10^{12} 1MeV n_{eq} / cm^2

5. Reliability ➡ fast insertion/removal for yearly maintenance

- possibility to access faulty components during yearly shutdown

➡ Services (power, cooling, R/O) connected only on one side

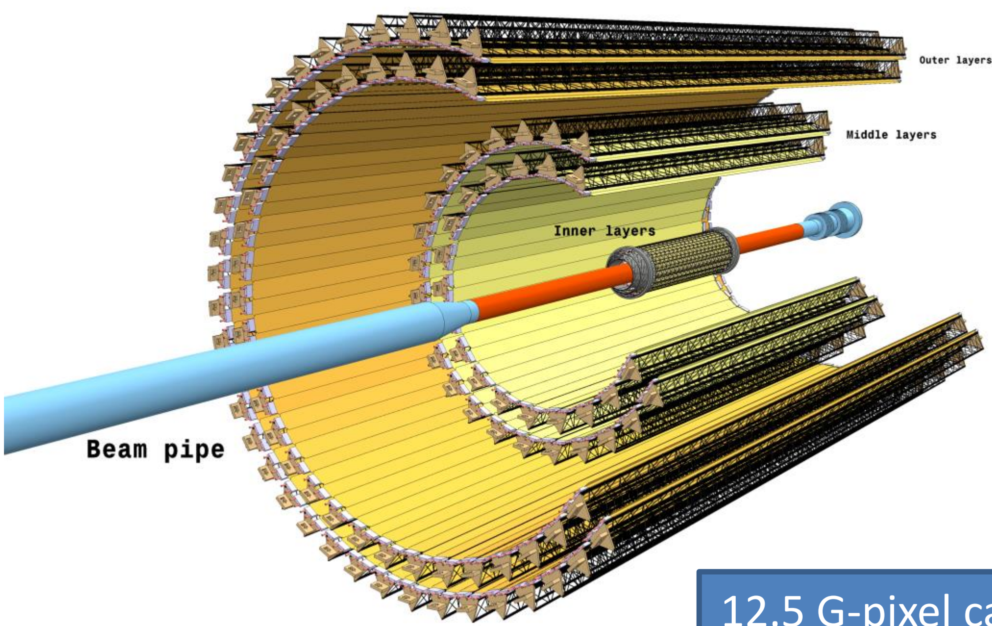
Layout of the new ITS

7-layer barrel geometry,
fully equipped (~24000 chips) with dedicated **MAPS:**

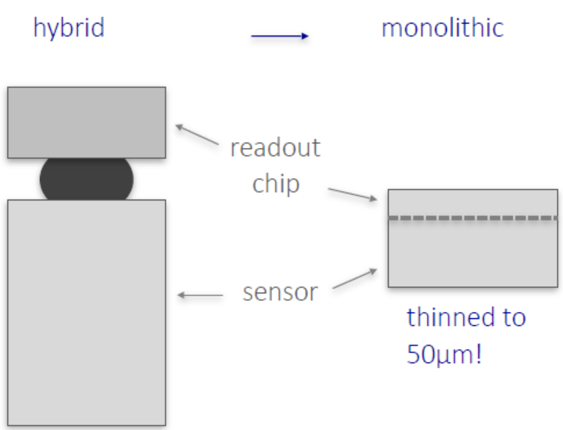
ALice PIxel DEtector (ALPIDE)

r-coverage: 23 – 400 mm

η coverage: $|\eta| \leq 1.3$



Monolithic Active Pixel Sensors



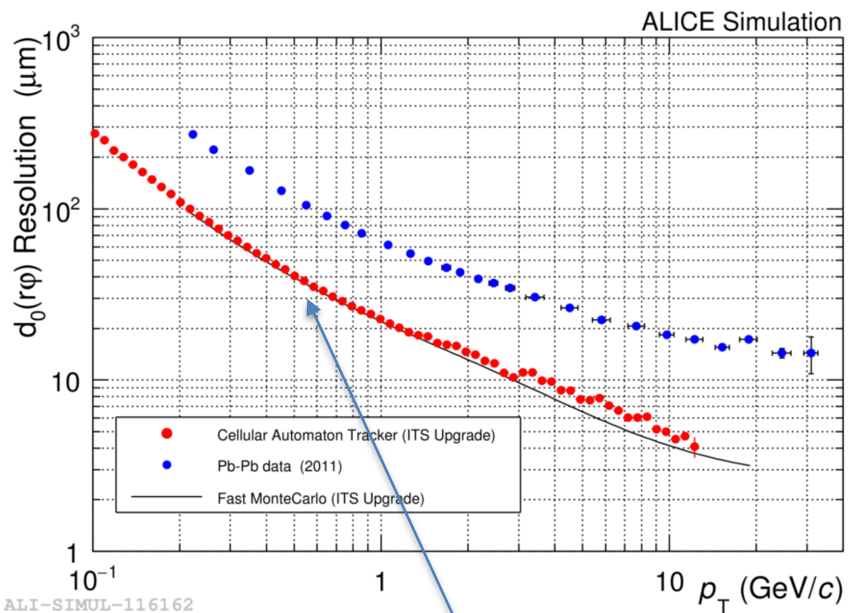
Material /layer : 0.3% X_0 (IB), 1% X_0 (OB)

12.5 G-pixel camera
(~10 m^2 active Si)
Binary read-out

Performance of new ITS (MC simulations)

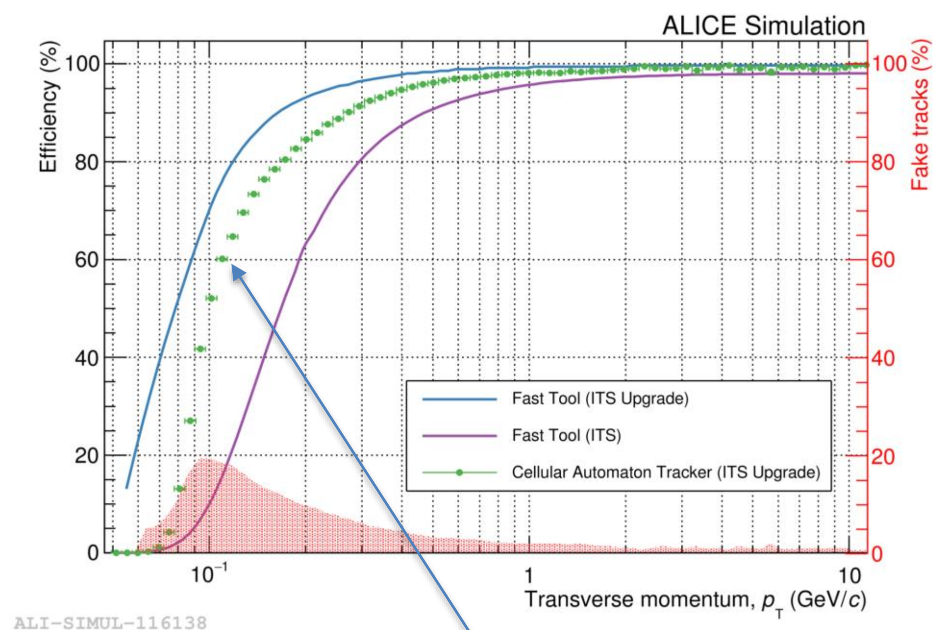
Cellular automaton ➡ poster by Maximiliano Puccio

Impact parameter resolution



40 μm at p_T = 500 MeV/c

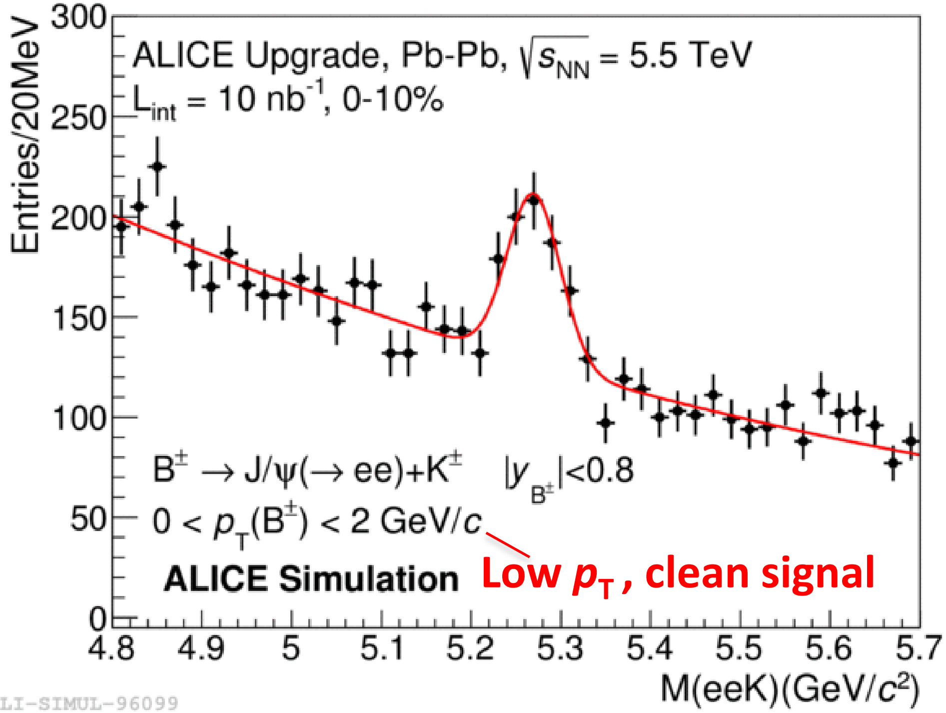
Tracking efficiency (ITS standalone)

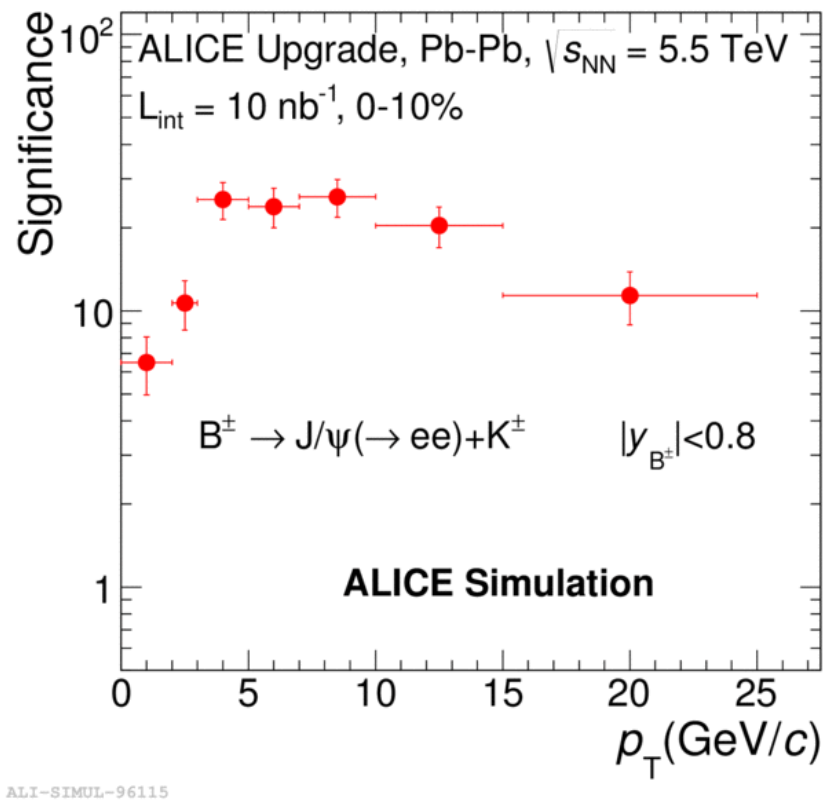


~60% at p_T = 100 MeV/c

Physics performance with the new ITS (MonteCarlo)

$B^{\pm}$ not accessible with the present ITS



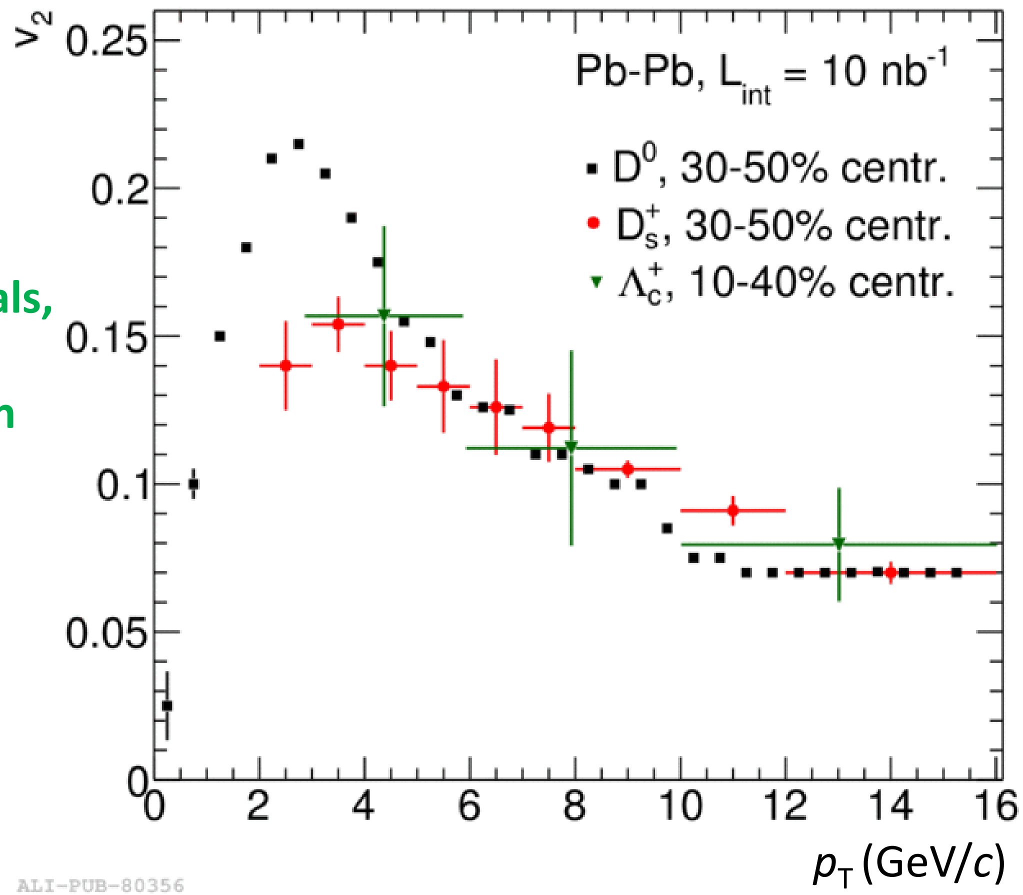


Measure energy loss for b,
quantitative verification of $\Delta E_c > \Delta E_b$ vs. p_T

Physics performance with the new ITS (MonteCarlo)

Λ_C not accessible (in Pb-Pb) with the present ITS
v_2 measurement possible with the new one

Large improvement also for D^0 & D_S signals, possibility to discriminate between thermal and coalescence hadronization models



R&D

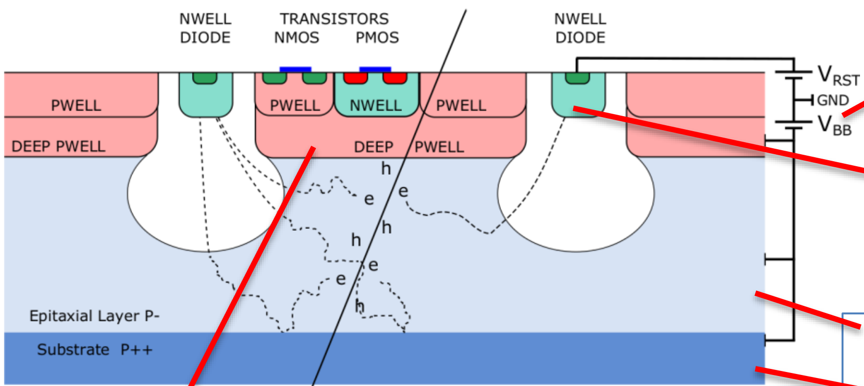
Huge R&D effort started 6 years ago

- Simulation
- Pixel sensor, connectivity
- Cooling, power distribution
- Read-out chain
- Assembly tools & procedure
- Construction database
- Mechanical support (carbon fiber)
- Integration in ALICE
- and more

First prototype usually does not meet all requirements

ALPIDE – Technology and Pixel Layout

Pixel Sensor using TowerJazz 0.18 μm CMOS Imaging Process



Reverse bias voltage (-6 V < V_{BB} < 0 V) to substrate (contact from the top) to increase depletion zone around NWELL collection diode

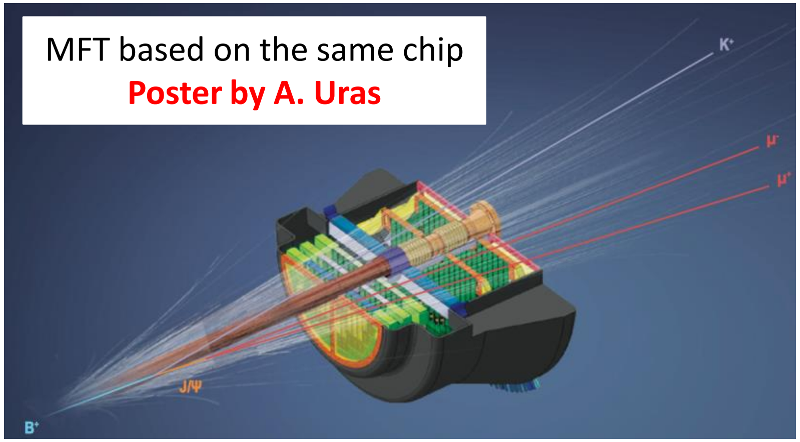
Small n-well diode (2 μm diameter), ~100 times smaller than pixel => low capacitance (~fF)

High-resistivity (> 1 kΩ cm) p-type epitaxial layer (25 μm) on p-type substrate

Deep PWELL shields NWELL of PMOS transistors (full CMOS circuitry within pixel active area)

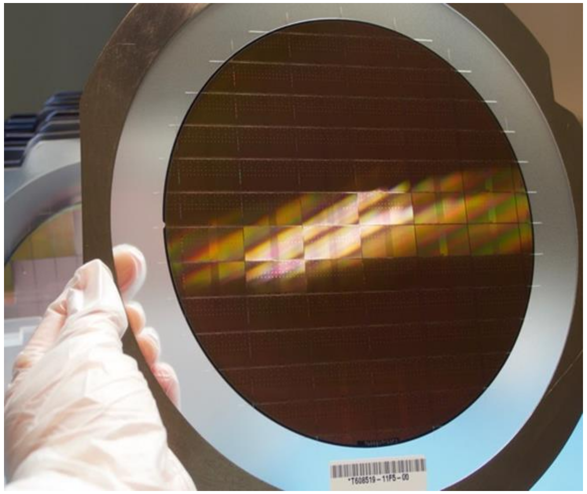
In-pixel:

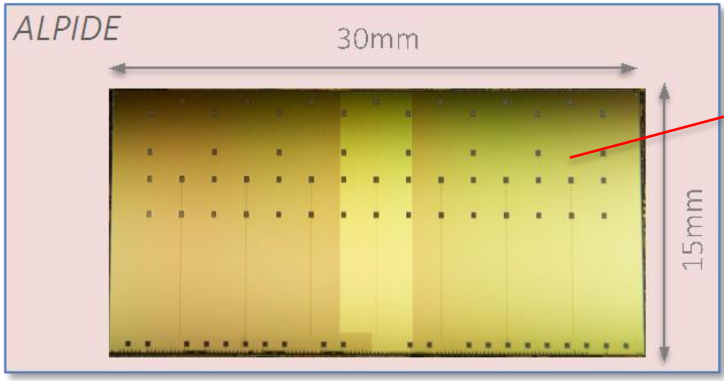
- Amplification
- Discrimination
- 3-hit storage register (MEB)
- In-matrix sparsification



ALPIDE – Final Version

Production started Dec 2016, to be completed by Dec 2017





Pad-over-matrix

Inner Barrel: 50 μm thick
Outer Barrel: 100 μm thick

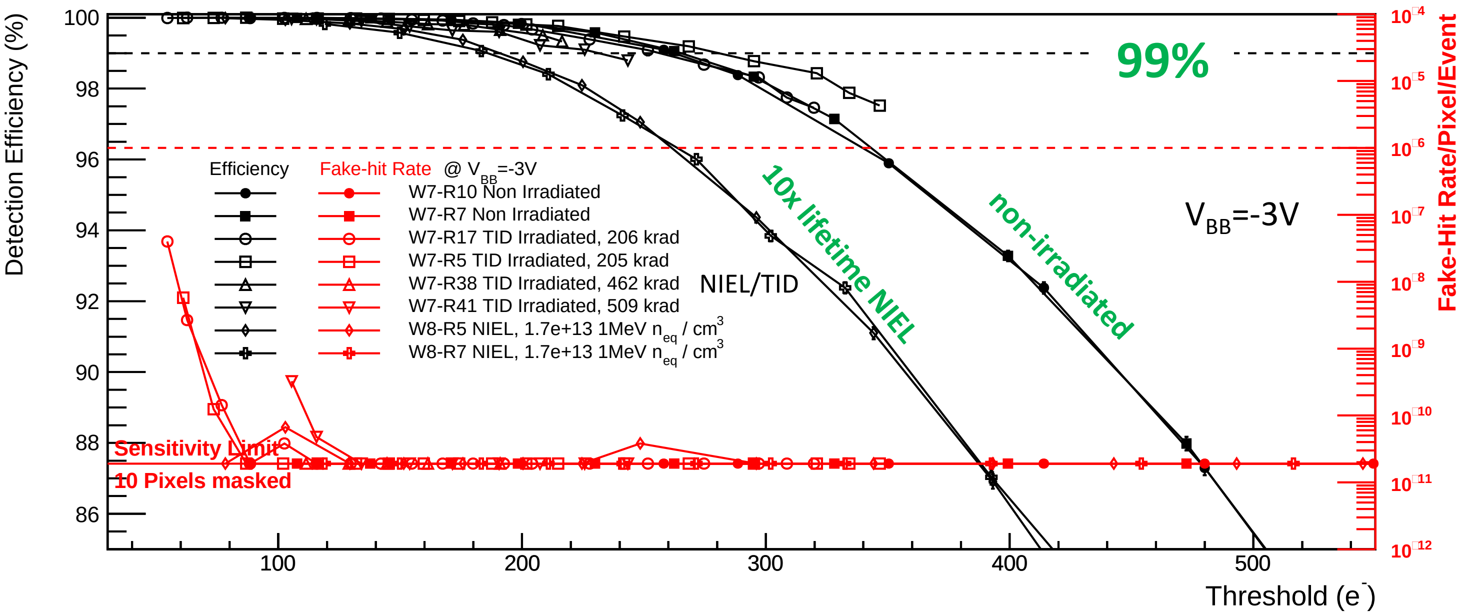
High speed serial data output (HSO)

- OB: 400 Mbit/s
- IB: 600 Mbit/s or 1.2 Gbit/s

Key features:

- Dimensions: 30 mm x 15 mm
- Pixel pitch: 29 μm x 27 μm
- Ultra-low power (entire chip): ~40 mW/cm^2, (requirement < 100 mW/cm^2) 140 mW full chip
- Triggered acquisition (200 kHz Pb-Pb, 1 MHz pp) or continuous (progr. integration time: 1μs - ∞)

ALPIDE – Detection Efficiency and Fake-Hit Rate

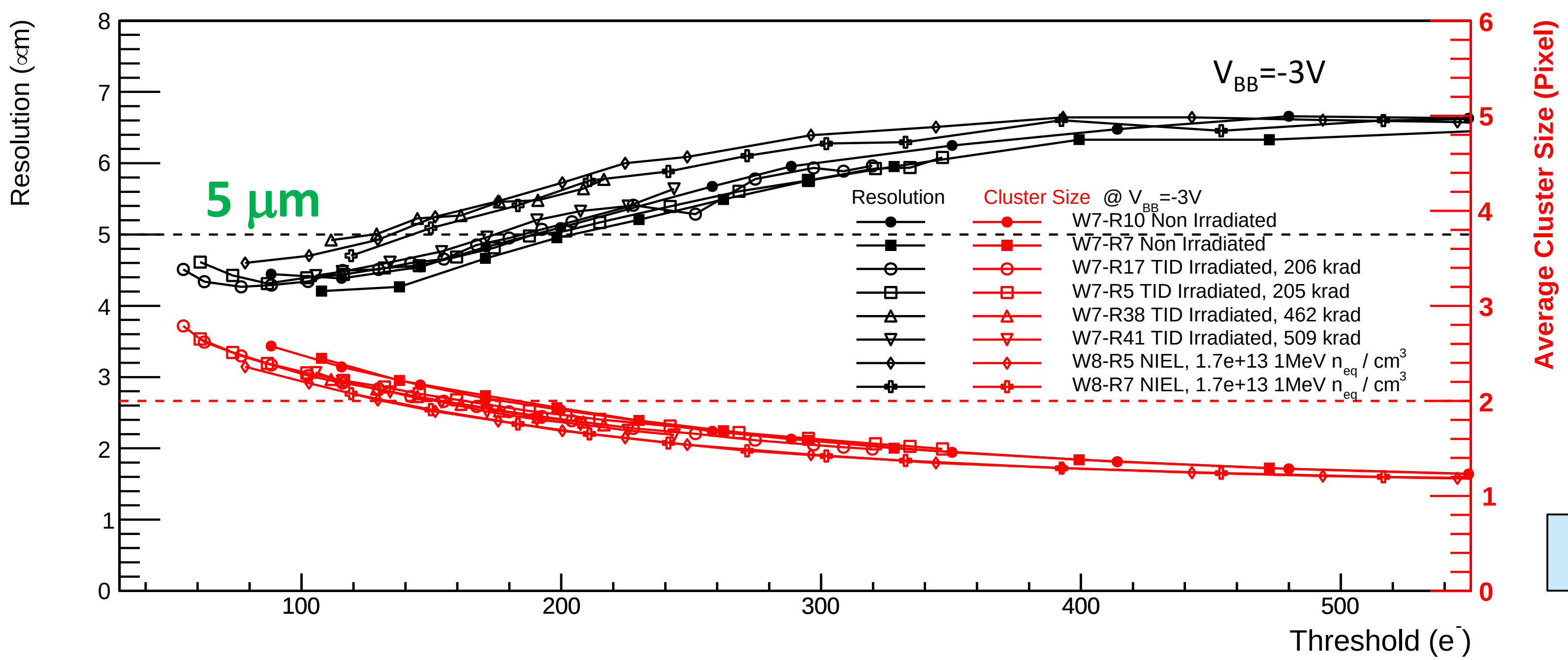


6 GeV/c π^-

- Big operational margin with only 10 masked pixels (0.002%), fake-hit rate < 10^{-10} pixel/event (requirement 10^{-6})
- Chip-to-chip fluctuations negligible
- Non-irradiated and NIEL/TID chips show similar performance
- Sufficient operational margin after 10x lifetime NIEL dose

Availability and excellent support from test beam facilities all around the world **(BTF Frascati, CERN, DESY, Pohang/Korea, SLRI/Thailand)** has been a key factor for the success of the development of the chip

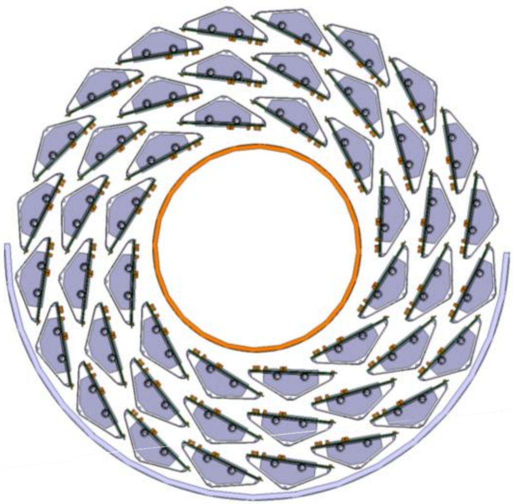
ALPIDE – Resolution and cluster size

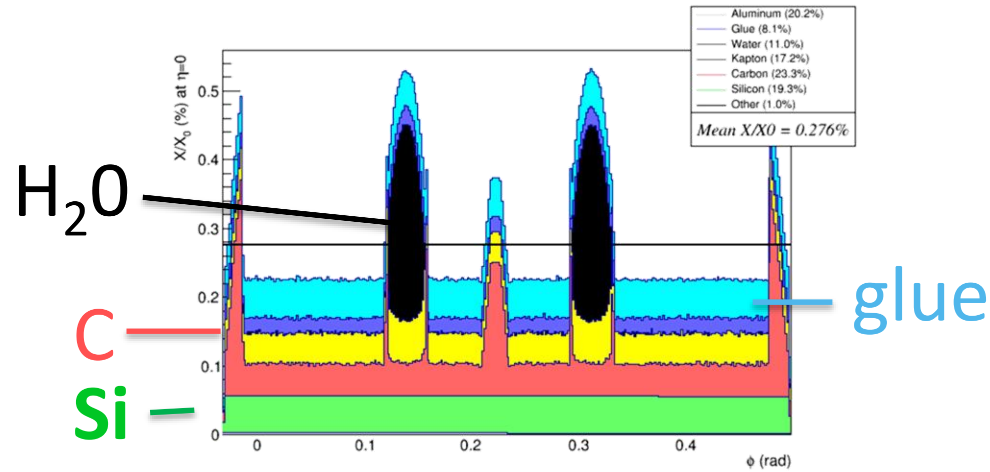


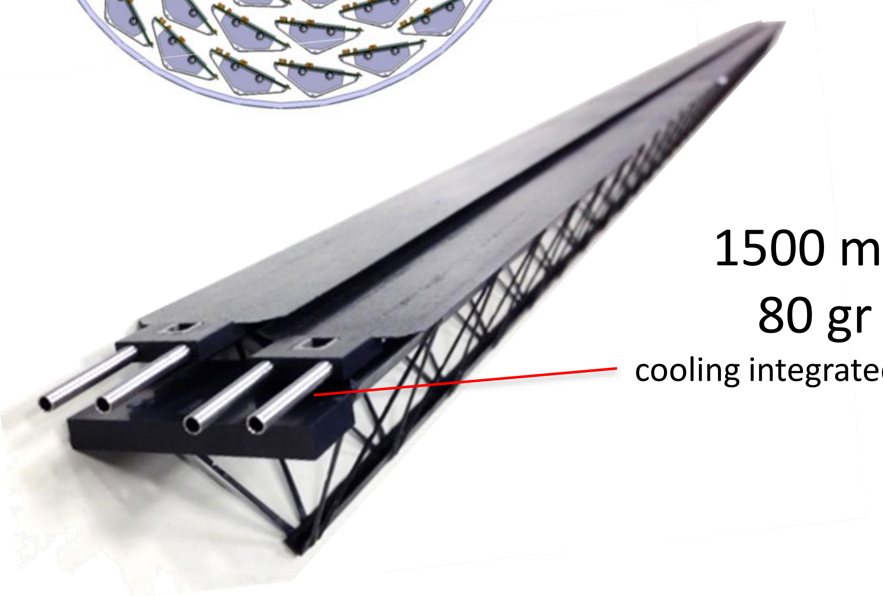
6 GeV/c π^-

- Chip-to-chip fluctuations negligible
- Non-irradiated and TID/NIEL chips show similar performance
- Resolution of about 5μm at a threshold of 200 electrons
- Sufficient operational margin even after 10x lifetime NIEL dose

Detector Barrel Staves



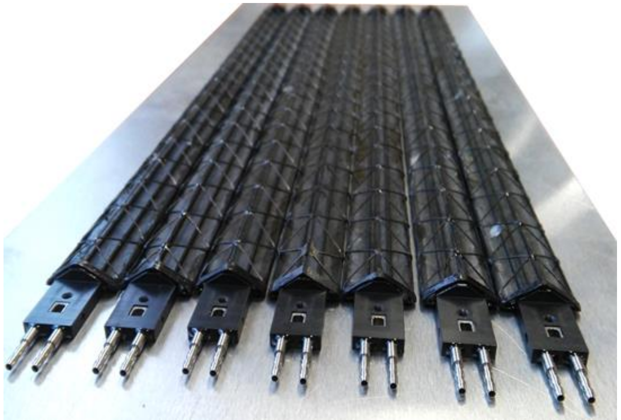




1500 mm length

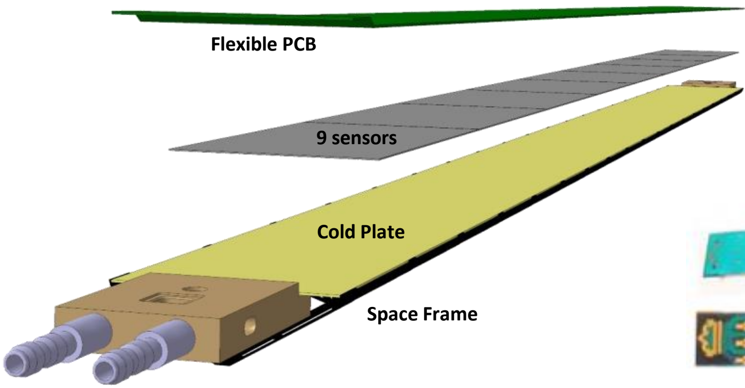
80 gr weight

cooling integrated in C fiber support

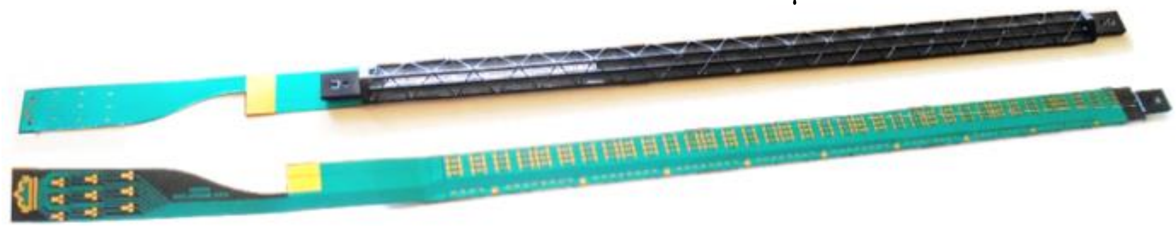


Stave Layout

Inner Barrel

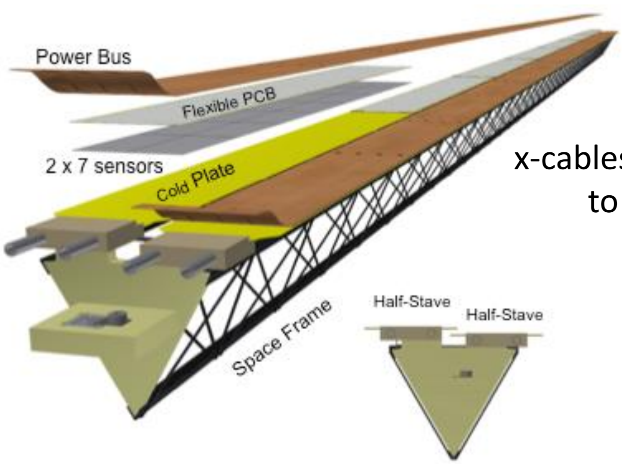


sensors thinned to 50µm

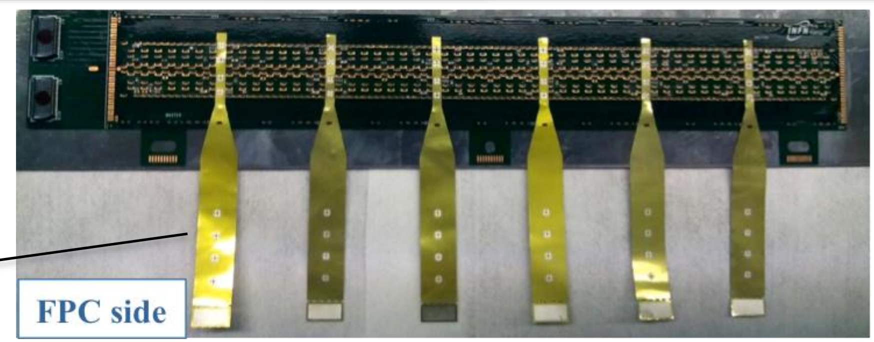


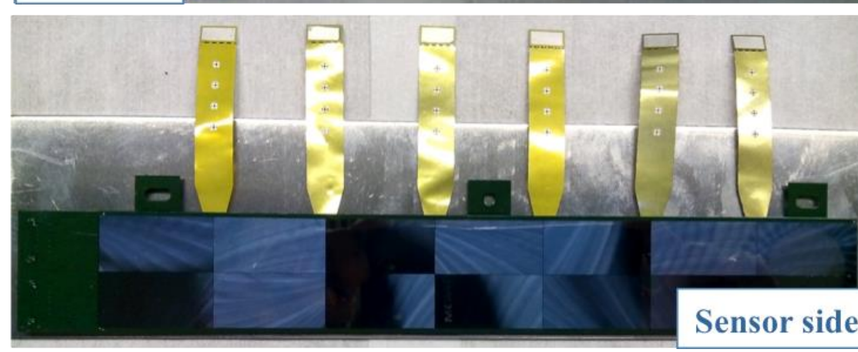
9 chips, stave length ~450 mm

Outer Barrel



x-cables for connection to power bus



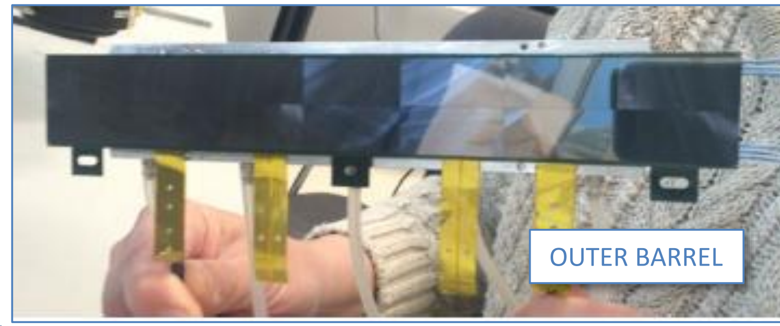


2x7 chips
length 245 mm

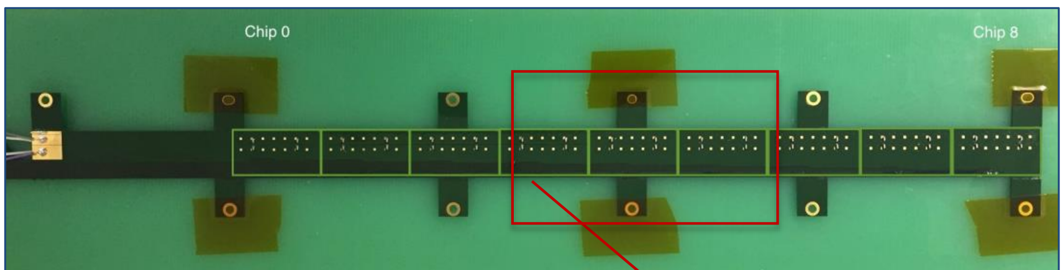
Hybrid Integrated Circuits (HIC) and Stave Prototypes

Prototype series of Inner Barrel and Outer Barrel HICs Staves with pALPIDE-3

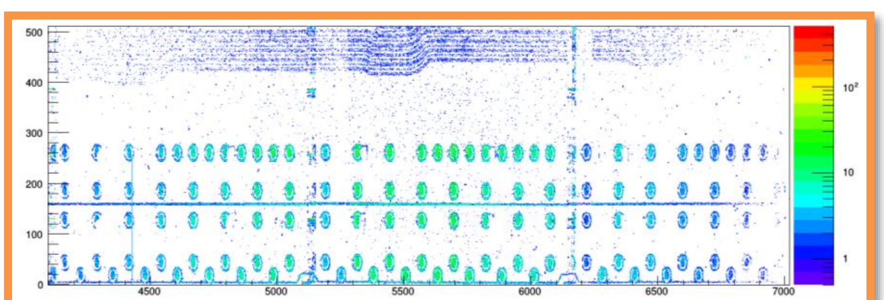
- Characterization with different modes of operation, readout rates and environmental conditions (power supply and temperature)
- Sensor performance comparable to standalone chip
- Pre-series production with ALPIDE chips starting now

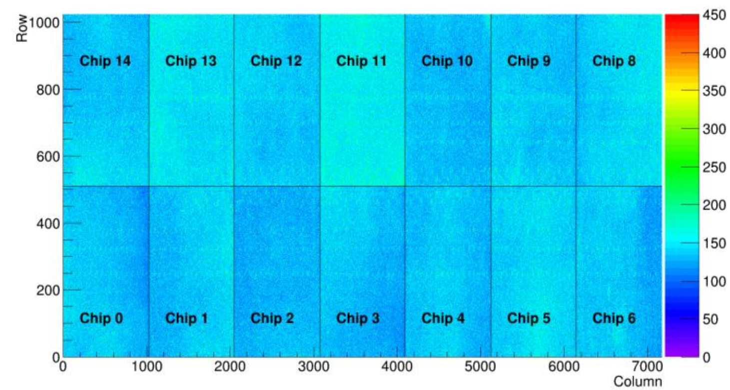


INNER BARREL



X-ray (^{55}Fe) image of IB HIC (radiography of 3 sensors)

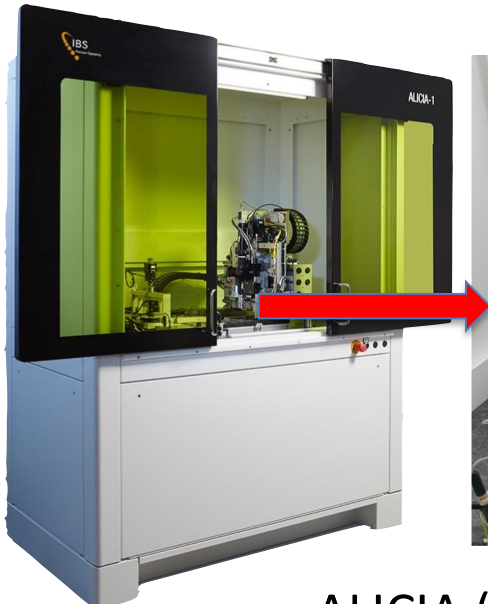


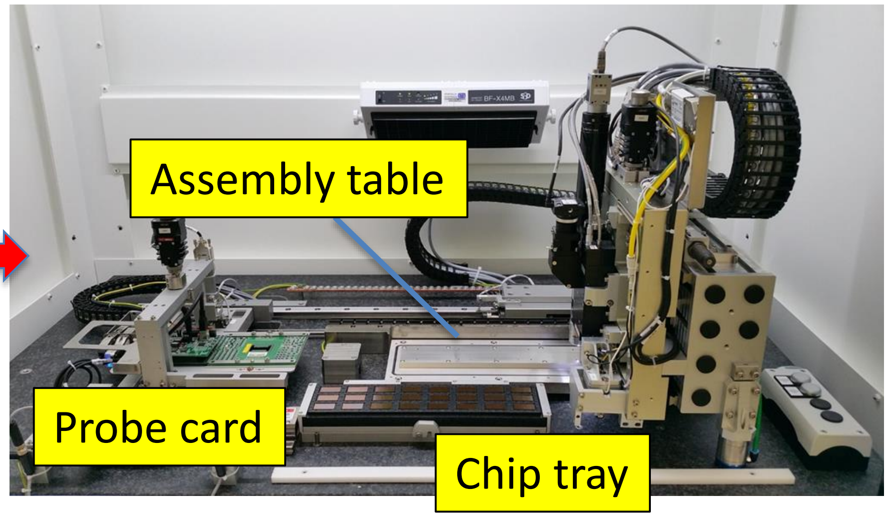


Outer Barrel HIC – threshold measurements

Chip series test and Hybrid Integrated Circuit (HIC) assembly

Machines installed at production sites, training started



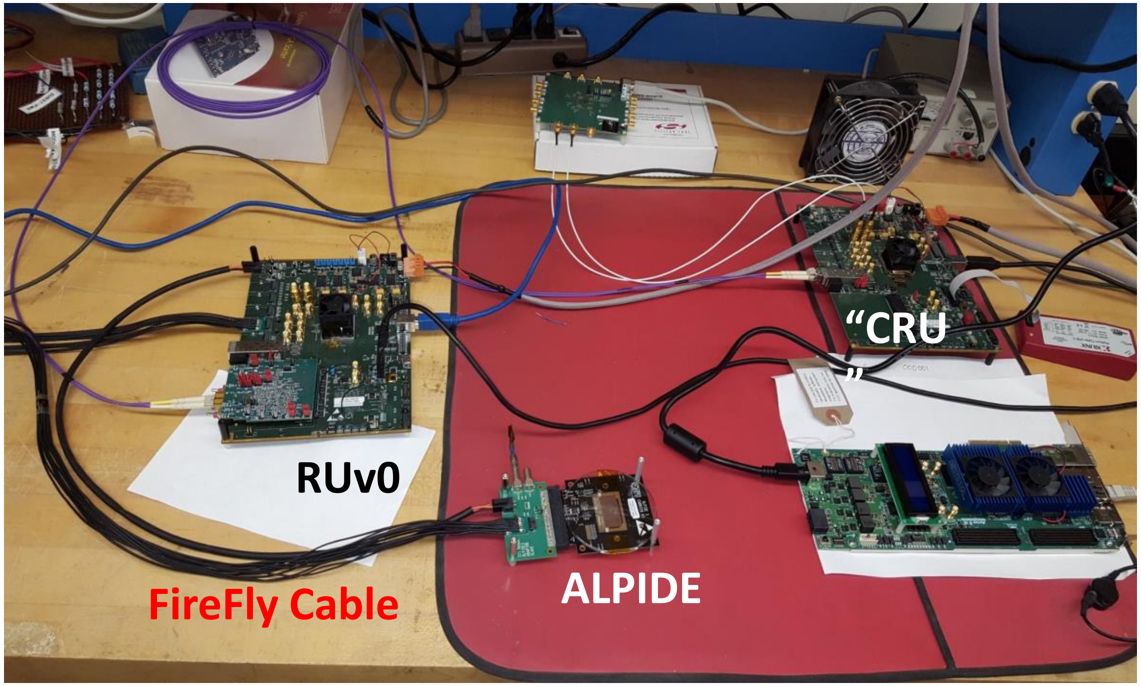


ALICIA (IBS)
6 machines (+1 MFT)
(Chip probe testing & HIC assembly)

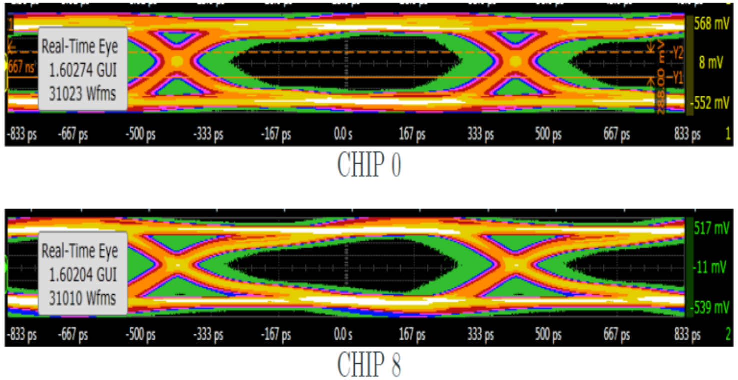
ALICIA = ALice Integrated Circuit Inspection and Assembly

Korea-YS01 (C-On)
1 machine
(mass chip probe testing)
24000 chips needed
+
MFT & spares

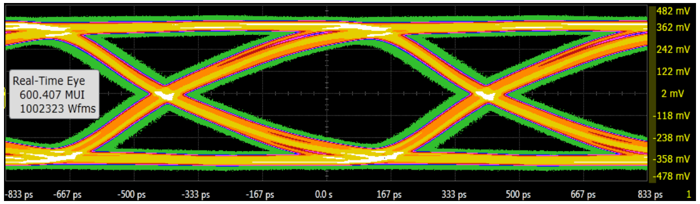
RUv0 – Readout chain with final ALPIDE verified



ALPIDE will be the only electronics component around the Interaction Point, the off-detector electronics will sit 5 m away

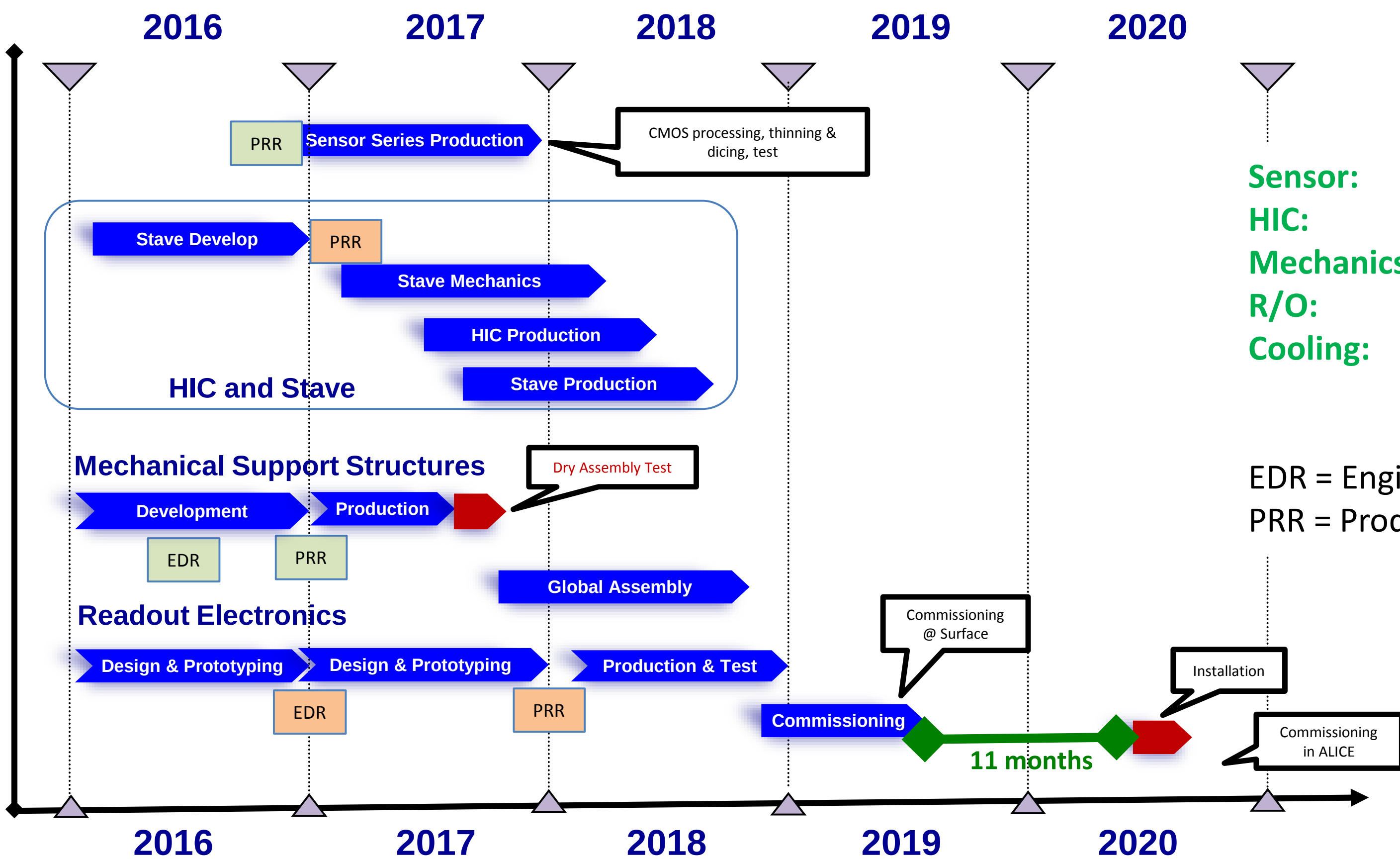


- Communication between detector (ALPIDE) and off-detector electronics via SAMTEC firefly cables
- Distribution of CLK and slow-control at 40MHz
- Data readout at **1.2Gb/s** (IB) & **0.4Gb/s** (OB)



Eye diagram of signal propagated over 5m-long cable
Measured BER (no errors over 14 h) < 1.6 10^{-14}

Overall ITS Planning (Simplified Global View)

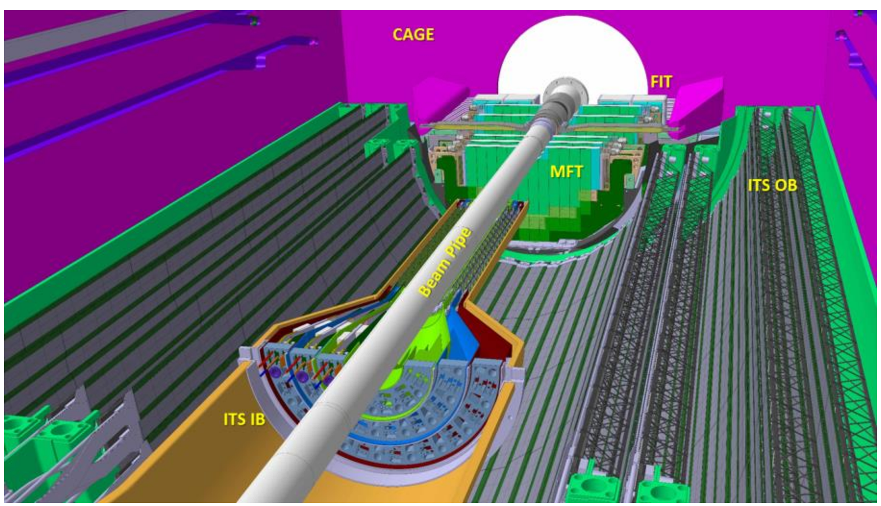


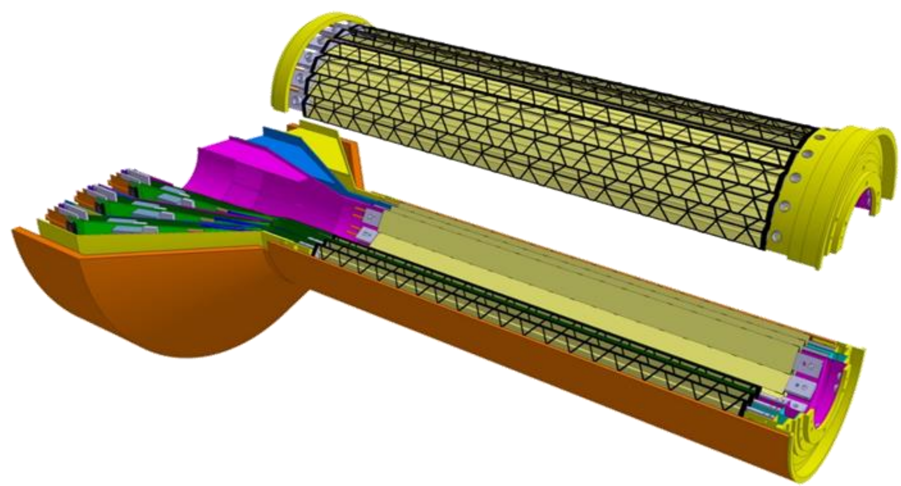
Sensor: Production started
HIC: EDR ok, PRR in March
Mechanics: PRR passed
R/O: EDR ok, PRR end '17
Cooling: PRR passed

EDR = Engineering Design Review
PRR = Production Readiness Review

Conclusions

- **The new ALICE Inner Tracking System project has successfully completed the R&D phase**
- **All requirements have been met or even exceeded**
- **With the start of the production of the ALPIDE sensor a major milestone was achieved**
- **Production sites are equipped with custom machines for test &assembly**
- **Detector production will enter full swing during 2017**
- **The project is well on track for installation starting middle 2020**





Posters related to the upgrade

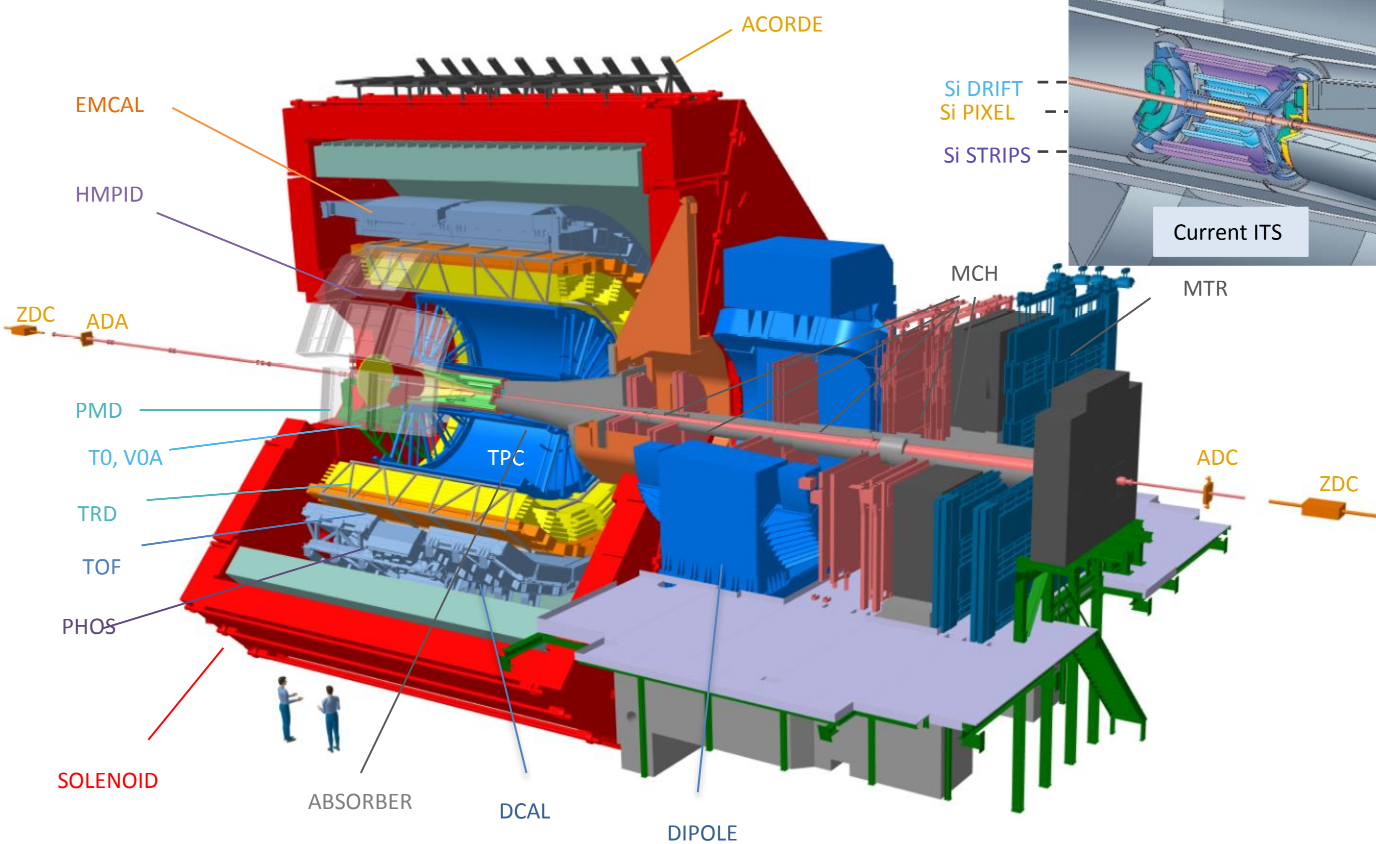
#348, “Performance evaluation of Si PAD detector for the ALICE FoCal development” by Tomoko Sakamoto
#454 “Prospects for ALICE physics with the Muon Spectrometer Upgrade and the new MFT” by Antonio Uras
#247, “Detector Control System of the new Muon Forward Tracker at ALICE” by Kenta Shigaki
#543 “A Cellular Automaton tracking algorithm for the Upgrade of the ITS of ALICE” by Maximiliano Puccio
#437, “The new Fast Interaction Trigger detector for the ALICE Upgrade” by Wladyslaw Henryk Trzaska
#442, “Forward high granularity electromagnetic calorimeter for direct photon measurements at LHC” by Hongkai Wang

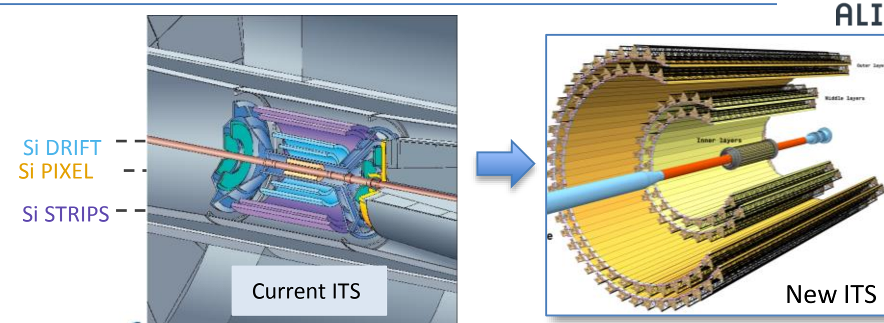
Posters related to the present detectors

#171, “Performance of ALICE EMCal and DCal in Electron Identification” by Erin Frances Gauger
#324, “Space-charge distortions in the ALICE TPC in LHC RUN 2” by Ernst Hellbar
#474, “Calibration and Performance of EMCal and DCAL Detectors at ALICE” by Justin Thomas Blair

SPARES

ALICE ITS Upgrade – entirely new, all-pixel detector, after LS2





Readout rate is currently limited by TPC and ITS (SDD)

~ 1kHz for Pb-Pb

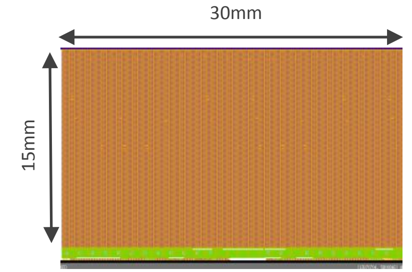
Central Barrel Tracking

- Silicon: 39 – 430 mm
- Gas (TPC, TRD): 88 – 368 cm

ALPIDE – Technology and Pixel Layout

May-2014 — pALPIDE-1

- **Full-scale prototype:** 1024 x 512
- 4 sectors with pixels variants
- pixel pitch: 28µm x 28µm
- 1 register/pixel, no final interface



May-2015 — pALPIDE-2

- 4 sectors with pixels variants
- Optimization of in-pixel and peripheral circuits
- NO high-speed output link (1.2 Gbit/sec replaced by a 40Mb/s)

Oct-2015 — pALPIDE-3

- 8 sectors with pixel variants, 3 registers / pixel
- All final features, including 1.2 Gbit/s data serial output

Aug - 2016 — **ALPIDE**

Chip Final Version

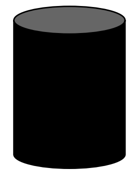
Main changes wrt pALPIDE-3

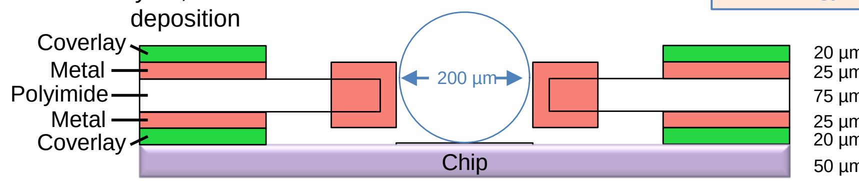
- Full matrix with same pixel type
- time skew of global signals
- Improved protection against SEUs
- Improvement of PLL ➔ High-speed Serial Output

R&D on Pixel Chip to FPC Interconnection – Selective Laser Soldering

Laser soldering: connection of Pixel chip to flexible printed circuit

Selective laser soldering





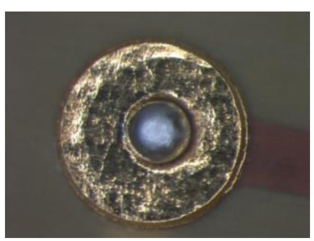
R&D addressed:

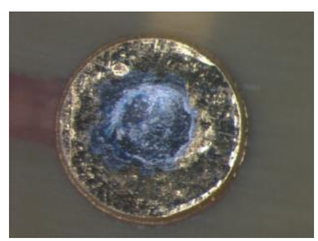
- Geometry of the interconnection
- soldering ball, interface pad and VIA
- laser beam profile and power time profile
- ….

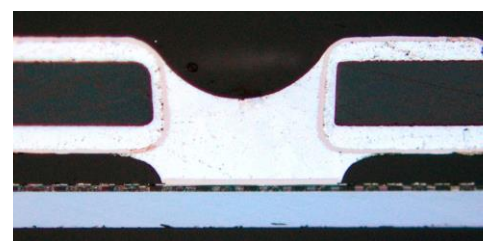
All process main issues were solved

More time needed to bring the process to a steady single interconnection yield of ~99.99%

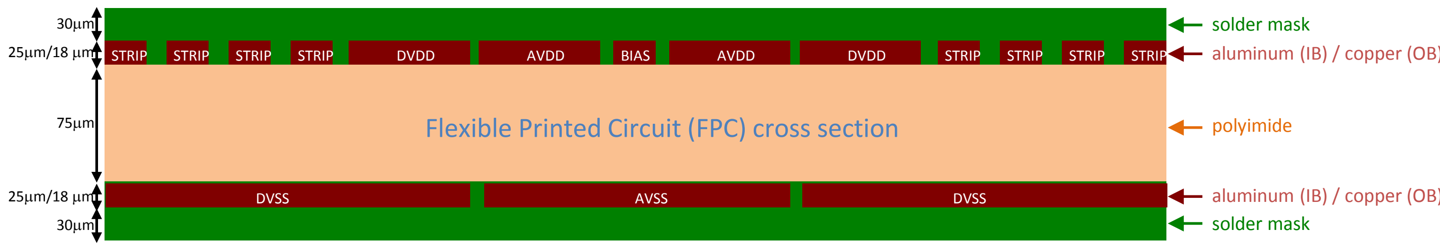
Remains a very promising interconnection technology for future applications



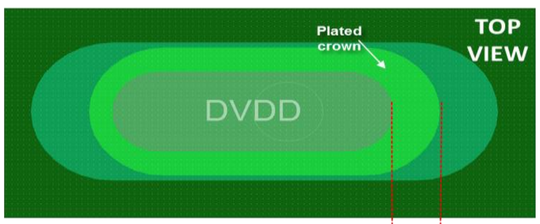


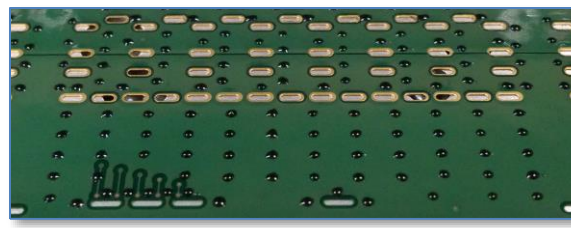


FPC to Chip interconnection – Wire Bonding

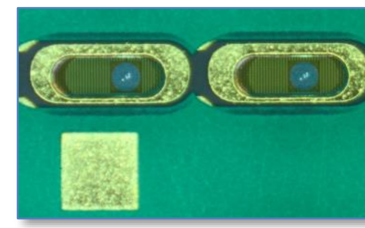


PCB conductor
aluminum Inner Layers
copper outer layers

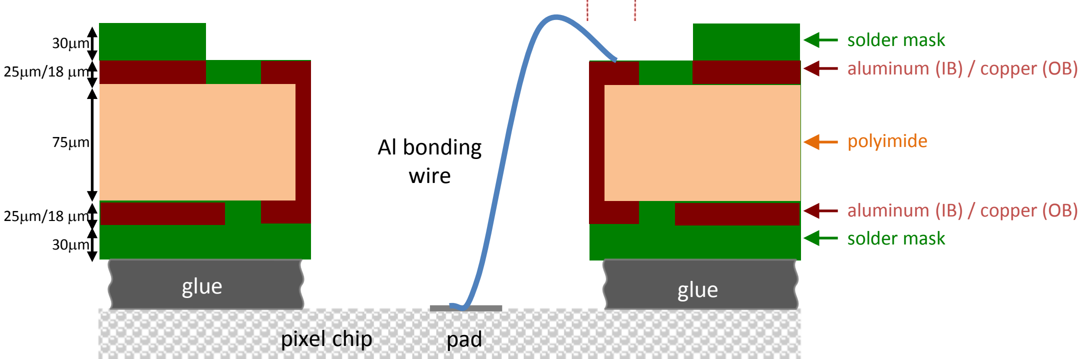


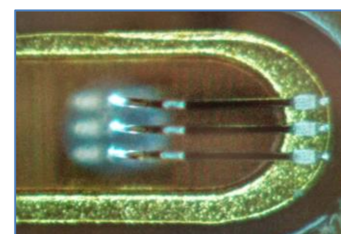


Droplets of glue (epoxy resin) dispensed on the FPC



chip pads aligned to FPC VIAs



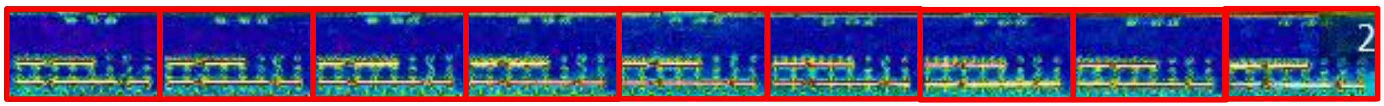


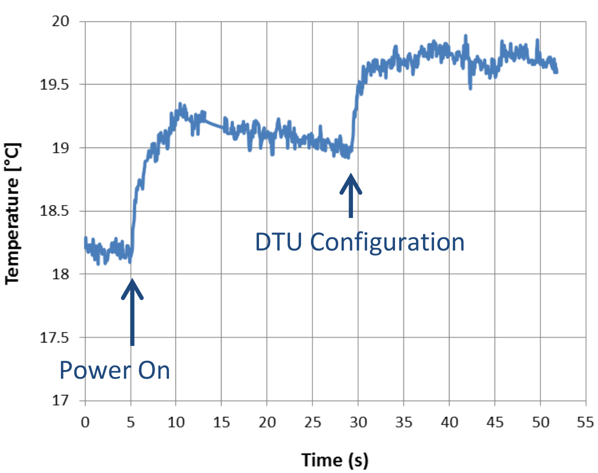
FPC to Chip interconnection (Al wire bonding)

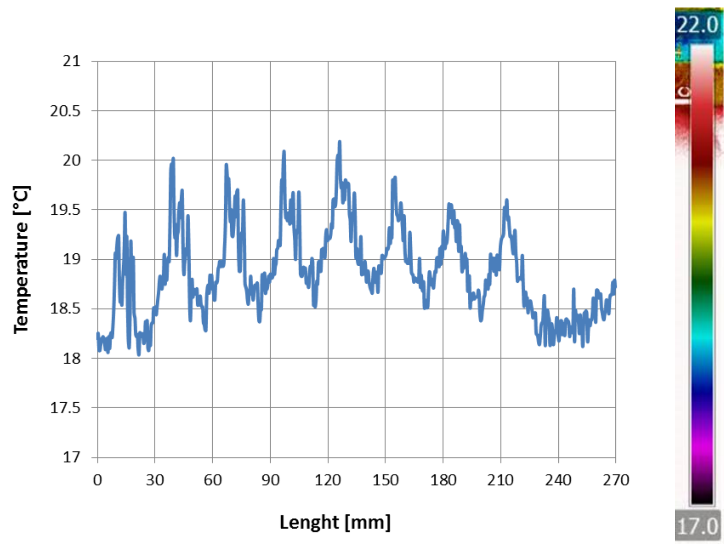
Hybrid Integrated Circuits (HIC) and Stave Prototypes

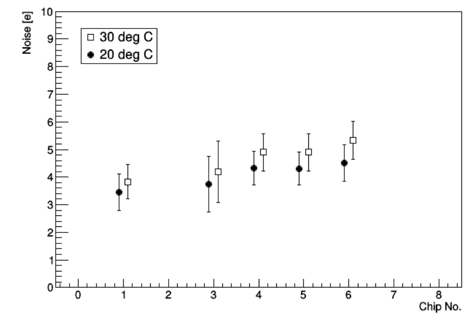
Stave temperature measurements while powering on stave in two steps

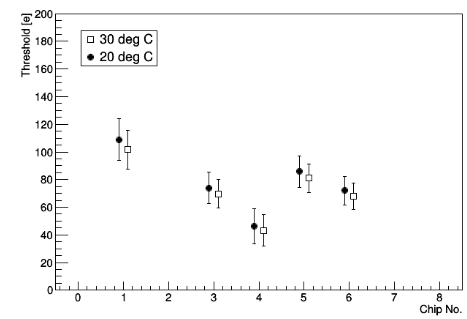
1) Power on (with CLK): ~ 80 mW digital + 20 mW analogue / chip
2) Activation of high-speed serial output (DTU): ~ 160 mW digital + 20 mW analogue / chip





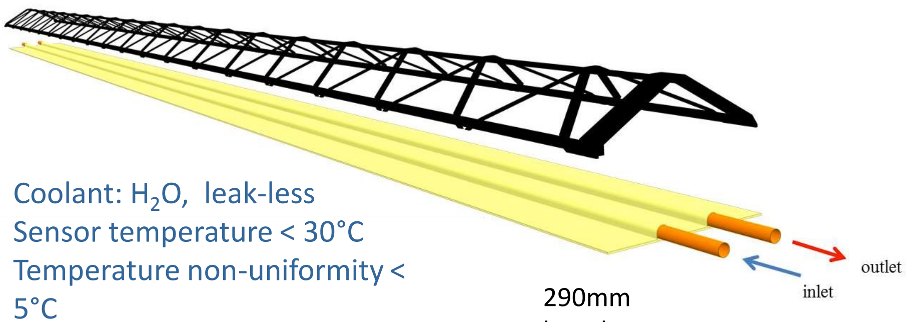






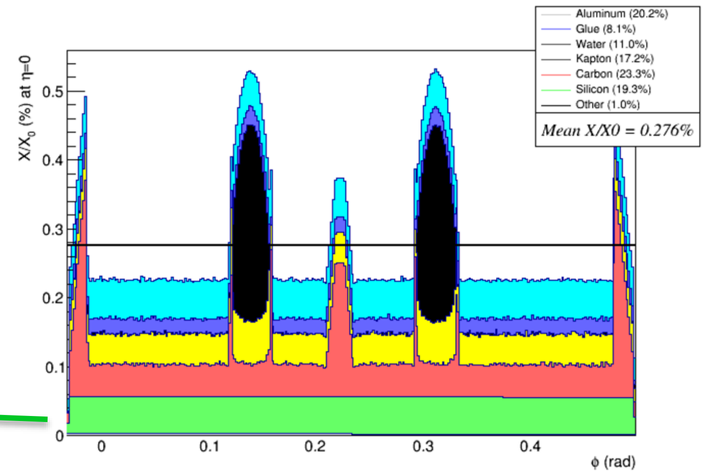
Inner Barrel Stave Mechanics & Cooling

ALICE ITS Upgrade



Coolant: H_2O, leak-less
Sensor temperature < 30°C
Temperature non-uniformity < 5°C

290mm length

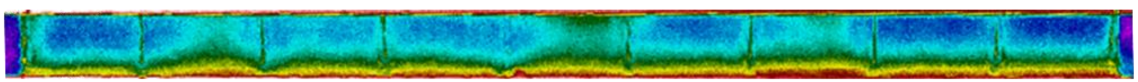


Si

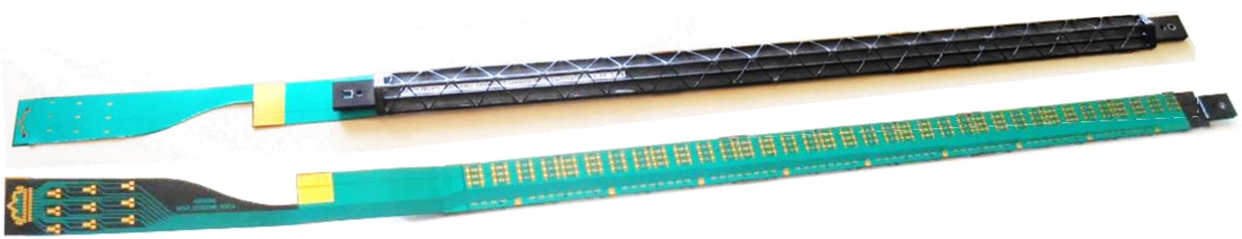
W = 100 mW / cm^2 (> x2 nominal), H_2O flow rate = 3 Lh^{-1}

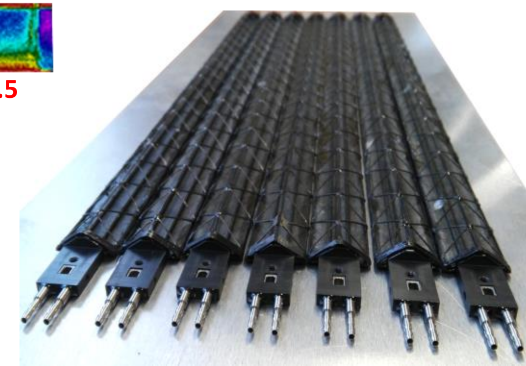
Tin=15.8° C

Tout=16.6 °C

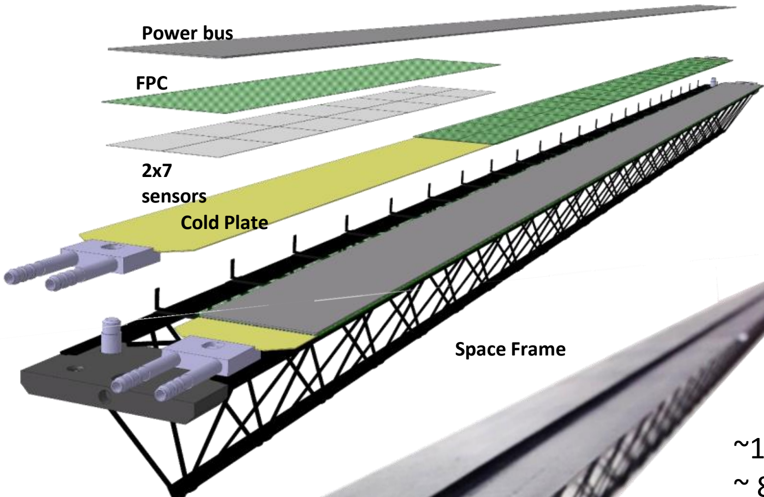


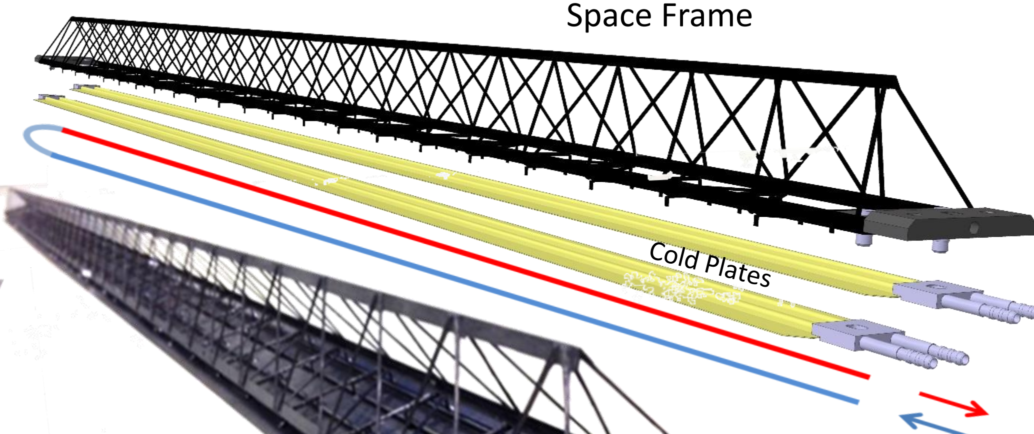
Max T periph=18.5

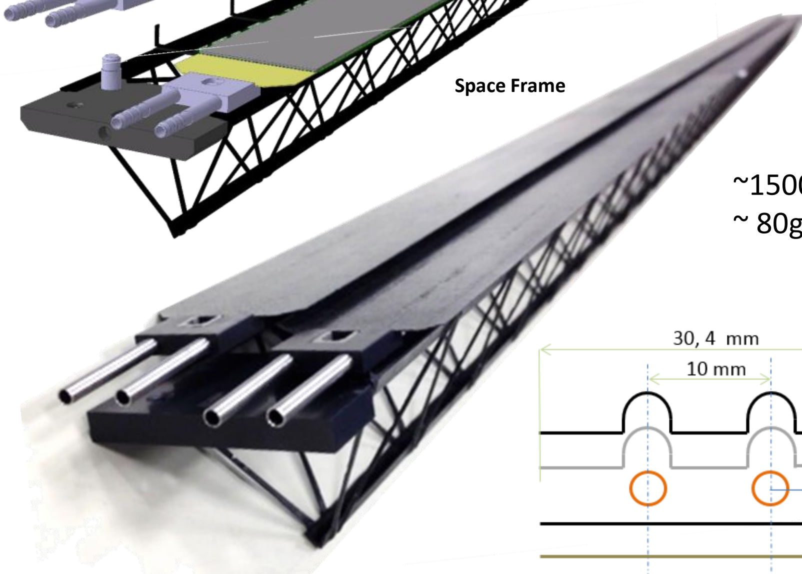


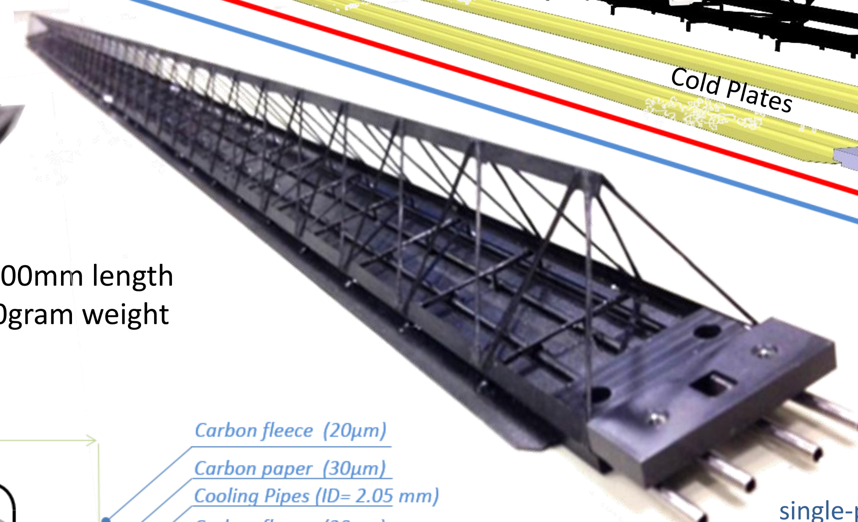


Outer Barrel Stave Mechanics & Cooling

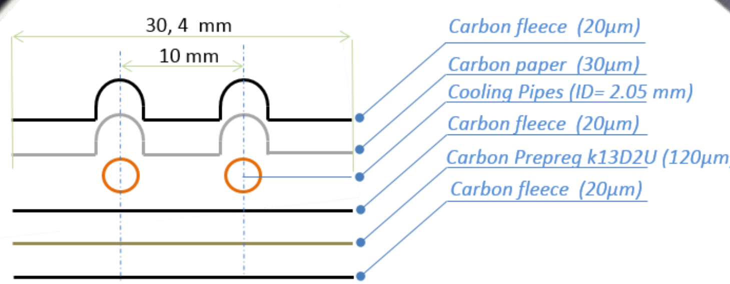








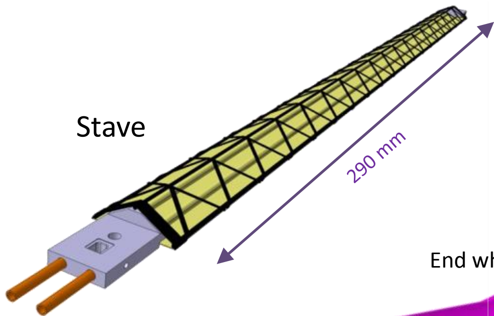
~1500mm length
~ 80gram weight

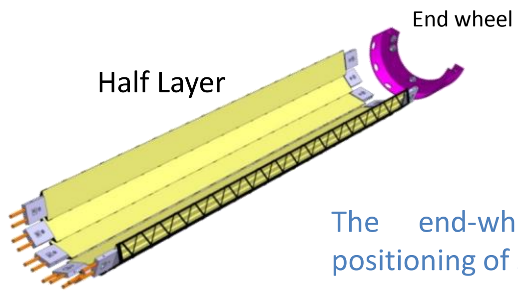


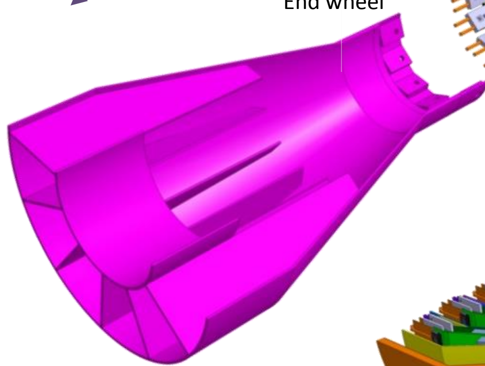
single-phase H_2O leak-less

- temperature < 30°C
- non-uniformity < 5°C
- dissipation < 100mW/cm^2

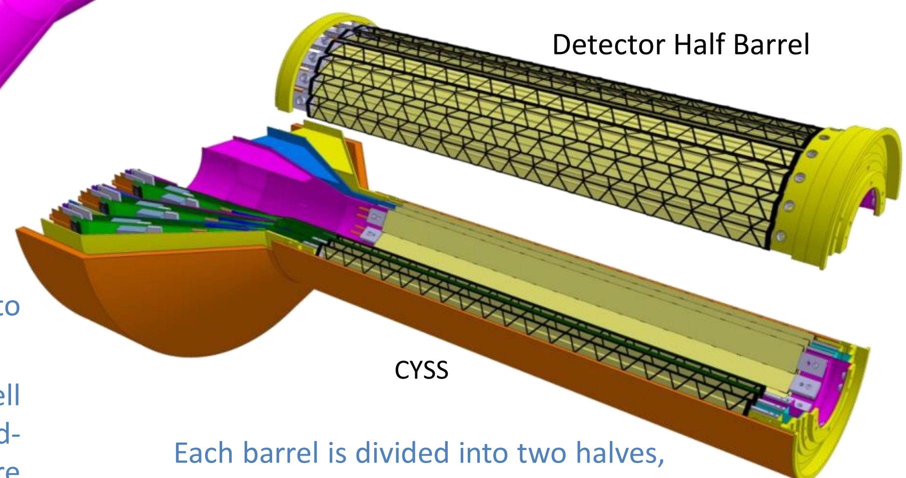
Inner Detector Barrel







The end-wheels, ensure precise positioning of staves in a layer

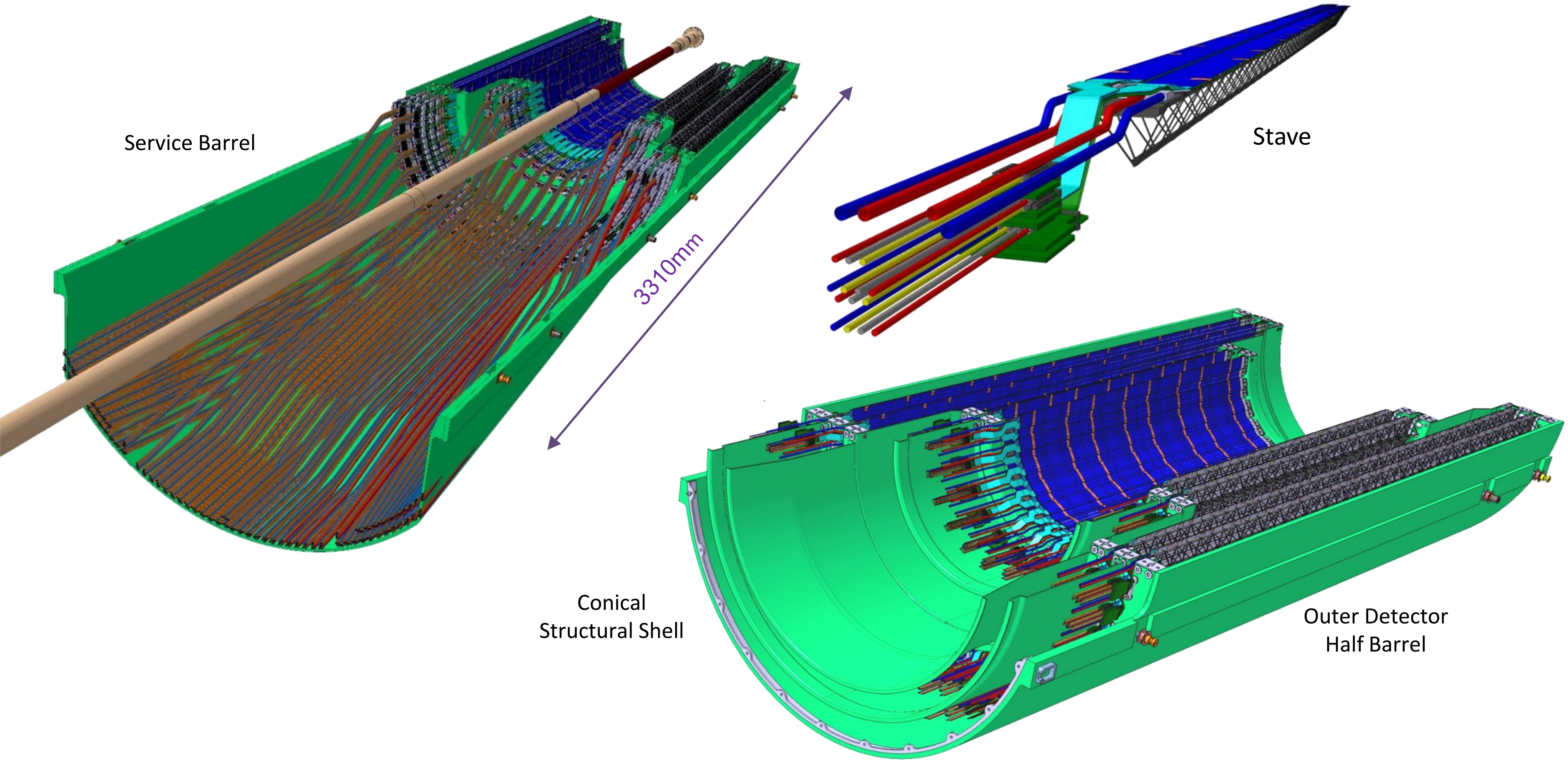


3 half-layers are connected together to form half-barrel

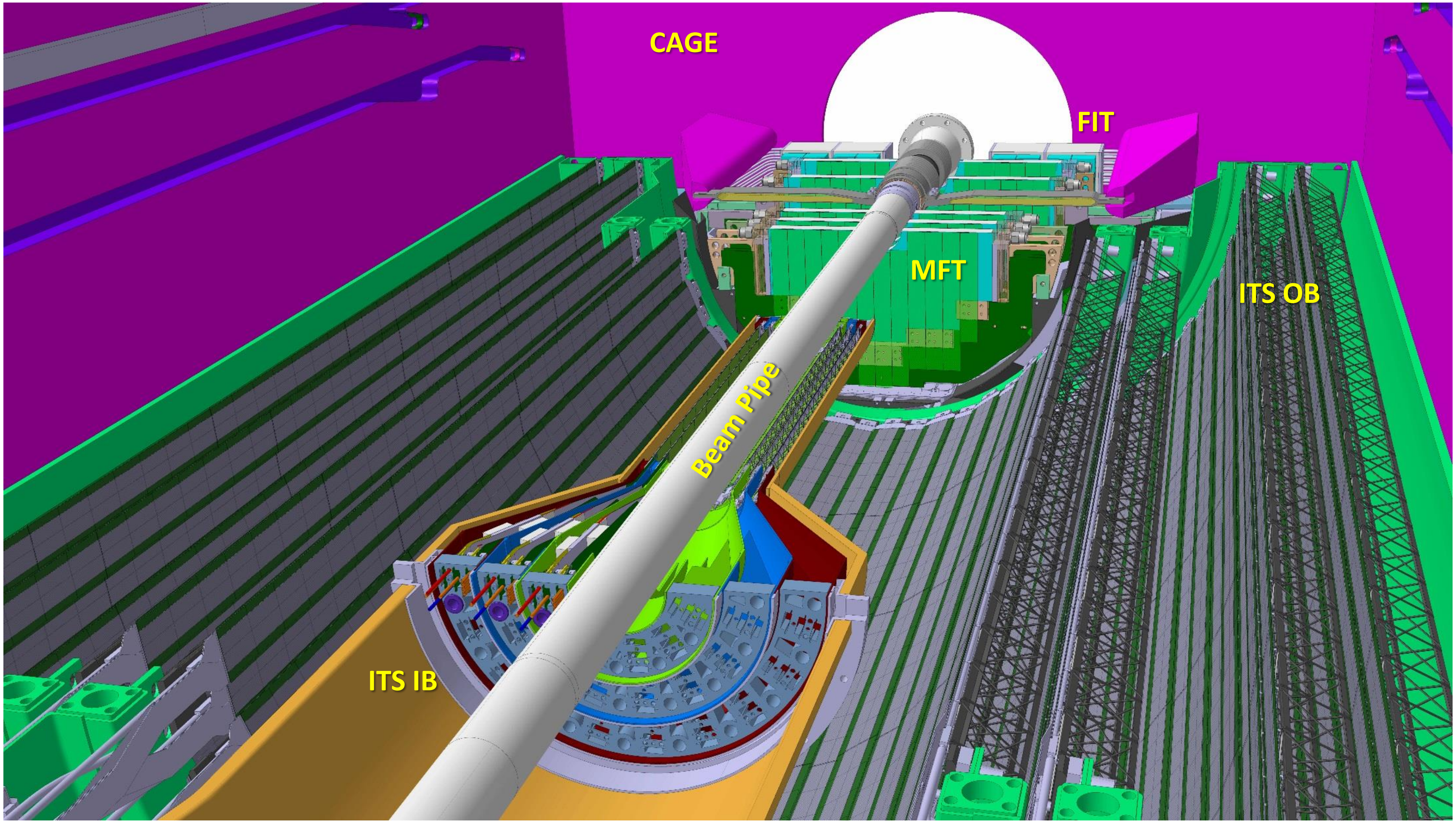
An outer Cylindrical Structural Shell (CYSS) connects the opposite end-wheels of and avoids external loads are transferred to Staves

Each barrel is divided into two halves, which are mounted separately around the beam pipe

Outer Detector Barrel

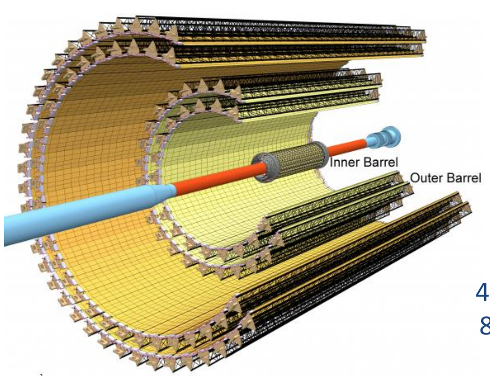


Detector Interfaces

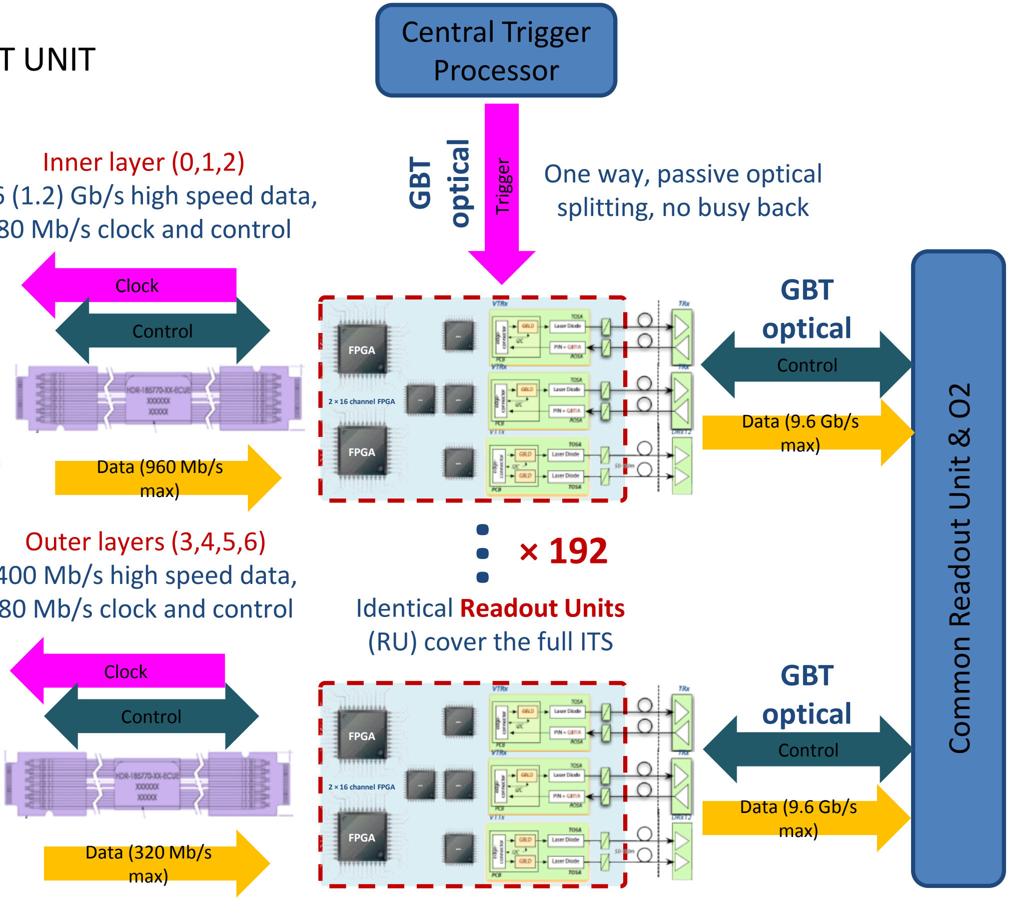


Readout Electronics - Architecture

Detector Readout ➔ 192 READOUT UNIT

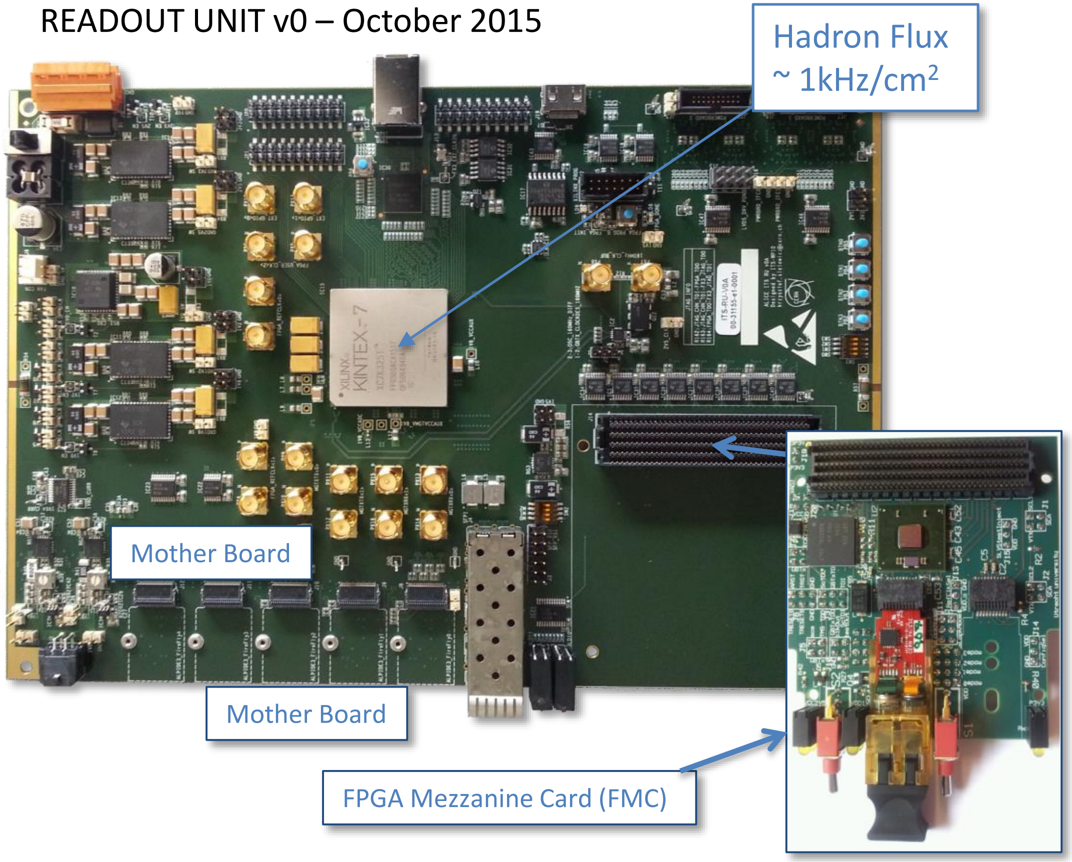


Each Readout Unit is connected to one stave both for Inner and Outer Barrels



Readout Unit - Prototype

READOUT UNIT v0 – October 2015



Prototype Readout Unit – 2015

- Based on SRAM FPGA (Xilinx Kintex7) + GBTx FMC (daughter board)
- Extensive use of radiation mitigation techniques
- ☛ Communication with Trigger and DAQ via GBT link validated
- ☛ Communication with sensors via high-speed copper serial links validated

Radiation induced fault rates

- Intensive SEU test campaigns :
- ☛ MTBF/device: ~2400 hours (10^9 h/cm^2)
- ☛ MTBF/entire system: ~12 beam hours
  System downtime ~ 10^{-5}

ALICE

Pixel Chip Requirements

Parameter	Inner Barrel	Outer Barrel	ALPIDE*
Silicon thickness	50µm	100µm	
Spatial resolution	5µm	10µm	~5µm
Chip dimension	15mm x 30mm		
Power density	< 300mW/cm^2	< 100mW/cm^2	<40mW/cm^2
Event time resolution	< 30µs		<10µs
Detection efficiency	> 99%		
Fake hit rate **	< 10^{-6}/event/pixel		<<< 10^{-6}/event/pixel
NIEL radiation tolerance ***	1.7x10^{13} 1MeV n_{eq}/cm^2	10^{12} 1MeV n_{eq}/cm^2	
TID radiation tolerance ***	2.7Mrad	100krad	

* extrapolation of the ALPIDE performance based on prototype results

** revised numbers w.r.t. TDR

*** including a safety factor of 10, revised numbers w.r.t. TDR